

CBC2: CMS microstrip readout for HL-LHC

[D. Braga], G. Hall, M. Pesaresi, M. Raymond (Imperial College)
D. Braga, L. Jones, P. Murray, M. Prydderch (RAL)
D. Abbaneo, G. Blanchot, A. Honma, M. Kovacs, F. Vasey (CERN)

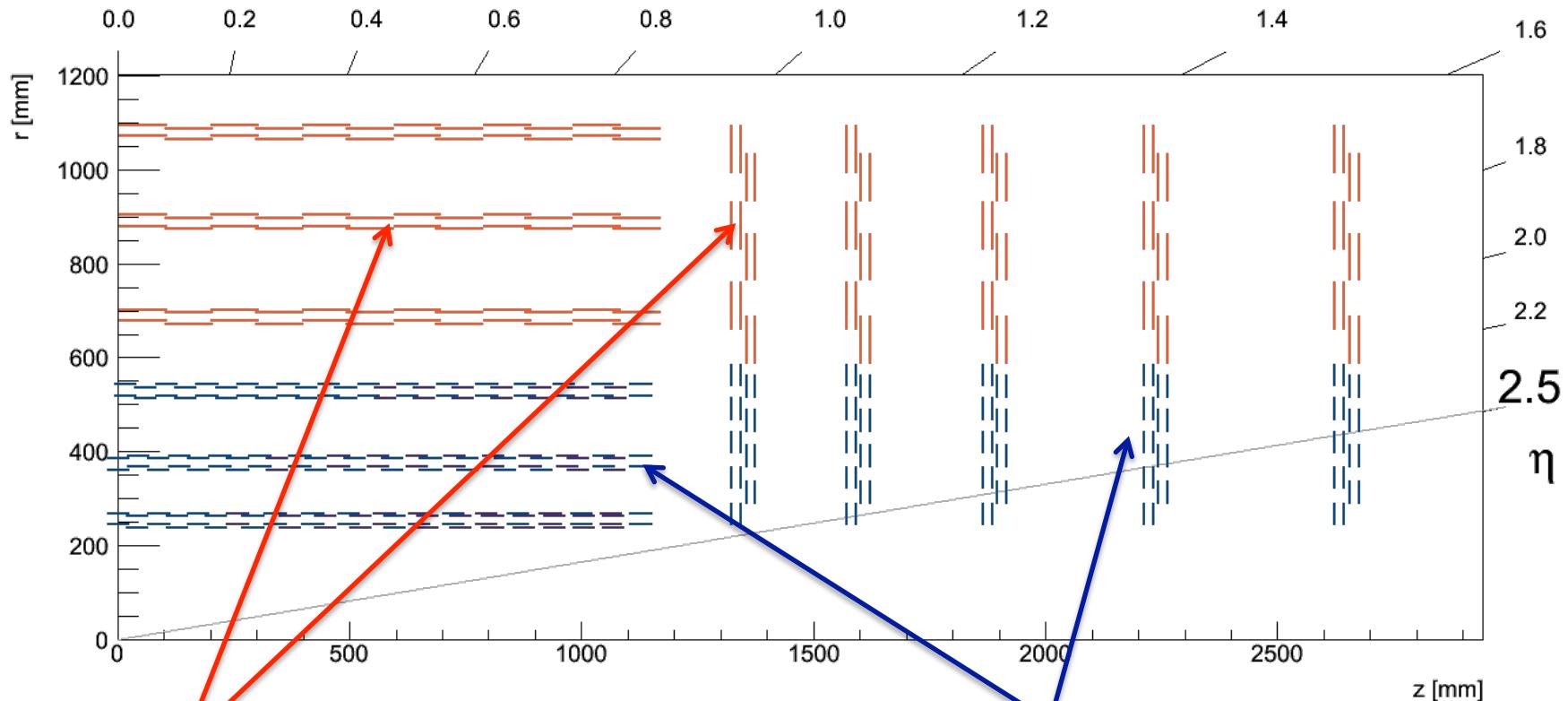
Background

- CMS upgrade under consideration for many years
 - objective to reach 3000 fb^{-1} in next decade or so
 - High Luminosity LHC (Phase II) requires new Tracker around 2023
 - Requirements:
 - lower material budget
 - increased granularity
 - enhanced radiation tolerance
 - tolerable power consumption
 - affordable cost
 - all compatible with physics objectives –some of which remain uncertain
 - e.g. will new physics be discovered in next running period?
 - but solid long term programme of Higgs & top studies, searches, etc...

Evolution of objectives

- Original goal
 - new – improved - tracker with similar angular coverage, constrained by re-using existing services
 - provide some part of tracker data to L1 trigger to contain rate to 100 kHz
- More recent developments
 - Baseline Tracker design now adopted
 - “conventional” barrel-endcap layout looks optimal
 - but CMS exploring enhancing forward region physics as well as standard physics programme
 - uncertainty if L1-track triggering will reduce rate to 100 kHz in 6.4 μ s
 - ideas (and detector requirements) not yet validated by simulations
 - possible objective of L1 readout up to 1 MHz/10-20 μ s
 - both approaches require on-detector data reduction

Baseline tracker layout (pixels not shown)



2S short strip double-layers
(~7500 modules)

PS strip-strikel double-layers
(~10,000 modules)

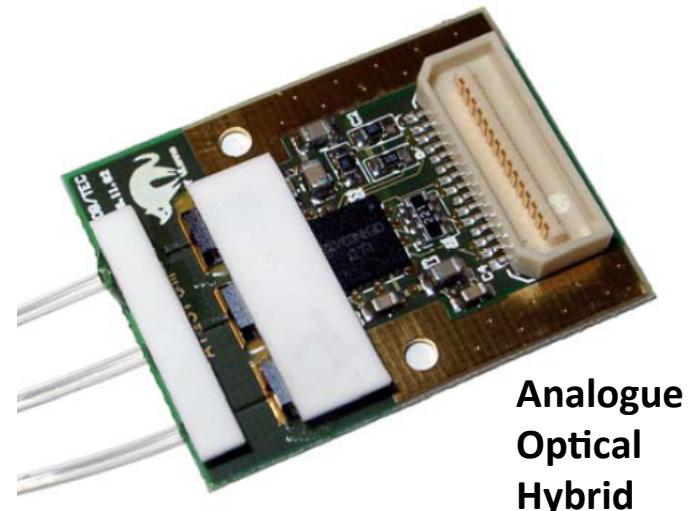
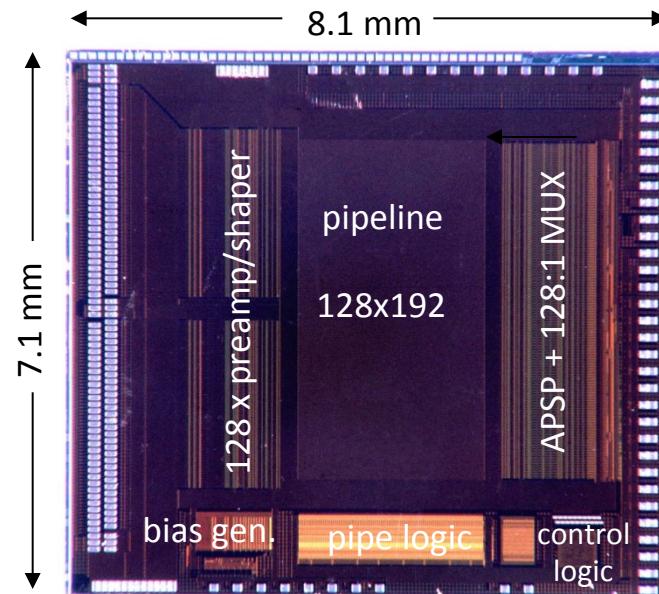
- Double layer readout compatible with trigger
- Geometry compatible with forward extension

ASIC development

- Earliest developments foresaw conventional outer tracker, plus some dedicated trigger (and pixel) layers
 - 128 channel CMS Binary Chip (CBC) produced and proven 2011
 - Readout architecture followed original tracker, using APV25
 - Analogue data abandoned for practical reasons
 - digital optical link components now commercially standard,
 - ADC power
 - 130 nm CMOS makes analogue memory cells harder to implement
- Subsequently, outer modules with trigger capability agreed
 - 254 channel CBC2 successfully developed – delivered 2012
 - optimised for new assembly method with mass production in mind

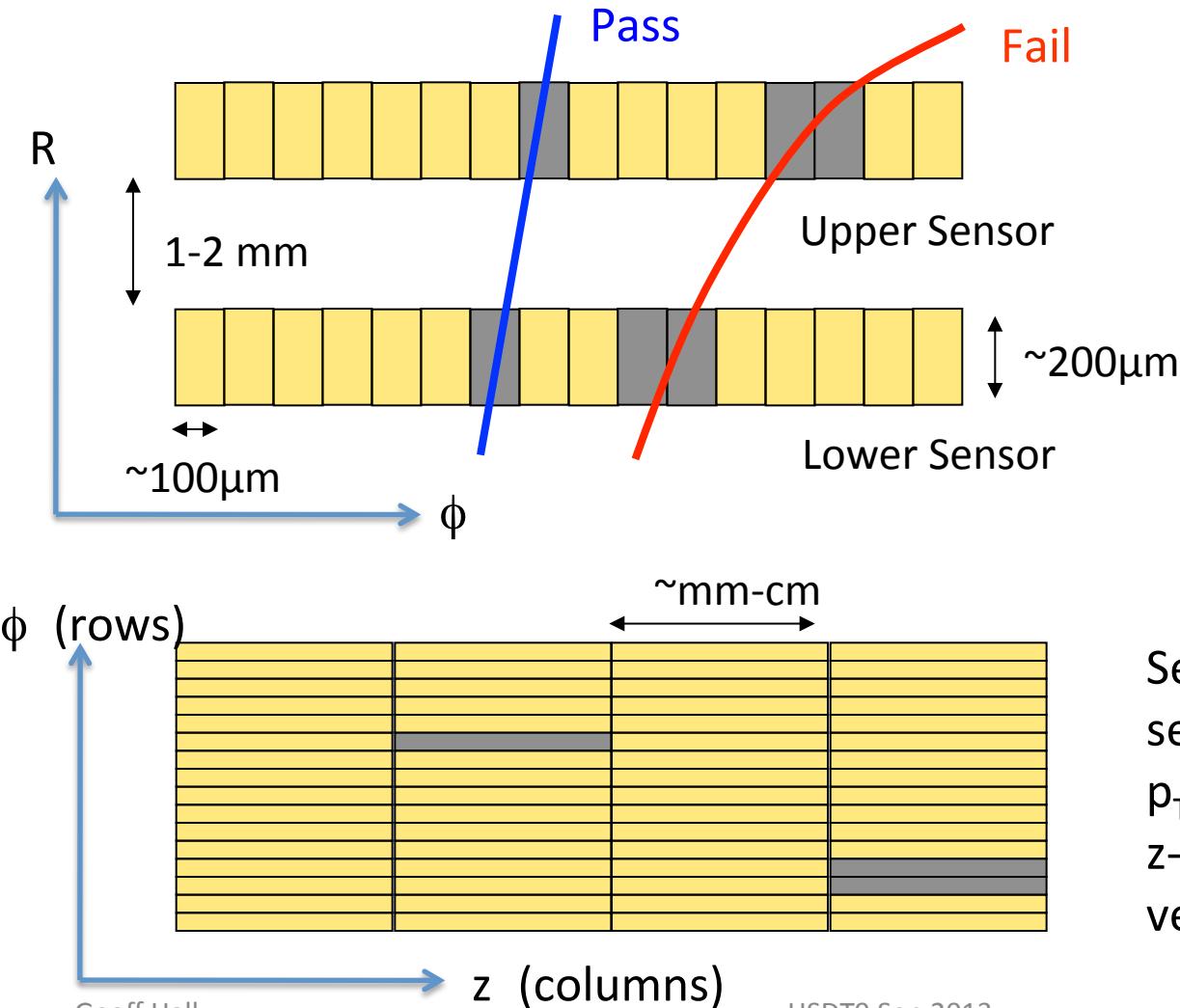
Present CMS Tracker architecture

- Analogue unsparsified readout
 - APV25 in 0.25 μ m commercial CMOS
 - synchronous
 - occupancy independent data volume
 - 2.7mW/chan for 10-20cm μ strips
 - analogue data transmission to external ADC & zero-suppression, clusters
 - semi-custom optical links @ 40Msps
 - 1310 nm single-mode Fabry-Perot lasers
 - **very successful**
 - reflected state of technology at the time
 - benefits
 - simple and easy to debug/evaluate
 - robust against noise



Basic trigger module concept

- Compare binary pattern of hit pixels on upper and lower sensors

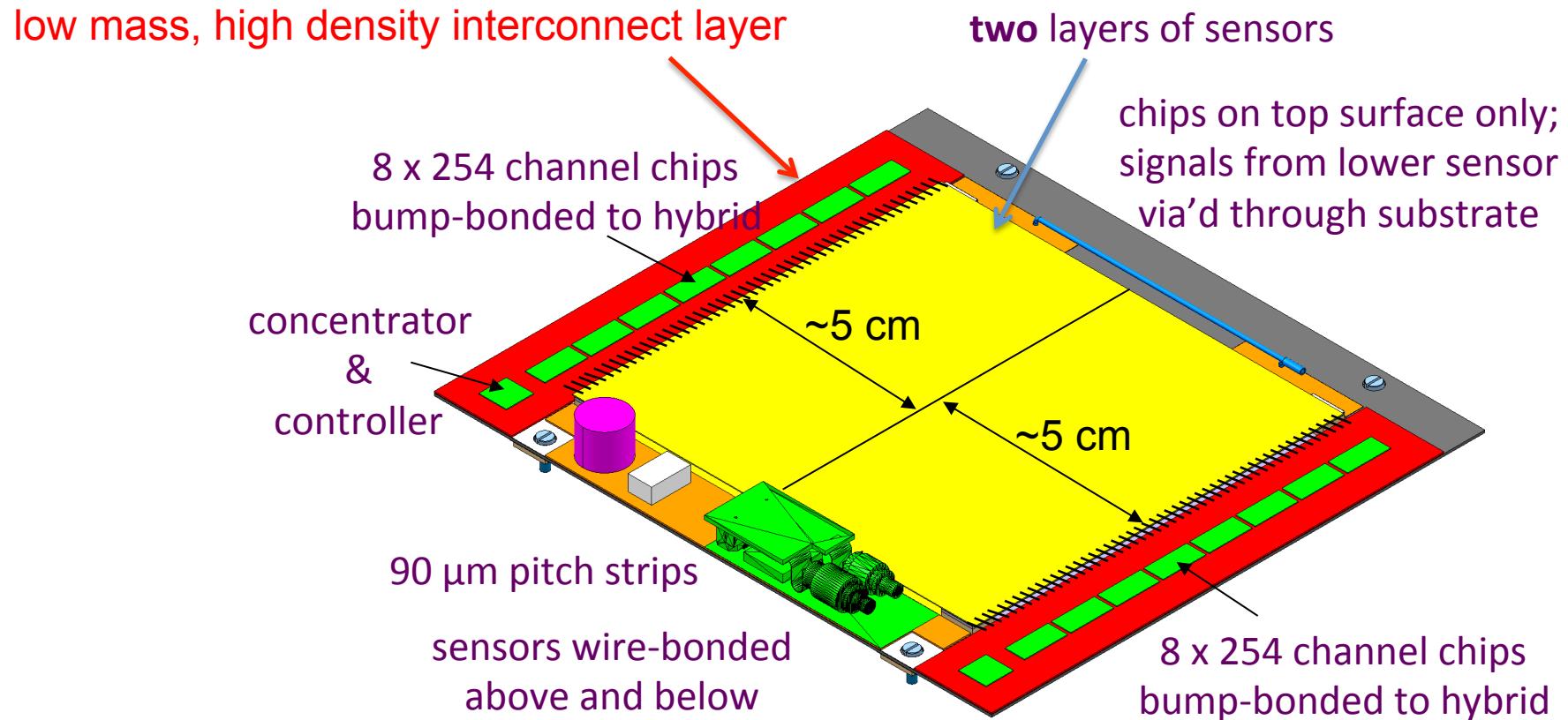


High p_T tracks can be identified if hits lie within a search window in $R-\phi$ (rows) in second layer

Sensor separation and search window determines p_T cut
 z -segmentation determines vertex capability

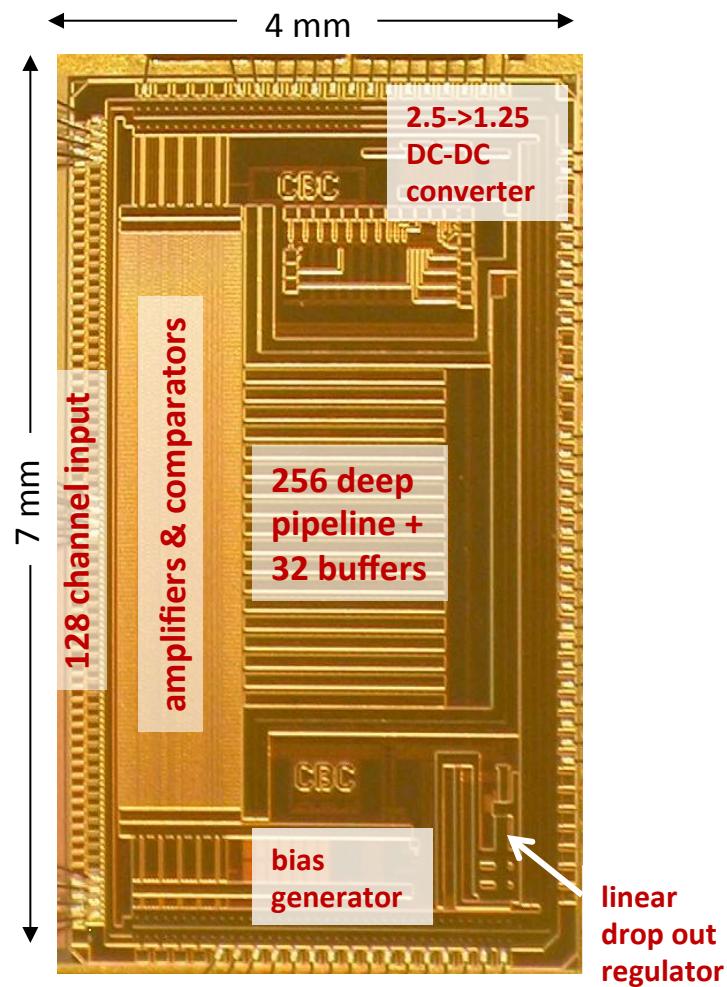
2S PT-module with CBC2

- **Track & trigger** μ strip module for outer tracker region
 - CBC2 logic correlates hits on two sensors to reject those from low p_T tracks

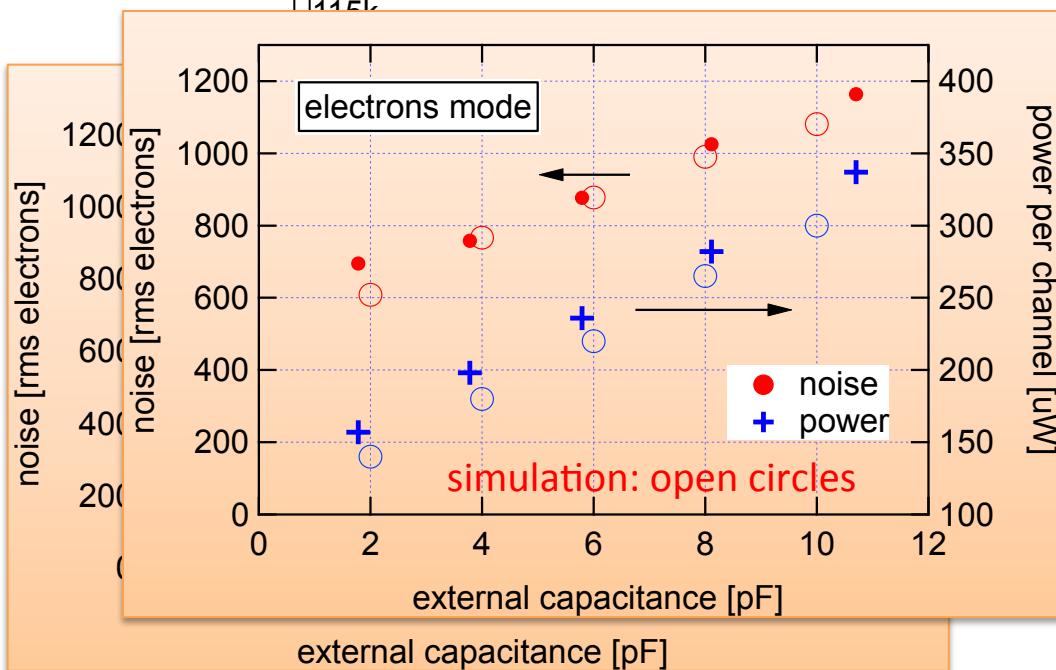
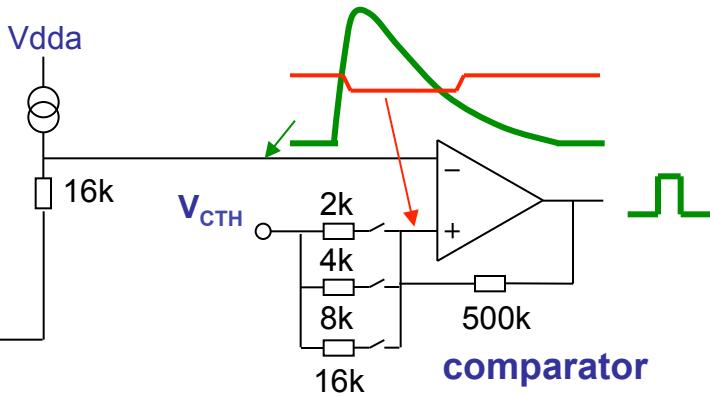
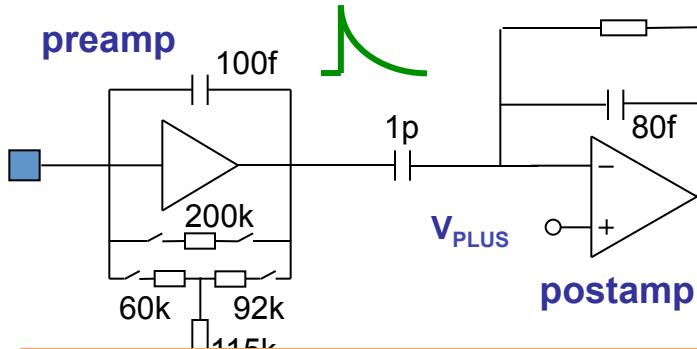


First version: CBC main features

- IBM 130nm CMOS process
- binary, unsparsified architecture
 - retains chip and system simplicity
 - but no pulse height data
- designed for $\sim 2.5 - 5\text{cm}$ μ strips $< \sim 10 \text{ pF}$
- 128 channels, 50 μm pitch wire-bond
 - either polarity input signal
- not contributing to L1 trigger
- powering test features:
 - 2.5 \rightarrow 1.2 DC-DC converter
 - LDO regulator (1.2 \rightarrow 1.1) feeds analogue FE
- fast (SLVS) and slow (I2C) control interfaces



CBC measured performance



analogue

- $130 + (21 \times C [\text{pF}]) \mu\text{W}/\text{chan}$

digital

- $< 50 \mu\text{W}/\text{chan}$

total

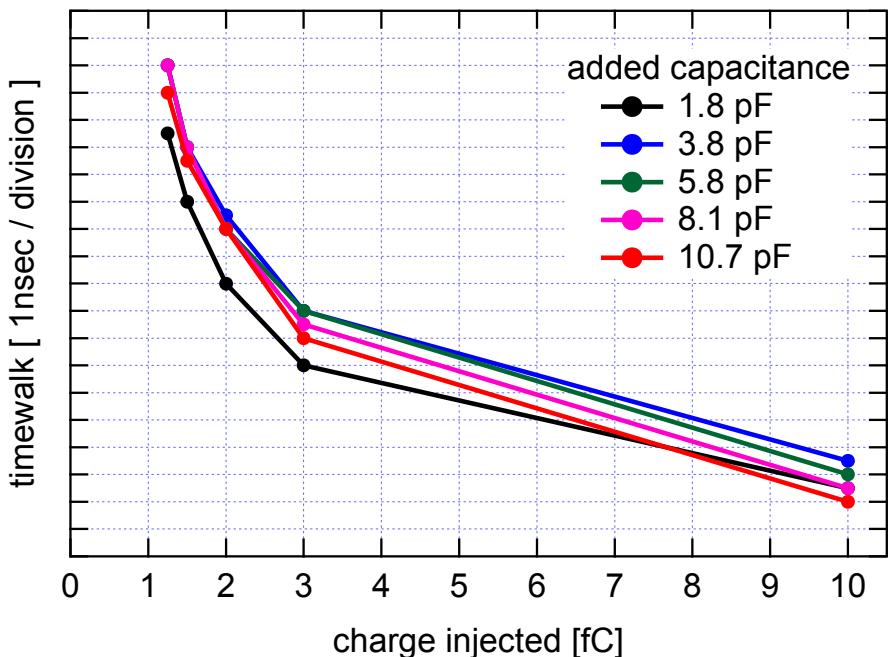
- $180 + (21 \times C[\text{pF}]) \mu\text{W}/\text{chan}$

e.g. $< 300 \mu\text{W} / \text{channel}$ for $C = 5 \text{ pF}$

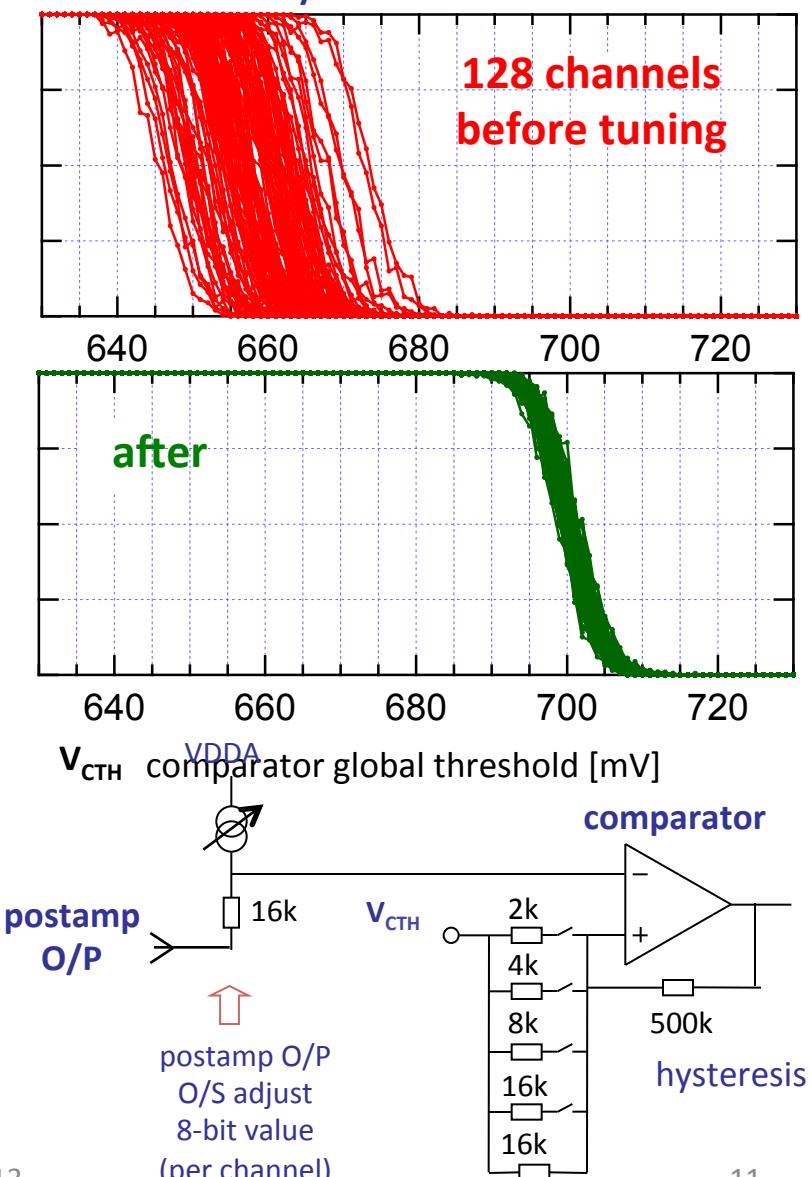
CBC comparator

- thresholds adjusted satisfactorily
- timewalk within spec

timewalk: threshold at 1 fC

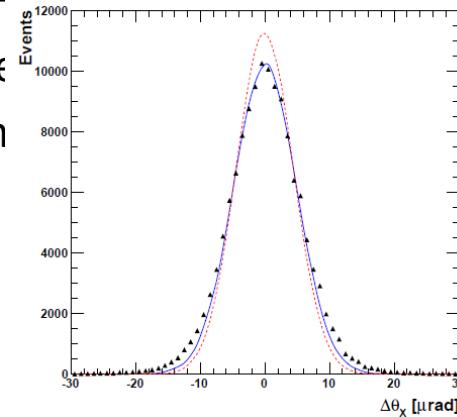
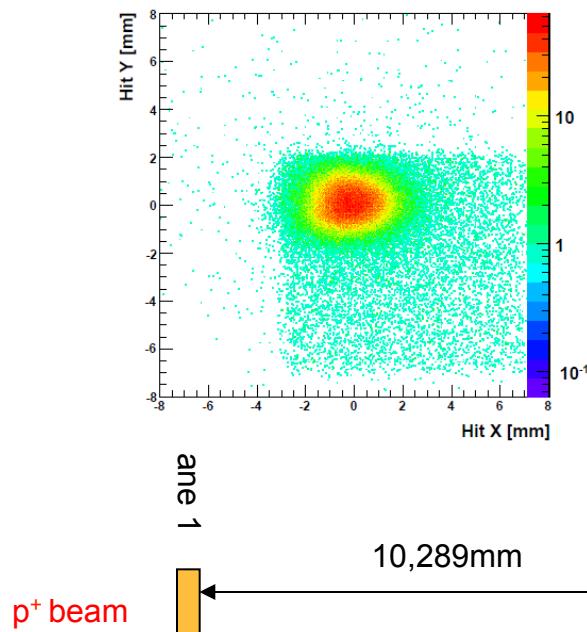


threshold uniformity



Beam telescope

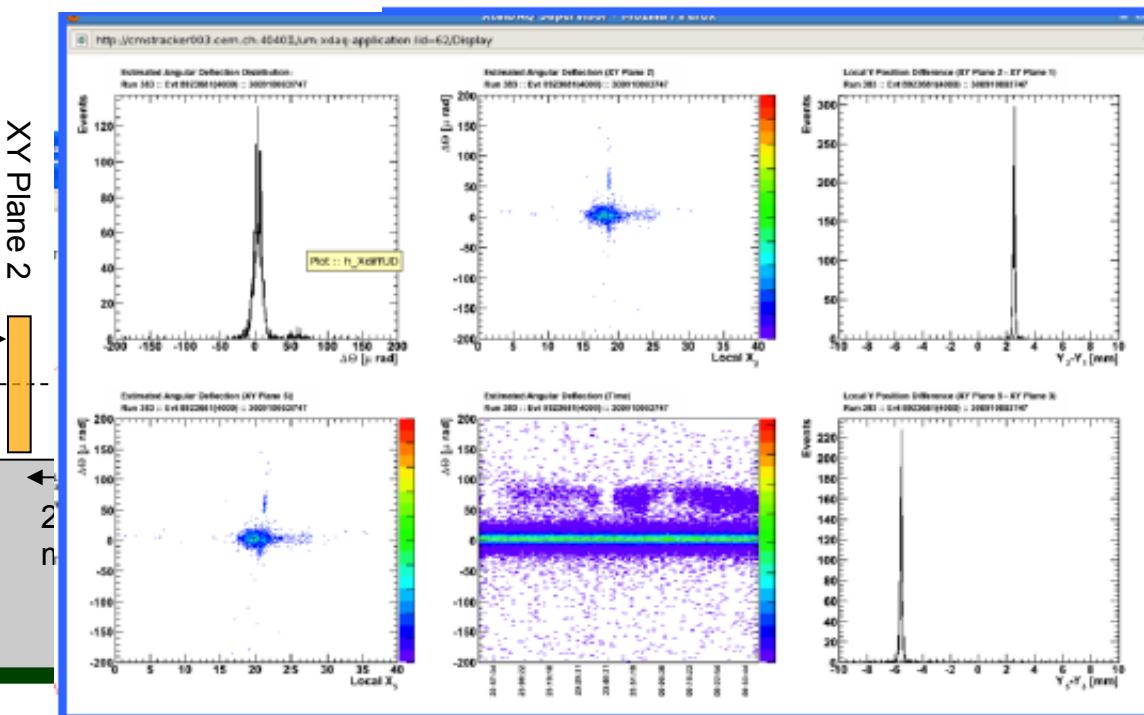
- Based on CMS Tracker DAQ ~~readout + hardware~~ software (used for UA9 studies)
- FED, APV25s, 100m fibre
- 50 kHz data taking during beam tests



n, multi-core PCs

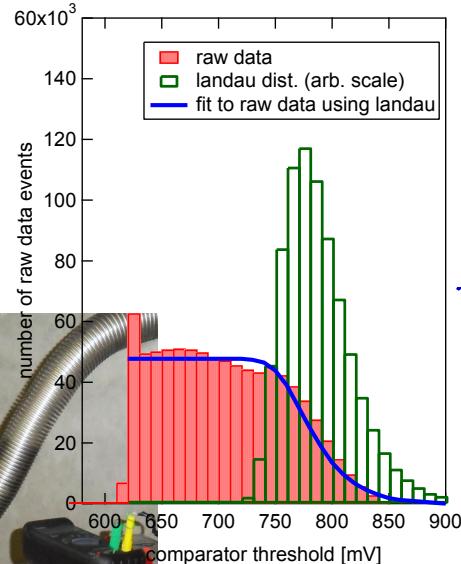
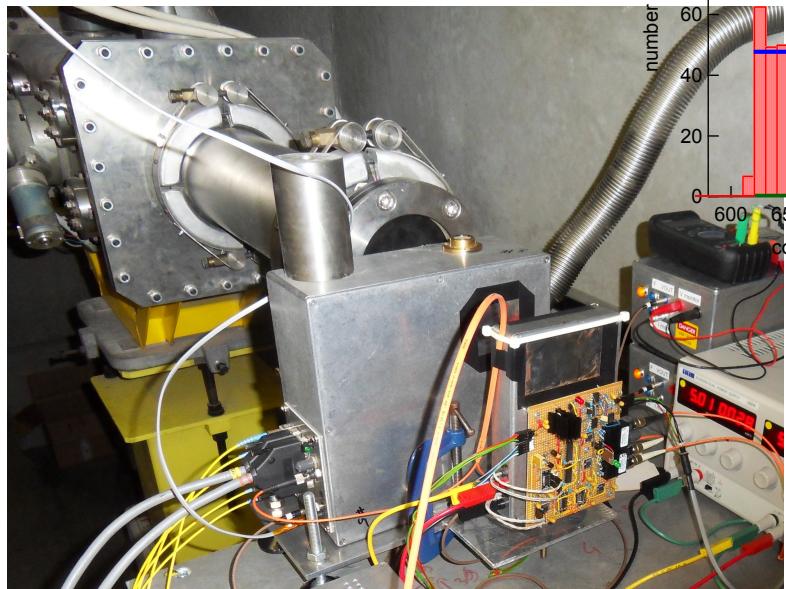
spatial resolution: 6.8-7.0 μm

angular resolution: 5.2 μrad

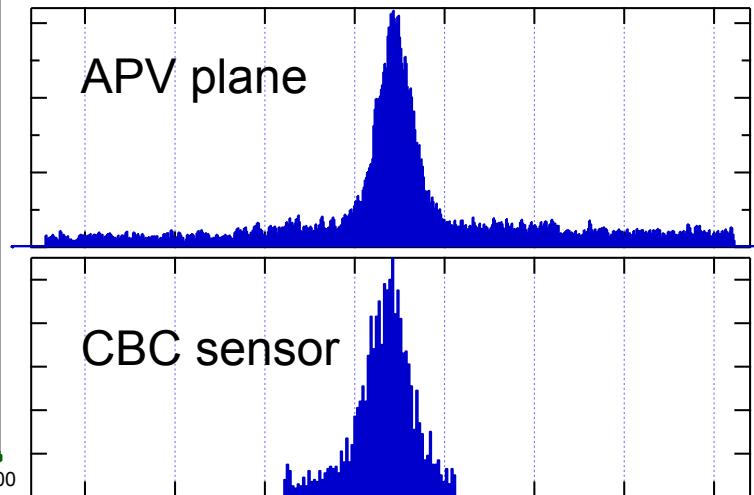


CBC beam tests 2011

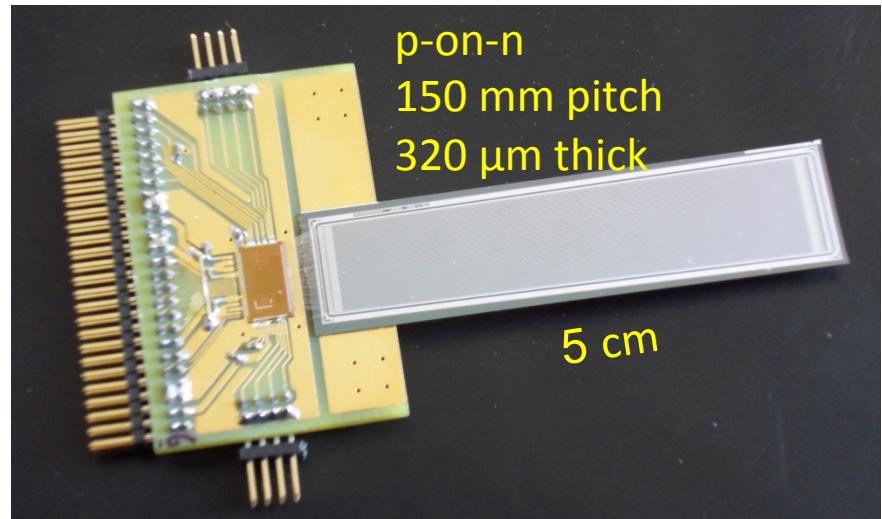
- CERN H8 beam line
 - 400 GeV/c protons



beam profile



5 mV / division

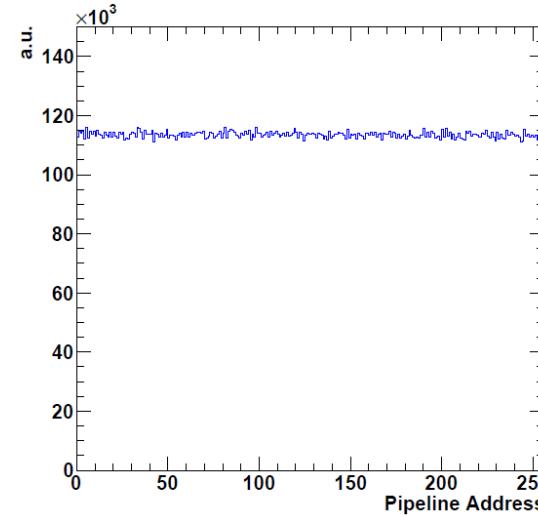
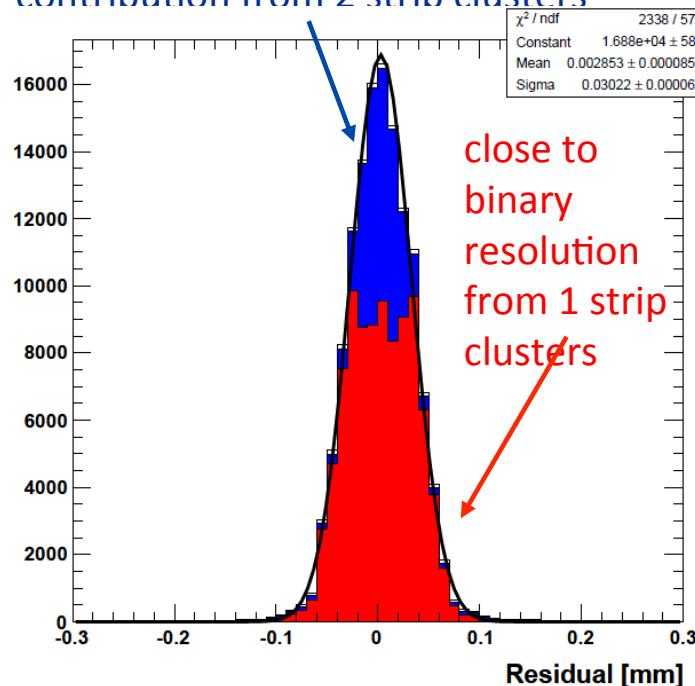


$64 \times 150 \mu\text{m}$ pitch strips bonded to
5 cm long, $320 \mu\text{m}$ thick fan
shaped p-on-n sensor

CBC performance in beam

- Successful operation
- Digital logic works well
 - no pipeline errors
 - no CBC errors in > 30M events

better than pitch/v12 due to contribution from 2 strip clusters



use telescope to select events at CBC module

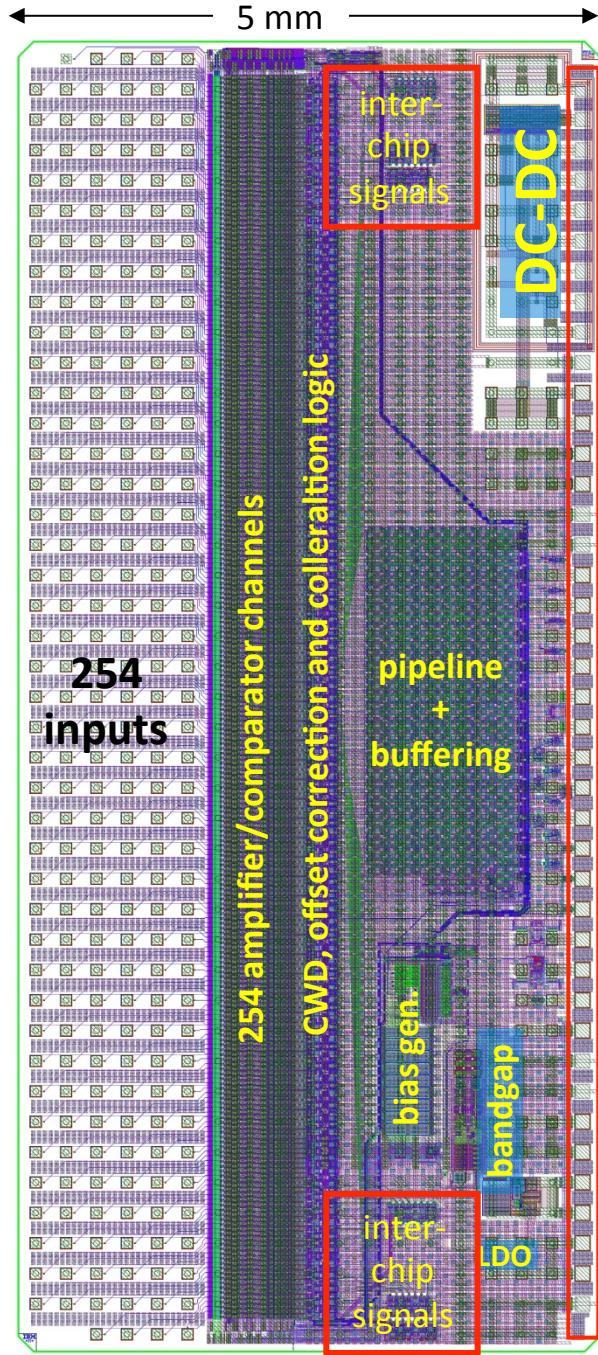
- single track events only (pileup eliminated)
- incident on CBC sensor (transverse to strips)
- incident in 3mm along strips (const $p=134\text{um}$)
- events within 7ns of sampling clock

measure resolution of CBC module from residual

- using telescope for track extrapolation
- factoring out telescope spatial resolution

resolution:

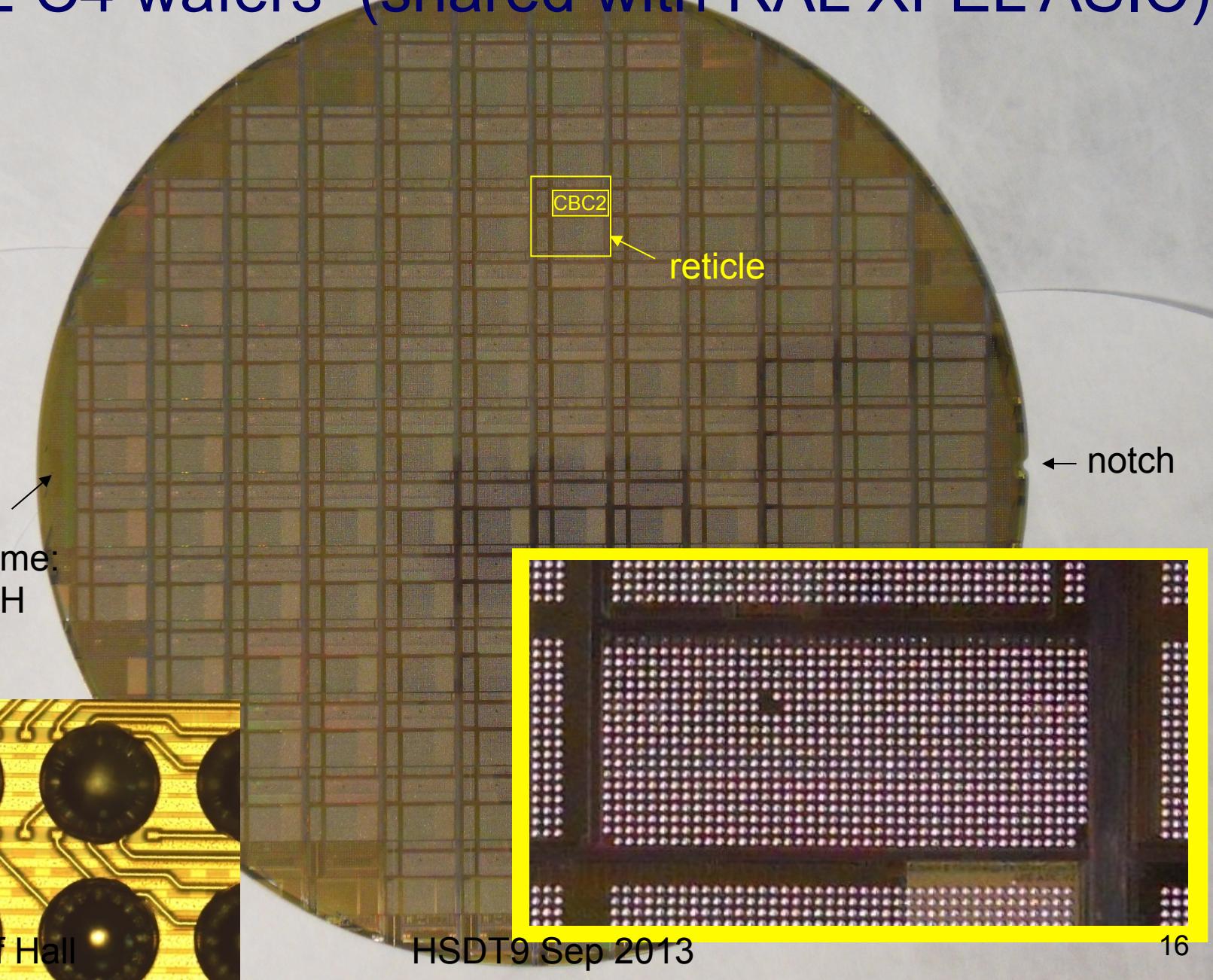
29.4 um



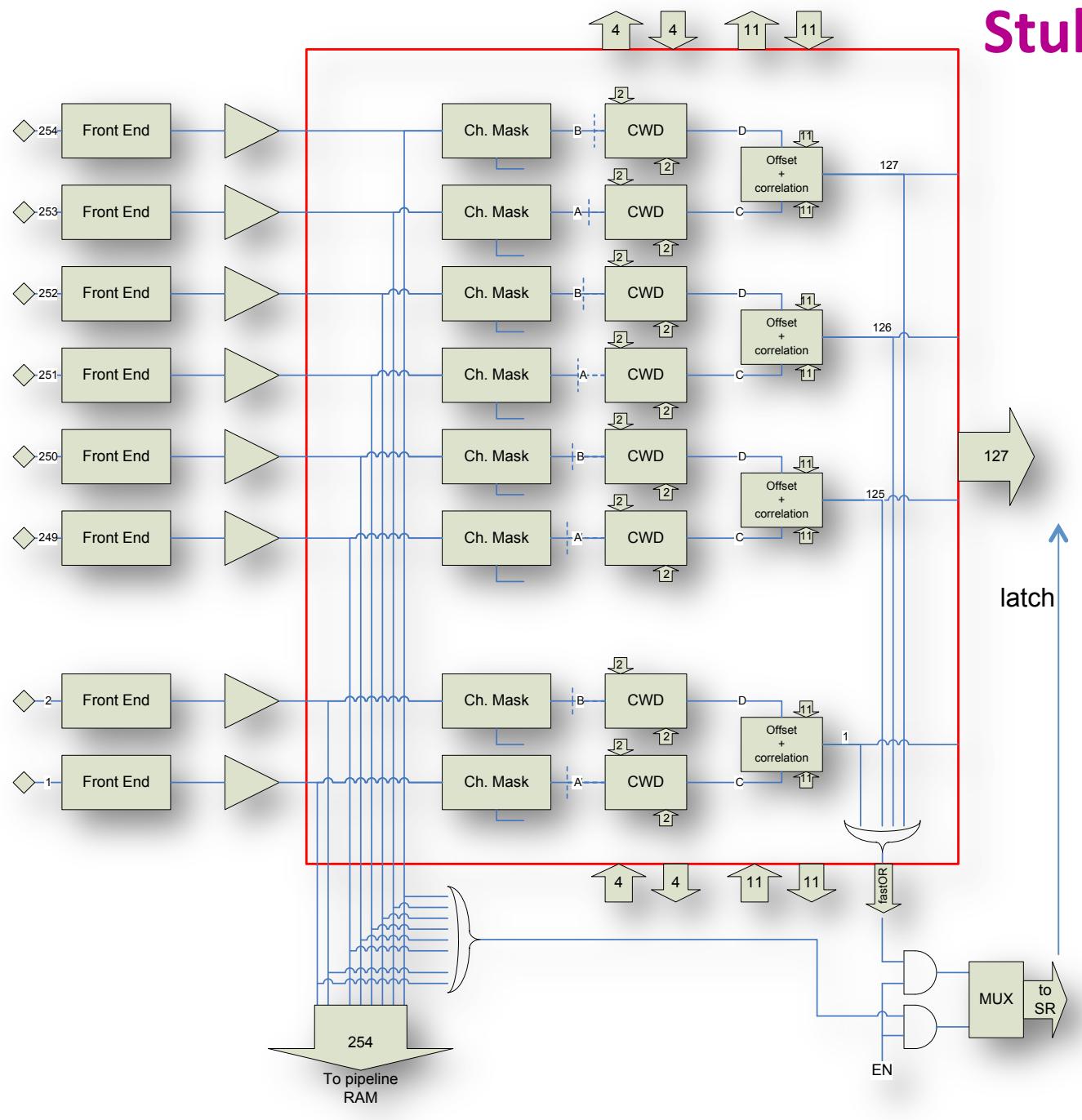
CBC -> CBC2: New features

- 250 μ m pitch C4 layout
 - aim for commercially assembled module
 - some gains in bond inductance
 - back edge wire-bond pads for wafer probe
- 254 channels for 127 + 127 strips
- correlation logic for stub formation
 - between top & bottom strips
 - vetoes wide clusters
- Test pulse
 - no time to implement on CBC
 - & other minor circuit improvements
- Improved DC-DC (CERN)
- received Jan 2013 – fully functional

CBC2 C4 wafers (shared with RAL XFEL ASIC)



Stub finding Logic



Individual mask for noisy channels
→ 254b from I2C reg.
(can be also used to inhibit coincidence logic)

Need to be able to inhibit stub shift register operation
→ 1b EN from I2C reg.

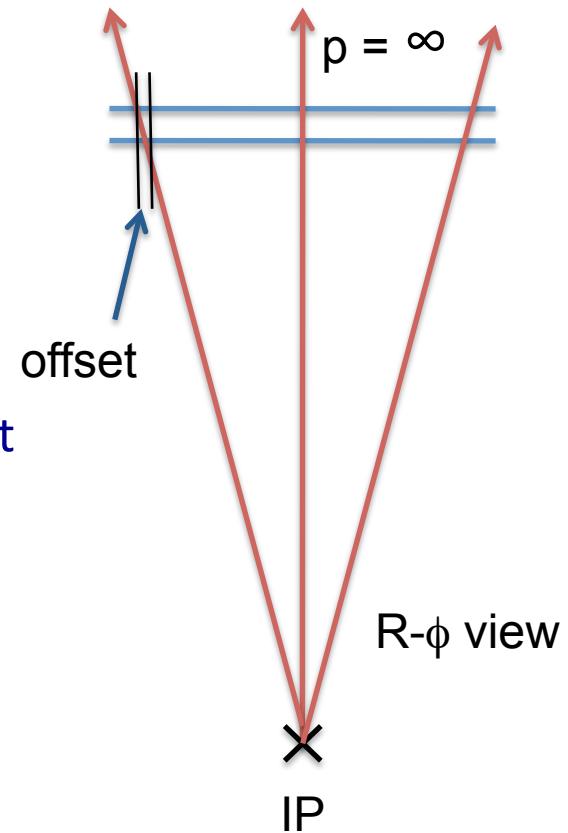
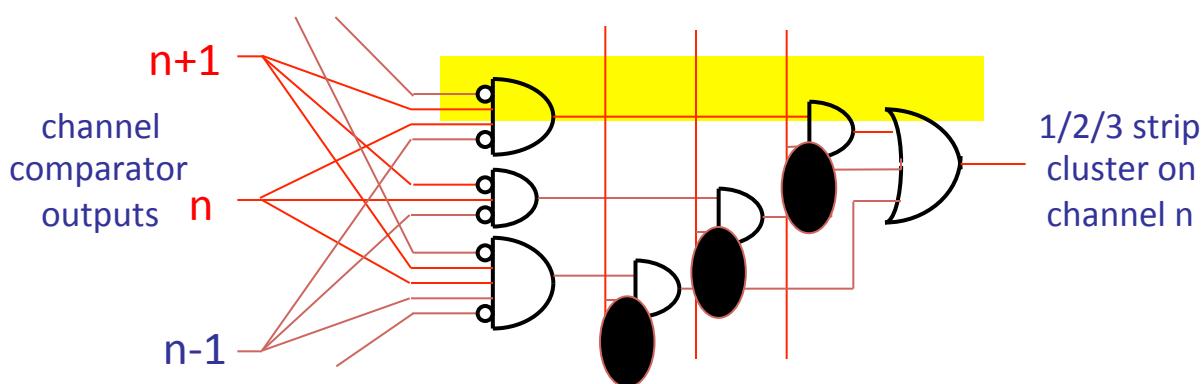
254-OR of channel outputs to signal any activity on chip

127-OR of stubs to control the stubs SR readout

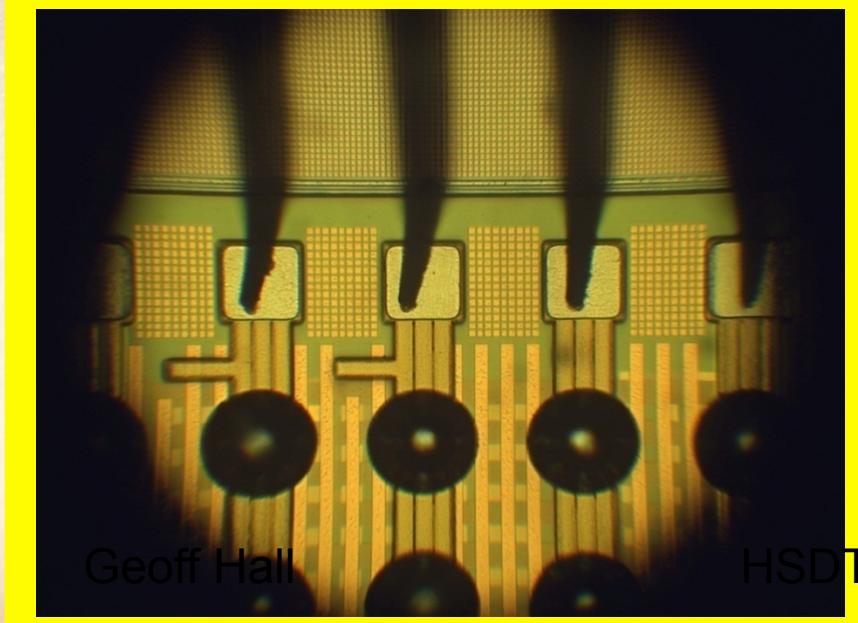
@40MHz

Stub logic features

- Cluster width
 - exclude clusters wider than 3 strips
- Offset correction and correlation
 - programmable window, selects pT
 - up to +/-8 channels
 - programmable offset, adjust lateral displacement
 - up to +/-3 channels

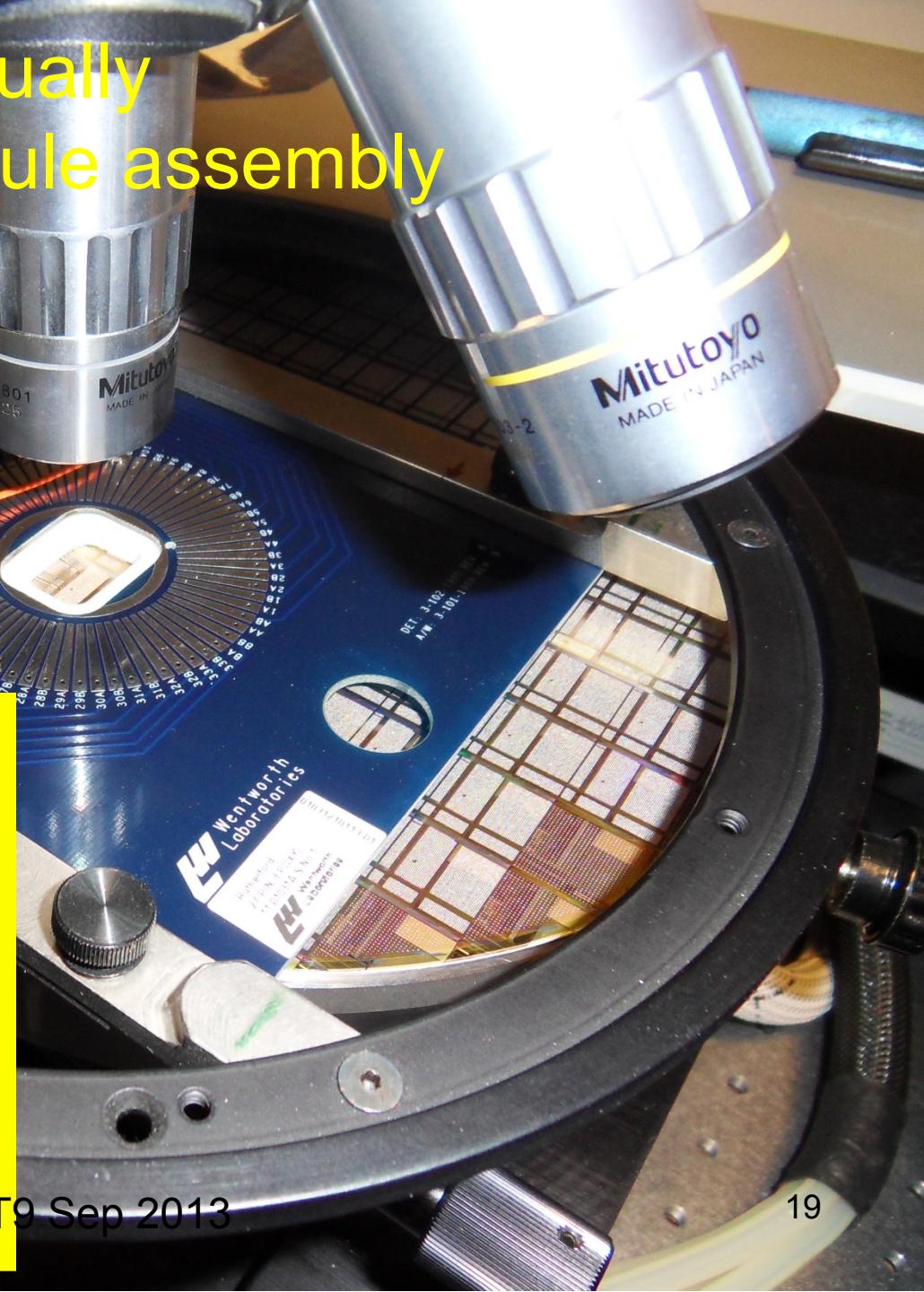


first wafer probed manually
to select chips for module assembly



Geoff Hall

HSDT9 Sep 2013



19

final yield for 1st wafer

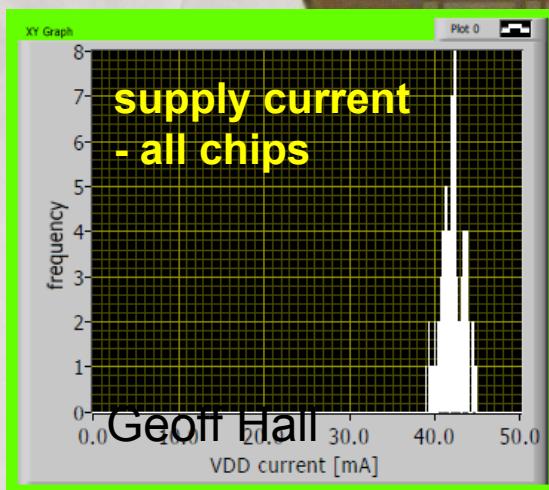
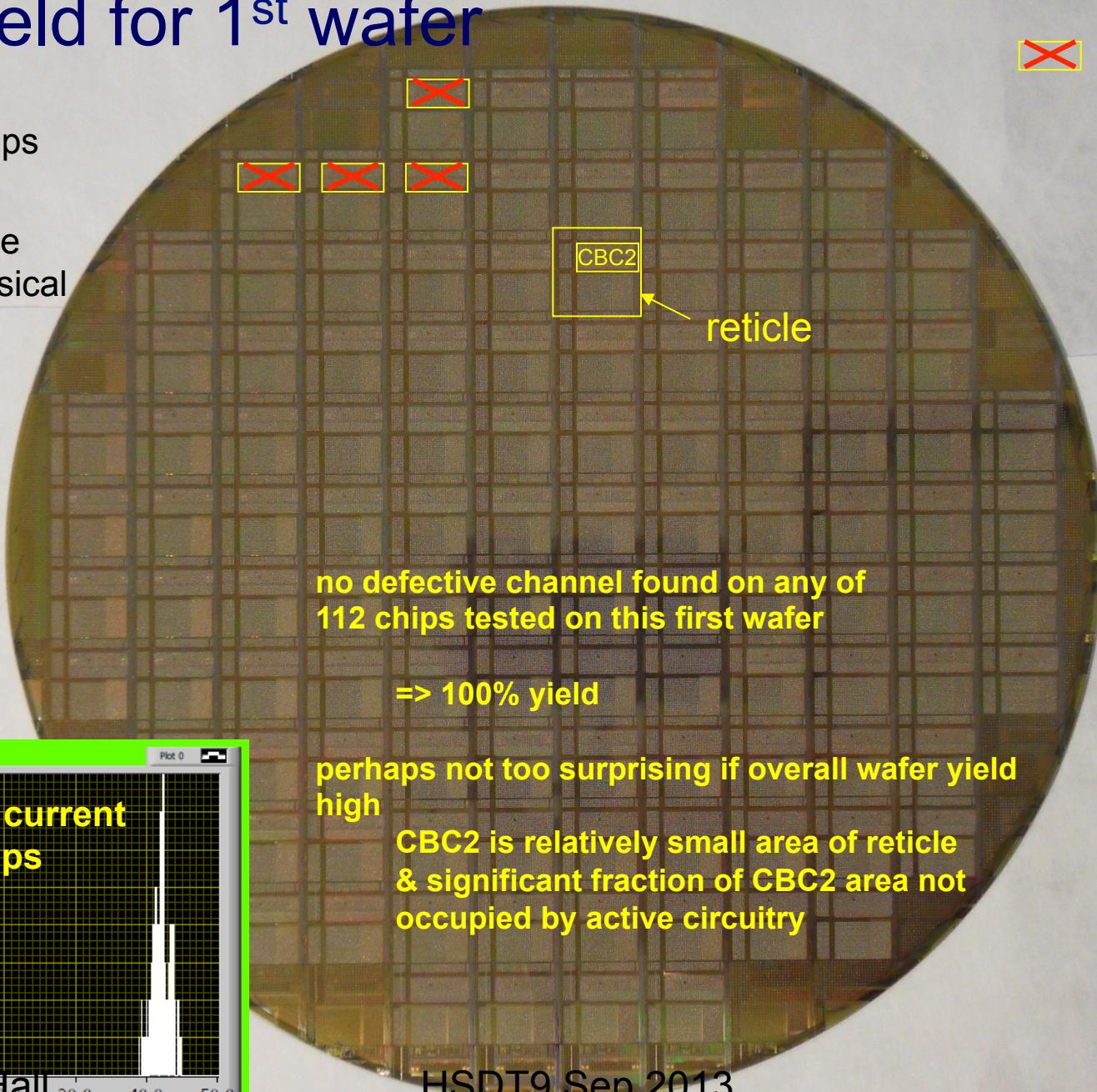
 bad chip

112 reticles

108 good chips

4 bad chips

bad chips due
solely to physical
damage
from
probe
card



no defective channel found on any of
112 chips tested on this first wafer

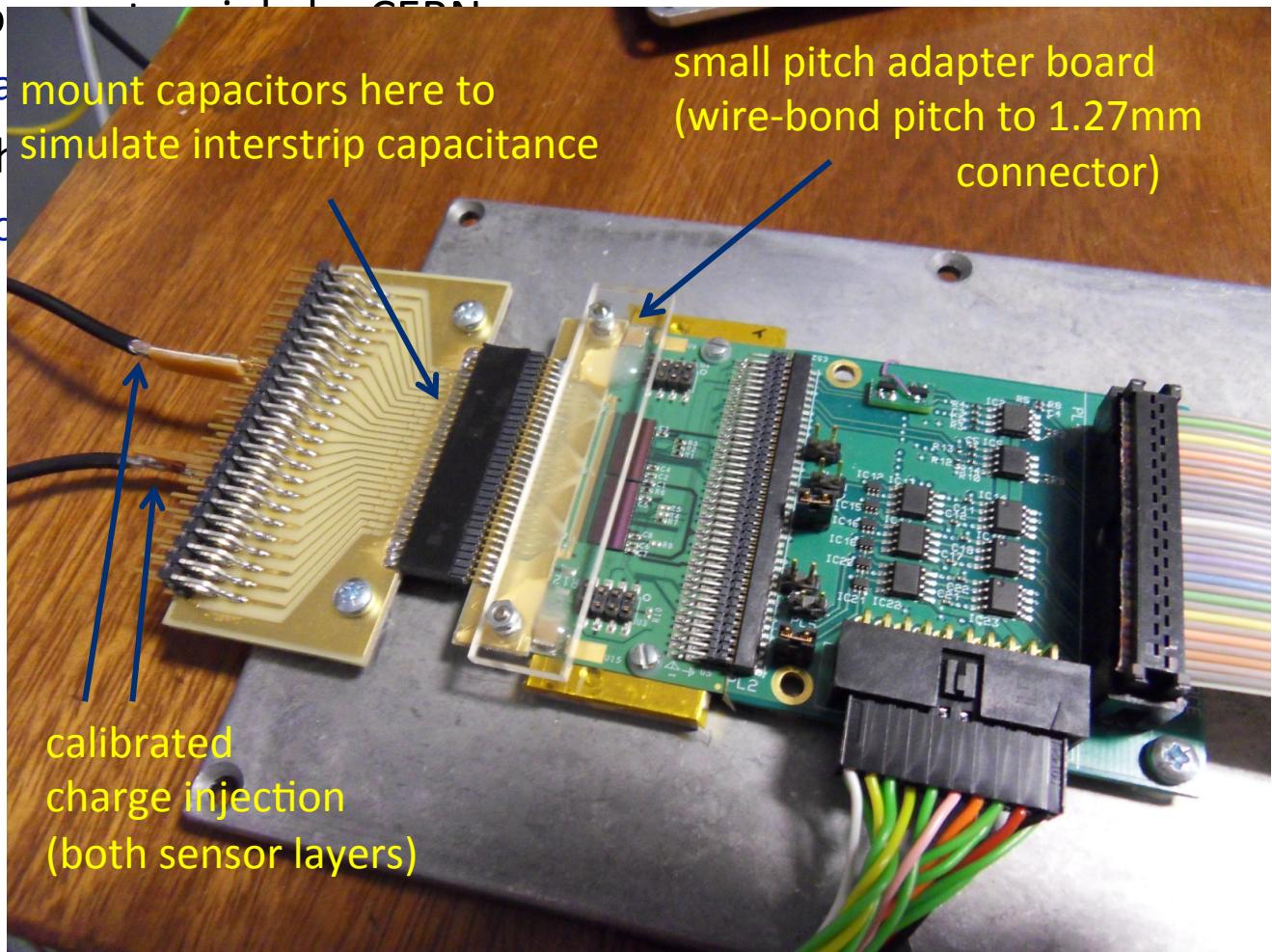
=> 100% yield

perhaps not too surprising if overall wafer yield
high

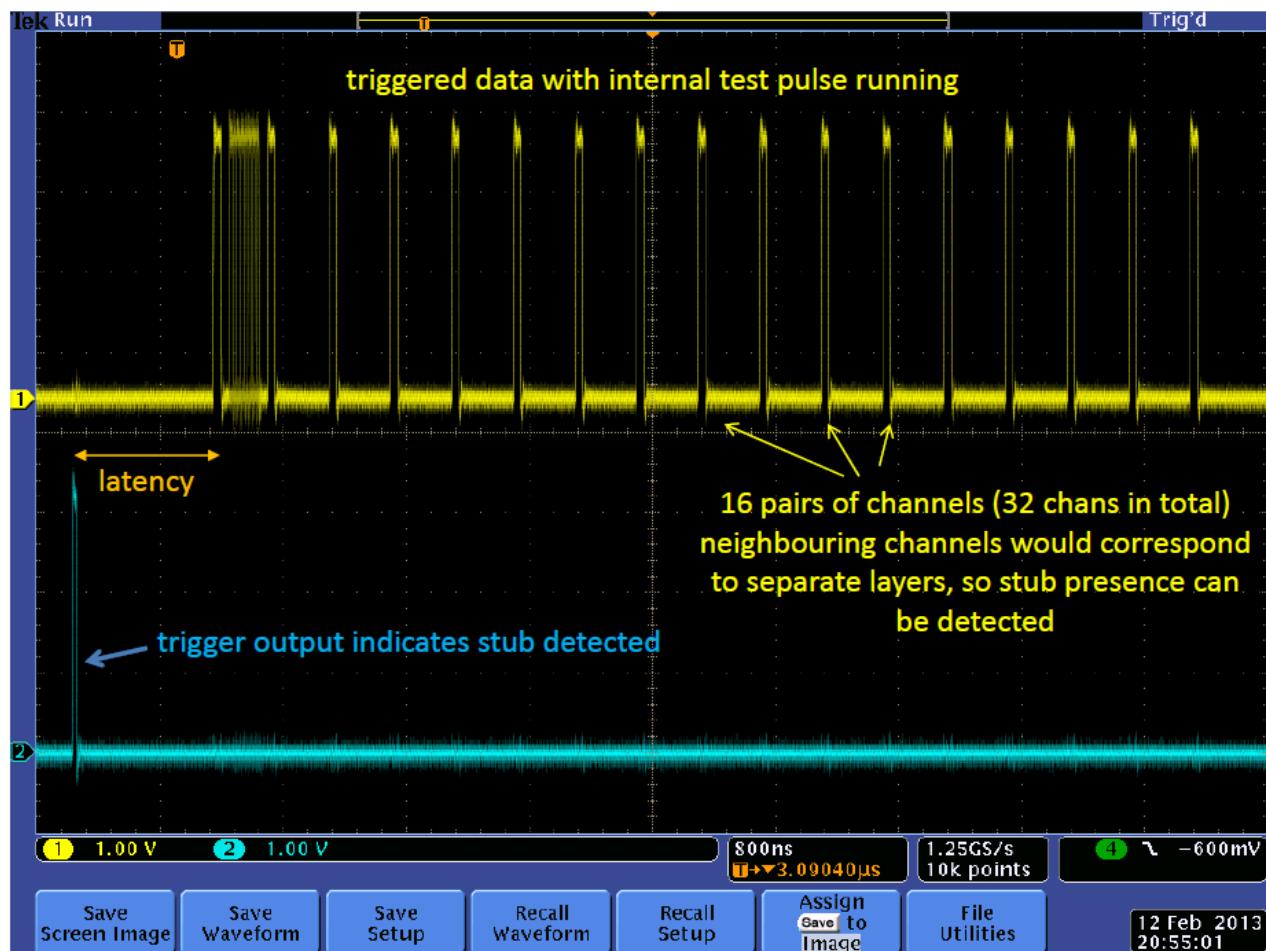
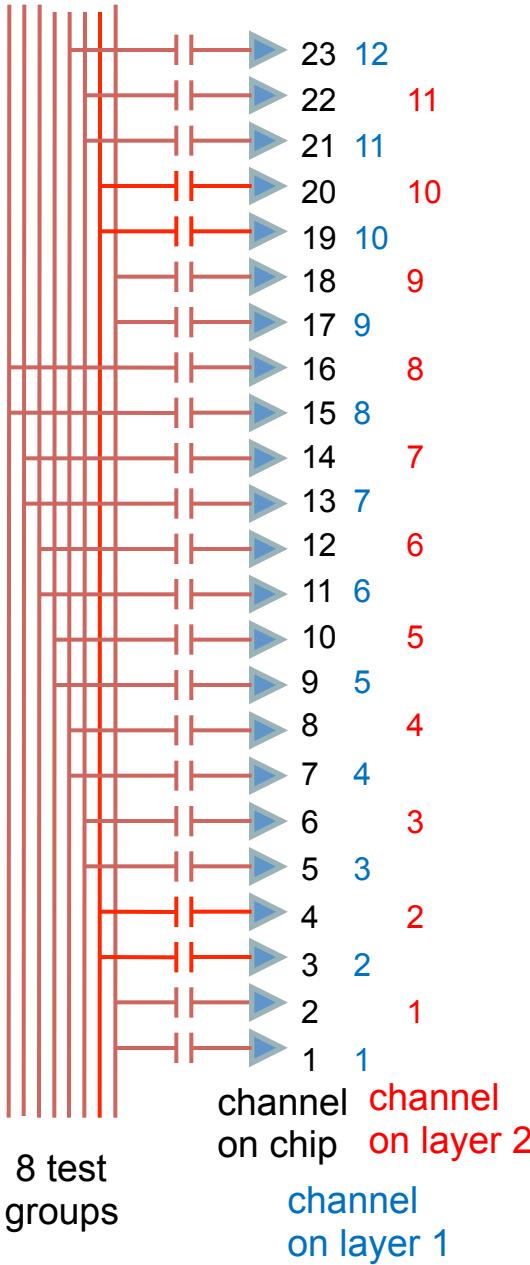
CBC2 is relatively small area of reticle
& significant fraction of CBC2 area not
occupied by active circuitry

2S module

- Development with CMS team
- Substrate development
 - Hybrid procured a small amount capacitors here to simulate interstrip capacitance
- First version: 2 channels
 - electrical validation

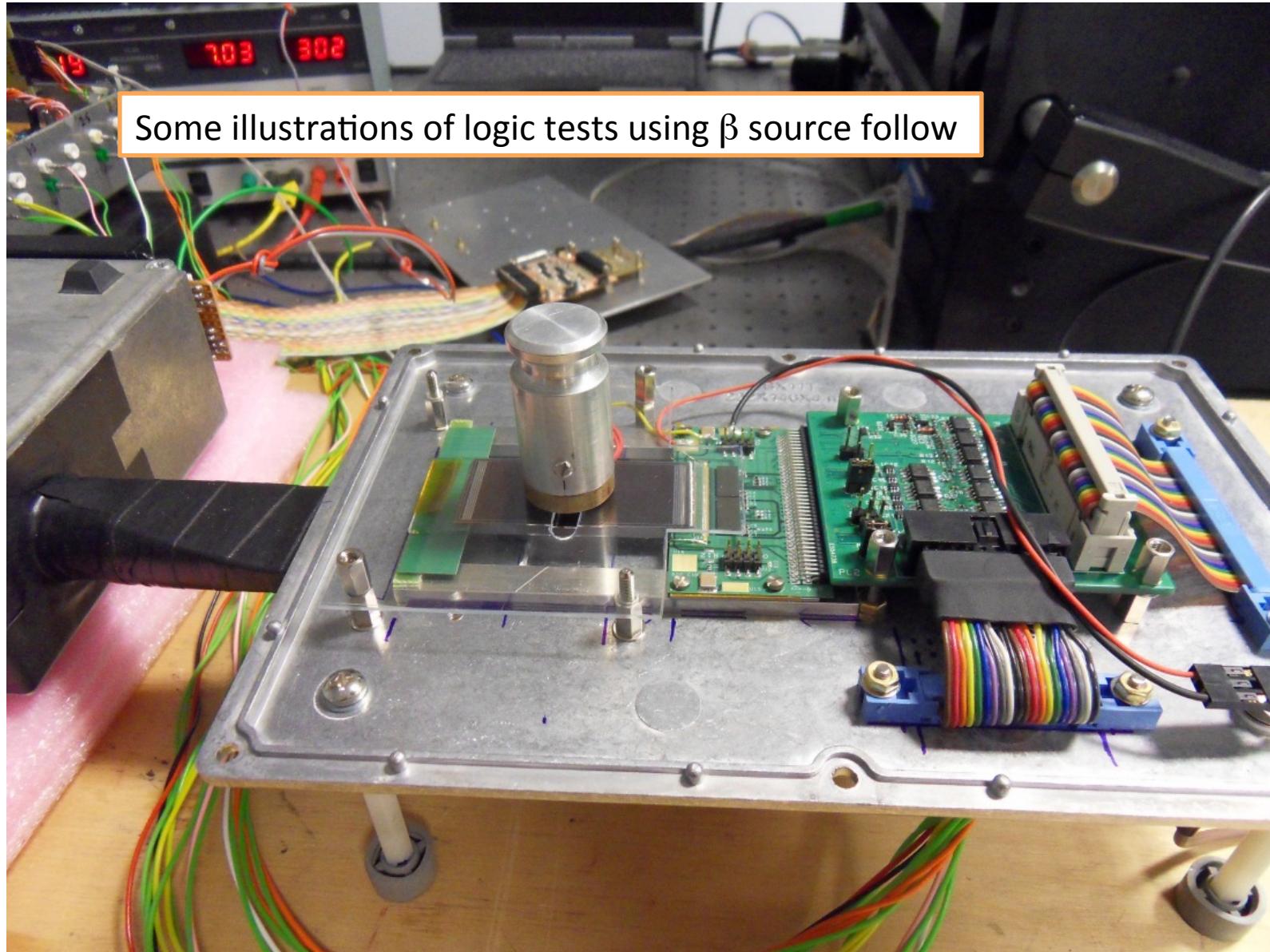


Result with test pulse

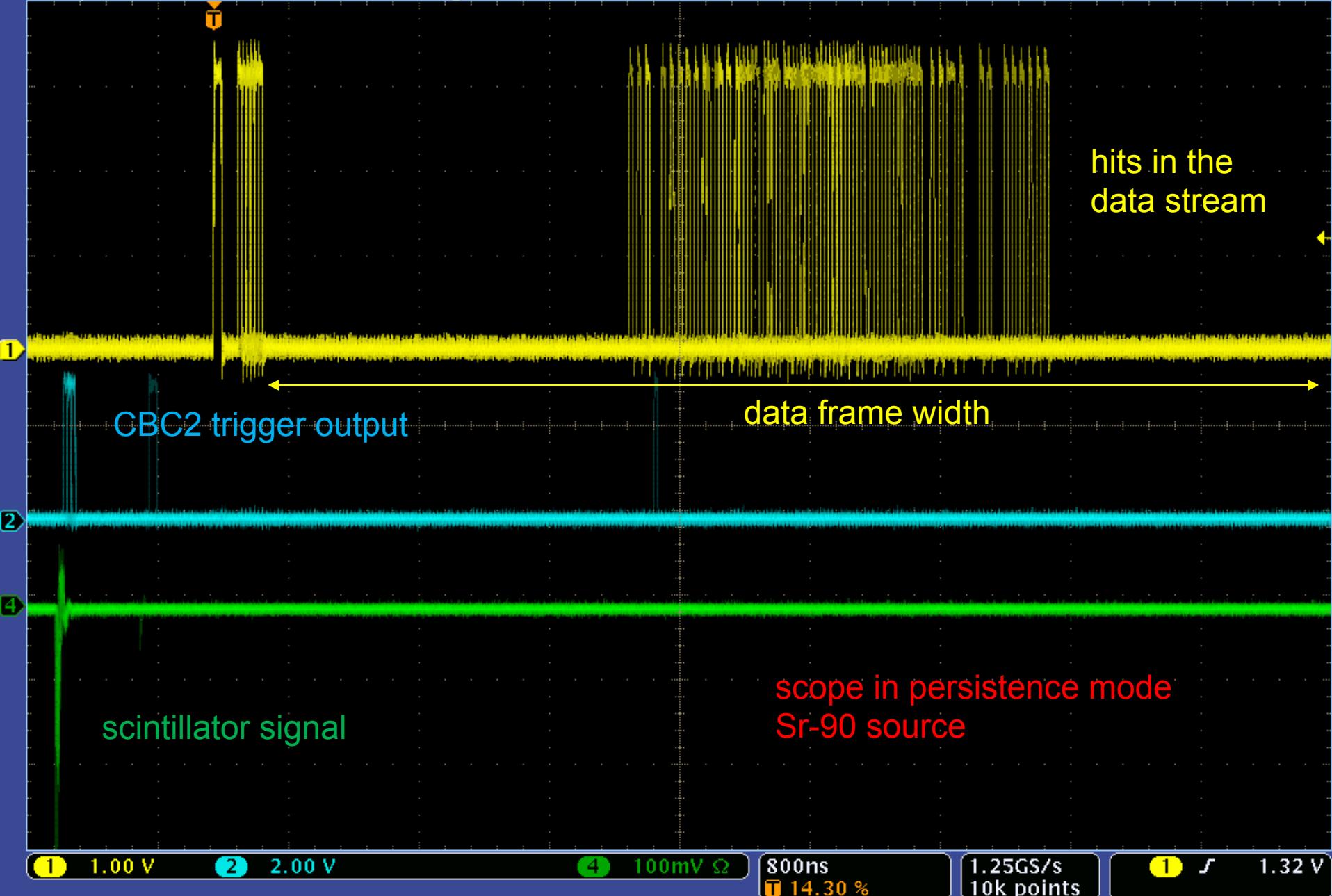


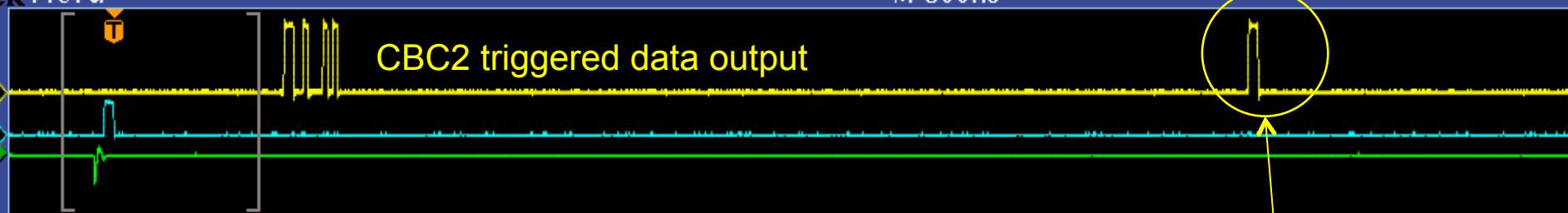
- Proves basic functionality but need real data for better test

2S mini-module

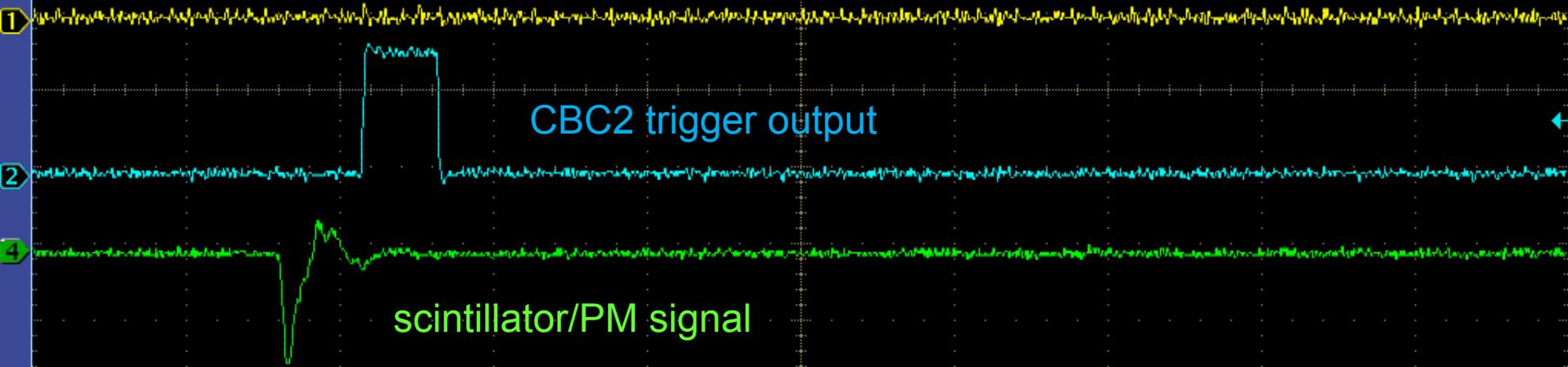


Tek Stop





hits in the data stream



① 1.00 V

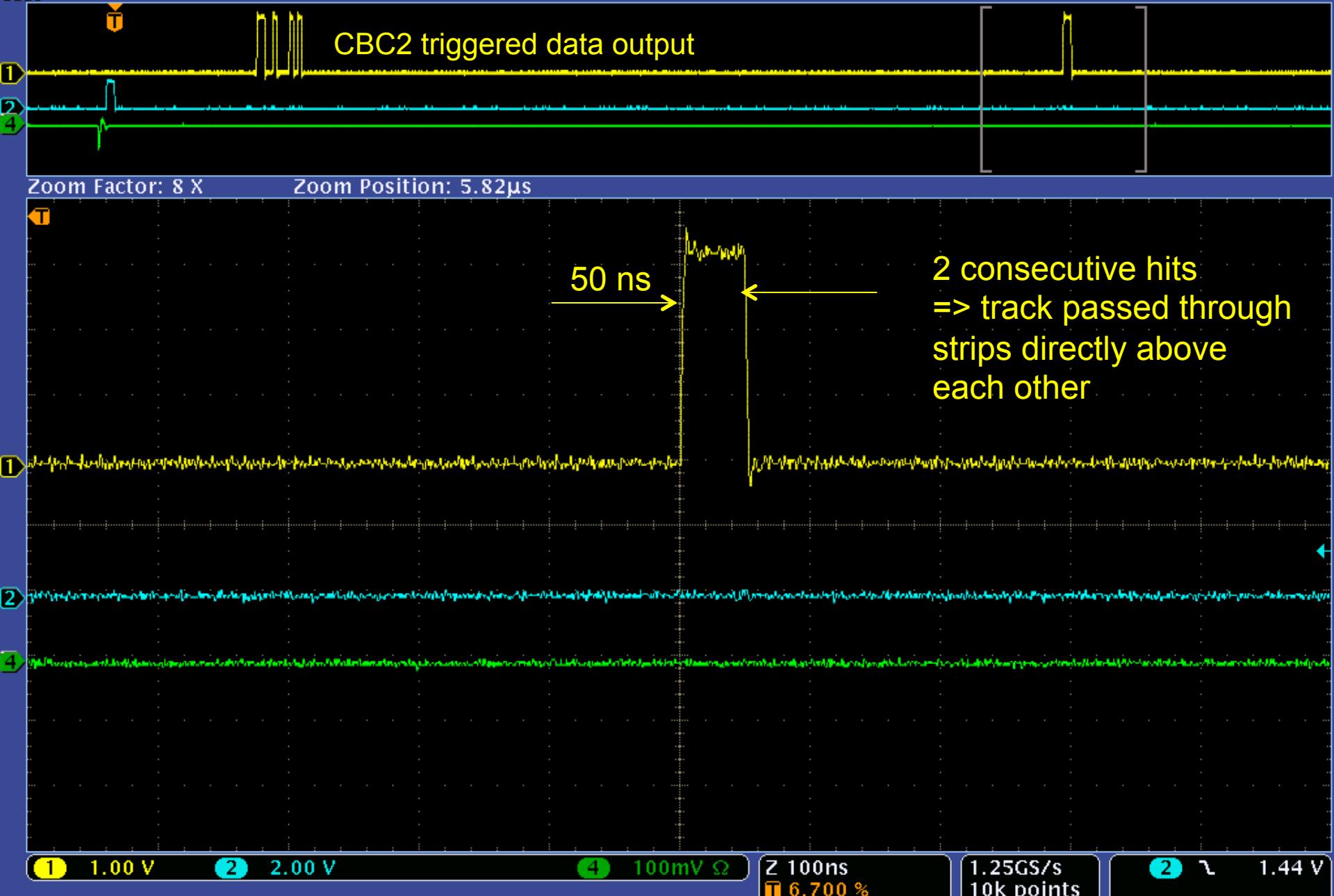
② 2.00 V

④ 100mV

Z 100ns
6.700 %

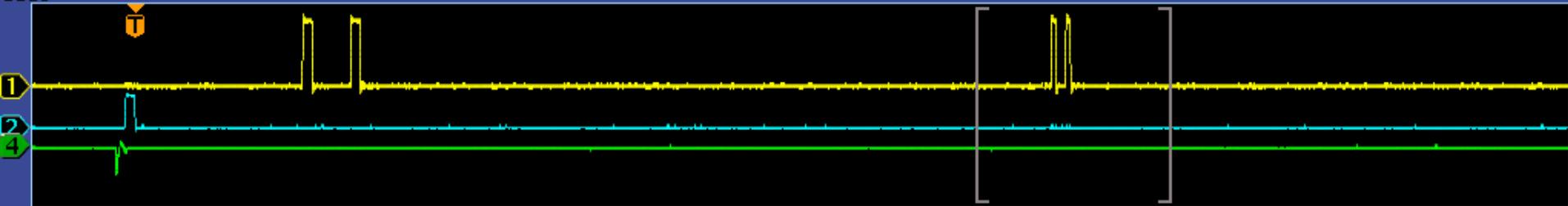
1.25GS/s
10k points

② 1.44 V



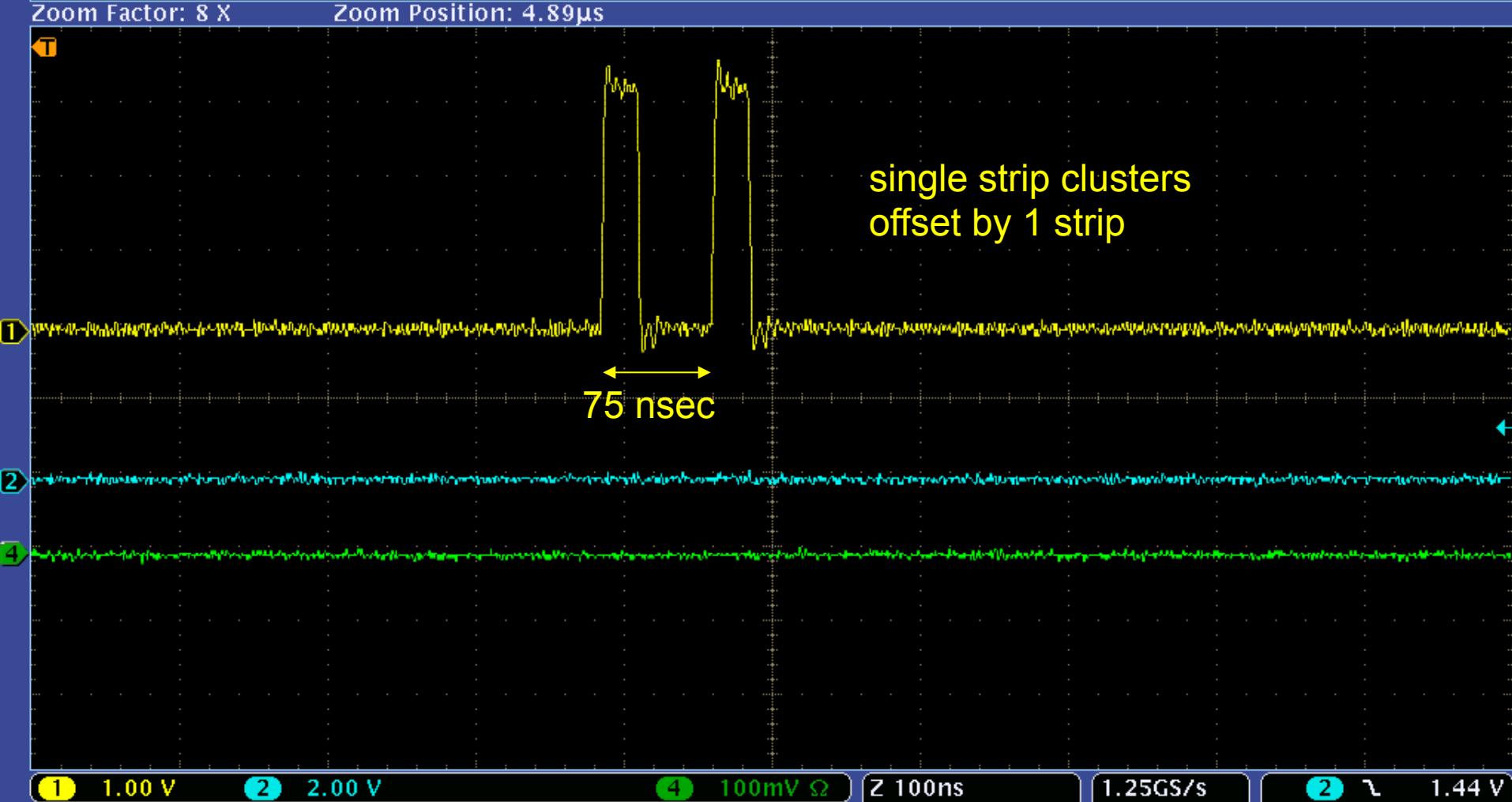
Tek PreVu

M 800ns



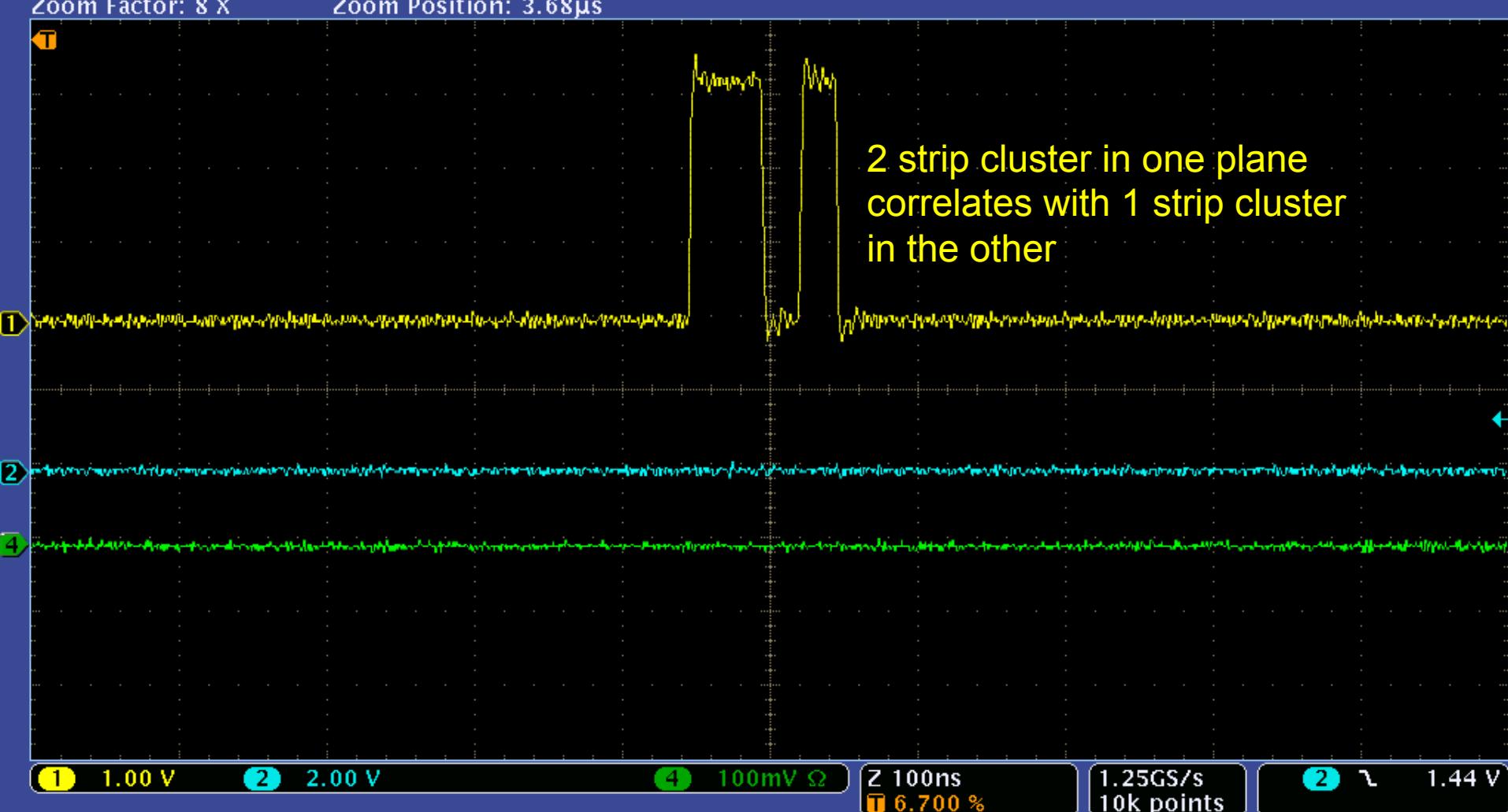
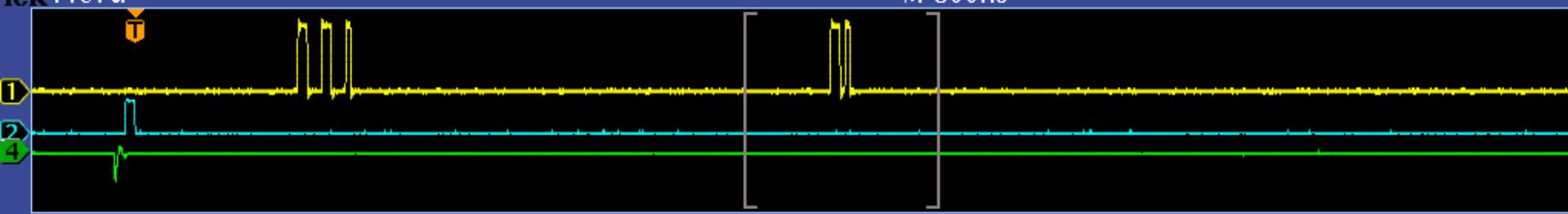
single strip clusters
offset by 1 strip

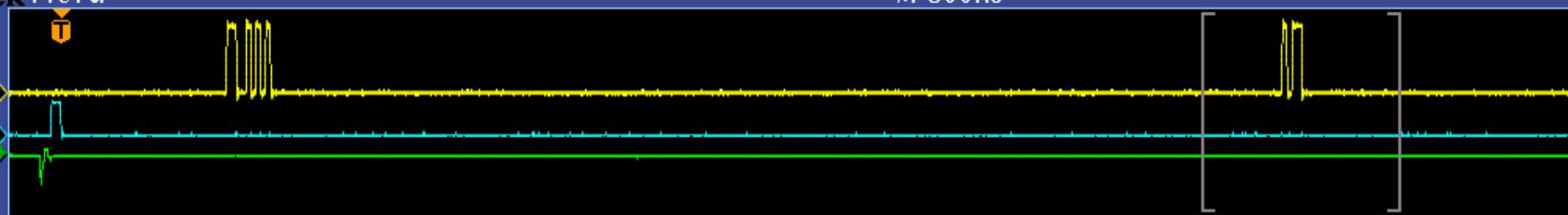
75 nsec



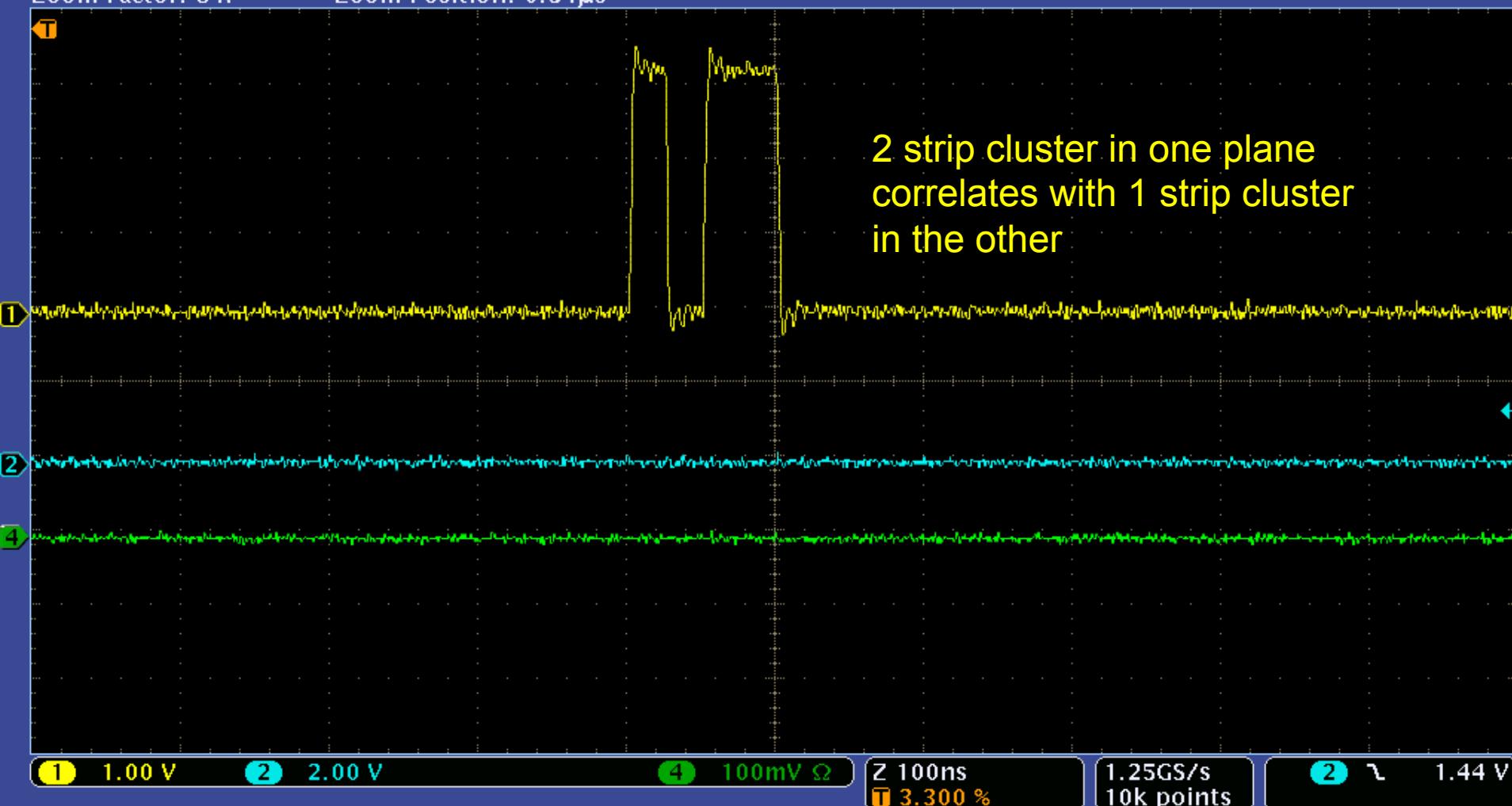
Tek PreVu

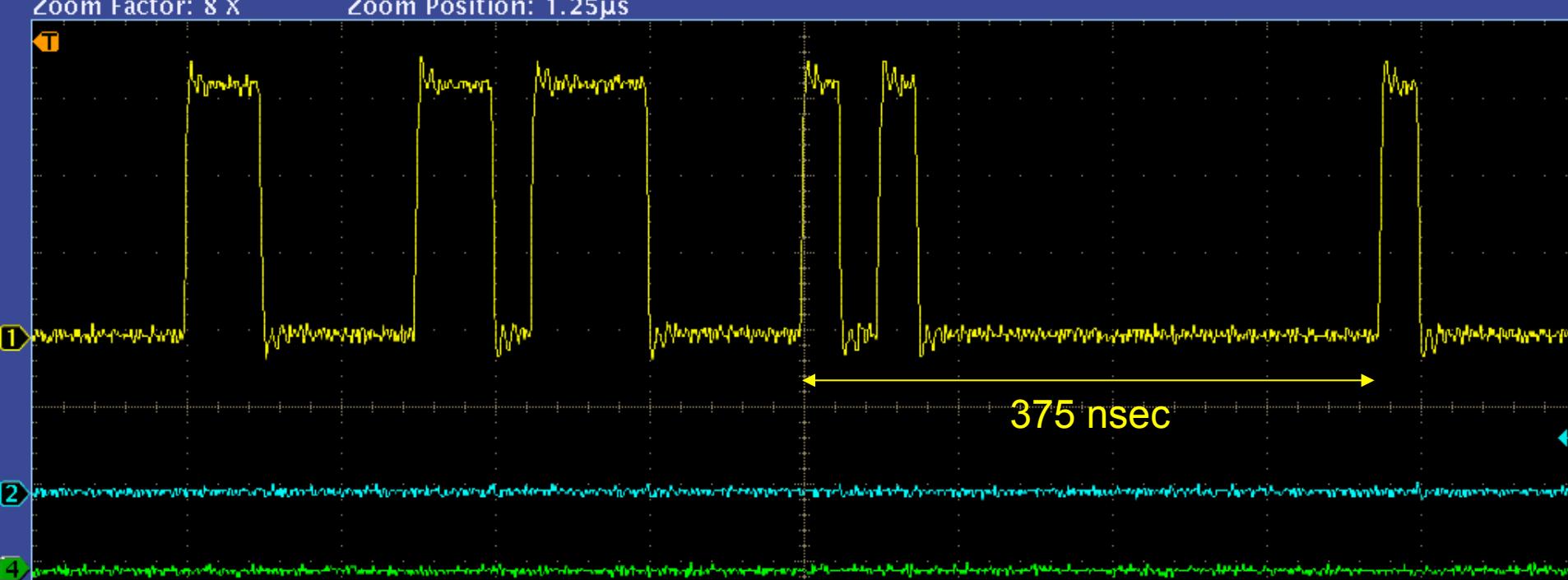
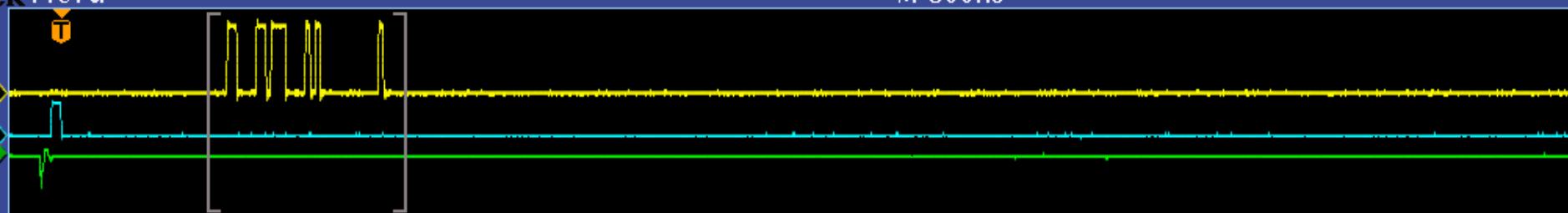
M 800ns





2 strip cluster in one plane
correlates with 1 strip cluster
in the other





2 strip cluster in lower sensor
correlates with 1 strip cluster
in the other, offset by 7 strip

1 1.00 V

2 2.00 V

4 100mV Ω

Z 100ns
3.300 %

1.25GS/s
10k points

2 λ 1.44 V

Rough road map

2011

CBC1

- analogue front end in 130nm
- wirebonded
- binary logic
- L1 triggered readout only, non-sparsified

2012

CBC2

- C4 bump-bonded
- full hit correlation logic
- L1 triggered non-sparsified readout, fast trigger OR

2013

2014

CBC3

- full readout architecture defined
- final data format
- additional correlation logic

2015

2016

CBC4

- optimisation
- final version

2017

2S-Pt prototype module studies

2S-Pt final module studies

start production

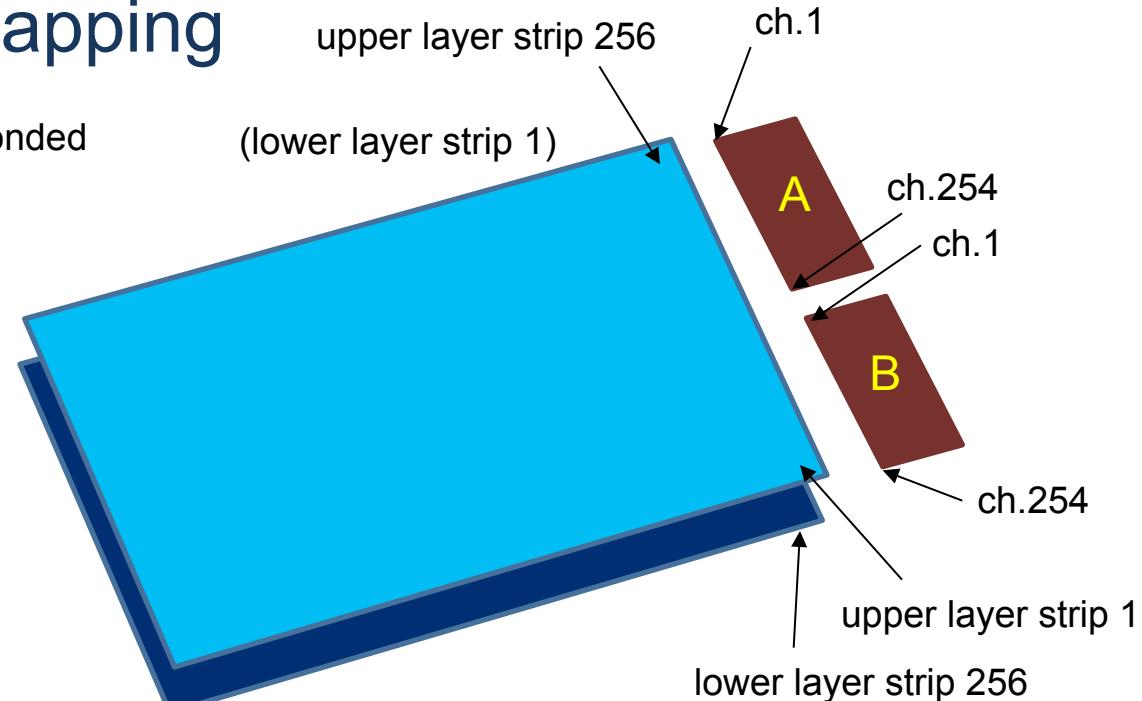
Summary & conclusions

- Two successful iterations of new outer Tracker ASIC
- First prototype version of 2S module in hand
 - functions well in lab environment
 - first beam tests foreseen late 2013
- Road map for future developments
 - detailed schedule depends on complete upgrade plan and HL-LHC approval process

Backup slides

channel to strip no. mapping

2 edge channels on each sensor not bonded
(i.e. strips 2 - 255 inclusive bonded)



chip channel vs. sensor strip #

chip A

2 4 6 8 250 252 254

chip B

2 4 6 248 250 252 254

upper
sensor

255 254 253 252 131 130 129

128 127 126 5 4 3 2

chip A

1 3 5 7 249 251 253

chip B

1 3 5 247 249 251 253

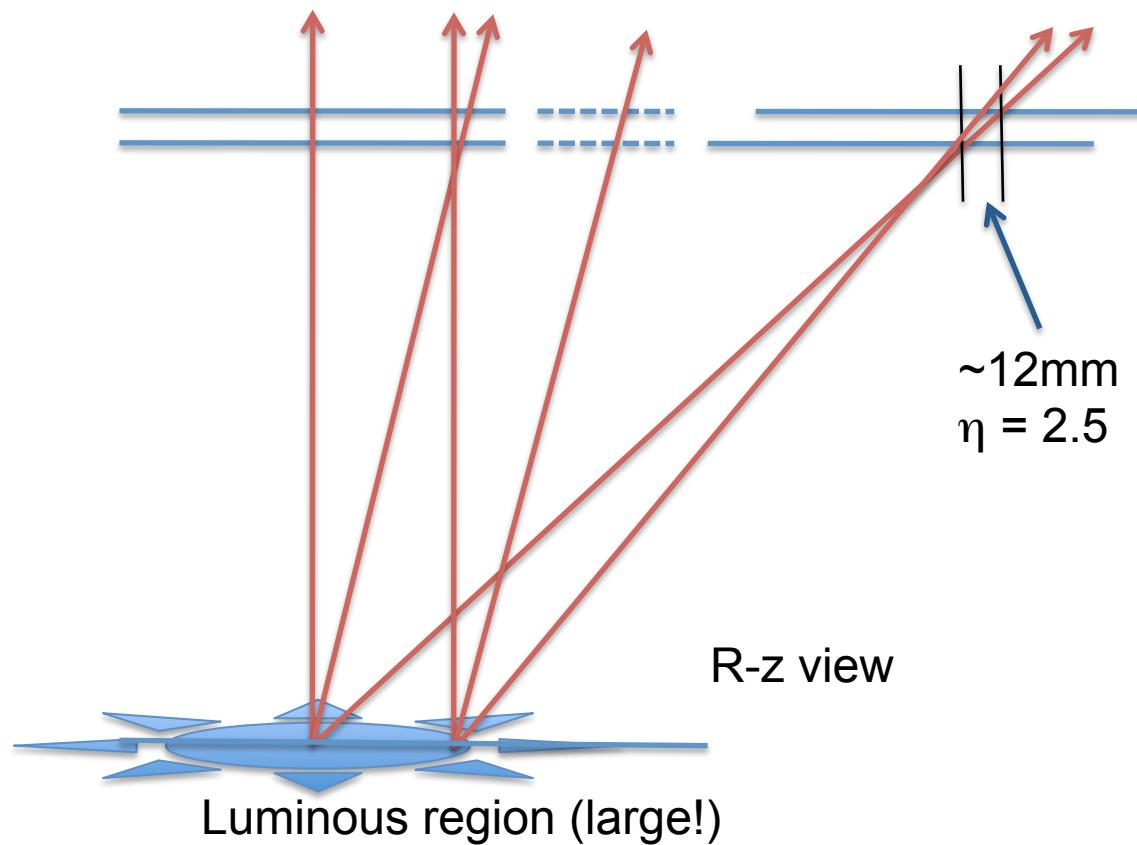
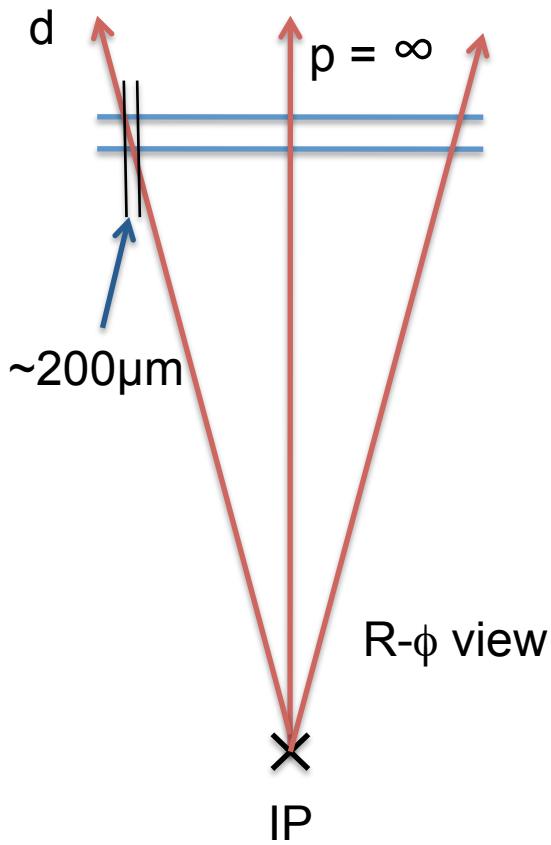
lower
sensor

2 3 4 5 126 127 128

129 130 131 252 253 254 255

Comparison logic

- Modules are flat, not arcs
- Compensate for Lorentz drift
- Orientation of module
=> position dependent logic



- Family of modules with offsets in z

CBC3 - the “final prototype”

next version of chip should incorporate all features required for HL-LHC

- **final choices for front end**

- ½ strip cluster resolution

- 2 strip cluster position assigned to mid-point

- **stub data definition**

- 8 bits address (for ½ strip resolution) of cluster in bottom layer

- 5 bit bend information

- address of correlating cluster in top layer

- **stub data formatting & transmission to concentrator**

- 13 bit / stub, up to 3 stubs/BX => 39 bits

- +1 bit unsparsified L1 triggered readout data

- => 40 bits / 25 nsec

- e.g. 10 lines at 160 Mbps (per chip)

- **other useful features**

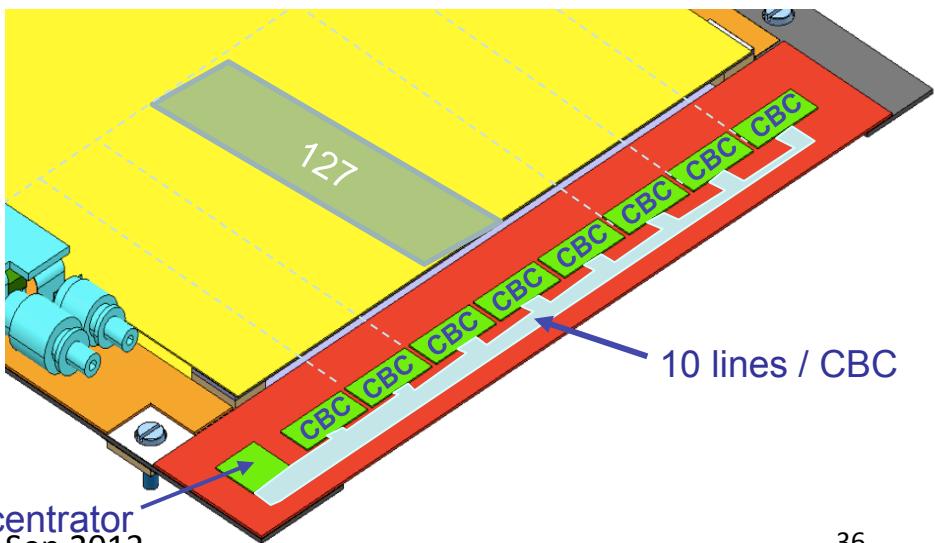
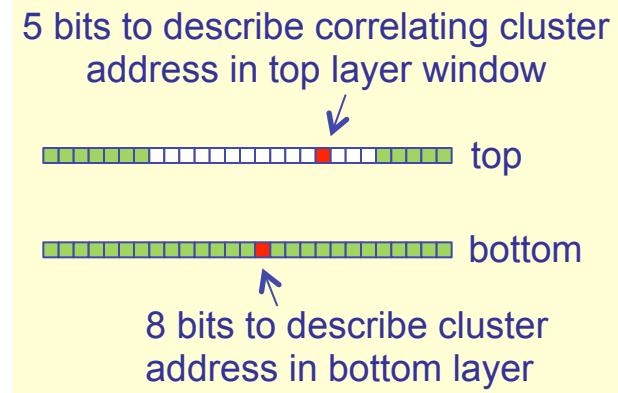
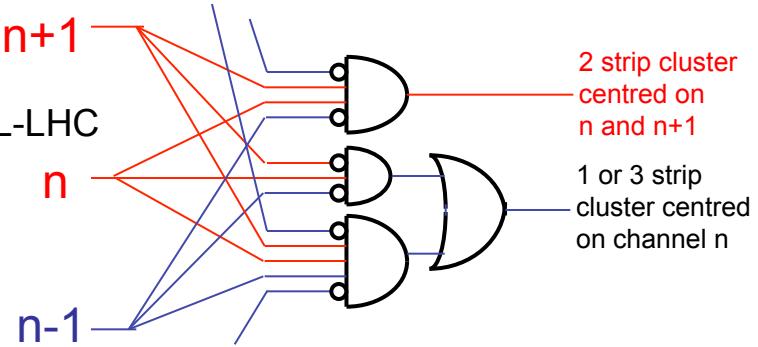
- e.g. slow ADC to monitor bias levels

- ...

CBC data to concentrator

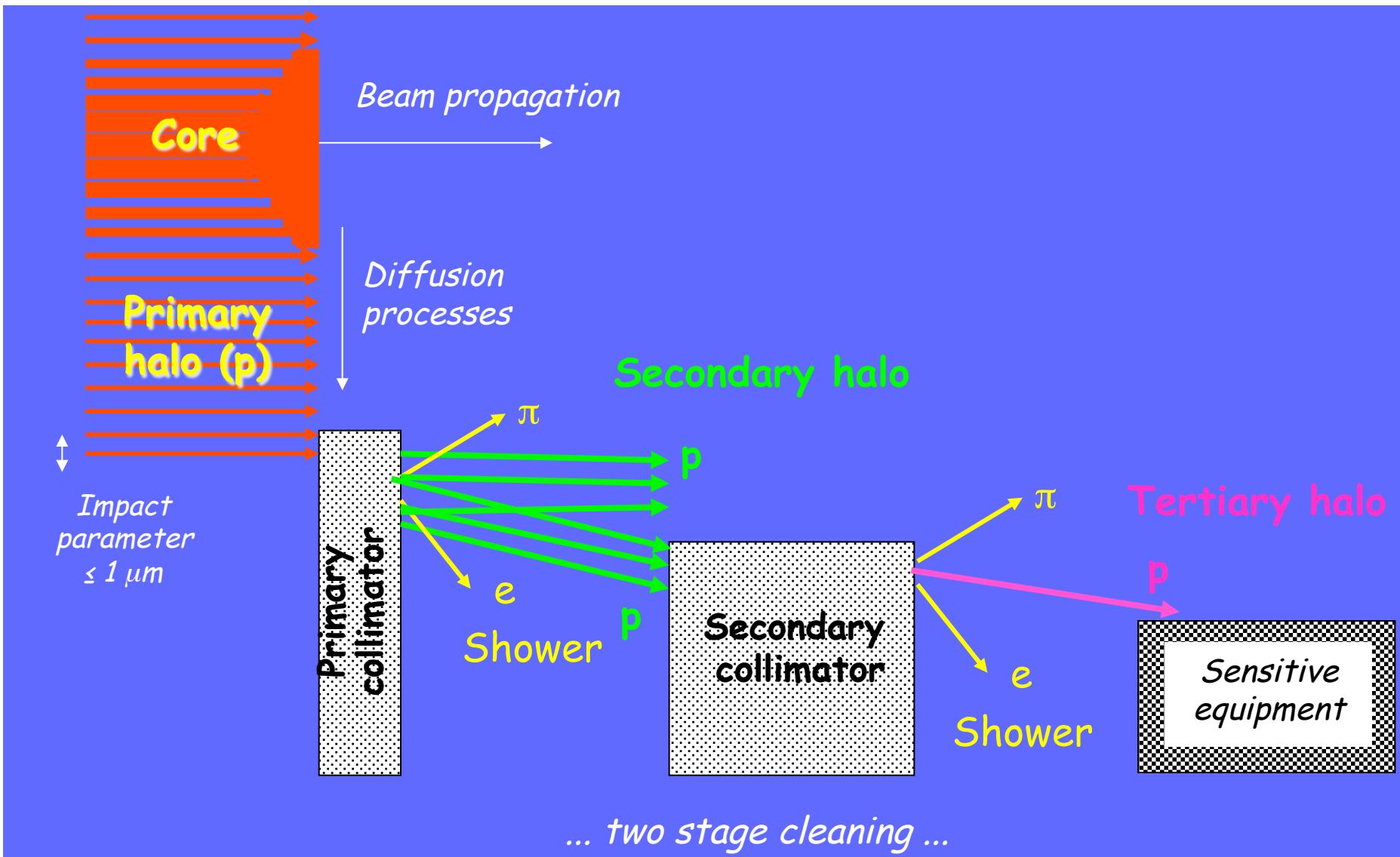
S1	B1	B1							
B1	B1	B1	S2						
S2	B2	B2	B2	B2	B2	S3	S3	S3	S3
S3	S3	S3	S3	B3	B3	B3	B3	B3	R

25 ns

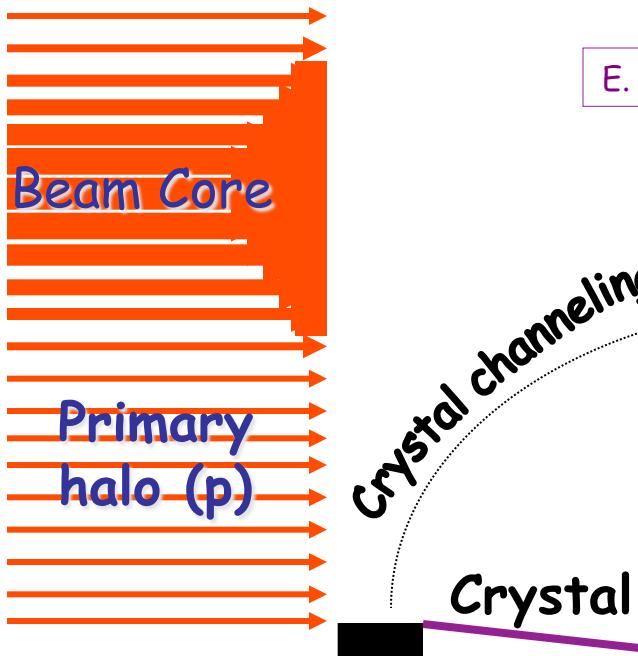


Principle of Beam Collimation

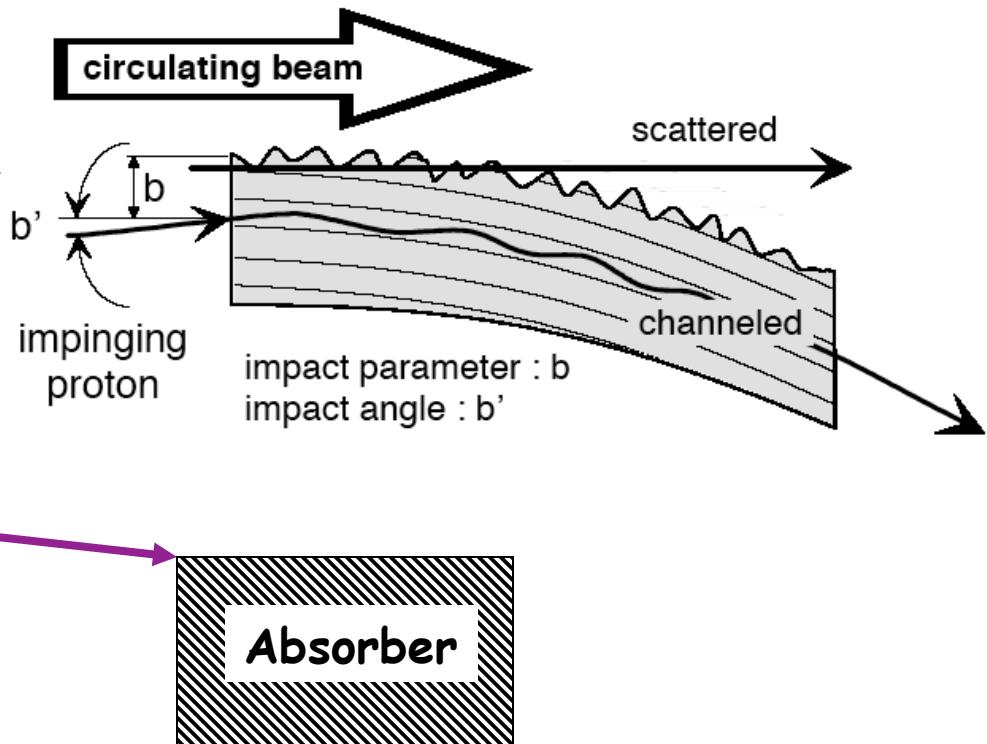
Walter Scandale, 2010



Crystal collimation



E. Tsyganov & A. Taratin (1991)



$$\alpha = \mathcal{O}(100\mu\text{rad})$$

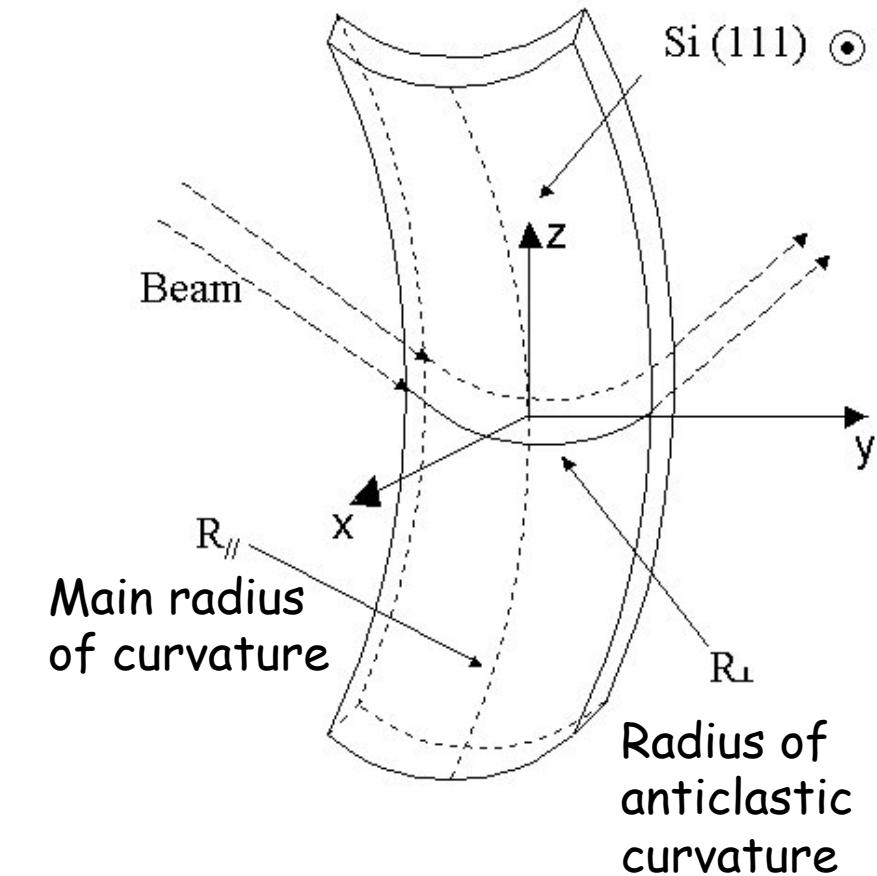
$$\ell = \mathcal{O}(10^{-2} \text{ m})$$

- ◆ Coherent deviation of the primary halo
- ◆ Very small probability of inelastic interaction in the crystal
- ◆ Larger collimation efficiency
- ◆ Less impedance
- ◆ Reduced tertiary halo

Strip crystals

Built at IHEP - Protvino and at INFN - Ferrara

The main curvature due to external forces induces the anticlastic curvature seen by the beam



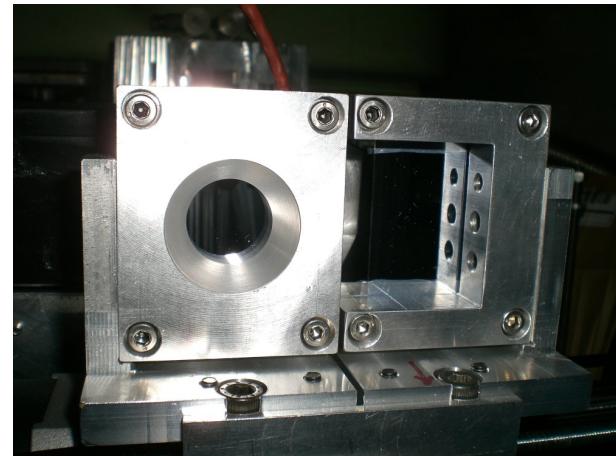
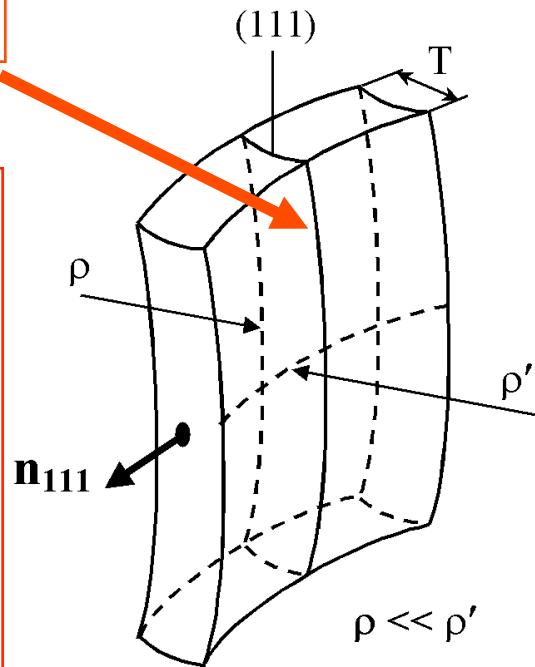
Quasimosaic crystals

Built at PNPI - Gatchina

Quasi-Mosaic effect (Sumbaev , 1957)

- The crystal is cut parallel to the planes (111).
- An external force induce the main curvature.
- The anticlastic effect produces a secondary curvature
- The anisotropy of the elastic tensor induces a curvature of the crystal planes parallel to the small face.

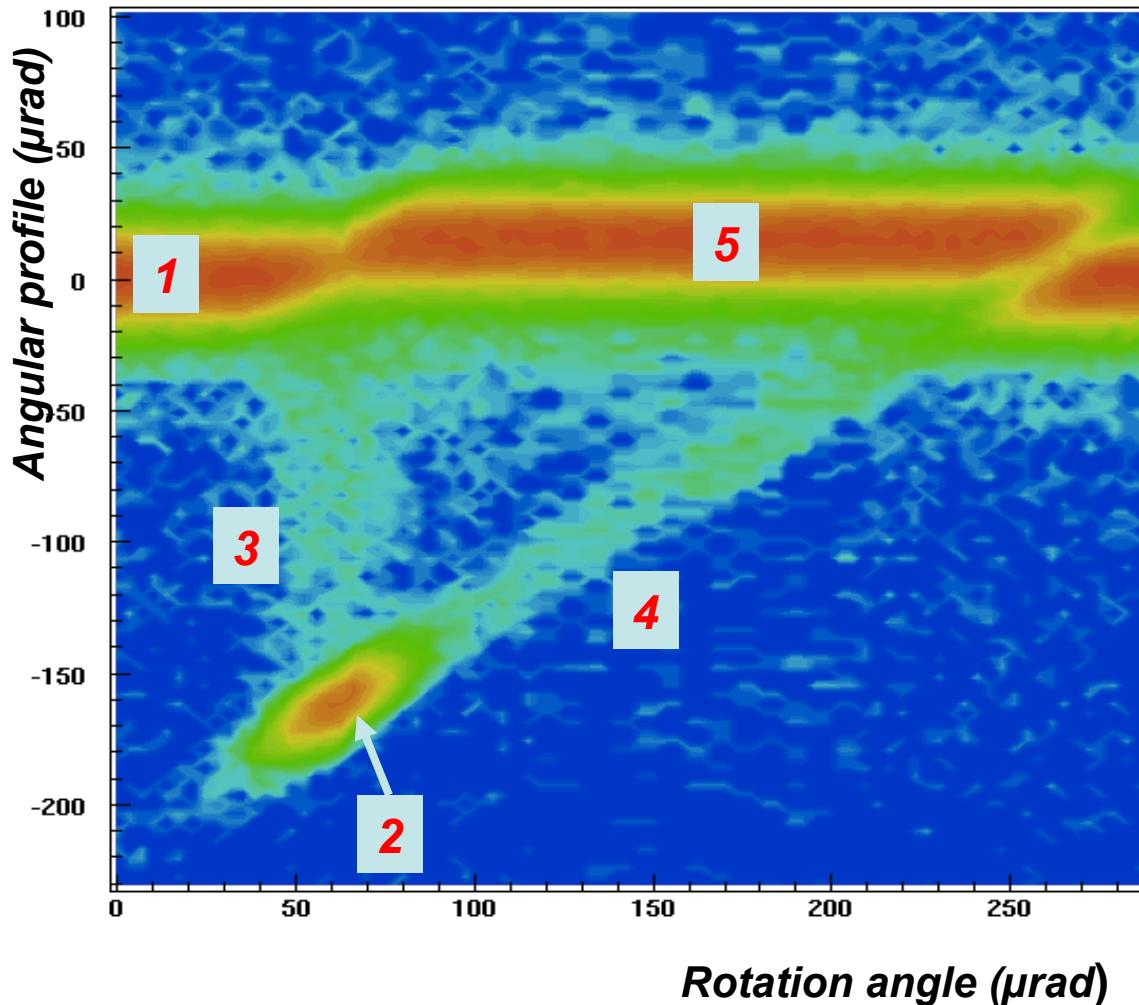
Beam direction



Crystal size: $0.7 \times 30 \times 30 \text{ mm}^3$

Angular beam profile as a function of the crystal orientation

9mm long Si-crystal deflecting 400GeV protons



The **angular profile** is the change of beam direction induced by the crystal

The **rotation angle** is angle of the crystal respect to beam direction

The **particle density** decreases from **red** to **blue**

- 1 - "amorphous" orientation
- 2 - channeling (50 %)
- 3 - de-channeling (1 %)
- 4 - volume capture (2 %)
- 5 - volume reflection (98 %)