CBC strip chip - power issues

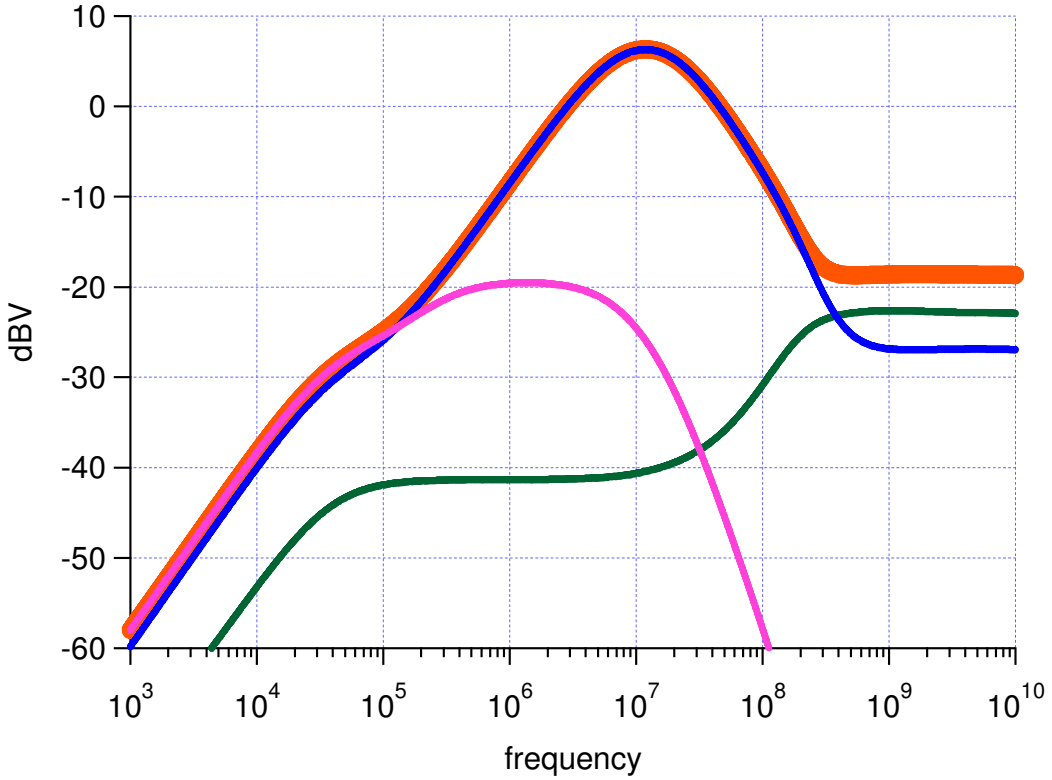
follows on from previous working group meeting – June ’09
http://indico.cern.ch/getFile.py/access?contribId=17&sessionId=9&resId=0&materialId=slides&confId=47292

OUTLINE

- brief reminder of relevant points from last time on PSR
- an LDO regulator design
- CBC front end performance when supplied by LDO

Mark Raymond – Imperial College

CBC FE PSR – as presented last time



preamp & postamp (no filtering)
preamp only (postamp supplied separately)
postamp only (preamp supplied separately)
preamp & postamp (with RC = filter (2.5Ω + 220nF))

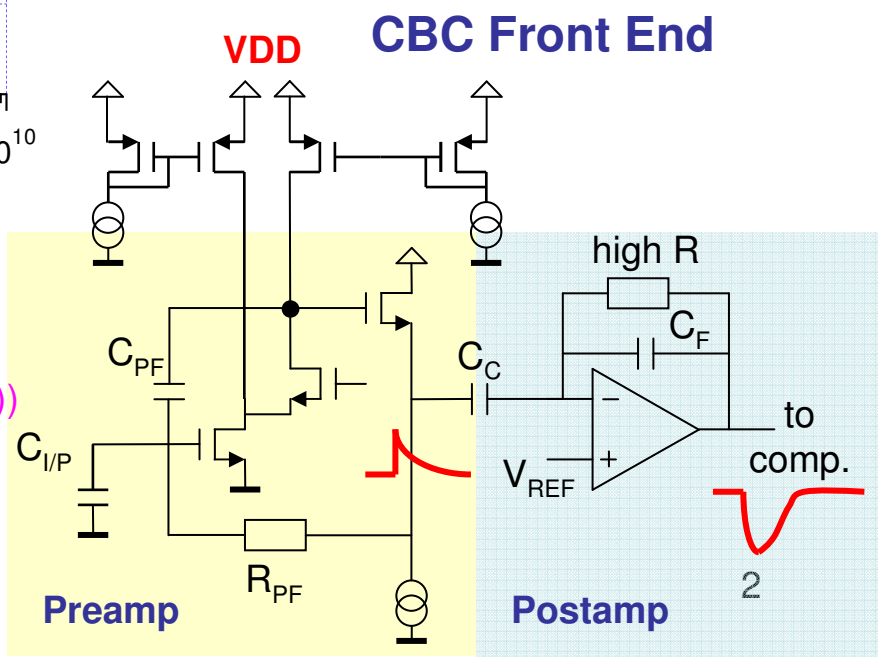
response to sinusoidal ripple on VDD supply to preamp, postamp or both

power supply rejection dominated by preamp response

no rejection at ~10 MHz

better at lower frequencies

filtering helps a lot



FE operating voltage

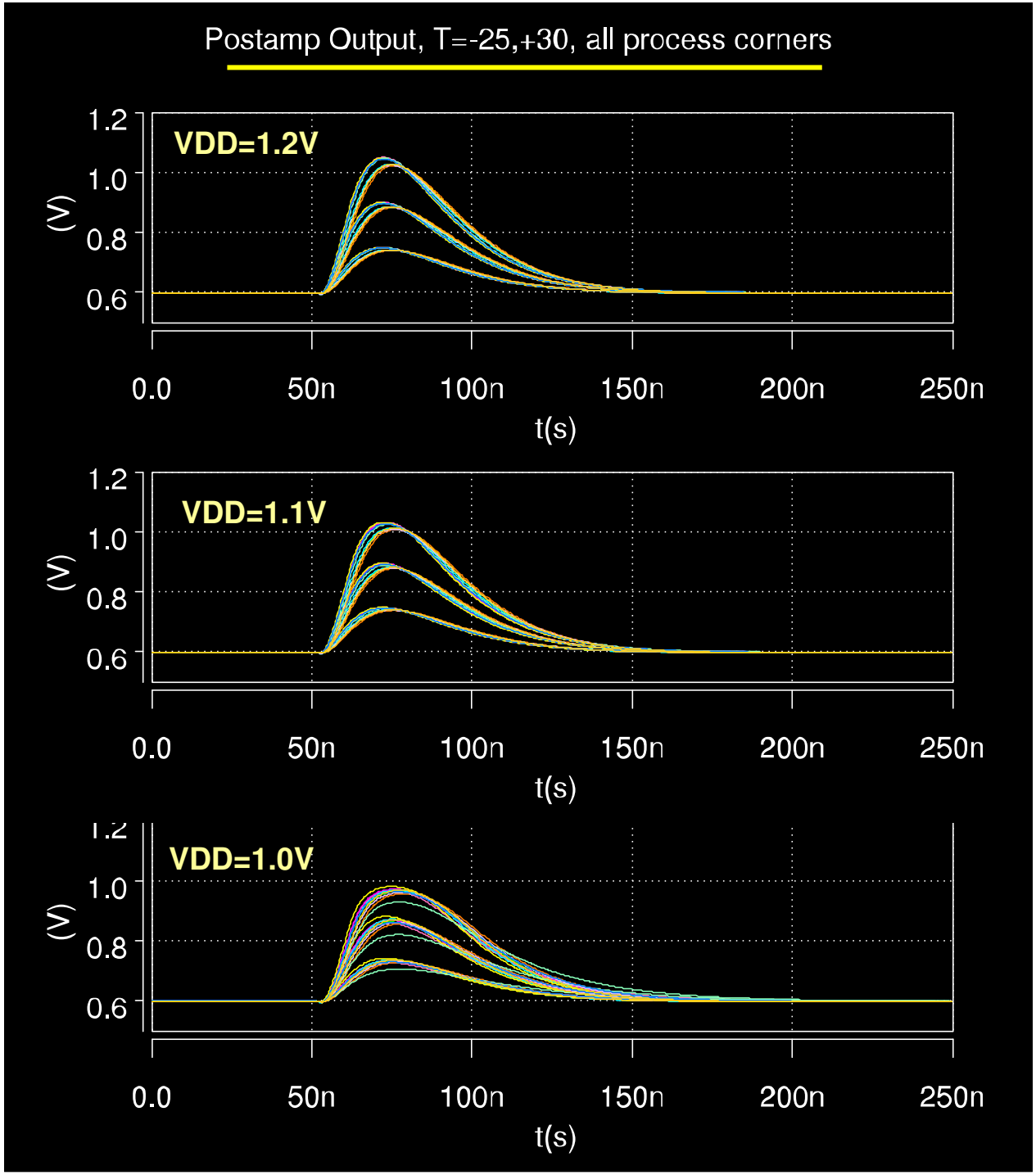
can operate comfortably at 1.1V

can make use of headroom to allow voltage drop across passive RC filter (works quite well - see last time)

or (suggestion from Federico) to allow headroom for LDO

LDO doesn't regulate to high frequencies, but should get filtering effect anyway from pass transistor resistance and O/P cap.

additional advantage of stable DC voltage to analogue circuits

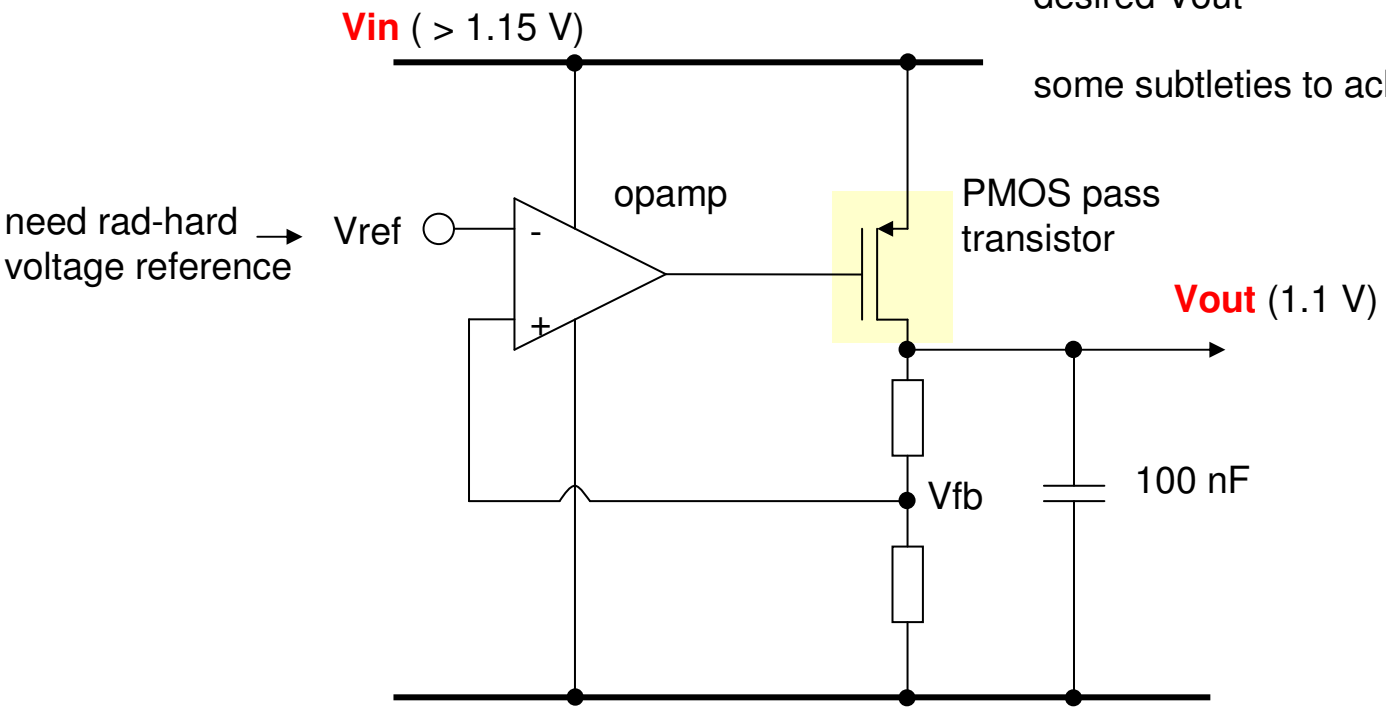


LDO design

simple in principle

Vfb = Vref, so choose resistor values to get desired Vout

some subtleties to achieving stability in practice



main LDO target specs for CBC powering

dropout

< ~50 mV for currents up to ~60 mA (CBC nominal ~ 20 mA)

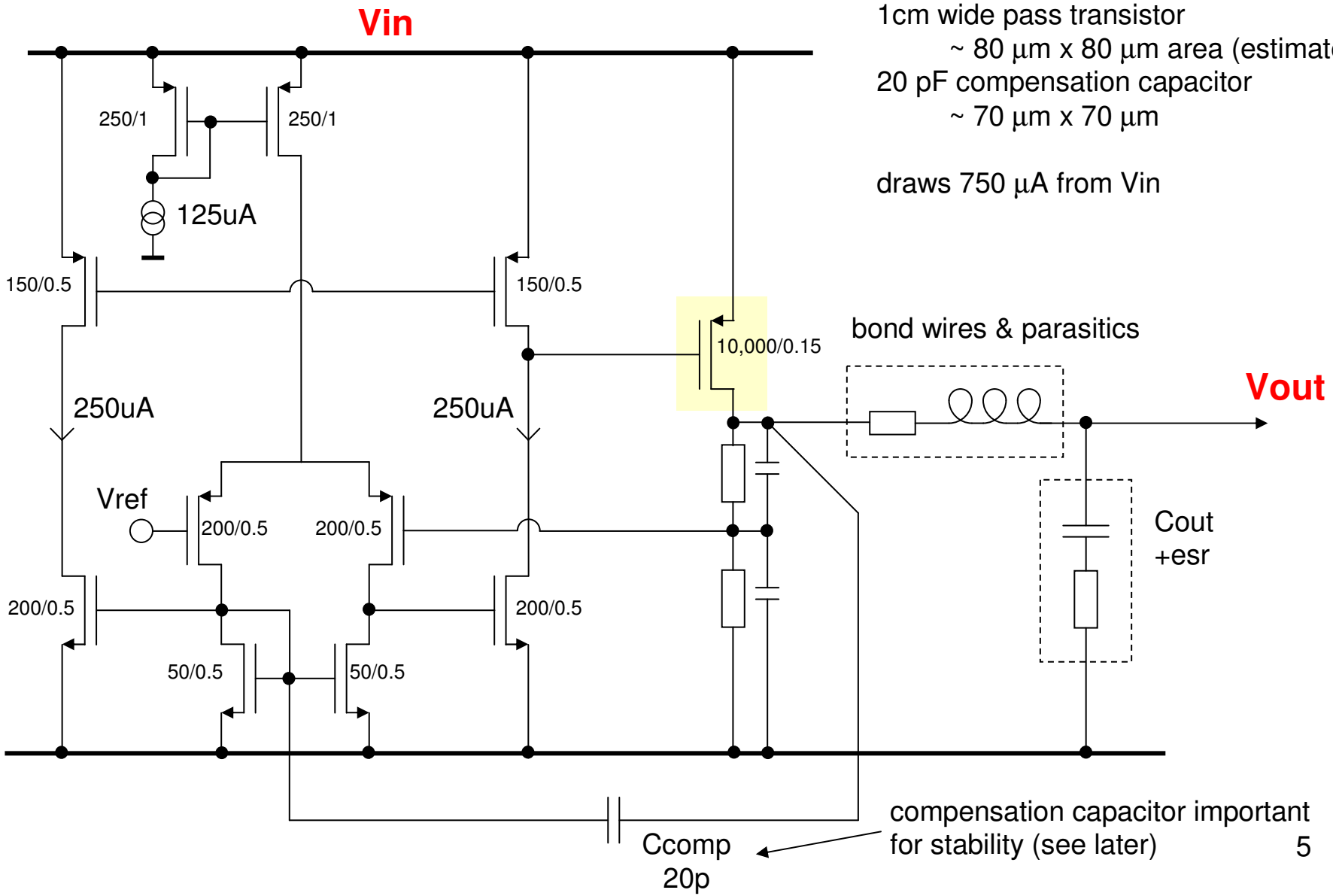
O/P cap

up to 100nF available in 0201 format (small)

others

… see what can be achieved

LDO – complete schematic



1cm wide pass transistor
~ 80 µm x 80 µm area (estimate)
20 pF compensation capacitor
~ 70 µm x 70 µm

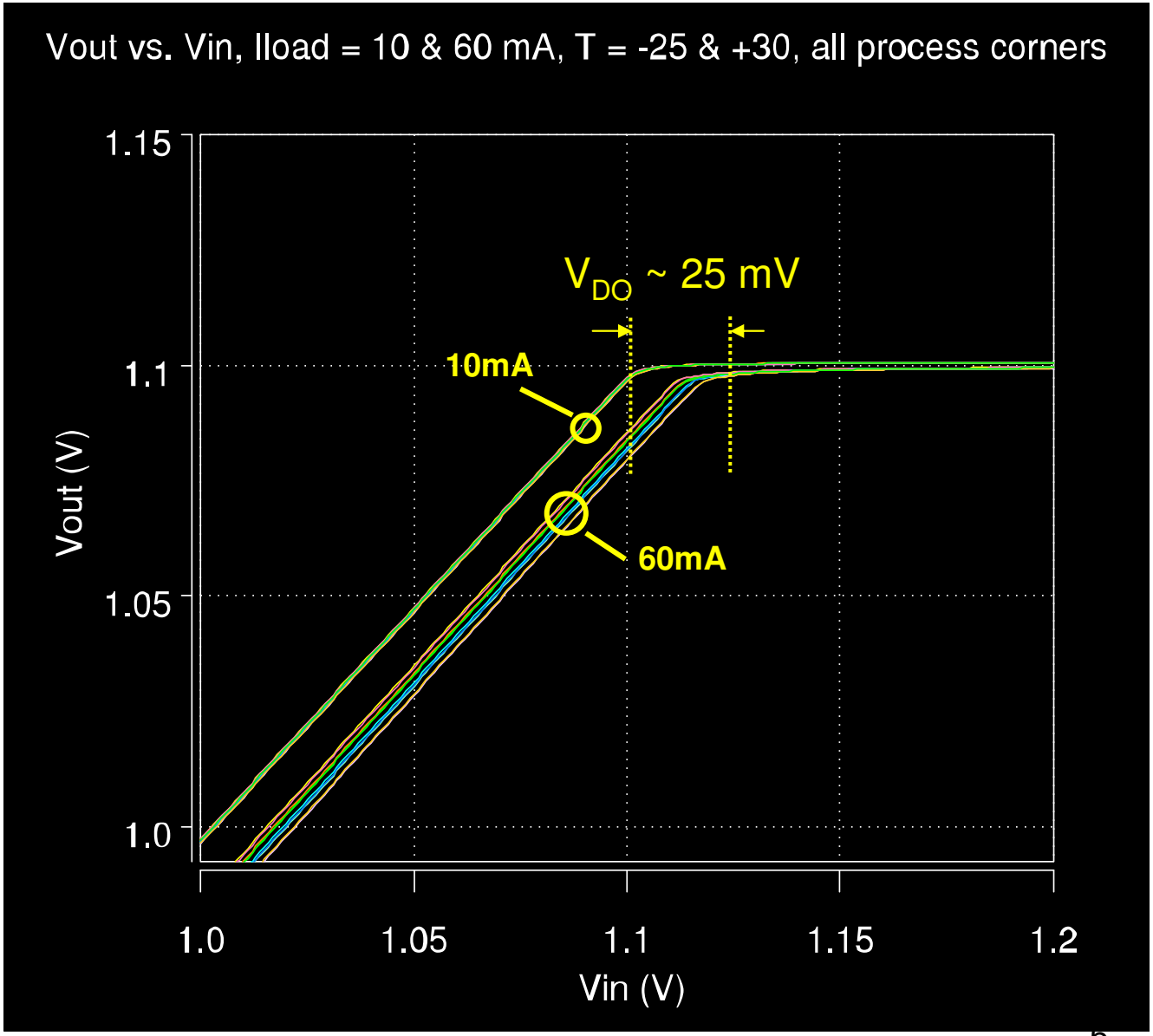
draws 750 µA from Vin

Dropout

Vout dependence on Vin

all process corners,
for I_{LOAD} = 10 & 60 mA,
for T = -25 & +30 deg.

V_{DROPUT} < ~ 25 mV,
not much T dependence

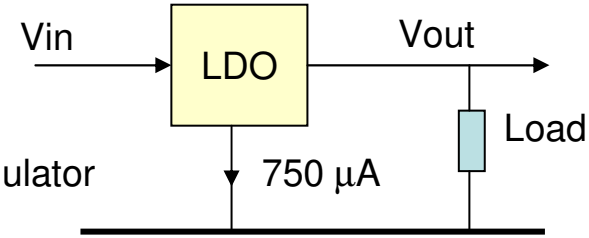


Quiescent Current

difference between input and output currents

~ 750 μA (including mirror device current) consumed by regulator

=> 0.9 mW excess power (~ 7 μW / chan. for 128 chan chip)



Efficiency

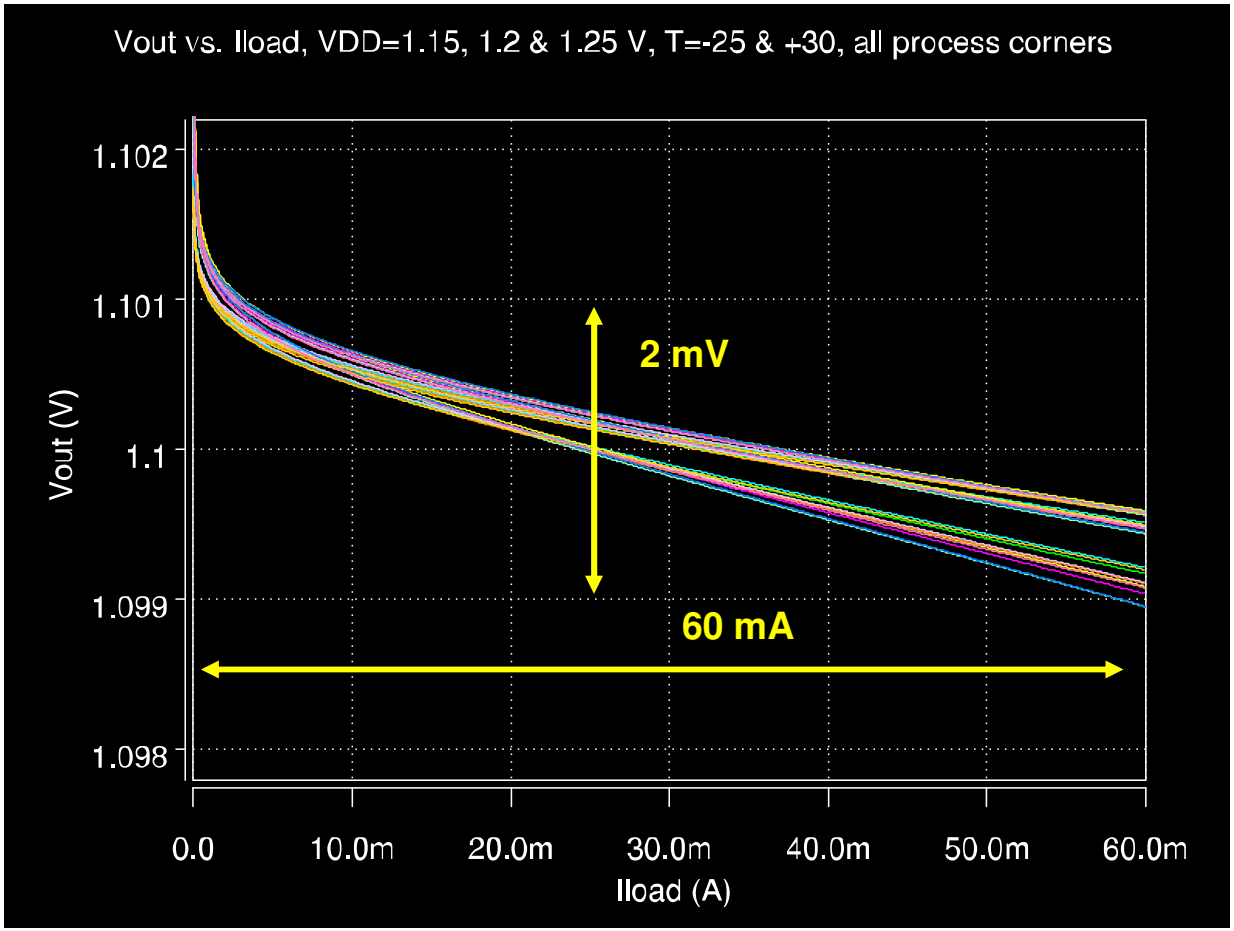
power consumed by load / external power delivered

taking normal load current = 20 mA, Vout = 1.1, Vin = 1.2 (=> 100 mV across pass device)

$$\text{efficiency} = \frac{20\text{ mA} \times 1.1}{(20\text{ mA} + 0.75\text{ mA}) \times 1.2} \times 100 = \sim 88\ \%$$ (dominated by dropout)

could be higher if operate at lower Vin, but want headroom for supply noise

Load Regulation



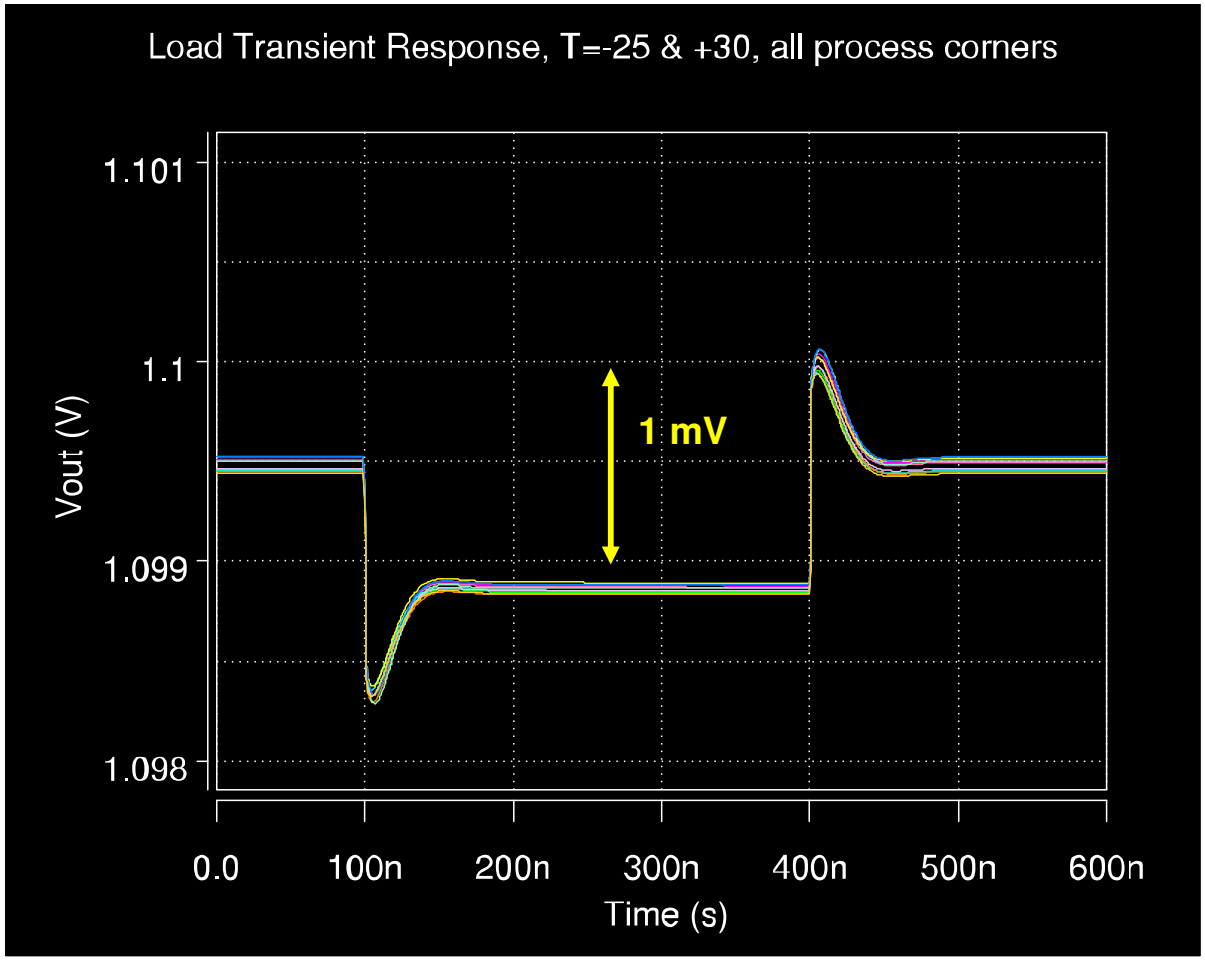
load regulation defined as

$$\Delta Vout / \Delta I_{LOAD}$$

plot shows Vout vs. I_{LOAD} for all process corners, T=-25 and +30 for Vin = 1.15, 1.2 & 1.25 V

~ 2 mV change in Vout for ~ 60 mA change in I_{LOAD}

Transient Load Response



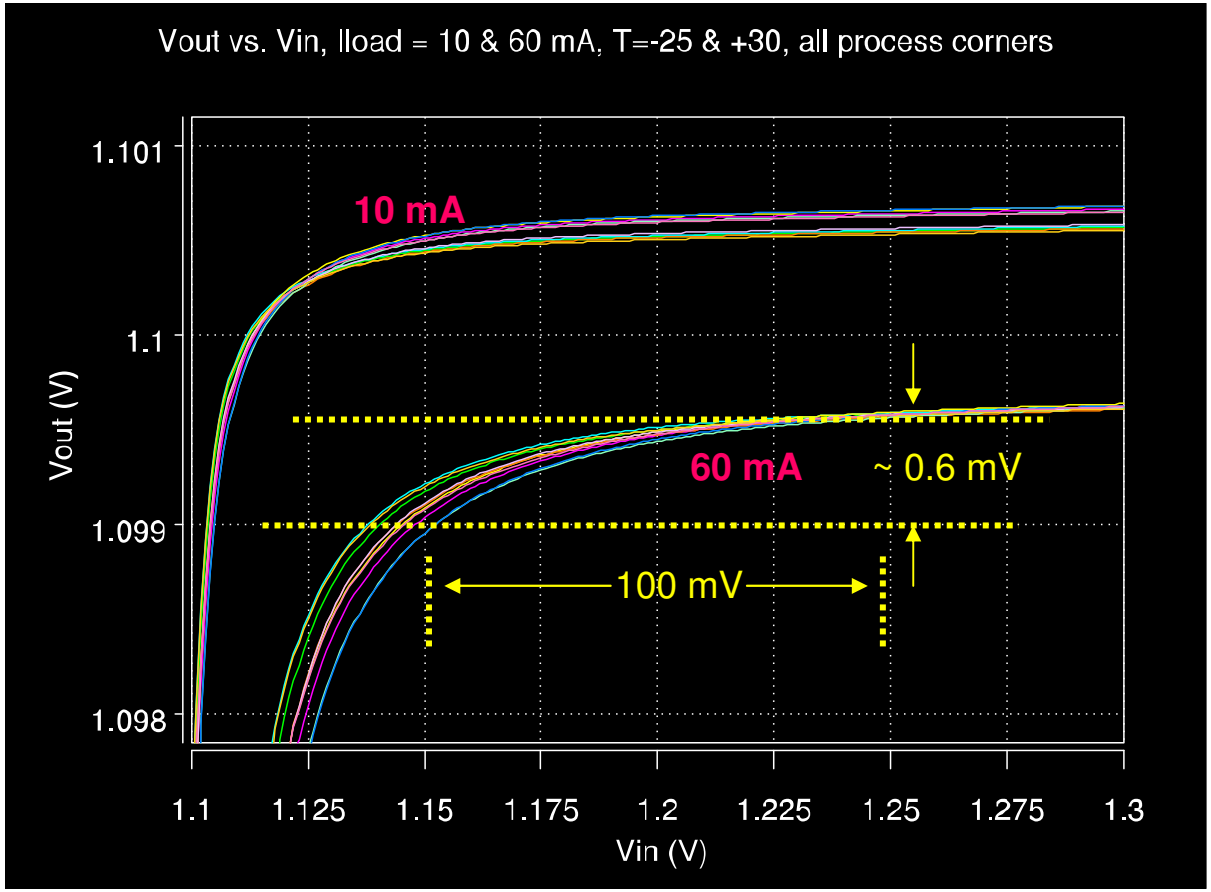
load current switched from 20 to 30 mA and back again

response simulated for process corners and -25, +30 deg.

~ 1 mV amplitude transients on output line

CBC analogue load should not vary anywhere near as much as this

Line Regulation



line regulation defined as

$$\Delta Vout / \Delta Vin$$

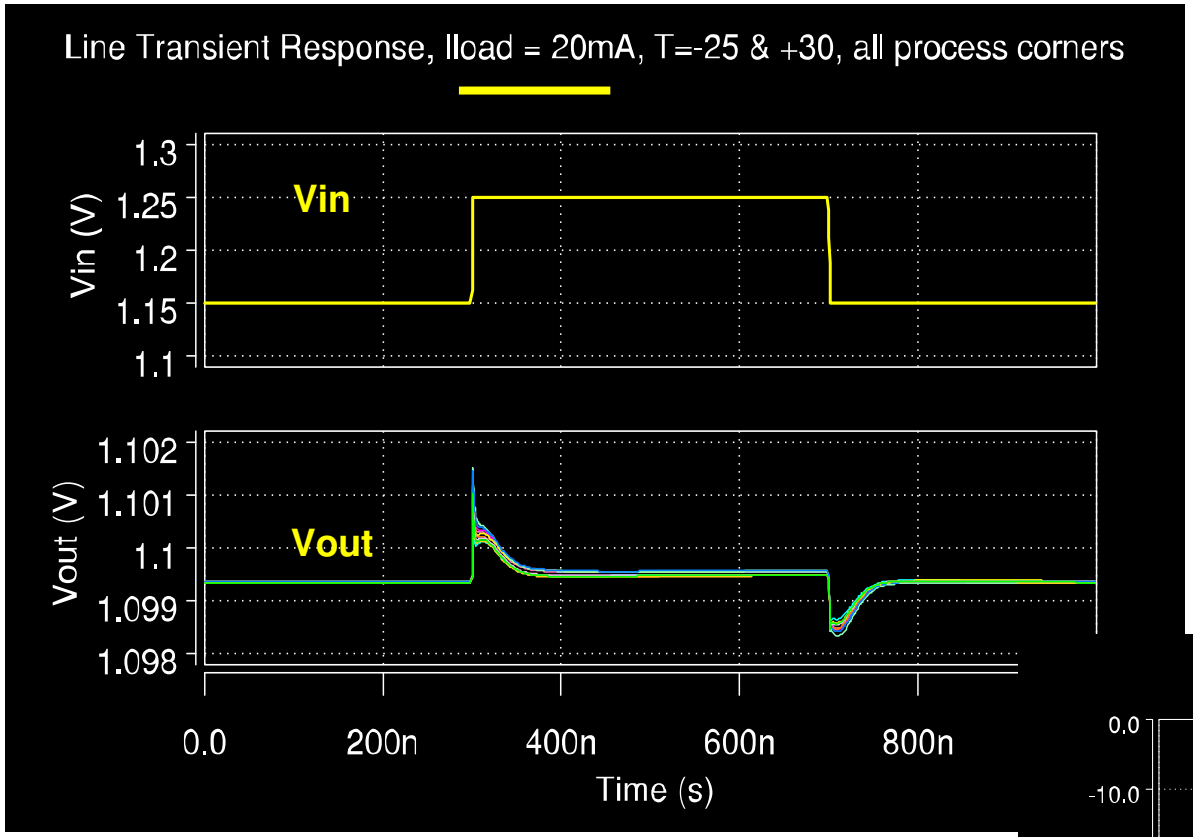
plot shows Vout vs. Vin for all process corners, T=-25 and +30 for I_{LOAD} = 10 mA & 60 mA

worst case line regulation for highest load
(in Vin = 1.15 -> 1.25 range)

0.6 mV / 100 mV = 0.6 %

not a particularly important parameter for us – more important is transient response to shifts in the input voltage (a noisy supply rail)

Transient Line Response



100 mV square pulse on Vin

Vout response simulated for
all process corners and T=-25,+30

plot shows behaviour for nominal
20 mA output load

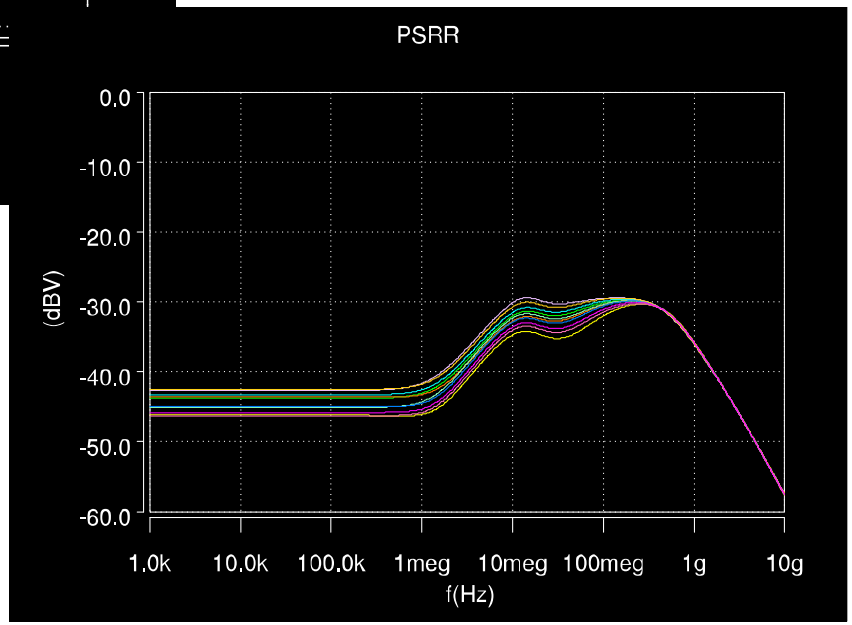
transient disturbance amplitude
~ 2 mV
(~ factor 50 less than Vin transient)

stable response

this behaviour related to PSRR

PSRR – output voltage response to sinusoidal ripple on Vin

shows > 30 dB rejection (factor ~ 30) ⟶

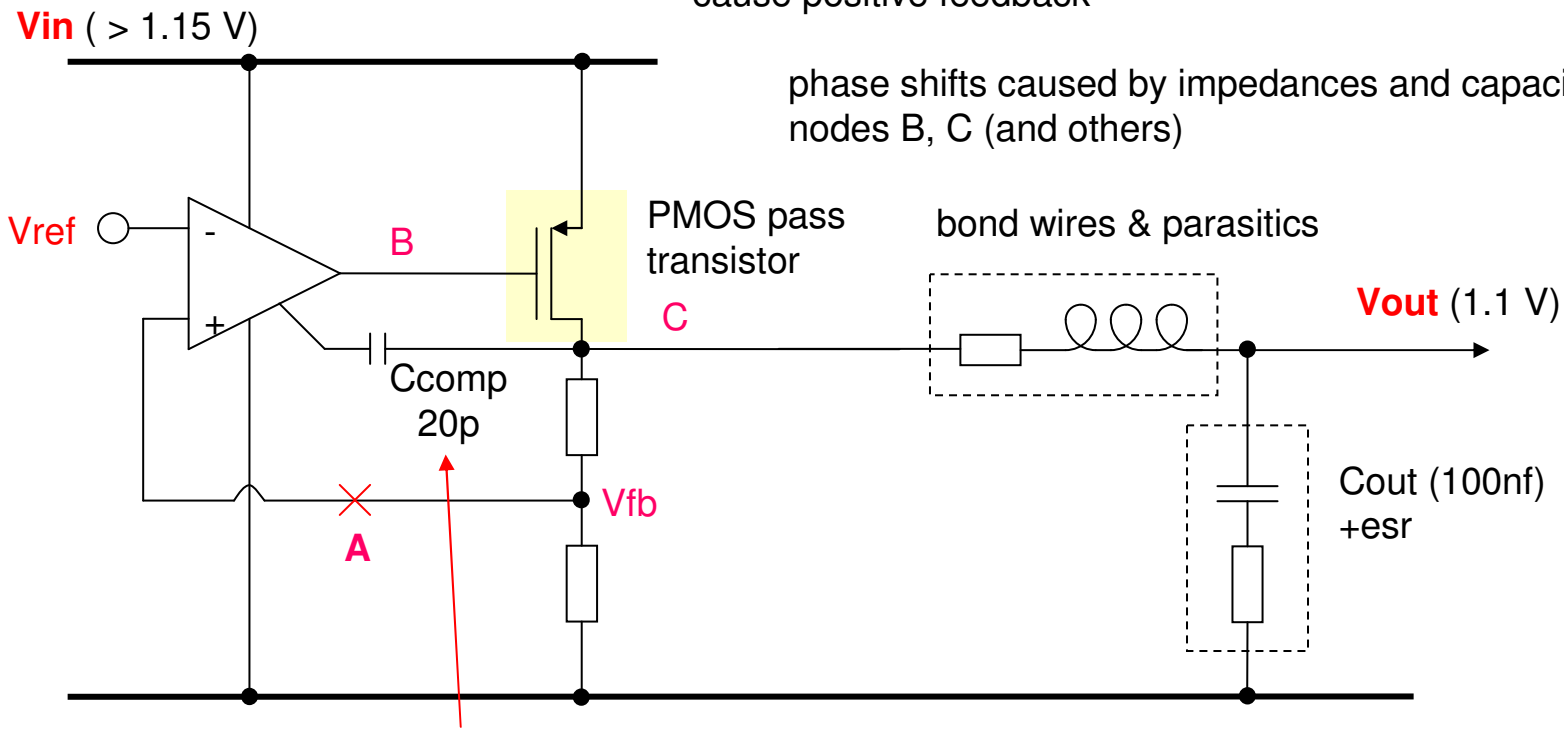


Stability

stability is the major design issue with LDO
a long story – keep brief here

important that feedback node Vfb not phase shifted enough to cause positive feedback

phase shifts caused by impedances and capacitances at nodes B, C (and others)

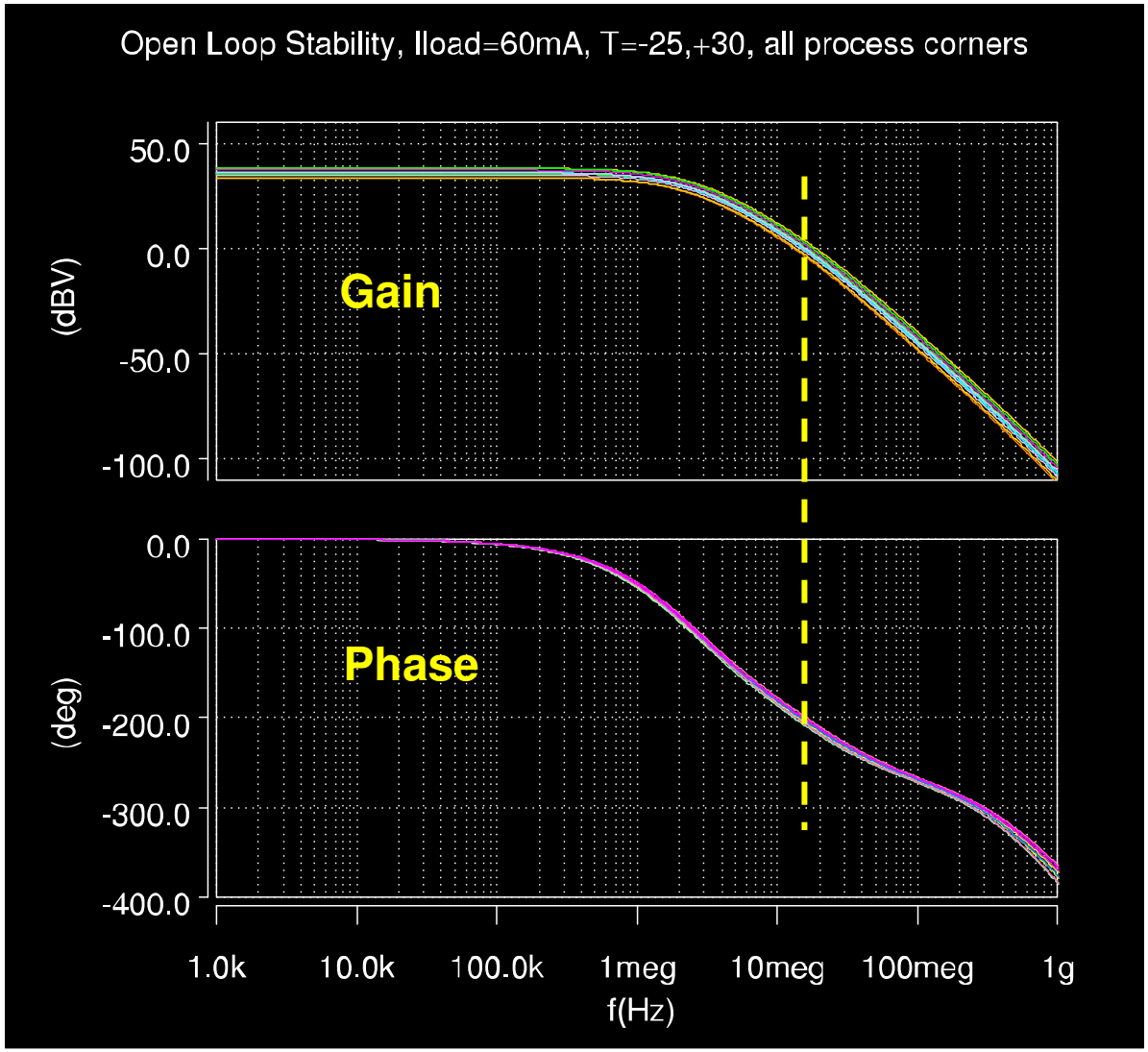


to analyse stability, break feedback loop at A, use Vref as input, take Vfb as output

require system to be unity gain stable
look at Vfb phase where OL gain reduces to unity
(more details on technique see *)

*http://users.ece.gatech.edu/~rincon/publicat/books/thesis/ldo_book.pdf

Stability – without compensation



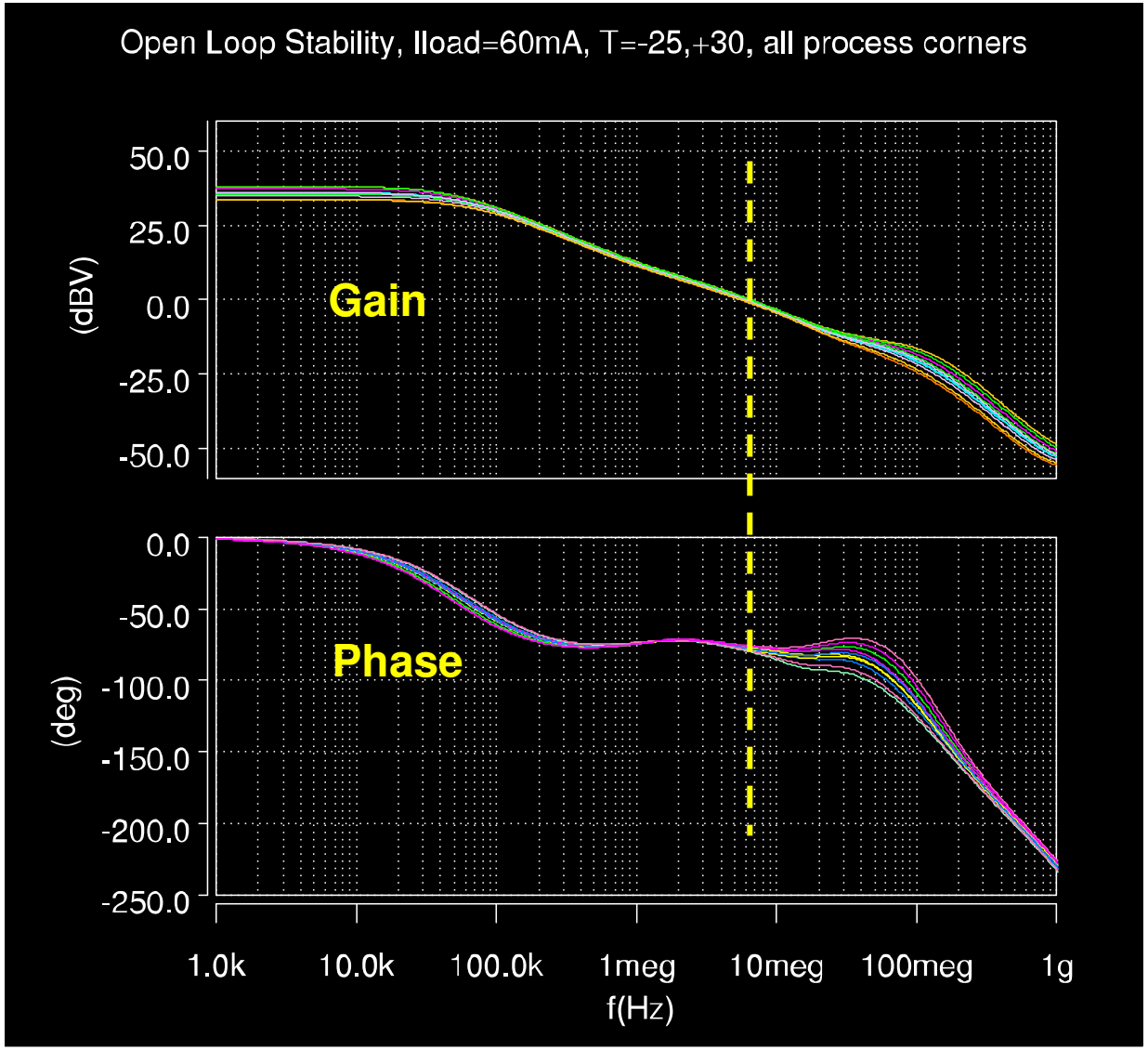
plot shows gain and phase at output node Vfb

no compensation

no phase margin at 0 dB gain (preferable to be at least 45^0)

not stable

Stability – with compensation



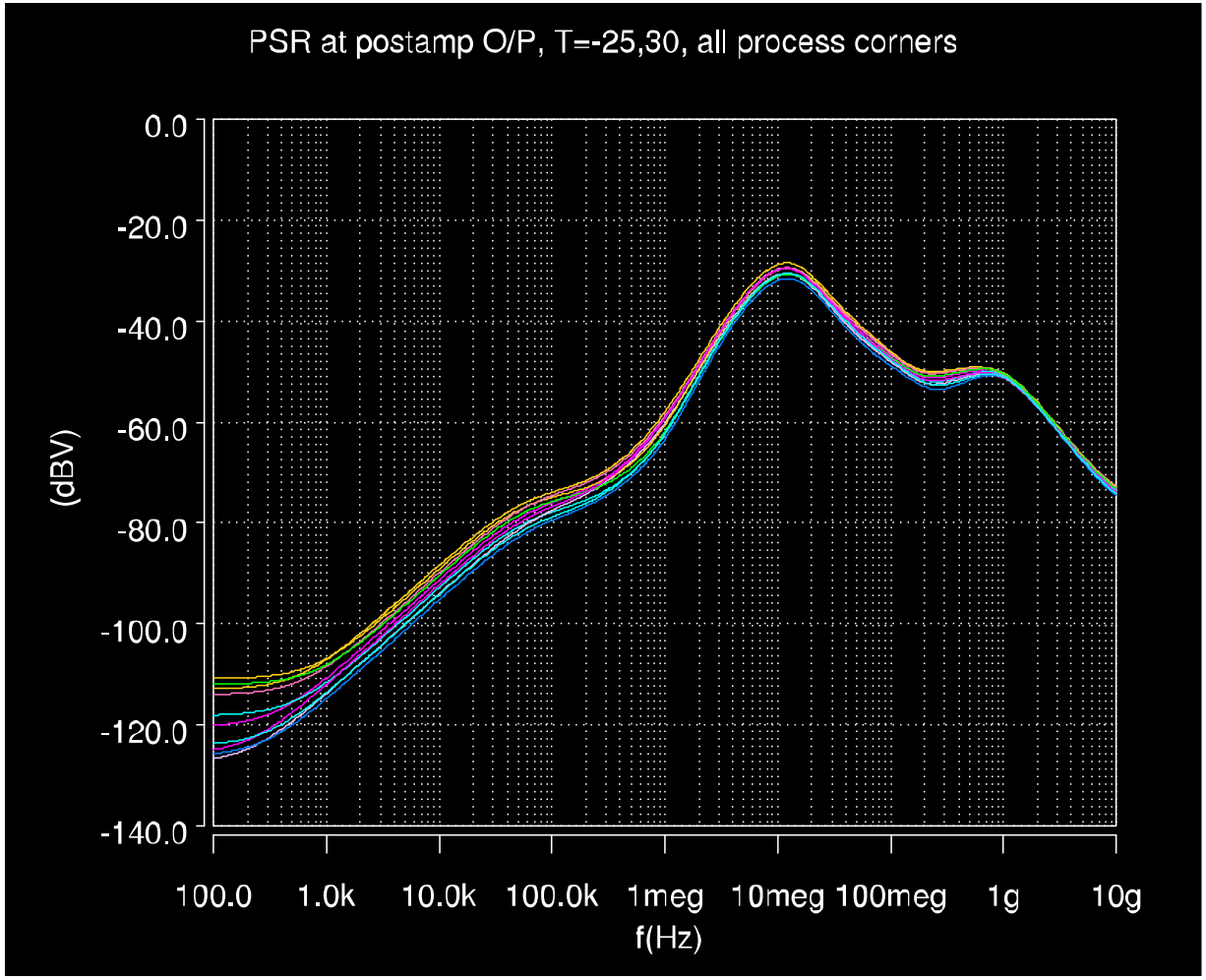
plot shows gain and phase at output node Vfb

dominant low frequency pole @ ~ 30 kHz

~90^{o} phase margin @ 0dB gain

stable

CBC front end PSR with LDO supply



frequency domain response

CBC front end powered by LDO
(1 channel + 25 mA dummy load)

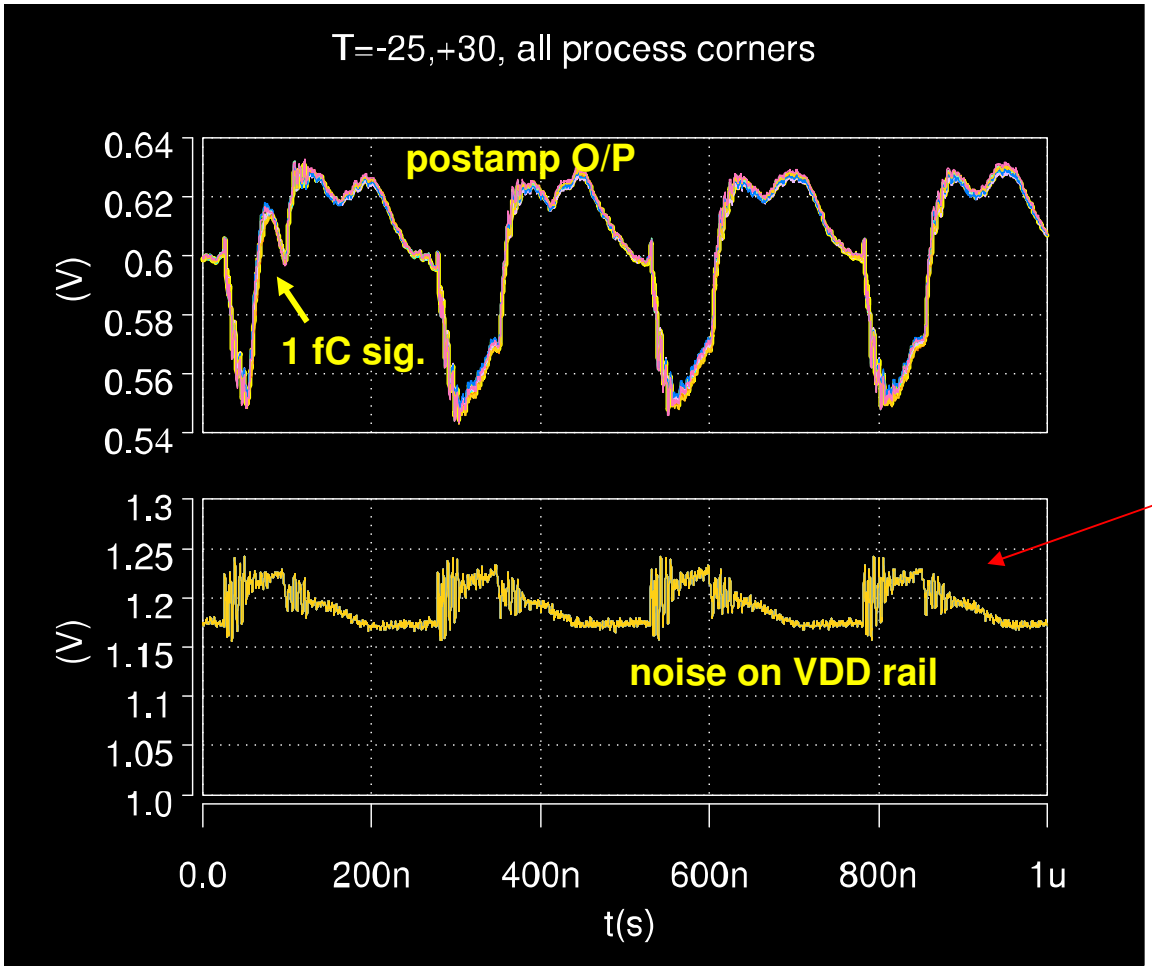
plot shows postamp output response
to sinusoidal ripple on Vin to LDO

still get peak at ~ 10 MHz (c.f. slide 2)

but overall rejection > 30dB

(very good at lower frequencies)

front end PSR without LDO supply



time domain picture

measured noise waveform added to VDD rail supplying FE circuit

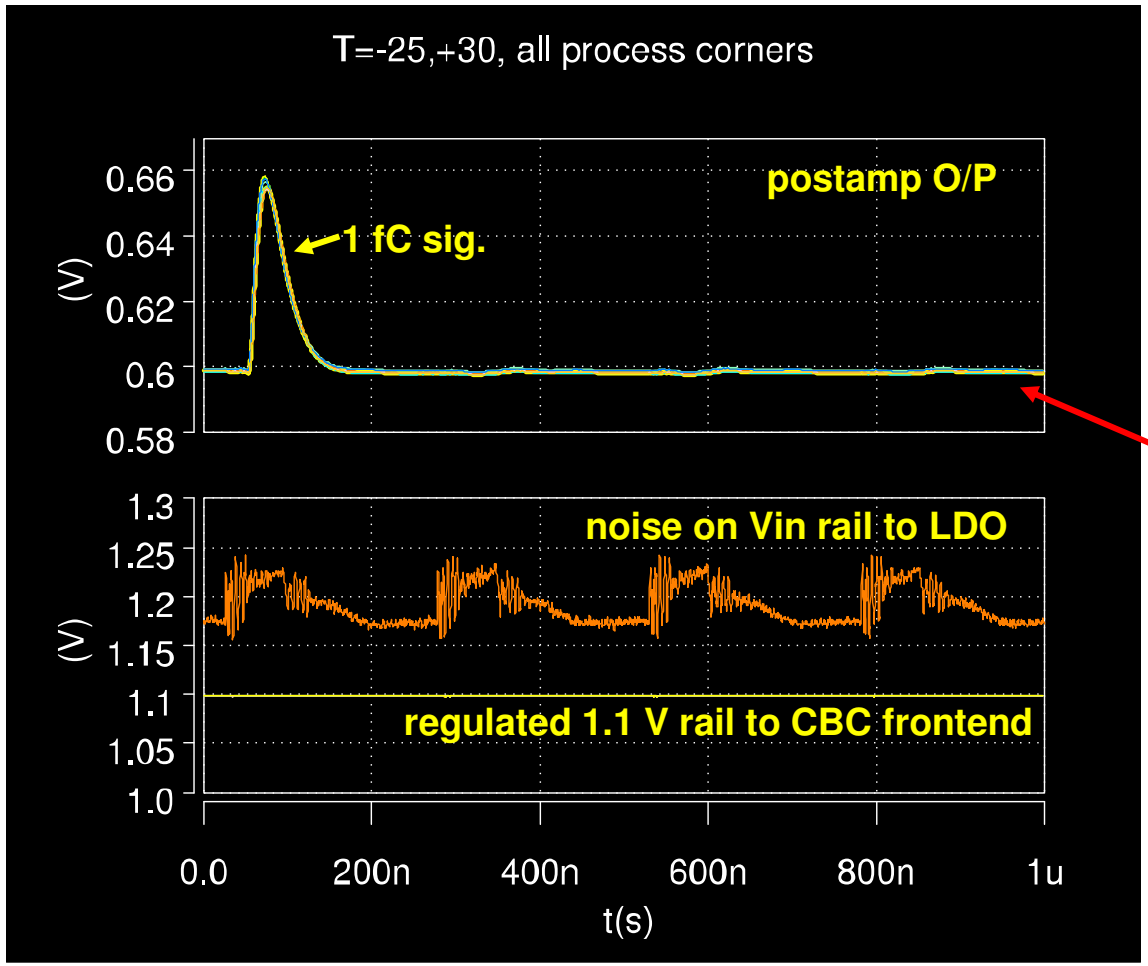
sampled scope data for Enpirion "quiet" converter provided by Aachen

but x10 to (artificially) make it noisier

~ 80 mV pk-pk

1 fC normal signal completely swamped by noise

front end PSR **with** LDO supply



measured **x10** (80 mV pk-pk) noise waveform now added to LDO Vin

LDO loaded by single CBC frontend + 25 mA extra dummy load

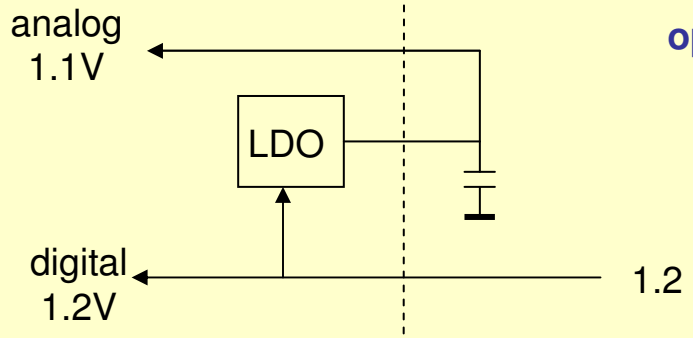
1 fC signal at postamp O/P now appears

postamp O/P noise just visible

~ 125e pk-pk

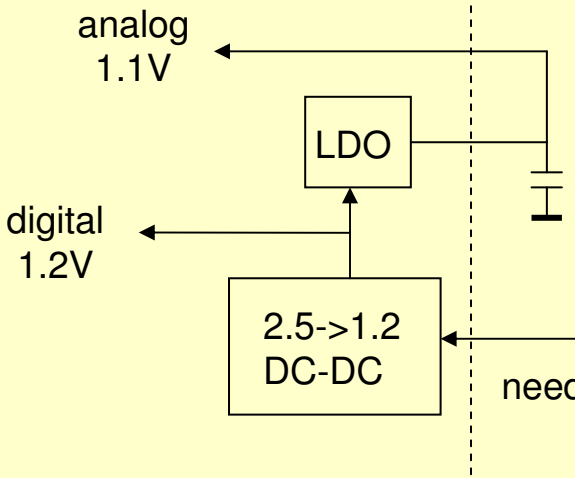
PS system – some options

incorporating LDO into CBC seems like a good idea – what are the options for the powering system?



option 1 – single ~1.2 V supply to chip

1.2 feeds digital
1.2 LDO regulated down to 1.1V for analogue



option 2 – single 2.5 V supply to chip

2.5 -> 1.2 switched cap. DC –DC
1.2 feeds digital
1.2 LDO regulated down to 1.1V for analogue

need 2 more external capacitors for DC-DC

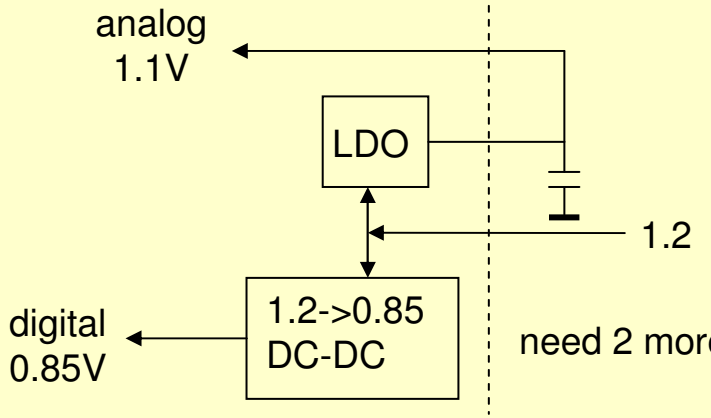
note: neither of these options allows to provide lower digital supply voltage

Summary

- PSR of single-ended FE stage not good
  - => vulnerable in DC-DC powered system
- can run analogue at lowest possible VDD (1.1) allowing headroom for passive filtering or LDO
  - LDO gives additional advantage of stable, reference related, DC supply
  - need reference voltage – proven designs already exist
- LDO design here demonstrates potential
  - big improvement to supply rejection
  - low risk option – appears stable - can bypass if necessary
  - could also switch to alternative, proven, design if available
- need to make a decision on power strategy for prototype chip
  - LDO or not, DC-DC on-chip or not, how to supply lower voltage for digital, …
  - can we (should we) prototype to test all possibilities?
  - suggest to converge on a decision in next ~2 months (at least before end of year) to allow timely incorporation into CBC prototype

Extra

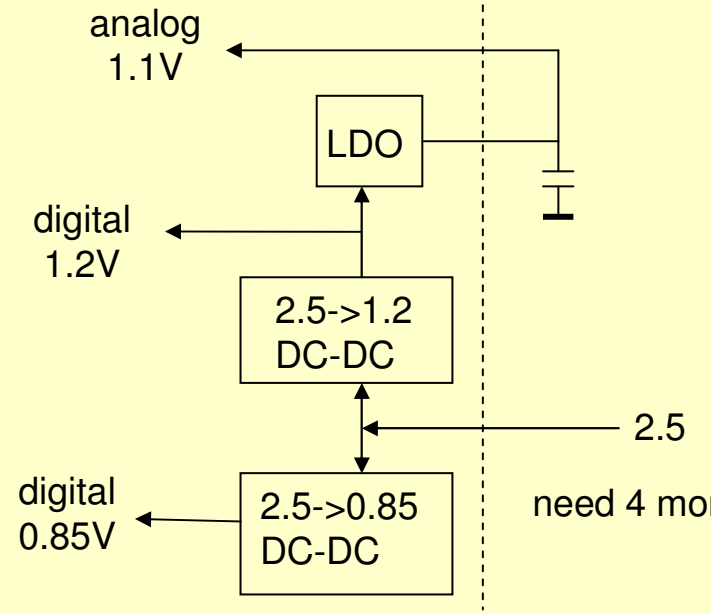
PS system – some more options



option 3 – single 1.2 V supply to chip

feeds 1.2 -> 0.85 swtiched cap. DC-DC
1.2 LDO regulated down to 1.1V for analogue

need 2 more external capacitors



option 4 – single 2.5 V supply to chip

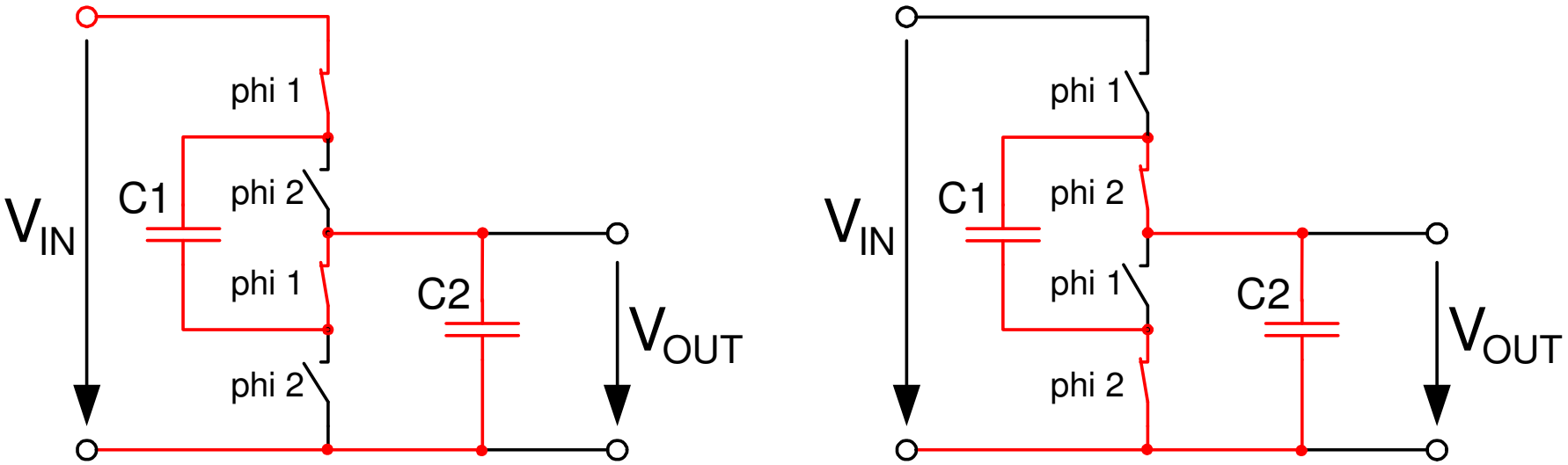
2.5 -> 1.2 switched cap. DC –DC
1.2 LDO regulated down to 1.1V for analogue
2.5 -> 0.85 switched cap. DC-DC feeds digital

need 4 more external capacitors

other options?
better ideas?

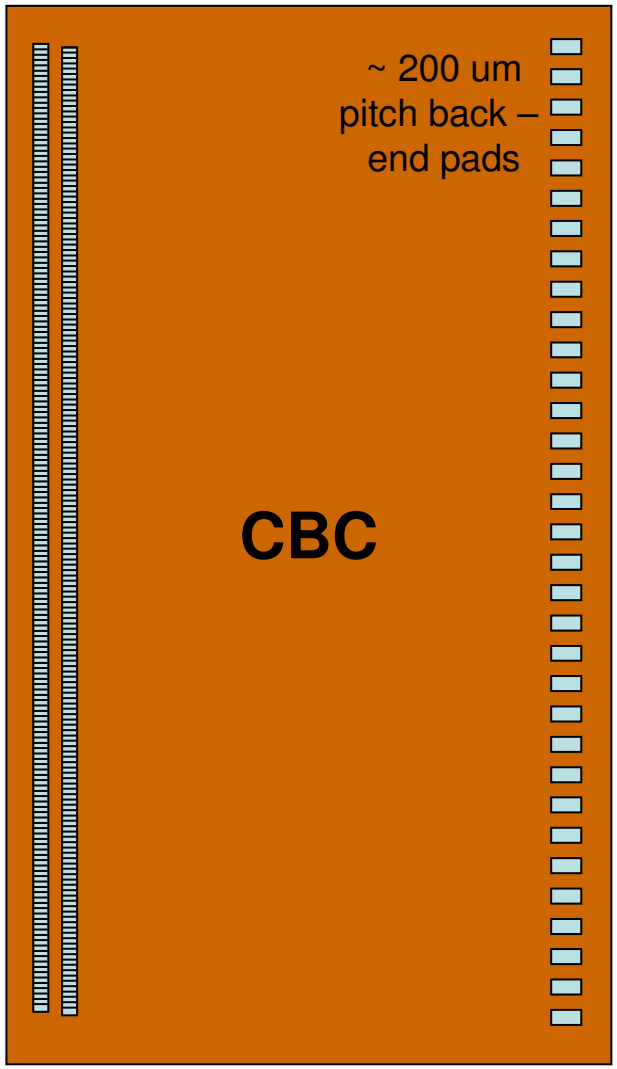
Beat Meier's switched cap. DC-DC converter

Principle



- Voltage divider by 2
- on chip: four switches, two phase generator and drivers
- external oscillator
- external capacitor C1 and C2 (10 … 100 nF)

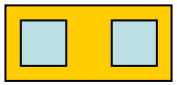
chip vs. passives size



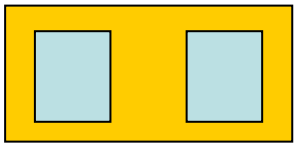
few mm

7 mm

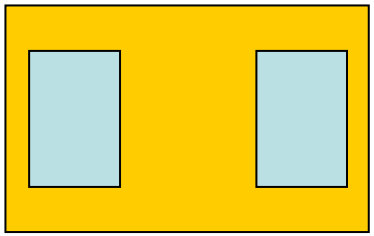
approximately to scale



0201 - up to 100 nF



0402 - up to 220 nF



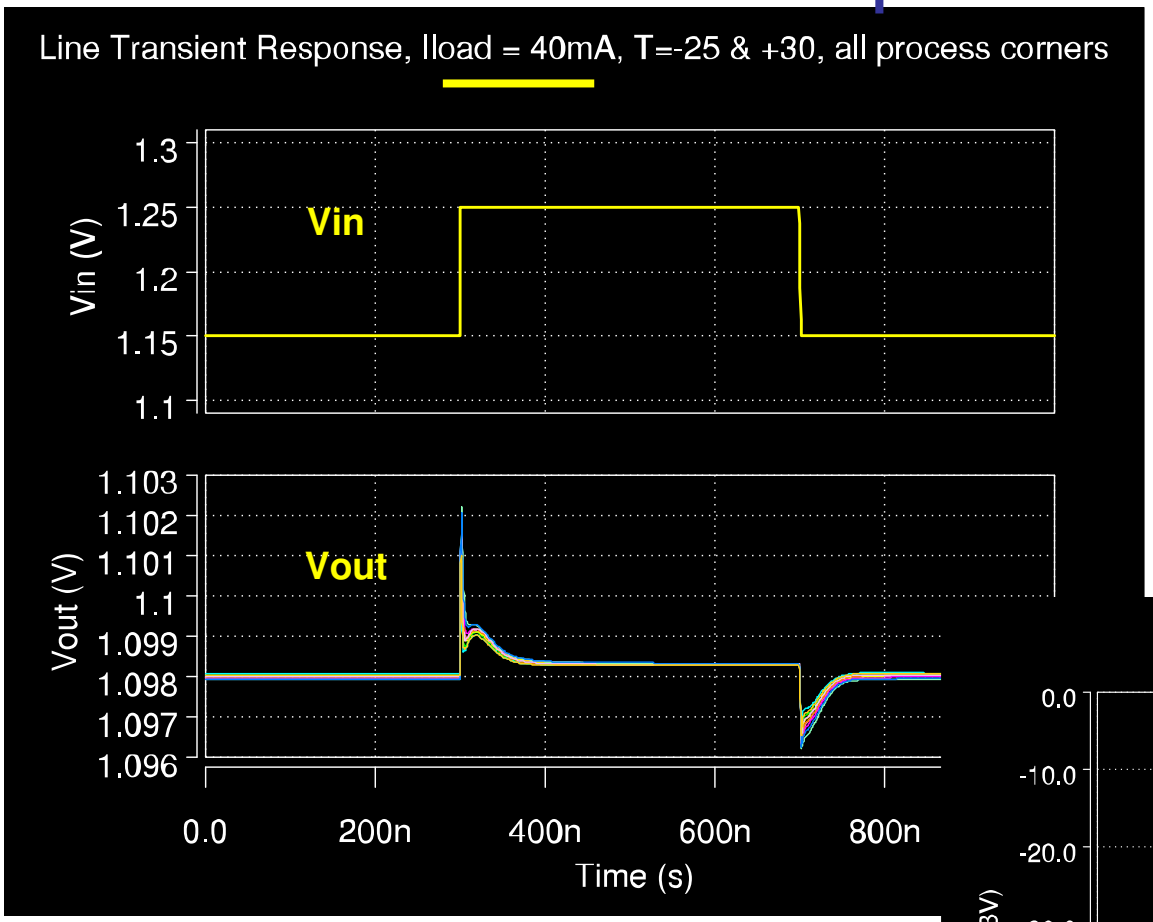
0603 - up to 10 uF

passives take space
don't want too many per chip

decoupling necessary – don't ignore

DC-DC / linear regulation on-chip will add more passives

Line Transient Response



100 mV square pulse on Vin

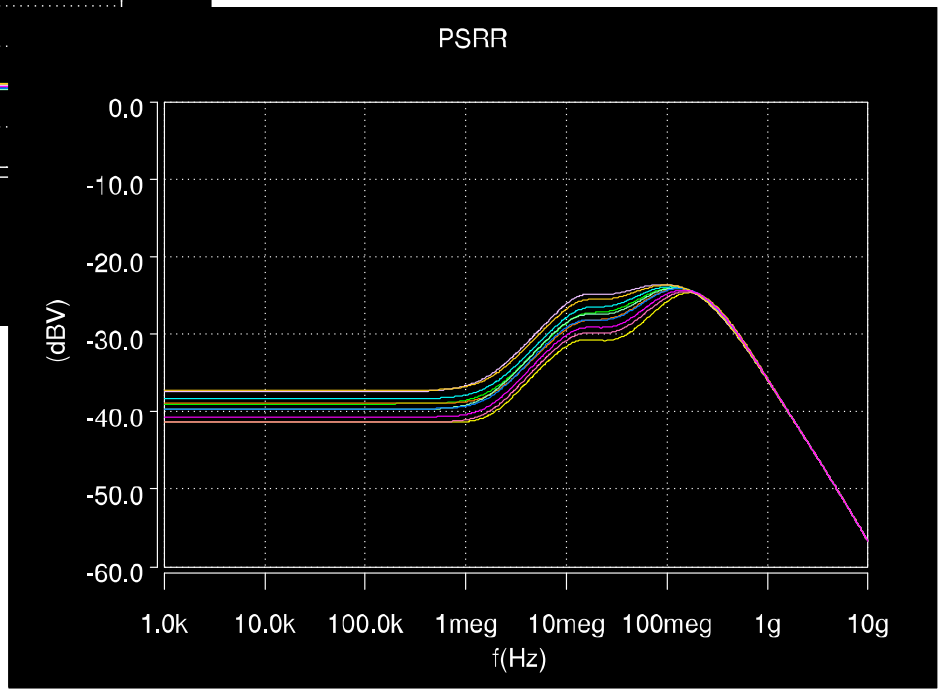
Vout response simulated for
all process corners and T=-25,+30

plot shows behaviour for **2x** nominal
40 mA output load

transient disturbance amplitude
~ 4 mV
(~ factor 25 less than Vin transient)

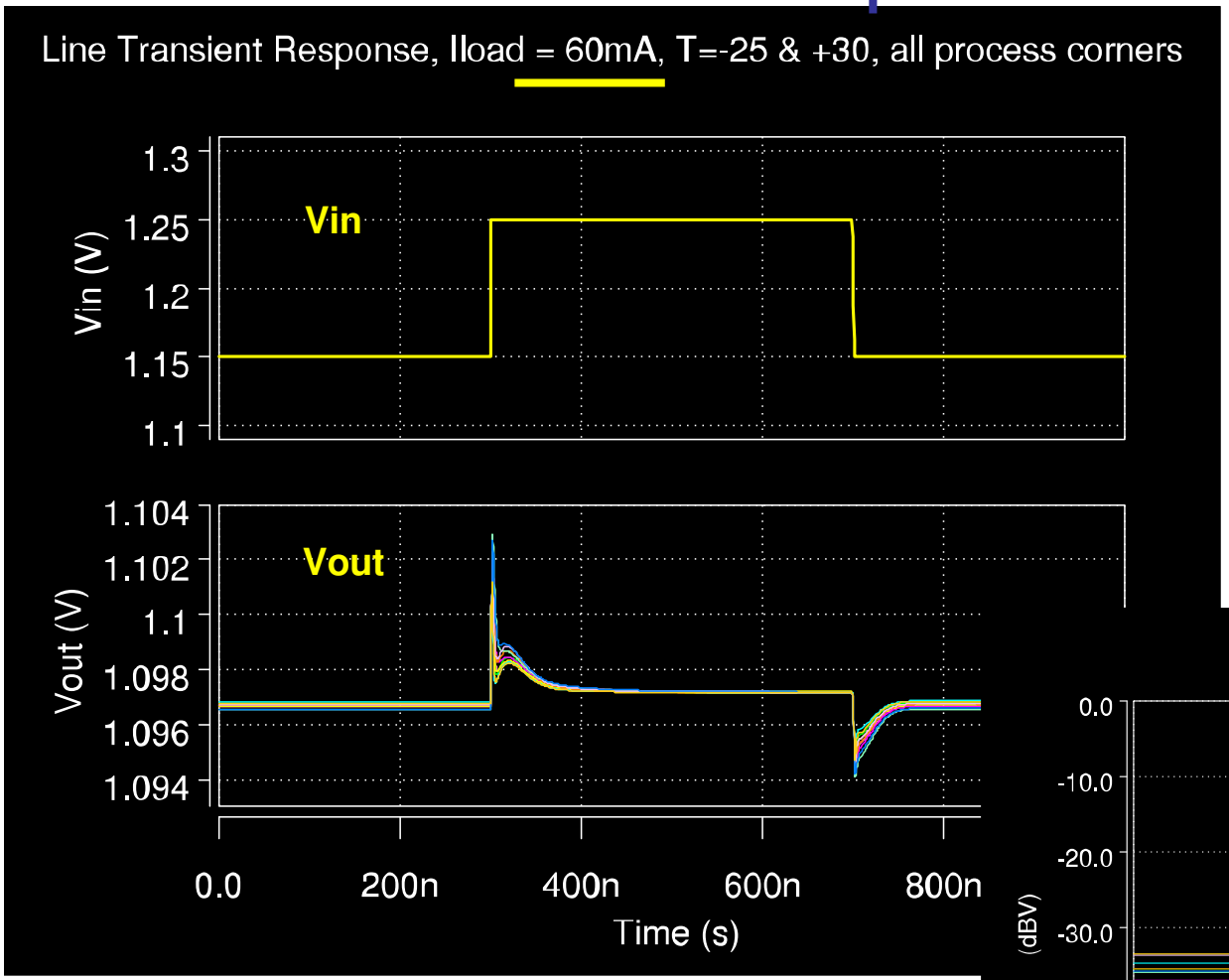
~ stable response (minimal ringing)

this behaviour related to PSR



> ~ 25 dB rejection (factor ~ 18) ⟶

Line Transient Response



100 mV square pulse on Vin

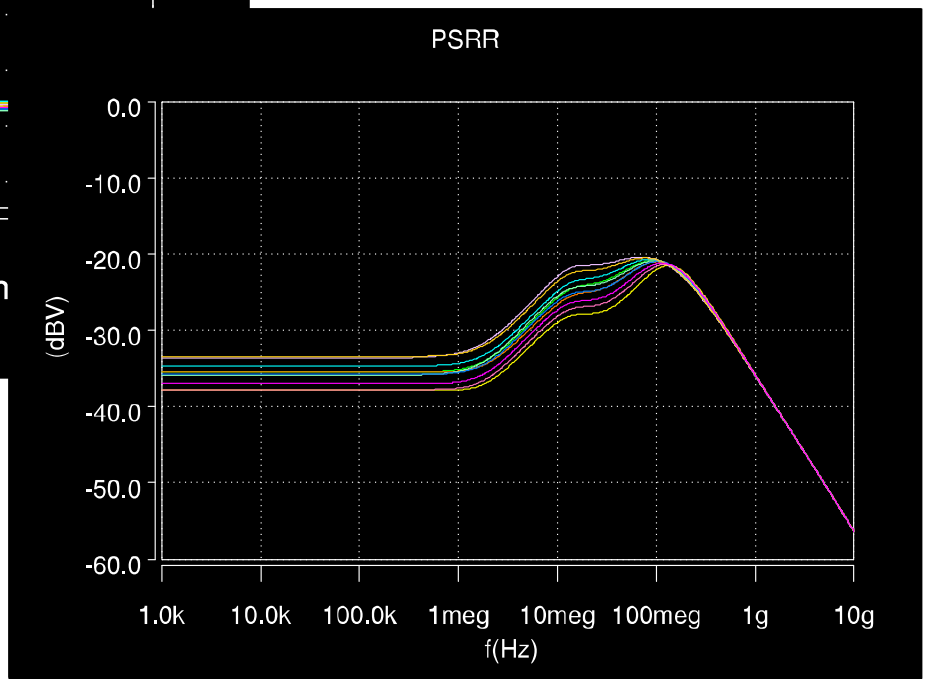
Vout response simulated for
all process corners and T=-25,+30

plot shows behaviour for **3x** nominal
60 mA output load

transient disturbance amplitude
~ 6 mV
(~ factor 17 less than Vin transient)

~ stable response (minimal ringing)

this behaviour related to PSR



> ~ 20 dB rejection (factor ~ 10) ⟶