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CBC (CMS Binary Chip) Design for Tracker Upgrade

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Overview of Talk

- Introduction
- Analogue Design
- Digital Design
- Test Results
- Conclusion
- Acknowledgements



- CBC is intended for use in the outer tracker of the SLHC with short strip detectors (2.5-5cm)

- The original LHC readout chip (APV25-S1) had an analogue non-sparsified readout architecture.

- For SLHC, a binary non-sparsified readout has been chosen as the target architecture for the CBC.

- This has the following advantages over a digital sparsified system.

- \checkmark Minimises amount of data to be processed
- ✓- Simplifies readout architecture
- ✓ Simpler on-chip logic
- ✓- No ADC
- ✓- Occupancy independent data volume
- ✓- Lower power
- \checkmark Can be emulated off-detector
- ✓ Simpler overall system



CMS Binary Chip (CBC) Overview

128 Channels

- preamp, postamp, comparator

Both polarities of signal

- optimised for both electrons and holes

Binary Conversion

- programmable hysteresis, less than16ns time walk

Pipeline memory 256 deep

- 2 port RAM, no SEU immunity

Buffer Memory 32 deep

- pipeline address has hamming encoding

Programmable Biases

fully programmable through I²C with 8bit resolution
referenced to bandgap (provided by CERN)

LDO Regulator

- unconnected internally

DC-DC Converter

- 2.5V to 1.2V, unconnected internally

- provided by CERN

I²C Interface
SLVS I/O
provided by CERN





Front End Specification

Detector Type:	Silicon Strip (both n-on-p and p-on-n)
Signal Polarity:	both (electrons and holes)
Strip length:	2.5 – 5 cm
Strip Capacitance:	3 – 6 pF
Coupling:	AC or DC
Detector leakage:	up to 1 uA leakage current compensation
Charge collection:	less than 10 ns
Noise:	less than 1000 electrons rms for sensor capacitance up to 5 pF
Leakage noise:	500 electrons rms for 1uA leakage
Overload recovery:	normal response within ~ 2.5 us after 4 pC signal
Power:	~ 500 uW / channell (for 5pF strips)
Operating temp.:	In experiment probably < -20C but will want to test at room temp.
Power supply:	1.1 V (assumes front end supplied through LDO to get supply noise rejection)
Gain - Linearity	50 mV/fC – 4fC
Timewalk:	less than16 ns for 1.25 fC and 10 fC signals with comp. thresh. set at 1 fC
Radiation Hard	the analogue is laid out using radiation hard techniques



CBC Front End



Preamplifier

-100fF feedback capacitor

- Selectable resistive feedback network absorbs leakage current

- 20ns time constant minimises effects of pile up

Postamplifier

- Optimised for both electrons and holes
- Coupling capacitor removes leakage current shift

- Programmable offset for trim 8 bits 200mV range

Comparator

- Global Threshold
- Programmable hysteresis
- Selectable polarity



Front End Simulations



Preamplifier

Single feedback resistor for electrons

T network for holes





Postamplifier

Offset adjustable using programmable current through resistor





0.6V

1p

Vplus 💼

In 🖿

Post Amplifier



(d)as

80f

~70nA

Bias Generator

1M.

lfpa = 2.5uA

-

h

Electrons

- Current mirror biases feedback transistor.
- Sources connect to Vplus As signal is negative going
- Current programmable through bias generator

Holes

Dut

- Sources of current mirror connect to output since signal is positive going.
- 1pF capacitor ensures gates track output to maintain linearity





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Comparator



Programmable hysteresis:

- Voltage at node A is modified using a resistive feedback network







CBC Digital Specification

Hit detection: Synchronises comparator to clock

- **Pipeline RAM:** Stores data until an external trigger
- Pipeline Depth: 256 columns
- Pipeline Latency: Up to 3.4us with a 40MHz clock
- **Buffer RAM:** Store triggered data until readout
- **Buffer Depth**: Up to 32 events waiting readout
- Shift Register: Runs at 40Mhz, 140 to 1
- **Slow Control:** I2C interface controls data registers
- **Fast control:** Through trigger input (RESET101 and trigger)
- Error Checking: Latency and data buffer overflow errors
- **SEU :** Flip-flops have SEU tolerant design,
 - data registers triple redundancy.





Hit Detection Logic

EN=1, SEL=1

- A synchronised version of the input is passed through to the output.

- If the pulse is too short and it may be missed

<u>EN=0</u>

- In case (c) the circuit is disabled and nothing passes to the output.

EN=1, SEL=0

- In cases (d) and (e), the comparator pulses are compressed or stretched to be one clock cycle in length.

- The output from the Hit detection circuit feeds directly into the pipeline RAM.

En	
Sel	
Clk	
In	(a) (b) (c) (d) (e)
Out	(A) (D) (E)



Pipeline Architecture

Latency Register

- defines separation of pointers

Pointer Start Logic

- enables the Write/Trigger Counters
- latency separation

Write/Trigger Pointers

- 8 to 256 decoders

Latency Check

- monitors counters
- if difference \neq latency then error

Pipeline/Buffer RAM

- dual port
- Buffer RAM configured as FIFO

Output Shift Register

- 140 to 1 parallel load and shift



Trigger and Readout Control

- Decodes fast control (trigger input)
- Controls transfer from pipeline to buffer when triggered
- Monitors Up/Down Counter to check for data
- Sequences loading of shift register and shifting of data







SEU tolerant Data Register (I²C)



- Triple RAM Cells with voting circuit
- Used in the I2C registers
- Settable and resettable versions
- Store the chip modes and bias settings



Data Format



7 clock cycles Trigger - Output

4 Clock cycles between packets



Full data packet is 140 bits

A two bit header "11"

Two error bits

- Buffer full
- Latency error

8-bit pipeline address

128 bits of channel data



Present Status

March 2009 – Design Started

Process – IBM 130nm CMOS Designers – Lawrence Jones, STFC Mark Raymond, IC Various Sub-blocks CERN

July 2010 – Design Submitted

Unexpected delays – Foundry busy

February 2011 – Testing Started

May 2011 – Chip is Fully Functional





Test Results

Provided by

Mark Raymond, Imperial College



CBC Test Results





- One full data frame and the start of a second.

- 1fC of charge injected into one channel via an external capacitor

- One full data frame showing charge injected through internal capacitors on every 8th channel

- Approximately 1.5fC



Bias Generator Measurements



- Register settings swept across the range 0-255 for each bias
- Individual bias currents are then inferred by measuring changes in the power supply current with the other biases set to default values
- Results are not linear but were not expected to be



Comparator S-curves

- No direct way of measuring analogue from front end
- Use comparator S-curves
- Sweep threshold across the signal and histogram results



- Obtain multiple S-curves for various signal sizes can extract gain and linearity





Gain and Linearity Measurements



comparator threshold VCTH [mV]

Electrons mode

- Gain ~ 50 mV / fC - Signals in range 1-8 fC in 1 fC steps

Holes mode

- Gain ~ 50 mV / fC
- Less dynamic range
- Linear in region where threshold will be set

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Channel Matching

- Comparator threshold set globally
- Individual channel tuning achieved by programmable offset on the comparator input signal
- 8-bit precision
- Before Tuning threshold spread is about 30 mV = 1 fC
- After Tuning threshold spread is about 1mV





Noise and Analogue Power

- The noise and the power consumption depend on the external input capacitance

- For differing input capacitance, the current in the input transistor is adjusted to maintain the pulse shape - so overall analogue power varies

- Measurements made for both electrons and holes
- Results close to simulation (open circles)
- Within target specifications
- Noise target spec. < 1000e for 5 pF sensor
- Power target spec < 500uW /channel





Digital Current Simulations

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- Important to minimise digital power consumption simulated current in supply
- Included in the simulation: Pipeline, Data Buffer, Output Shift Register, Pipeline Control, Trigger Decoder and Readout Sequencing Logic, parasitic RCs.
- Not Included: I²C interface and registers, SLVS Rx/Tx, DC-DC Converter
- Simulated for maximum trigger rate of 13.3MHz and also for no triggers.







Simulated

- The Digital power Consumption is shown in the table below.
- Clock Rate of 40Mhz, Power Supply 1.2V, No SLVS Tx/Rx , I²C

Trigger Rate	Temp	Current mA (RMS)	Power (1.2V) mW	Power/ Channel uW
0	-50	3.4	4.1	32
0	+50	3.7	4.4	35
13.3MHz	-50	4.7	5.6	44
13.3MHz	+50	5.1	6.1	48

Measured

- Digital Power Consumption < 50uW/channel</p>
- Compares nicely with simulations





CBC Power Consumption

Measured	per channel
Analogue	130 + (21 x C _{SENSOR} [pF]) uW
Digital	50uW
Total	180 + (21 x C _{SENSOR} [pF]) uW
5pF Sensor	300uW (Target <500uW)
APV25	~2.6mW (long strips)

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Known Problems

Global comparator threshold (VCTH)

> When hits occur on multiple channels get interaction with VCTH through the feedback resistors. Fixed by providing external voltage

Not difficult to fix on next version

Decoupling required

> External decoupling is required on several of the biases

Dummy analogue channel

> The dummy analogue channel does nor provide a clean signal, there is transient ringing – can be used for DC behaviour

> May be an issue with the test board

Conclusions



CBC prototype working well

- Performs within noise and power budget

A lot more testing to do

- Powering options including onchip DC-DC converter and LDO

- Temperature
- Tests including sensors
- Radiation
- Test Beam

Future Work

- 256 channel chip
- Inclusion of on-chip test pulse
- On chip DLLs for timing adjust
- Dual layer strip coincidence logic for providing trigger signal

- Bump bonding





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Imperial College

Mark Raymond for his design work on the front end, and all the testing

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Thanks for listening

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