CBC performance with switched capacitor DC-DC converter

Mark Raymond, Tracker Upgrade Power Working Group, February 2012.

CBC power features

2 powering features included on CBC prototype

LDO regulator (1.2 -> 1.1) feeds analog FE

provides stable voltage rail and supply noise rejection

2.5 -> 1.2 DC-DC converter

allows to power CBC using single 2.5 V rail

thanks to Michal Bochenek and Federico Faccio for the design and help with incorporating the layout into the CBC



CBC power features - DC performance

DC-DC switched capacitor converter

converts $2.5 \rightarrow 1.2$

clearly functioning, high efficiency ~ 90%

study of DC-DC switching effects on noise follows in next slides

LDO linear regulator

provides clean, regulated rail to analog FE

~ 1.2 Vin. 1.1 Vout

dropout ~ 40 mV for 60 mA load

provides > 30dB supply rejection up to 10 MHz

for further details see:

http://www.hep.ph.ic.ac.uk/~dmray/CBC documentation/ CBC Tracker Electronics May 11.pdf



1.10

1.05

1.04 1.05 🗕 60mA load

1.15

LDO input voltage [V]

1.20



DC-DC powering option

can power CBC from single +2.5V supply 1 MHz diff. clock to DC-DC circuit DC-DC 1.2V feeds VDDD (dig. supply) and VLDOI (LDO I/P) 4 external capacitors minimum (actually 5 in this picture)



to study effects on analog performance



GND

+2.5V

at least 2 possibilities for adverse effects

- 1) noise on DC-DC O/P rail could affect analogue performance via VDDA rail (though LDO should reject)
- 2) DC-DC circuit noise could couple to front end via another path (substrate, GND, ..)

study here concentrates on 2nd path by providing analogue rail from external clean supply

will provide digital rail either from external supply or from DC-DC output (when DC-DC operating)

adding external capacitance

want to measure noise (from s-curves) dependence on external capacitance plug-on boards containing arrays of capacitors connect to bonded out channels acquire s-curve for one of the bonded out channels





s-curves:reference measurement

measure s-curves for single channel for different external capacitances

conditions for measurements on this slide

digital circuitry supplied with external 1.2 V supply

DC-DC not running

CBC triggered at fixed time following a fast reset

=> always triggering same pipeline location

gives cleanest possible measurement as reference

(no reason to expect any effect from random triggering, but just to check)



s-curves: DC supply (random trigger)

now repeat for random triggering

digital circuitry still supplied with external 1.2V supply

DC-DC still not running

but fast reset removed

pseudo-random trigger, so now triggering locations throughout pipeline

no effect on s-curves visible (i.e. no effect on noise)

(as expected)



s-curves: DC-DC running (fixed trigger time)

now feed digital circuitry with DC-DC 1.2 V

DC-DC now running

return to triggering at fixed time following a fast reset

DC-DC clocked at 1 MHz with fixed phase relationship to fast reset

once again - no significant effect on s-curves

=> DC-DC circuit doesn't affect intrinsic noise



s-curves: DC-DC running (random trigger)

now try pseudo-random triggering again

DC-DC still running

s-curves now distorted for larger capacitance

=> something to do with random triggering when DC-DC circuit operating

an effect associated with specific pipeline locations?

try to understand what's going on with a more systematic study

=> look at s-curve dependence on triggered pipeline location

s-curve dependence on triggered pipeline loc'n



increasing external capacitance



effect becomes much more noticeable

for largest external capacitance



s-curves in top plot colour coded to show which ones correspond to which point in bottom plot

some distortion visible for most negatively shifted curves (out of amplifier linear range)

so DC-DC circuit operation somehow affects channel pedestal

magnitude of effect proportional to external capacitance to ground

repeat for external DC supplies



just to check

effect goes away completely if DC-DC circuit not operational

what's going on?

behaviour most likely due to DC-DC circuit operation causing difference between internal and external grounds

would result in spurious charge injection proportional to $\mathrm{C}_{\mathrm{EXT}}$



can anything be done to improve situation?

better connection between GND_{INT} and GND_{EXT} ?

ultimately limited by bond wires

is present test setup optimal?

have tried to improve following discussions with CERN engineers

start by taking a critical look at CBC test board

CBC test board copper layout



double-sided pcb

~ solid ground on bottom surface connected (PTH) to ground on top surface

CBC glued on the centre ground area

ground brought out from under chip to bond pads

possible deficiencies



too cautious about keeping bonding area clear - capacitors could have been positioned closer to chip

could have put more plated through holes in

have tried to "make improvements" to existing board to see whether performance is affected

"improvements"

have tried to improve grounding and decoupling by turning this

into this





 this is the final version of the test board after all modifications

chip glob-topped to protect bonds

will go through modifications step-by-step for clarity - describing changes and showing resulting effects on s-curves

first take reference measurement



measure s-curves as before for 3.8 pF added external cap.

look at 3 channels at top, middle and bottom of chip

improved ground coupling between CBC and external capacitor board



three lengths of tinned copper braid soldered to ground plane on back of CBC board

connected to ground area on external capacitor board



effect of improved grounding



some differences - most noticeable for channel 60

improved 2.5 V rail decoupling



2.5V decoupled closer to the chip

extra copper piece added adjacent to 2.5 V input, soldered to ground

additional 100 nF capacitor soldered as close as possible to bond pad

improved 2.5 V rail decoupling - reality



effect of improved 2.5 V decoupling



ch124 gets appears to get worse, ch 4 gets better

24

extra ground contacts



effect of extra ground contacts



not much difference

additional shielding



efect of additional shielding



channel 60 now looks a bit strange

28

some more capacitor repositioning



some more capacitor repositioning



effect of capacitor repositioning



some effects on all three channels - not obvious what conclusions to draw

conclusions?



no dramatic improvement in behaviour

clearly some effects but no strong indication of a "magic solution"

might be able to do better with new improved board layout?

but seems unlikely that all "undesirable" effects can be made to go away

summary

fundamental performance of DC-DC circuit itself is good

high efficiency for 2:1 step down conversion

no significant effect on intrinsic noise

but switching transients appear to couple to internal chip ground causing pedestal shifts

- magnitudes dependent on external capacitance

worth noting: this would likely not be a problem for hybrid pixel chips

low sensor capacitance low inductance bump-bond coupling between sensor and chip grounds

what next?

more measurements? - I'm open to suggestions

CBC2 will include same DC-DC circuit

bump-bond layout ought to help significantly with performance (better coupling between on and off-chip grounds)

