CBC update

CBC prototype

last report on CBC prototype results in October tracker week
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_status_Oct_2011.pdf

some recent measurements of switched capacitor DC-DC circuit will be shown in PWG
(1 slide summary here)

CBC2 - 254 channel, C4 bump-bondable chip for 2S-Pt modules

outline of plans for next CBC version by Davide Braga (RAL) at Nov. Fermilab workshop
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Davide_FNAL_Nov_11.pdf

reminder of architecture, new features, current status and schedule here

CBC prototype summary

features

- designed for short strips, ~2.5–5cm, < ~ 10 pF
- full size prototype - 128 channels
  - 50 μm pitch wirebond
- binary un-sparsified readout
- powering test features
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analog FE

main functional blocks

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- fast (SLVS) and slow (I2C) control interfaces

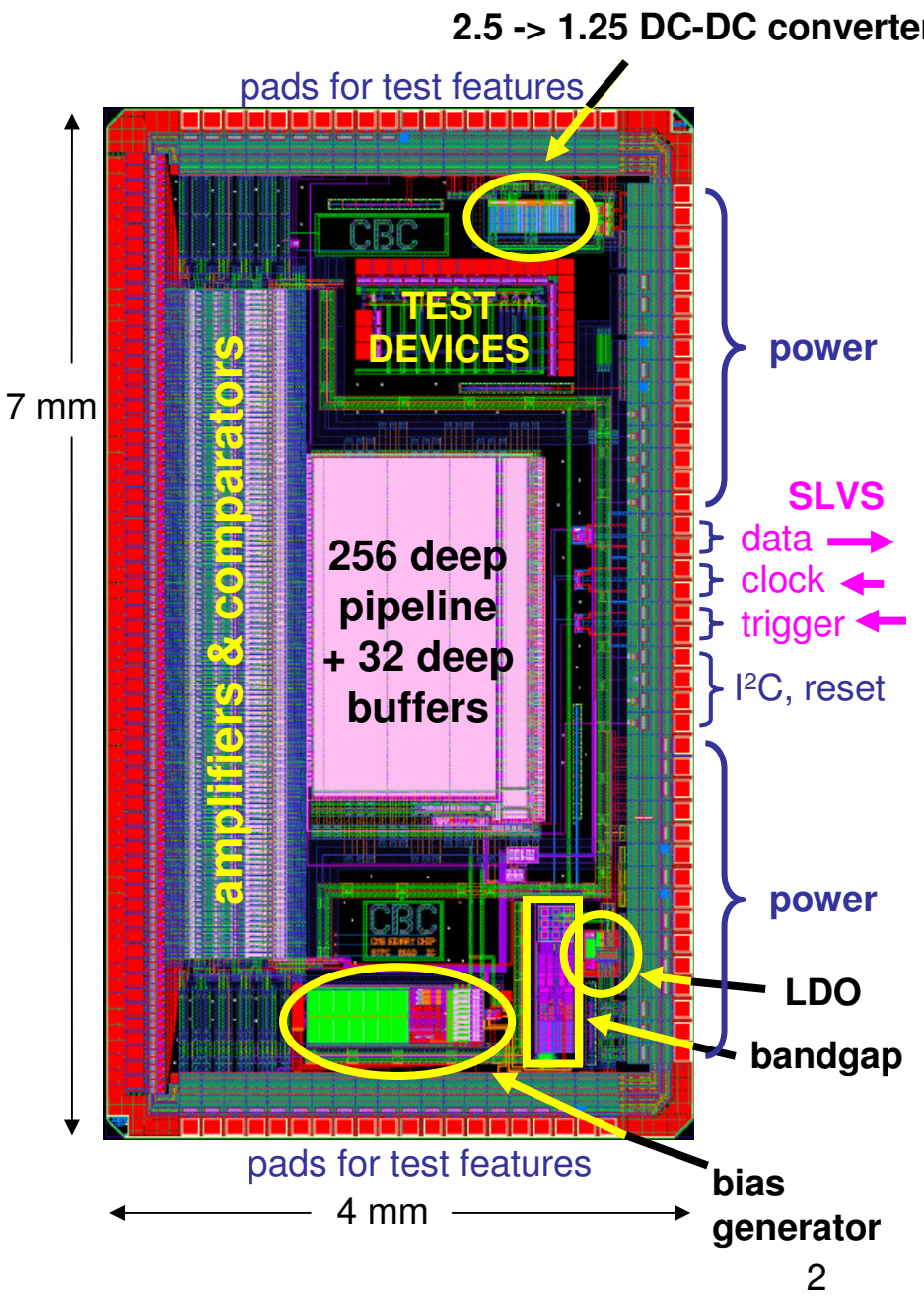
front end

- DC coupling to sensor – up to 1 uA leakage
- can be used for both sensor polarities

for 5 pF input capacitance

noise ~800e

power ~300 μW / chan.



DC-DC results: 1 slide summary

DC-DC circuit works well

high efficiency for 2:1 step down conversion
no effect on intrinsic noise

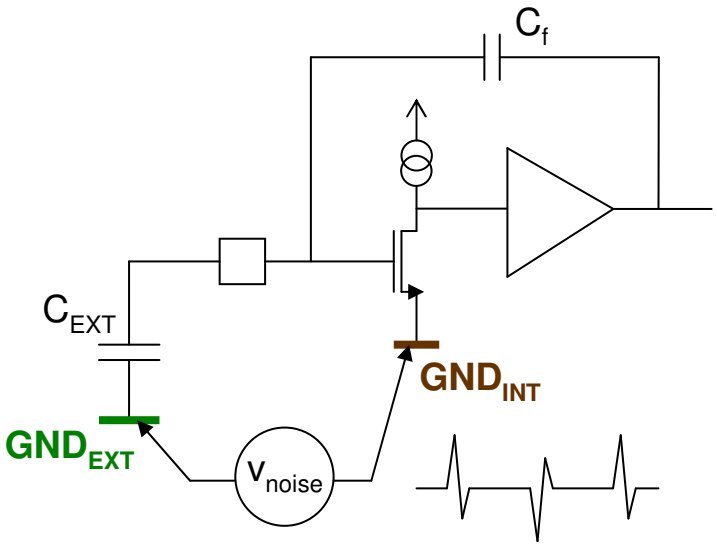
but switching transients appear to couple to internal chip ground causing pedestal shifts

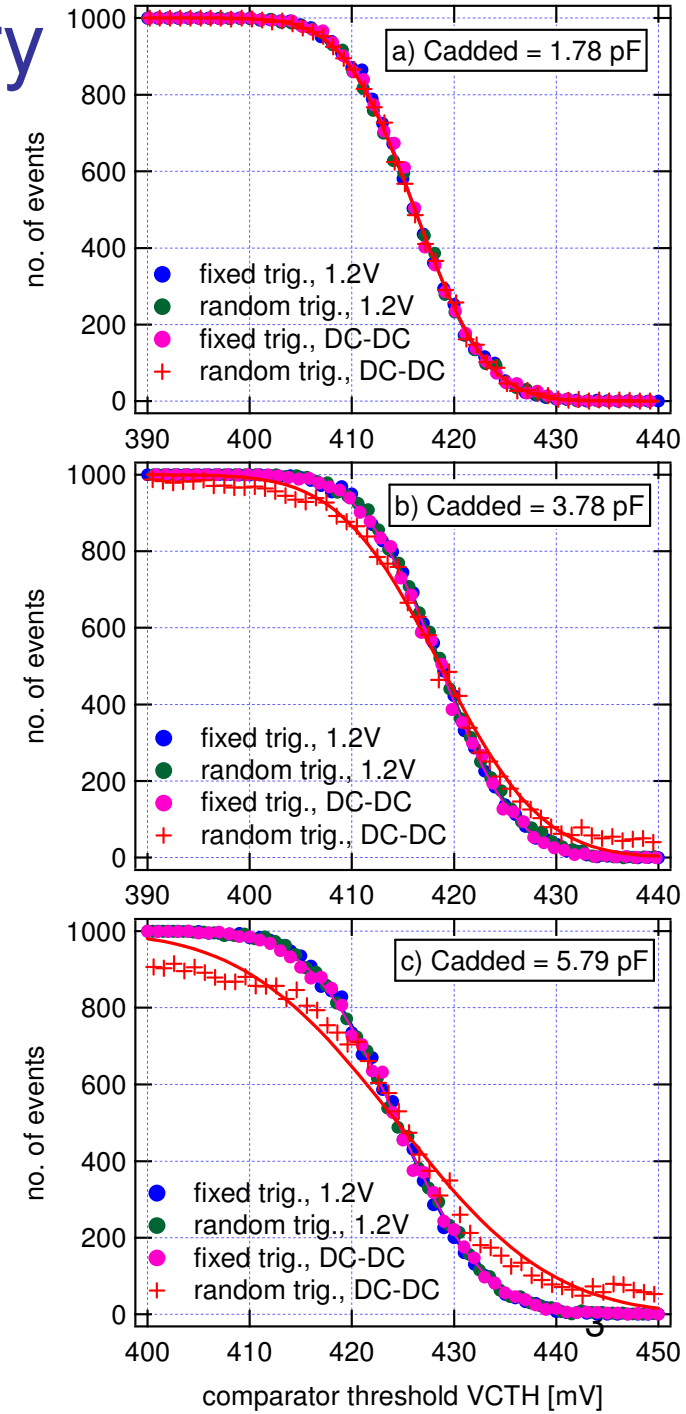
- magnitudes dependent on external capacitance

appears as extra noise if trigger randomly

see PWG talk for details of studies and efforts made to improve

note: this would probably not be a problem for hybrid pixel chips
low sensor capacitance and low inductance coupling between on and off-chip grounds



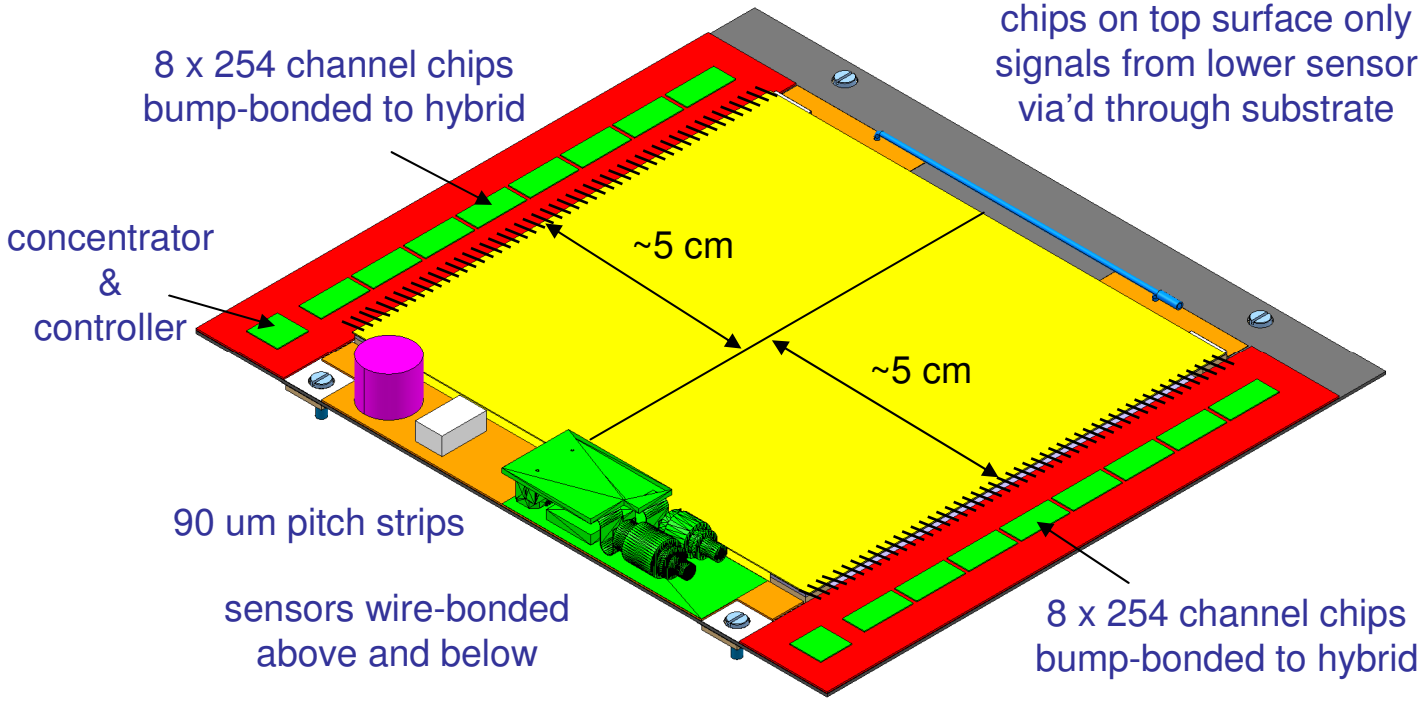


CBC2 introduction

2S-Pt “2-in-1” module concept proposed for outer tracker layers
- bring signals from 2 strip sensor layers together in one chip
- look for cluster correlations to identify high Pt stub

plan to prototype logic to implement correlation in CBC2
- allows to study issues involved with constructing such a module

=> 254 channel bump-bondable chip required
- 4064 channels total in 2 sensors



CBC(1) -> CBC2

features kept

L1 triggered architecture remains ~ same
(some bug fixes)

powering features
DC-DC and LDO
bump-bonding should help a lot with
DC-DC circuit performance

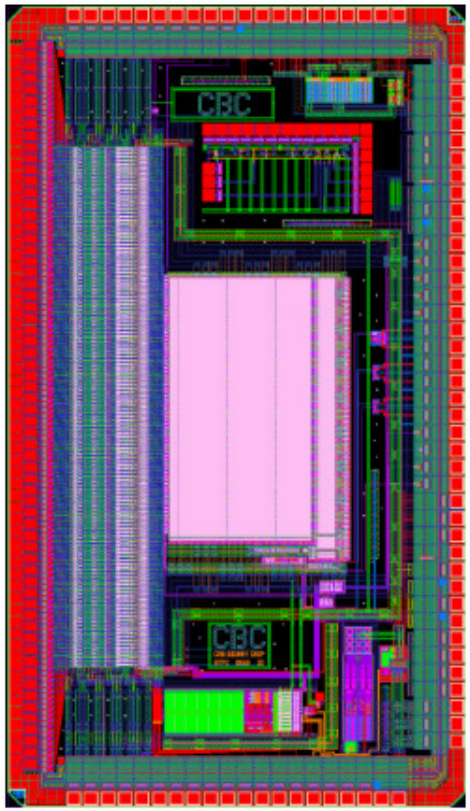
new features

250 μm C4 bump-bonding

254 channels (not 256)
allows correlation between 127
strips on top and bottom sensors
(one spare binary code)

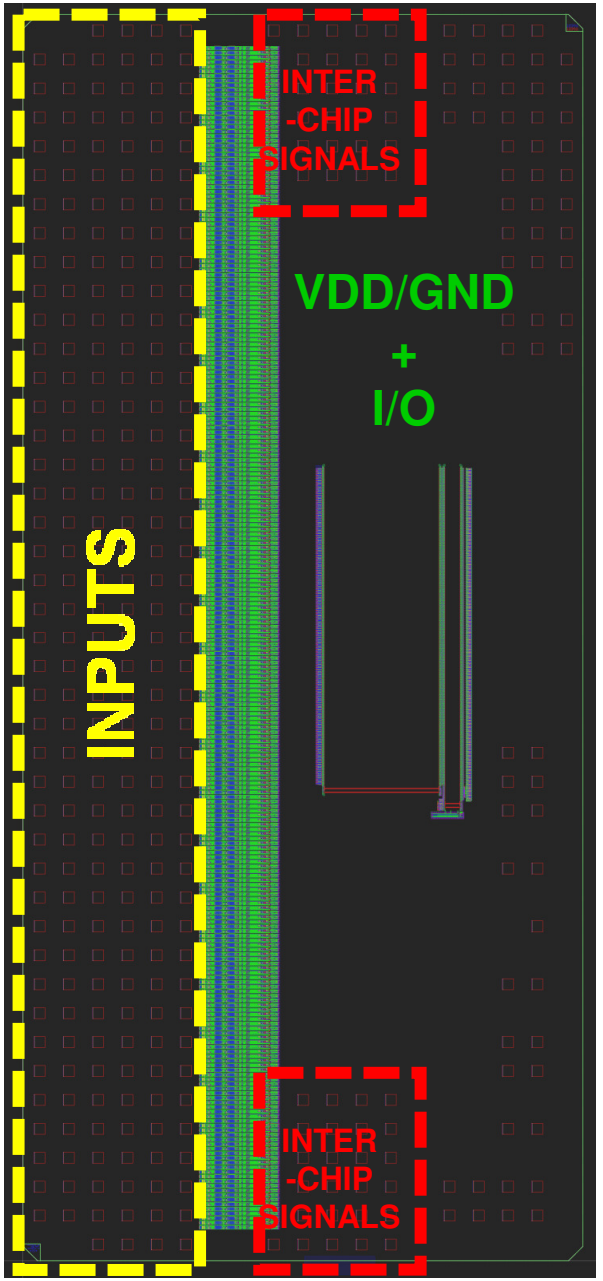
internal test pulse
programmable amplitude & delay

trigger output if correlation between clusters
programmable window and offset

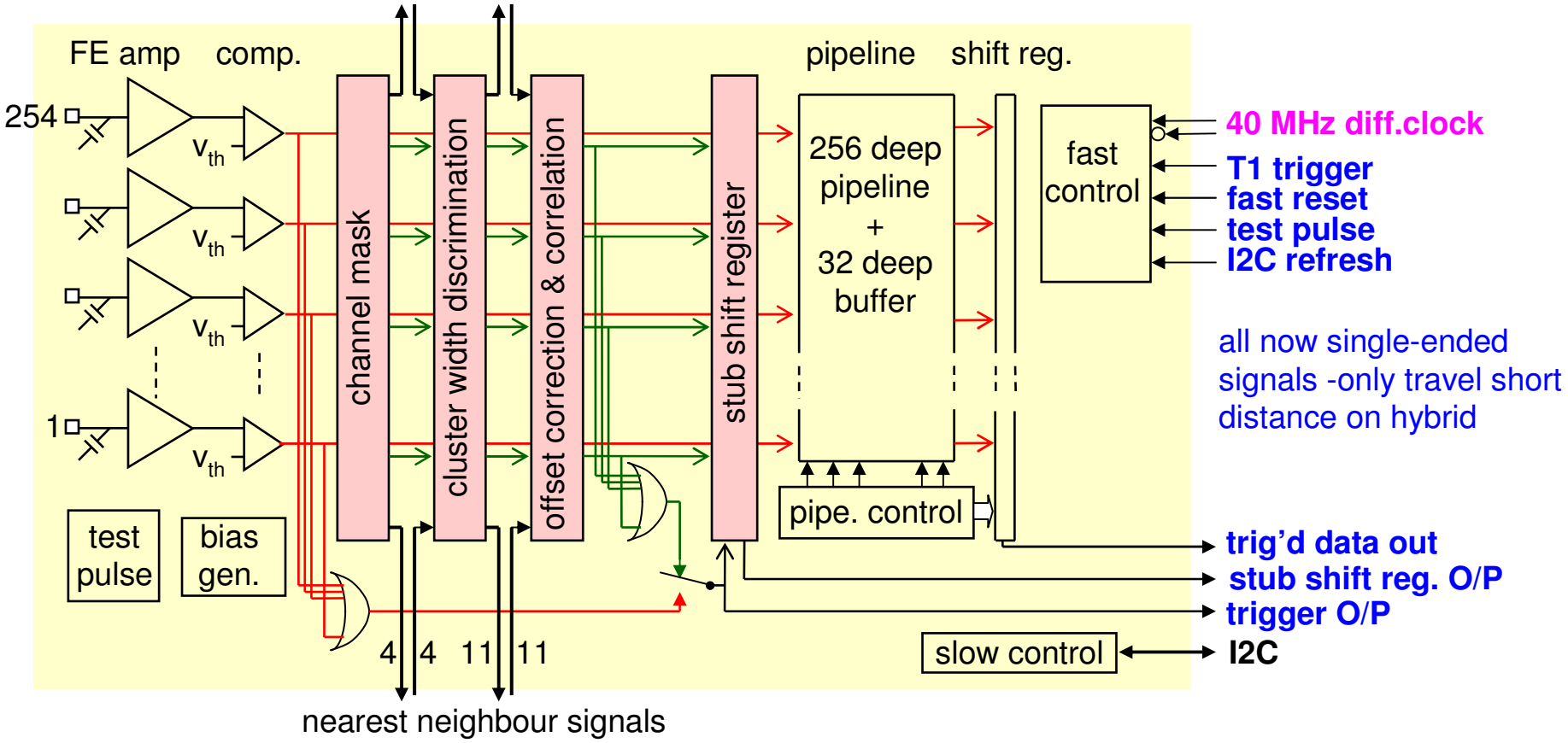


existing chip
128 channels
wirebond: 50 um pitch
7mm x 4mm

next version
254 channels
bump-bond: 250 um pitch
10.75mm x 4.75mm



CBC2 architecture



blocks associated with Pt stub generation

channel mask: block noisy channels

cluster width discrimination: exclude wide clusters

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip

for normal operation choose correlation O/P

neighbour chip signals - comparator O/Ps

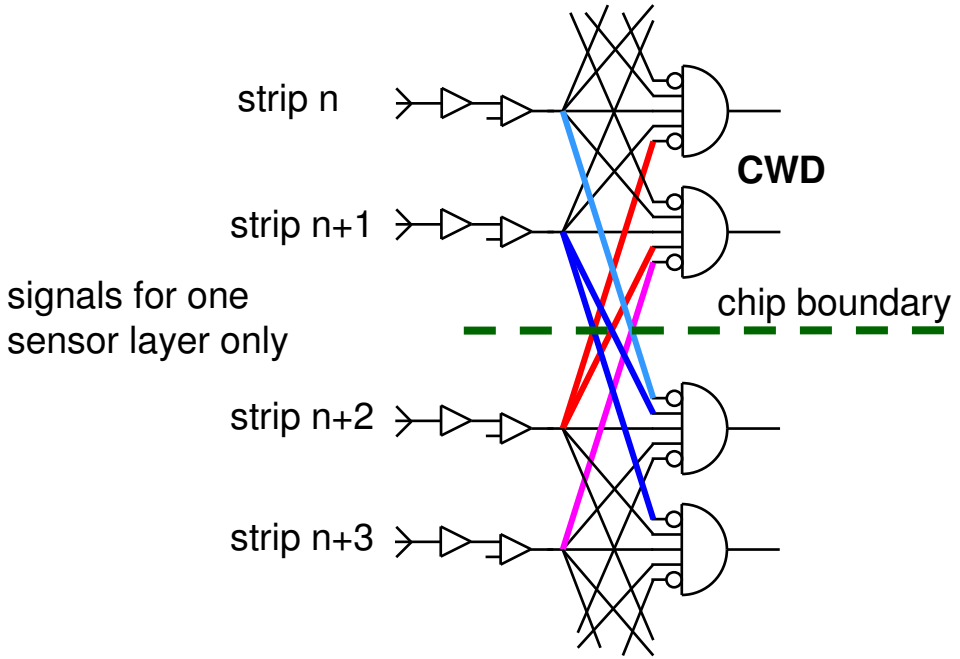
need to transfer signals across chip boundaries

for cluster width < 3 need (for each sensor layer)

to pass comp. O/Ps from 2 edge channels to neighbour
to receive comp. O/Ps from 2 edge channels on neighbour

=> 4 signals for single sensor layer

=> 8 signals for both layers



neighbour chip signals - CWD O/Ps

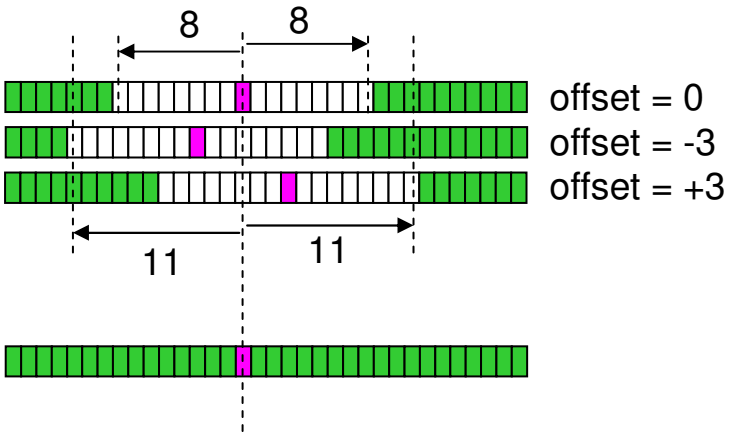
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

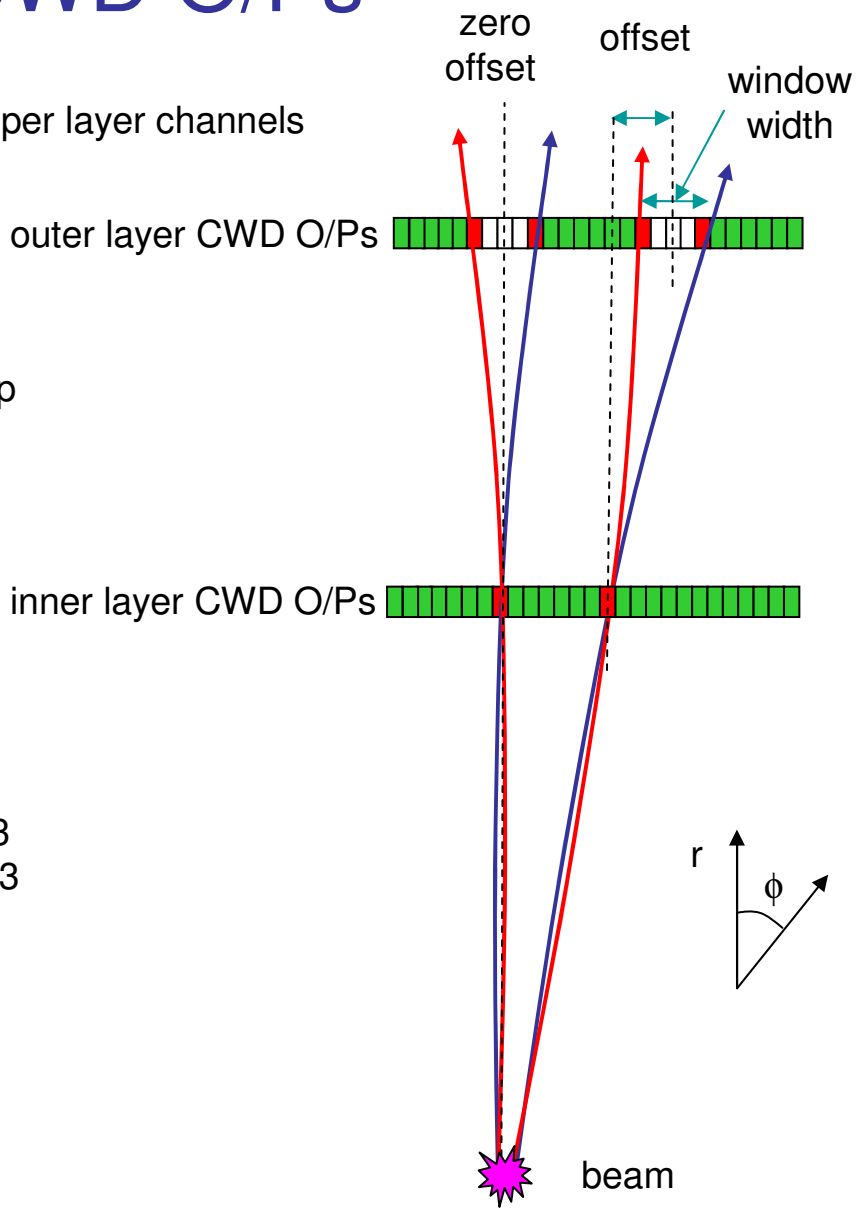
window defines Pt cut
width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
11 to receive from neighbouring chip

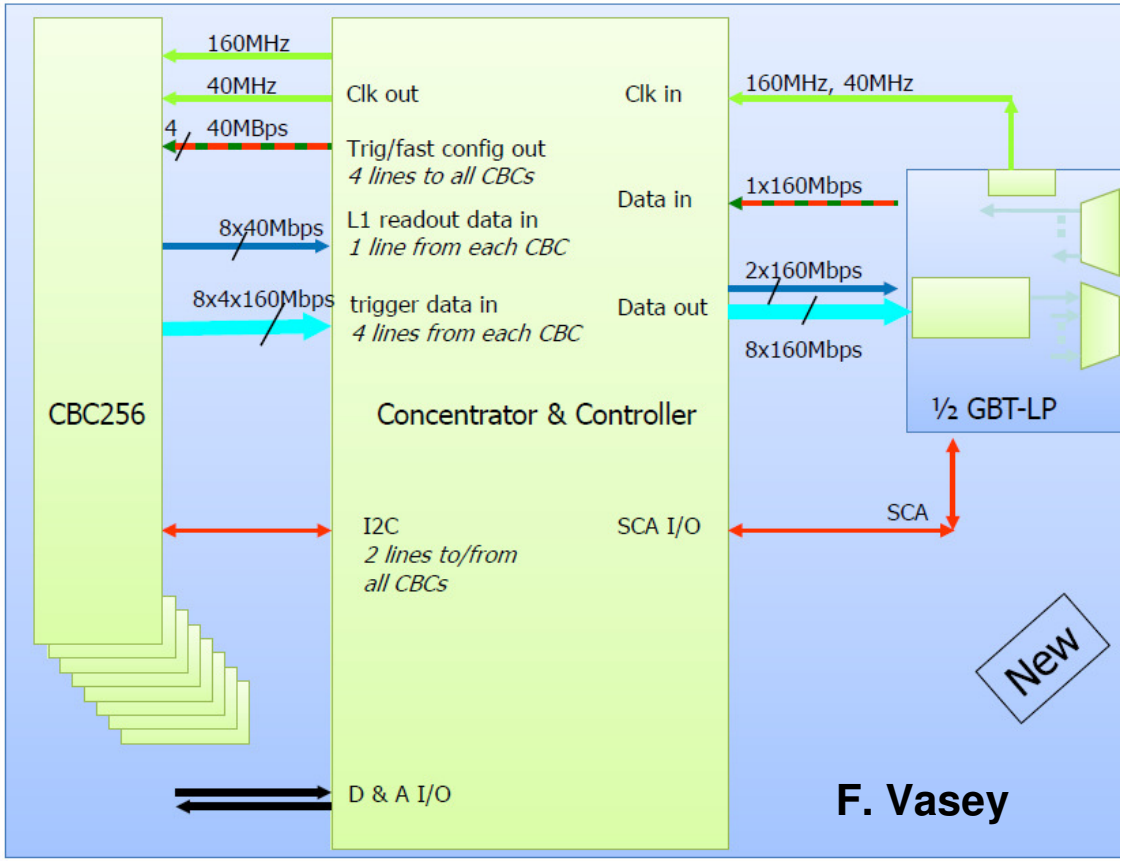
= 22 signals





adding comp O/Ps -> 30 signals altogether, top and bottom of chip

trig./fast config lines



departure from APV and CBC prototype triggering scheme (trigger/fast reset101/test pulse all encoded on single 40 Mbps line)

now use 4 single-ended 40 Mbps lines from GBT-LP (via concentrator)

trigger: initiate readout of pipeline
- consecutive triggers allowed
=> can trigger and read out contiguous pipeline samples

fast reset: equivalent to reset 101
- relaunches pipeline pointers

test pulse: inject charge at amplifier inputs
should be followed (a latency period later) by normal trigger

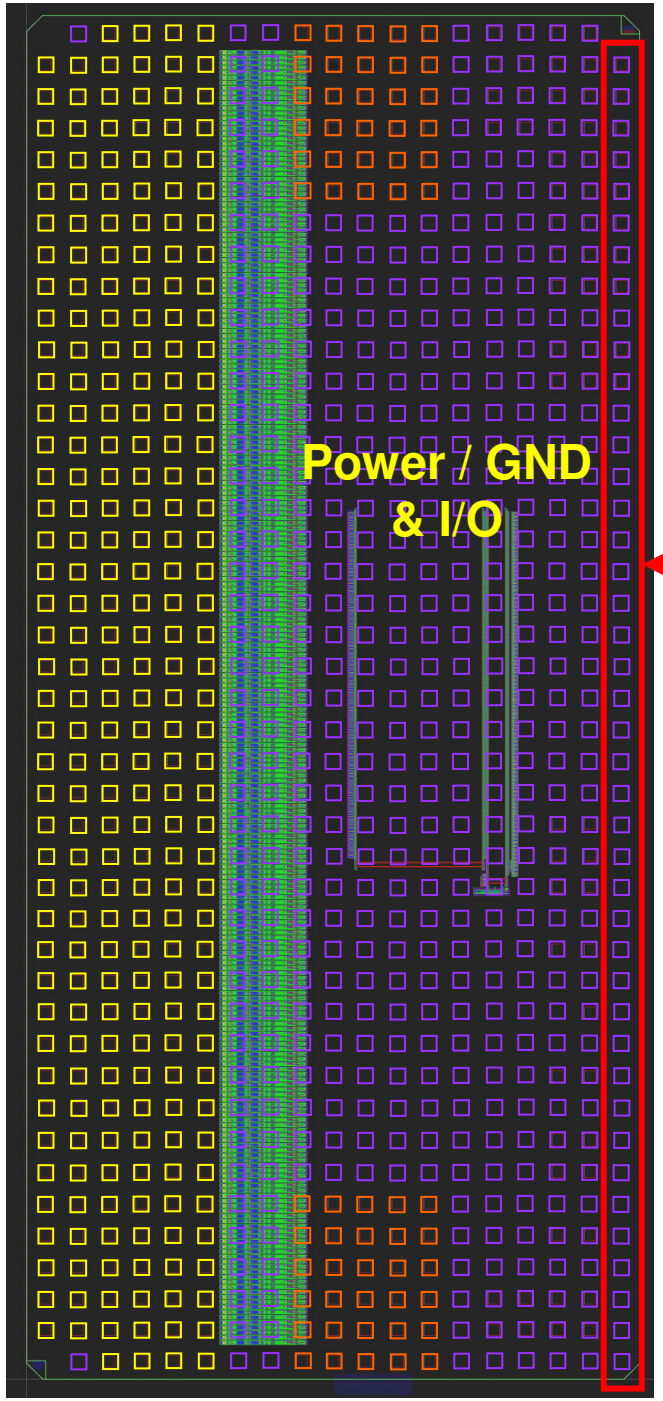
I2C refresh

I2C registers are triplicated with majority voting logic
1 upset - result stays the same, 2 upsets - voting logic changes output

NEW

I2C refresh restores all 3 blocks to same result => single upset is cancelled
using external line to do this allows to choose how often to refesh

layout status



43 rows x 19 cols = ~ 800 bumps

10.75 x 4.75 mm^2

inputs

outputs to / inputs from neighbours

probe-able pads for wafer test

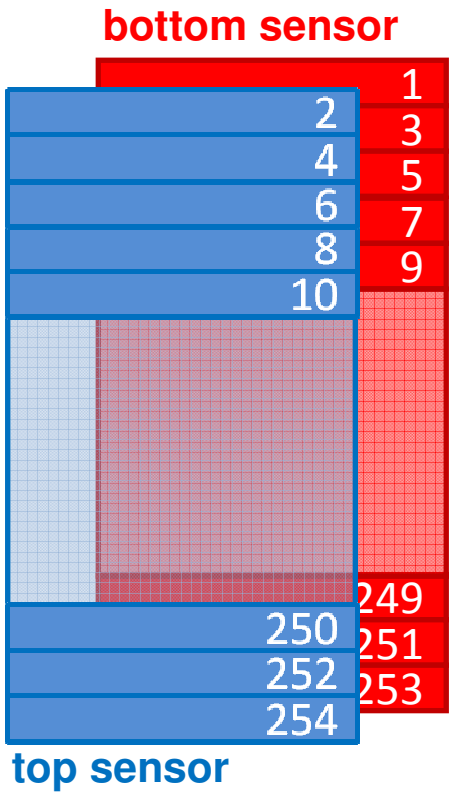
access to:
- power
- fast control
- I2C
- outputs

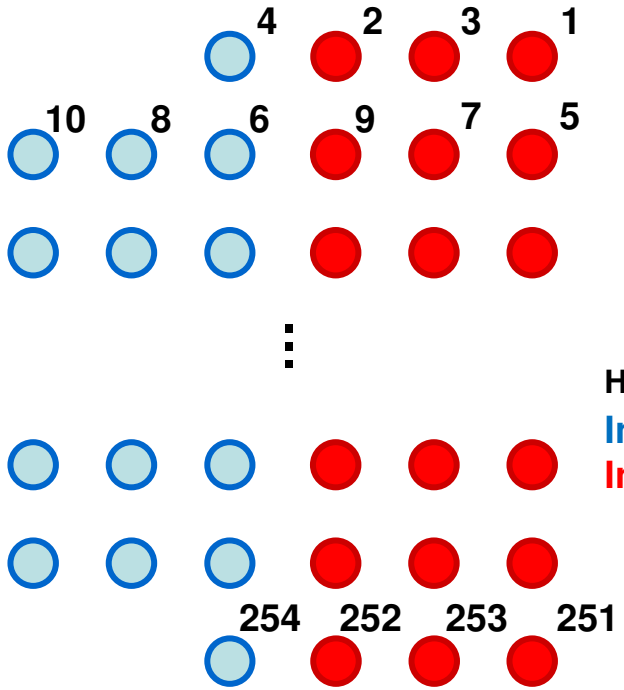
should be able to provide quite thorough test of chip functionality

connection to sensor

previously planned programmable input de-scrambler now dropped

pad assignment now fixed (agreed with Georges Blanchot)



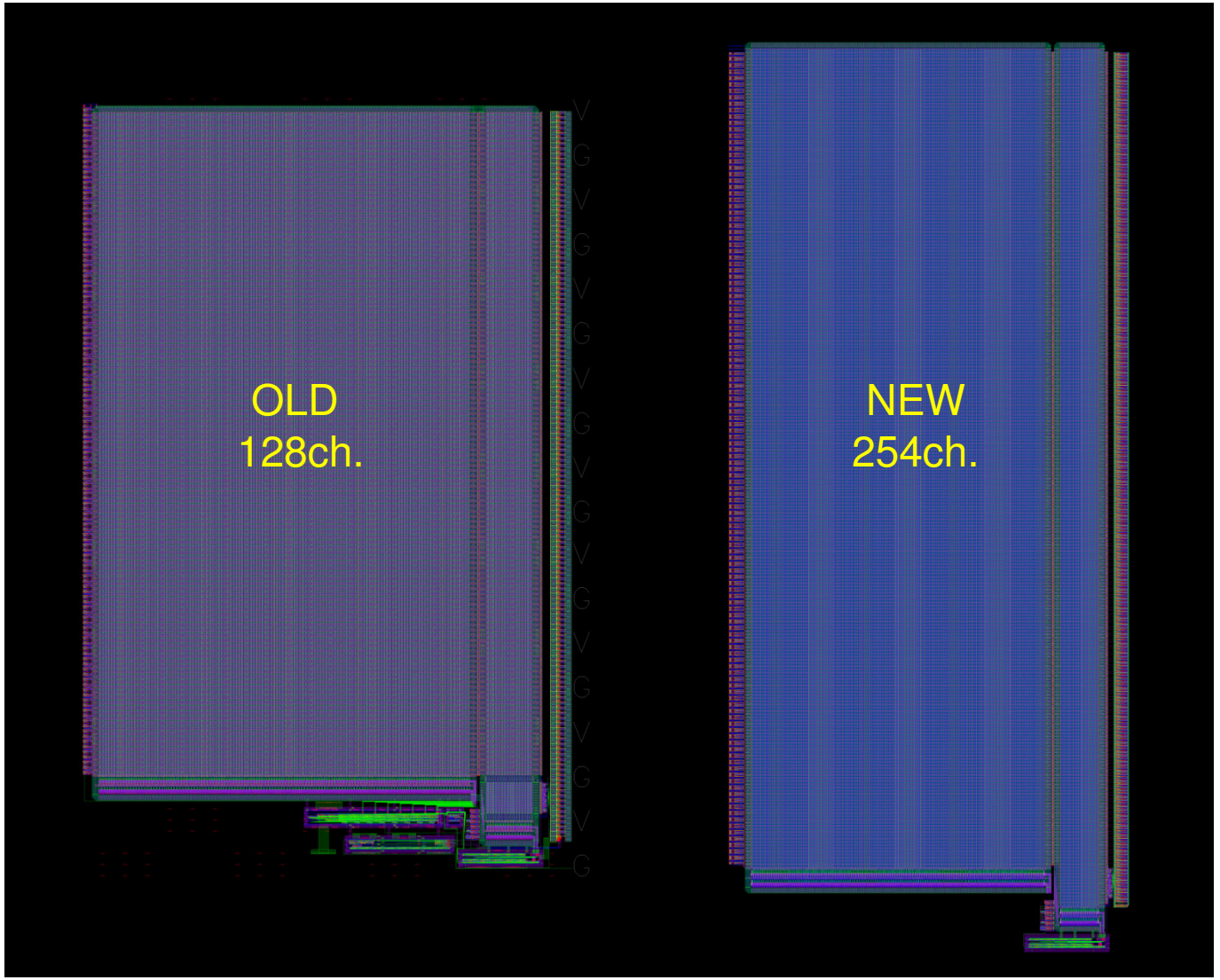


Hybrid footprint:

Inputs from top sensor

Inputs from bottom sensor

new pipeline layout



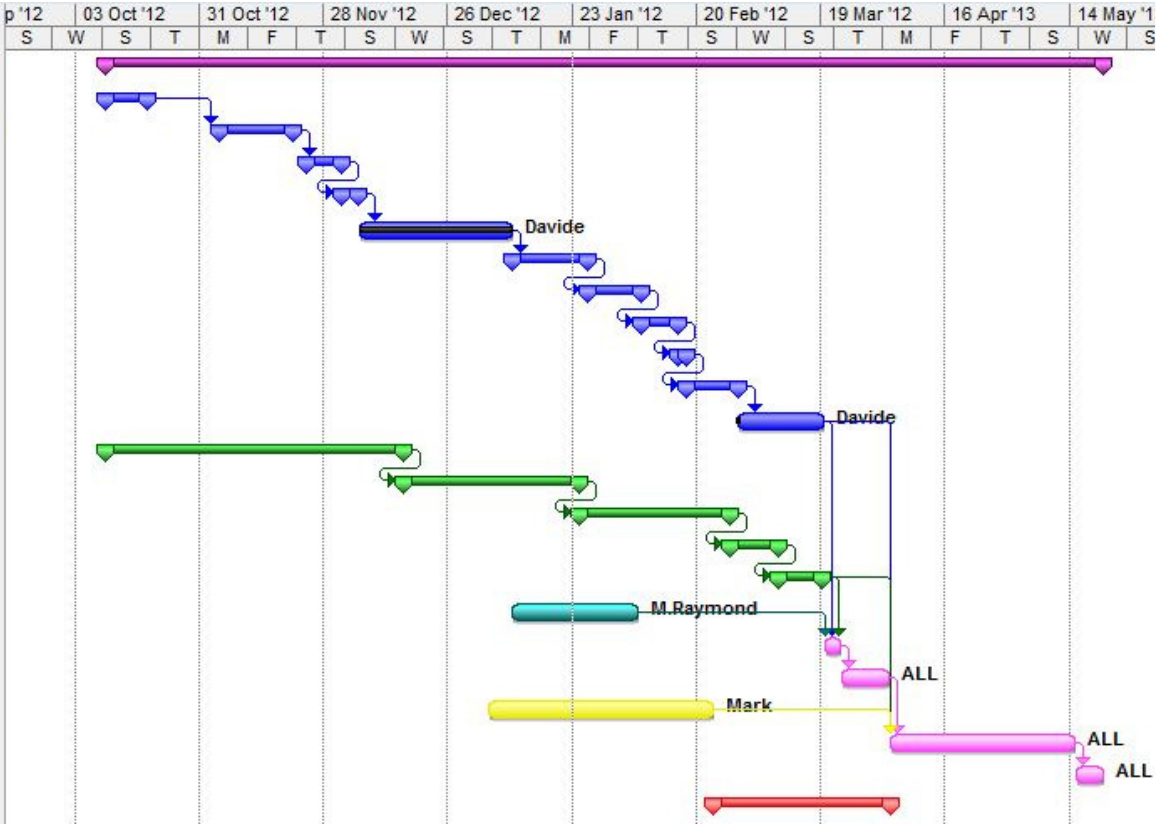
RAM cells now have folded layout: they share power lines.

Safe approach: minor modification to previous layout, keeps Wrt/Rd lines to a reasonable lenght

Write/Read drivers adapted for new extracted load and simulated.

schedule

Task Name	Start	Finish
256 channel bump-bondable CBC	Mon 10/10/11	Mon 21/05/12
Comparator Modification	Mon 10/10/11	Wed 19/10/11
Cluster Width Discrimination logic	Fri 04/11/11	Mon 21/11/11
Hit Correlation (OC&C) logic	Thu 24/11/11	Fri 02/12/11
OR of correlation outputs	Fri 02/12/11	Tue 06/12/11
Restructure & expand Pipeline	Tue 06/12/11	Mon 09/01/12
CWD, OC & C prog register	Mon 09/01/12	Thu 26/01/12
Neigbour CWD and OC&C I/O pads	Thu 26/01/12	Tue 07/02/12
OR Transmission Off Chip	Tue 07/02/12	Thu 16/02/12
OR of 256 comparator outputs	Thu 16/02/12	Fri 17/02/12
hit detect circuit re-triggering	**Fri 17/02/12**	**Wed 29/02/12**
Synthesis & Layout of digital circuits	Wed 29/02/12	Mon 19/03/12
Calibration Circuit	Mon 10/10/11	Thu 15/12/11
Parallel Command input circuit	Fri 16/12/11	Tue 24/01/12
I2C modification (1MHz + Voting Logic Refresh)	Tue 24/01/12	Mon 27/02/12
256 bit shift reg for Hit and CWD logic	Mon 27/02/12	Fri 09/03/12
Channel Masking Circuit	**Fri 09/03/12**	**Mon 19/03/12**
Analogue Design Changes (inc Band Gap)	Mon 09/01/12	Mon 06/02/12
Major Design Review (+ preparation)	Mon 19/03/12	Fri 23/03/12
Analogue Layout Changes (inc Band Gap)	Fri 23/03/12	Tue 03/04/12
Modify DRC & LVS rules for ELT	Wed 04/01/12	Fri 24/02/12
Top Level Assembly & Checks	Tue 03/04/12	Tue 15/05/12
Final Design Review & Submission	Tue 15/05/12	Mon 21/05/12
Wish List Items	**Fri 24/02/12**	**Tue 03/04/12**



CBC design team at RAL

Davide Braga, Peter Murray, Mark Prydderch

currently on track for chip submission in ~May

fabrication plans not yet finalized but probably CERN MPW run

plans

this year (2012)

single chip tests

mount untested chips on single chip substrate - Georges Blanchot (maybe dual-chip?)

untested wafer ok - yield of good chips should be high

develop wafer probing setup

probe card + custom test hardware/software
(plenty of issues to understand)

next year

8 chip substrate for module development

provide probing system to company to allow wafer test, dicing and chip mounting
all within same facility

summary

CBC prototype

switched capacitor DC-DC results in PWG meeting

CBC2

254 channel bump-bondable version for 2S-Pt modules

includes logic to implement correlation operation between clusters in 2 sensor layers

trigger output just a single bit (indicating Pt stub found)

scheme for encoding stub addresses & transmission still under consideration

expect to submit ~May