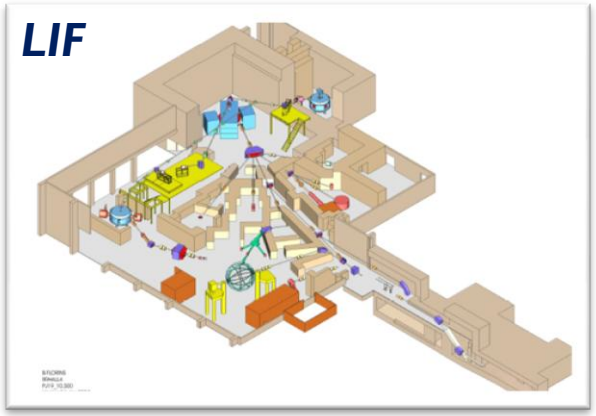
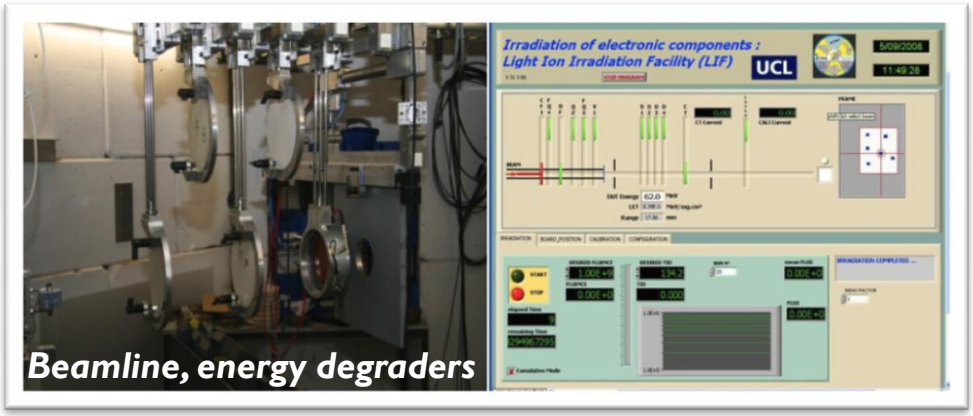
Imperial College London

UCL Université catholique de Louvain





CBC2 SEU test report

Phase 2 TK Electronics during Tracker week,
6th November 2014

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Juan Cabrera, Christophe Delaere, Jérôme de Favereau @ Universite Catholique de Louvain

Testing overview

The goal is to estimate SEU rate of CBC2 at HL-LHC empirically.

Hadron flux @ HL-LHC

$\Phi_{HL\text{-}LHC}^{Hadron(>20MeV)}$ **$=3.4\times10^{6}\ cm^{-2}s^{-1}$**

L=5x10^{34} cm^{-2}s^{-1}, *CMS_pp_7TeV_v3.0.0.0_FLUKA, r=60cm, z=260cm,*
by FLUKA
https://cms-project-fluka-flux-map.web.cern.ch/

SEU cross section measurement result on silicon in NIM A 450(2000)155-172

SEU cross section of hadrons with 2-20 MeV is one order smaller than that above 20 MeV.

SEU cross section of hadrons with more than 20 MeV are almost the same and energy independent.

- Beamtest on 8th & 9th in Sep. 2014
  - Proton beam line at UCLouvain
  - Flux Φ_{LIF} **$\sim2.5\times10^{8}\ cm^{-2}s^{-1}$**
  - 62.0 MeV
- SEU rate of CBC2 at HL-LHC

  Assuming the hadron flux at HL-LHC to be, $\Phi_{HL\text{-}LHC} = 1\times10^{7}\ cm^{-2}s^{-1}$,
  the SEU cross section by proton at LIF representing that by hadrons at HL-LHC,

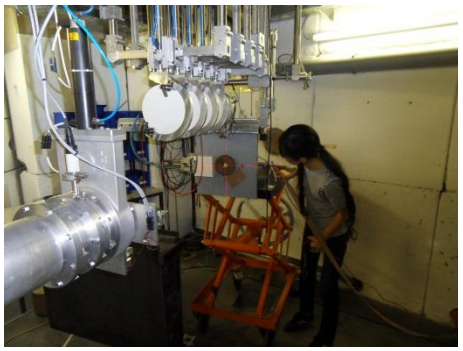
  SEU rate @ HL-LHC
  = 0.04 x SEU rate at the beamtest

  Just scaling the rate by the ratio of the flux of proton at LIF to the hadron flux at HL-LHC.

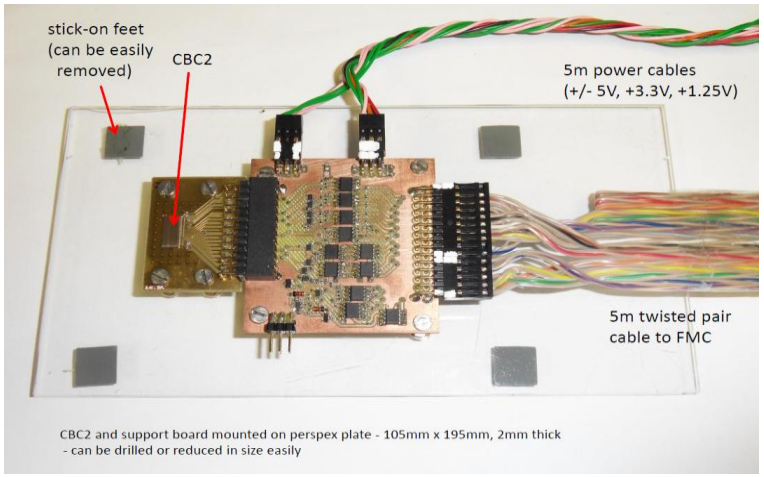
Beamtest setup

- **Beam : Proton Cyclotron in Light Ion Irradiation Facility (LiF) at UC Louvain.**

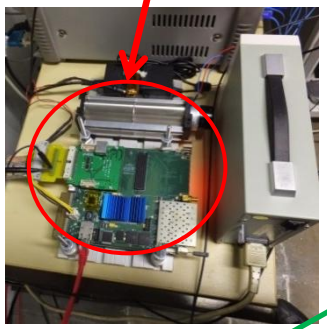
Property	Value
Energy	Up to 62 MeV
Max Flux	$5x10^8$ p $cm^{-2}s^{-1}$
Homogeneity	10%
Spot size	8cm

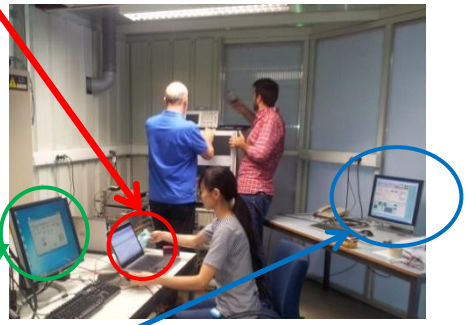


- **CBC2 module setup : 1 CBC2**



- **Error monitoring :**
  1 BE GLIB (Modified firmware)
  & CbcTest software





- **CBC current and beam monitoring system**
  Thanks to Christophe and his colleagues

Three types of SEU test for different components

Pipeline logic [SEU tolerant D-type FF]

SEU effect shows up in the error bits or incorrect pipeline address in the header.

Pipeline cells [SEU tolerant D-type FF]

SEU effect shows up in the channel hit information in the data.

I2C registers

majority voting scheme :

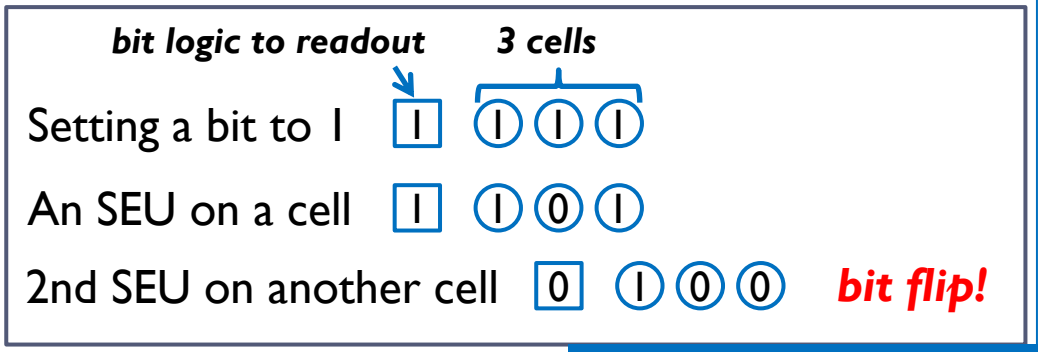
There are triplicated logic cells for each bit and the majority state is the output

Refresh (external signal for CBC2) :

Sets all three cells to the majority state. If only a single cell has flipped, the refresh can reset the flipped cell to the initial state. If two cells flipped, refresh set the unflipped cell to the flipped state.

- A single SEU does not flip the bit. Reasonable frequency of refresh should reduce the number of flipped bits.

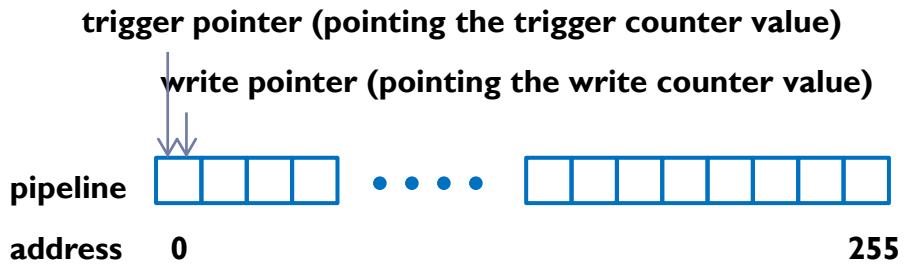
SEU is monitored by reading the I2C registers periodically. (The refresh signal was also enabled for some runs to check the performance of the reset.)



We want to send refresh before the 2nd SEU

Pipeline test

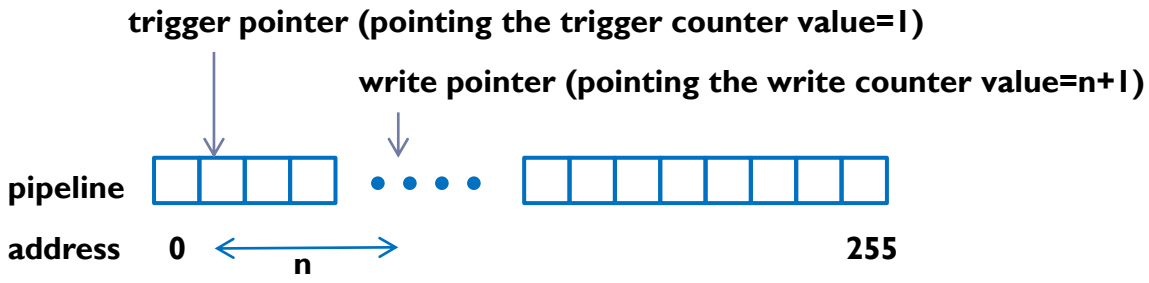
- Pipeline read / write procedure
  - Reset signal is sent to CBC2,
    CBC2 resets the pipeline logic and starts the write counter.



Pipeline test

Pipeline read / write procedure

- Reset signal is sent to CBC2,
  CBC2 resets the pipeline logic and starts the write counter.
- After n clock cycle (I2C register setting: trigger latency),
  CBC2 starts the trigger counter.

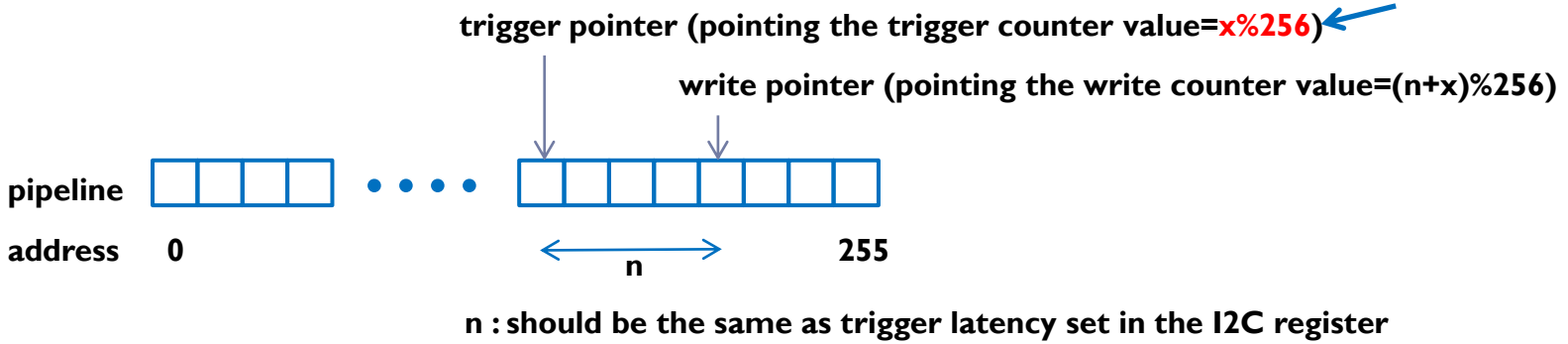


Pipeline test

Pipeline read / write procedure

- Reset signal is sent to CBC2,
  CBC2 resets the pipeline logic and starts the write counter.
- After n clock cycle (I2C register setting: trigger latency),
  CBC2 starts the trigger counter.
- Trigger is sent to CBC2 after a certain number of clock cycles(n+x) from the reset,
  CBC2 reads the data stored at trigger pointer,
  and checks if the difference between write and trigger counters matches trigger latency in I2C register,
  if they do not match, the error bit is set in the header.

Checked in the pipeline logic test



Pipeline logic test result

- 3 errors in 1.2×10^4sec (3.3 hrs)
  - An event with all channels set to 1 instead of 0
    (VCTH is set so that no channel is fired in normal case.)
  - 2 events with wrong pipeline address in the header

SEU(related to pipeline logic) rate per chip at HL-LHC

$[3.6 \pm 2.0] \times 10^{-2}$ hour^{-1}

these "chips in error" would be recoverable using fast reset

Pipeline cell test result

- No data bit flip was observed in 3.1×10^3sec (0.86hrs).

  The time corresponds to 22 hours at HL-LHC,
  but the test is done for only 1 out of 256 pipeline column.

SEU rate in pipeline cells per chip at HL-LHC upper limit

$$R_0 = 7.1 \times 10^{-3}\ sec^{-1}\ (CL=90\%)$$

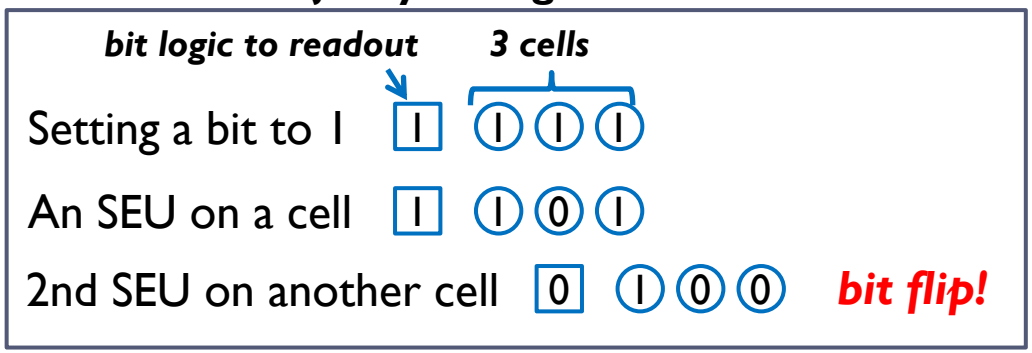
=> Negligible

I2C register test

- I2C register test cycle
  - I2C registers are set.
  - Refresh signals are sent periodically for some runs.
  - I2C registers are readout after T_0 from the setting.

The probability of logic flip per bit during time T_0 is expected to be proportional to T_0^2
$P(T_0) = 3r^2T_0^2$, where r is the rate of SEU on a cell (page 18).

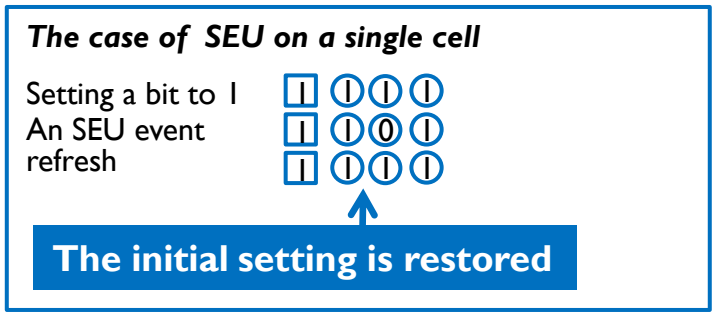
majority voting scheme

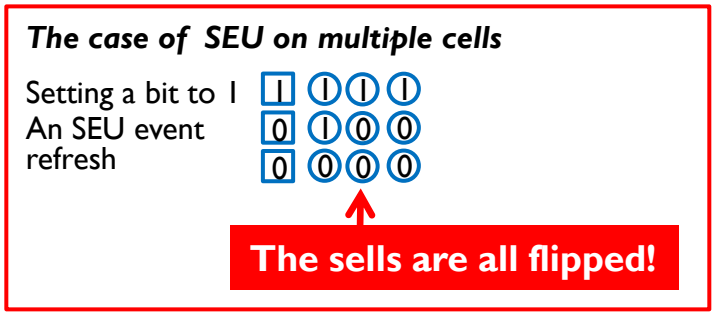


I2C register test result

- 21 of 0 → 1 and 57 of 1 → 0 bit flips were observed for total 33 cycles of T_0=10 mins w/o refresh signal.
- 12 of 0 → 1 and 30 of 1 → 0 bit flips were observed for 20 cycles of T_0=10 mins with refresh signals.
  refresh signal does not give a good improvement.

  Possibly the triple cells are too close to each other ~μm.
  → A single SEU on multiple cells could therefore be suspected.





- The overall SEU rate is low, but in some cases, multiple bit flips are happening in a single 8-bit register???

Time	Page	Address	Written	Read	
Sep 8 19:09:24	1	A9	0101,0111	**1101,0111**	
Sep 8 19:09:24	1	B1	0100,0110	**0101,0101**	!
Sep 8 19:09:24	1	D2	0100,0011	**0100,0001**	
Sep 8 19:19:51	1	E0	0101,0000	**0101,0101**	!
Sep 8 19:30:19	1	6D	0101,1100	**0101,1000**	
Sep 8 19:40:45	0	45	0100,1100	**0100,0101**	!

I2C register test result

The probability $P(T_0)$ to observe bit flip during T_0 is different for the two cases,

- The case with SEU on a single cell,

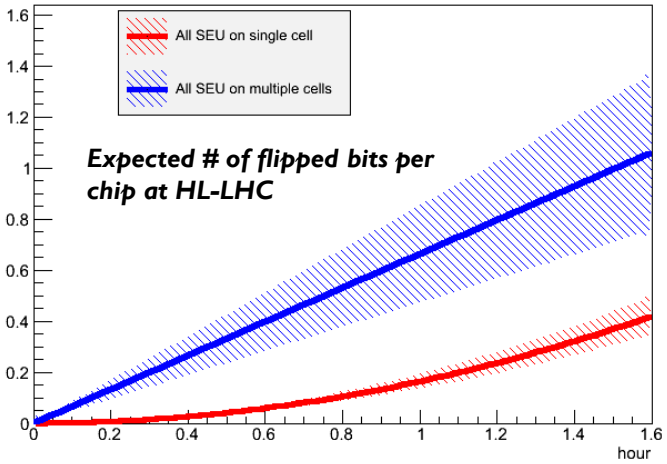
  $P(T_0) = 3r^2T_0^2$, where r is the rate of SEU per cell (p18).

- The case with SEU on multiple cells.

  $P(T_0) = rT_0$, where r is the rate of SEU per bit (p19).

Expected # of flipped bits in I2C register per chip at HL-LHC using data from the runs without refresh

$N = [1.6 \pm 0.3] \times 10^{-1}$ SEU in an hour
with the assumption that SEU happens on each cell independently.
$N = [6.6 \pm 1.9] \times 10^{-1}$ SEU per hour
with the assumption that SEU happens on multiple cells at the same time.



The time duration between write procedures w/o refresh

I2C register setting should be written before a run to start and left for a run ~ 1 day.

Current situation does not satisfy the requirement.

Possible Solutions

- ***Use the same architecture as pipeline,***
- ***Separate cells for the triplicated logic,***
- ***etc.***

Summary

Estimation of SEU per chip at HL-LHC with the assumption of $\Phi_{HL\text{-}LHC} = 1 \times 10^{7}\ cm^{-2}s^{-1}$

- SEU rate per chip in pipeline logic

  $r = [3.6 \pm 2.0] \times 10^{-2}\ hour^{-1}$
  (If we consider the all 3 errors are due to the pipeline logic.)

- SEU rate per chip in pipeline cell

  $r < 7.1 \times 10^{-3}\ sec^{-1}$ (CL=90%)

- Expected # of flipped bits in I2C register per chip without refresh.

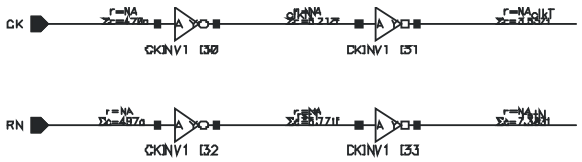
  $N = [1.6 \pm 0.3] \times 10^{-1}$ SEU in an hour
  with the assumption that SEU happens on each cell independently.

  $N = [6.6 \pm 1.9] \times 10^{-1}$ SEU per hour

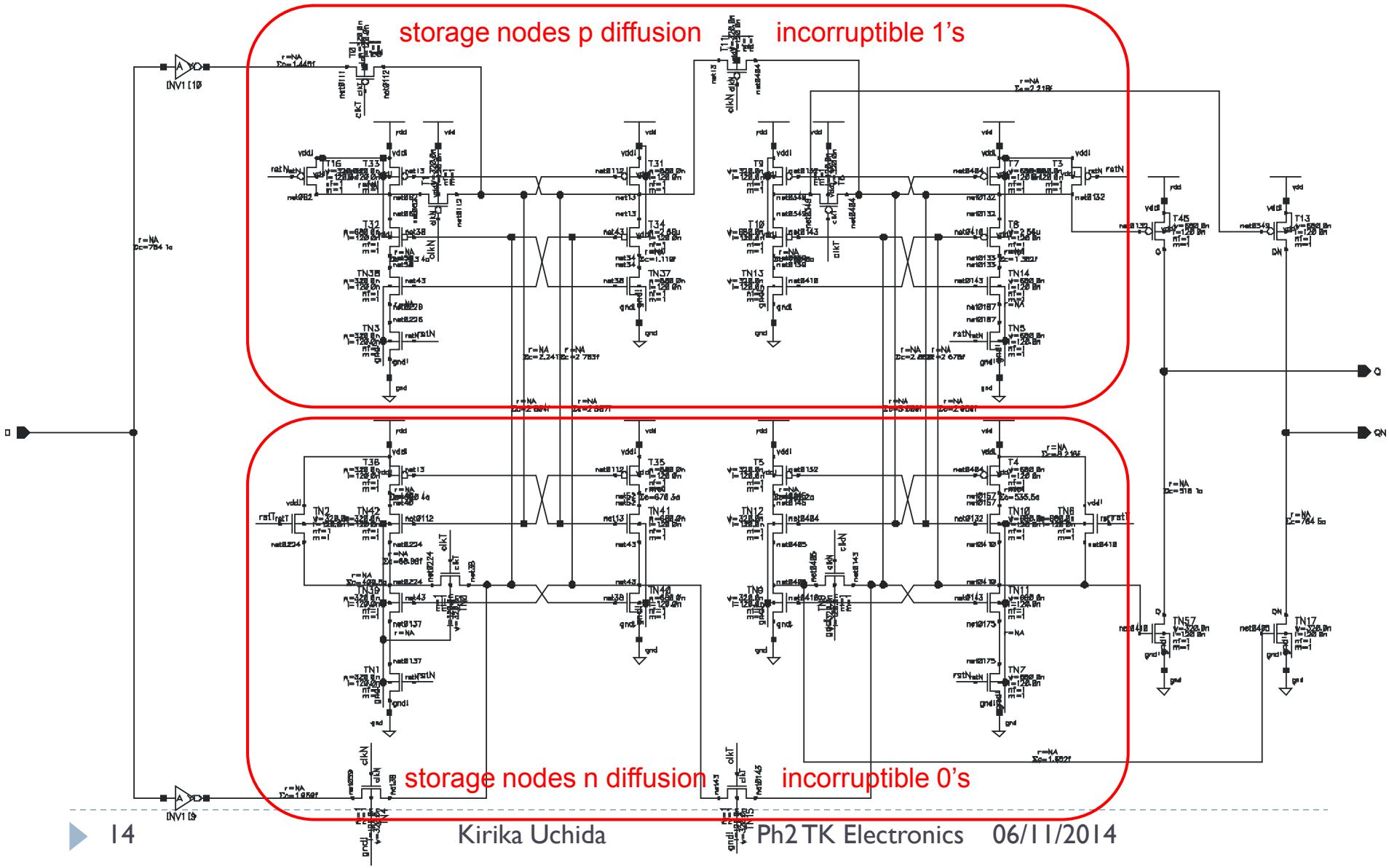
  with the assumption that SEU happens on multiple cells at the same time.

- ***Pipeline logic and pipeline cells are performing very well, only a low "fast reset" rate will be required to recover upset chips***
- ***I2C registers need to be mitigated more to be stable for a single run period.***
  - ***we are planning to do this for CBC3***
- ***Many more details in backup - note in preparation***

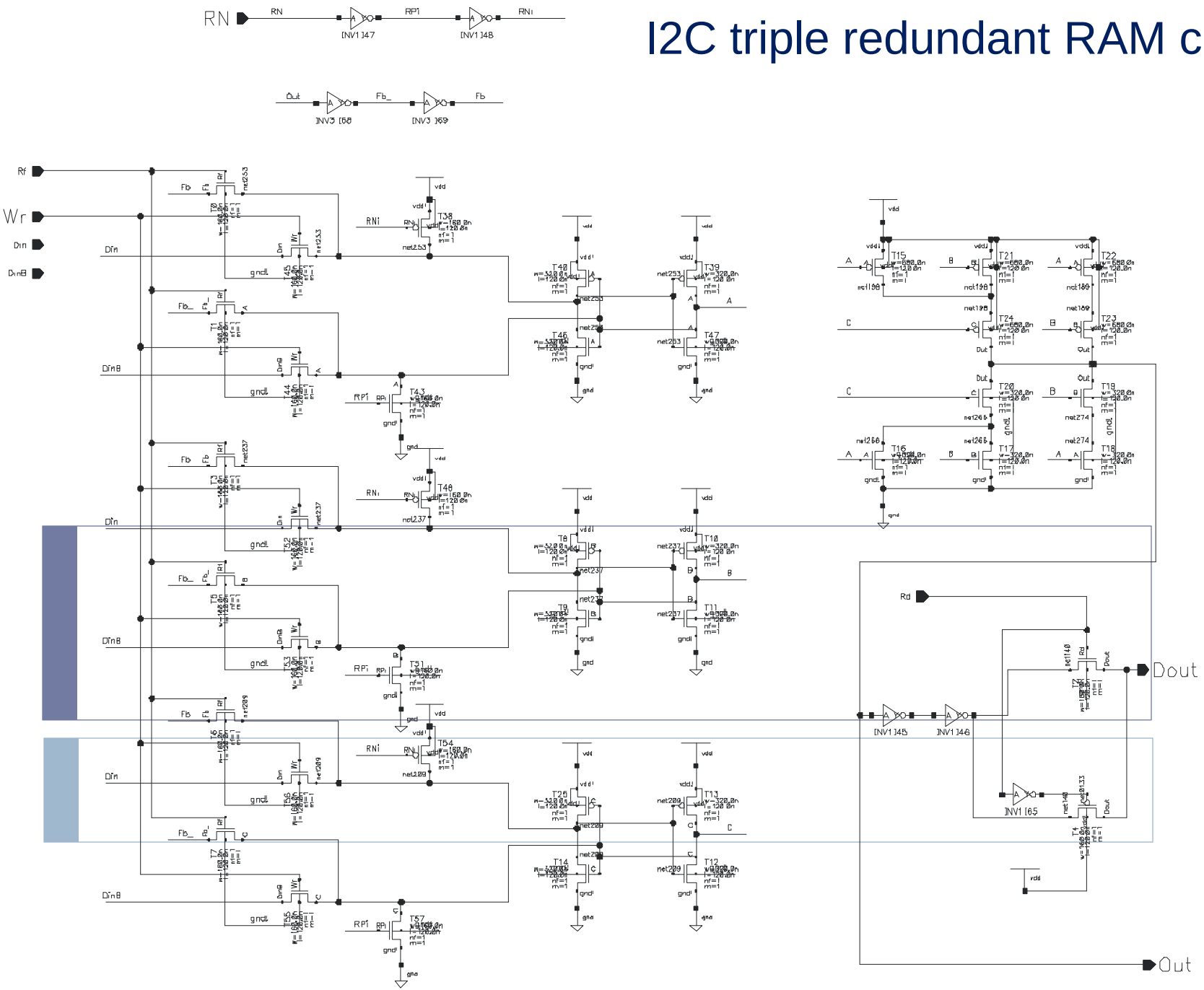
SEU tolerant D-type



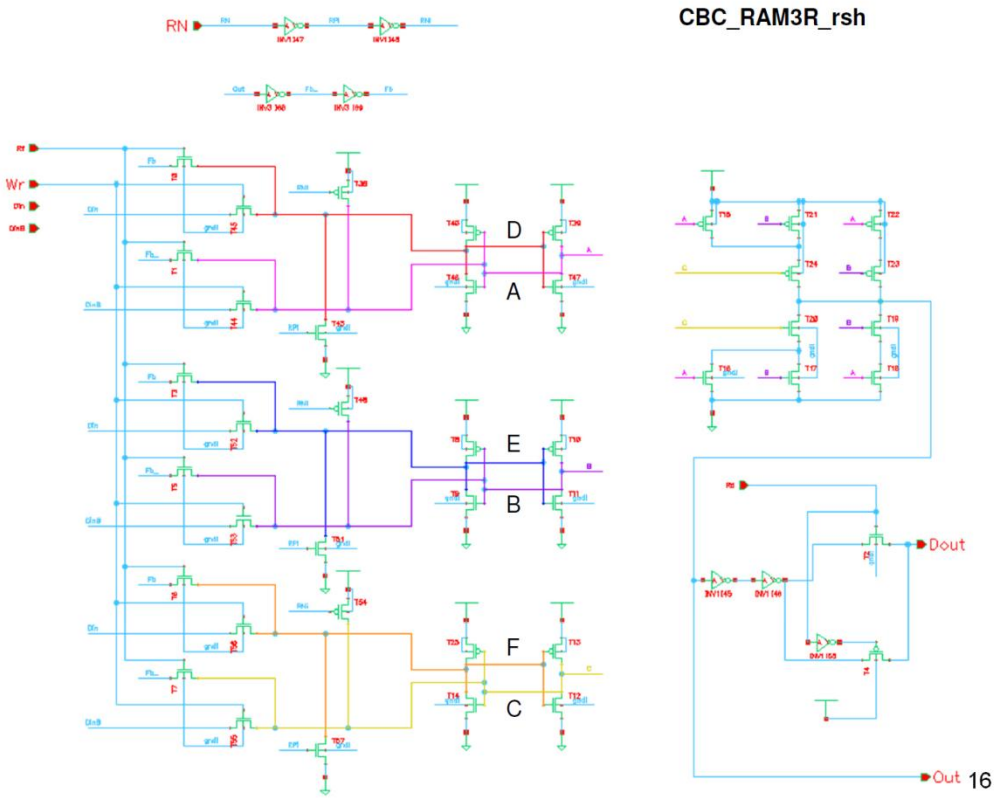
data in uncorrupted section provides feedback to recover any corruption in other block



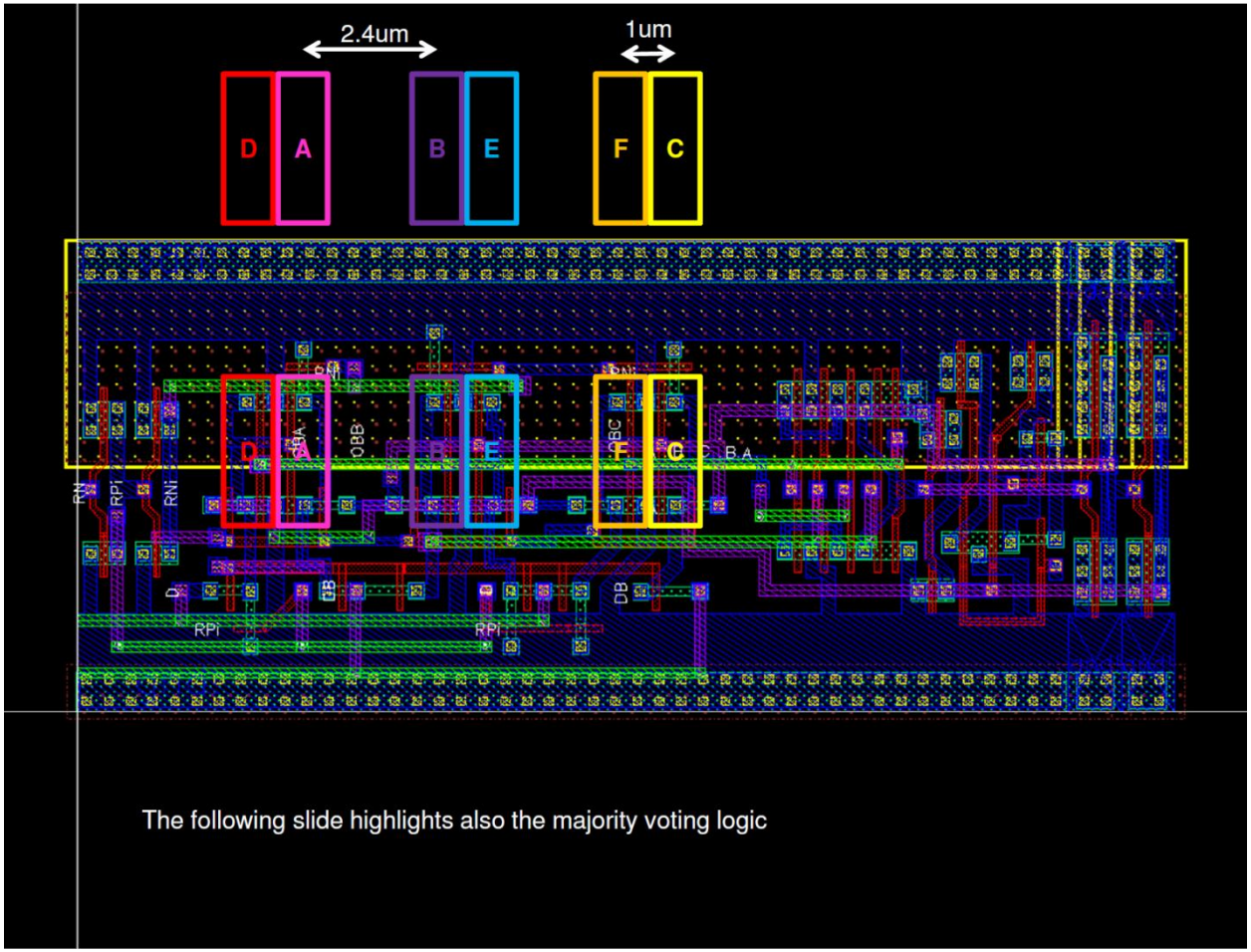
I2C triple redundant RAM cell



CBC I2C register bit triplicated logic



CBC I2C register bit triplicated logic layout



The formula to calculate SEU cross section per cell (The case of SEU on a single cell)

At least 2 out of 3 cells have to have SEU to flip the bit.

- Set I2C registers
- Read the I2C registers after T_0 sec

The probability of two cell flips out of three cells in time T_0 is

$$P(T_0) = {}_3C_2 \int_0^{T_0} r dt_1 \int_0^{T_0} r dt_2 = 3r^2 \int_0^{T_0} dt_1 \int_0^{T_0} dt_2 = 3r^2 T_0^2$$

where r is the rate of a flip on a cell and $rT_0 << 1$ is assumed.

The probability of a flip on a cell at time t_1 for dt_1 and a flip on another cell at time t_2 for dt_2 are integrated over t_1 and t_2 from 0 to T_0, and multiplied by the combination of two cells out of three.

Symbol	Description
σ	SEU cross section per cell [cm^2/cell]
r	SEU rate per cell [$cell^{-1}sec^{-1}$]
Φ	Proton beam flux [$cm^{-2}sec^{-1}$]
$P(T_0)$	probability to flip two cells out of 3 in time window T_0 sec [bit^{-1}]
N^{bit}	# of I2C register bits in a chip
N^{read}	# of register reading in the run
N^{SEU}	# of I2C register bits flipped in the run

$N^{SEU} = N^{bit} \times P(T_0) \times N^{read}$ where $P(T_0) = 3r^2T_0^2$ → $r = N^{SEU} / (3r^2T_0^2 \times N^{bit} \times N^{read})$, $\sigma = r/\Phi$

Correlation between cells is not taken into account and the cross section need to be reasonably small.

The formula to calculate SEU cross section per bit (The case of SEU on multiple cells)

- Considering that a flip on I2C register bits comes from single SEU on multiple cells, the flip rate per bit(r) & cross section(σ) are simply obtained from

$$N^{SEU} = N^{bit} \times r \times N^{read} \times T^{0}$$

$$\rightarrow r = N^{SEU} / (N^{bit} \times N^{read} \times T^{0}), \sigma = r/\Phi$$

I2C register test result (break down in runs)

	Beam	# of bit flips			T sec	N read	I2C refresh Hz
		Total	0->1	1->0			
Day1Run1	ON	0	0	0	10	20	Disabled
Day1Run4	ON	16	5	11	600	7	Disabled
Day1Run6	ON	6	1	5	600	7	1(*)
Day1Run8	ON	10	6	4	600	6	10(*)
Day1Run9A	ON	26	5	21	600	4	10
Day1Run9B	OFF	0	0	0	600	3	10
Day2Run12	ON	20	4	16	600	6	Disabled
Total		78	21	57			

307 registers x 8 bits = 2456 bits (0 is set on 1208 bits, 1 is set on 1248 bits)

Question about refresh function

- (*) : I2C refresh is controlled from software, and the pulse length sent to CBC2 is ~1ms (**long pulse**).
- I2C refresh is enabled and frequency is raised from Day1Run6 to Day1Run8 by factor 10, but the result does not show a better performance.
- The long pulse length was suspected to be causing the problem, so firmware commissioning loop is enabled which creates 25ns I2C refresh pulse. But result shows no improvement.

Measured SEU cross section on I2C registers (The case of SEU on a single cell)

r & σ calculation without taking into account the refresh.

SEU 0->1 (N^{bit} = 1208)

CBC2 is tilted by 45 degree in day2

Run	T_0	N^{read}	N^{SEU}	I2C refresh Hz	$\Phi\ 10^8\ cm^{-2}$	r	σ
Day1Run4	600	7	5	Disabled	2.44±0.09	$[2.3\pm0.5]\times10^{-5}$	$[9.4\pm2.1]\times10^{-14}$
Day1Run6	600	7	1	1(*)	2.42±0.03	$[1.0\pm0.5]\times10^{-5}$	$[4.2\pm2.1]\times10^{-14}$
Day1Run8	600	6	6	10(*)	2.39±0.14	$[2.8\pm0.6]\times10^{-5}$	$[1.1\pm0.2]\times10^{-13}$
Day1Run9A	600	4	5	10	2.64±0.01	$[3.1\pm0.7]\times10^{-5}$	$[1.2\pm0.3]\times10^{-13}$
Day2Run12	600	6	4	Disabled	2.57±0.61	$[2.3\pm0.6]\times10^{-5}$	$[9.1\pm2.3]\times10^{-14}$

Average of Day1Run4 & Day2Run12 : $\sigma=[9.2\pm1.6]\times10^{-14}$

SEU 1->0 (N^{bit} = 1248)

Run	T_0	N^{read}	N^{SEU}	I2C refresh Hz	$\Phi\ 10^8\ cm^{-2}$	r	σ
Day1Run4	600	7	11	Disabled	2.44±0.09	$[3.4\pm0.5]\times10^{-5}$	$[1.4\pm0.2]\times10^{-13}$
Day1Run6	600	7	5	1(*)	2.42±0.03	$[2.3\pm0.5]\times10^{-5}$	$[9.2\pm2.1]\times10^{-14}$
Day1Run8	600	6	4	10(*)	2.39±0.14	$[2.2\pm0.6]\times10^{-5}$	$[8.9\pm2.2]\times10^{-14}$
Day1Run9A	600	4	21	10	2.64±0.01	$[6.2\pm0.7]\times10^{-5}$	$[2.5\pm0.3]\times10^{-13}$
Day2Run12	600	6	16	Disabled	2.57±0.61	$[4.4\pm0.6]\times10^{-5}$	$[1.8\pm0.2]\times10^{-13}$

Average of Day1Run4 & Day2Run12 : $\sigma=[1.6\pm0.1]\times10^{-13}$

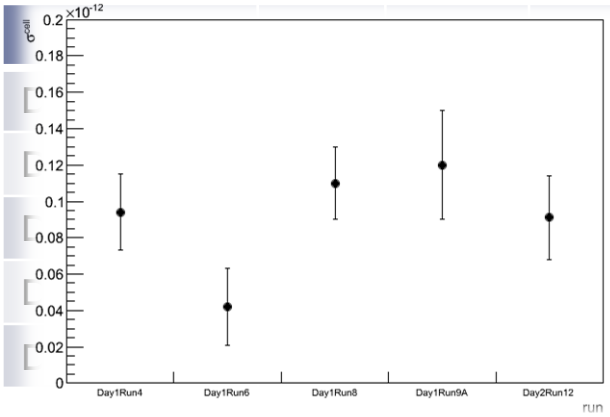
The refresh is not working properly and not reducing the SEU effect well. Higher frequency, shorter refresh pulse does not help.

Measured SEU cross section on I2C registers (The case of SEU on a single cell)

r & σ calculation without taking into account the refresh.

CBC2 is tilted by 45 degree in day2

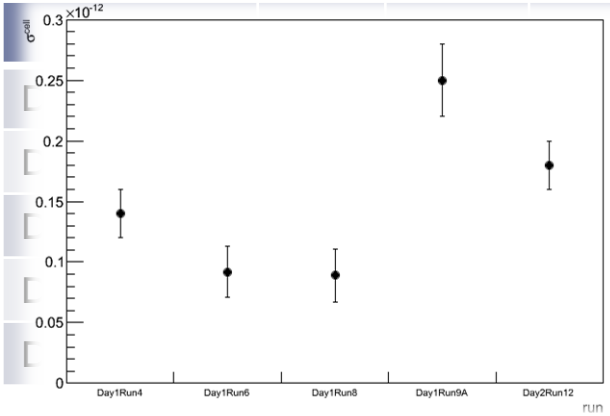
SEU 0->1 (N^{bit} = 1208)



I2C refresh Hz	Φ 10^8 cm^{-2}	r	σ
Disabled	2.44±0.09	[2.3±0.5]x10^{-5}	[9.4±2.1]x10^{-14}
1(*)	2.42±0.03	[1.0±0.5]x10^{-5}	[4.2±2.1]x10^{-14}
10(*)	2.39±0.14	[2.8±0.6]x10^{-5}	[1.1±0.2]x10^{-13}
10	2.64±0.01	[3.1±0.7]x10^{-5}	[1.2±0.3]x10^{-13}
Disabled	2.57±0.61	[2.3±0.6]x10^{-5}	[9.1±2.3]x10^{-14}

Average of Day1Run4 & Day2Run12 : σ =[9.2±1.6]x10^{-14}

SEU 1->0 (N^{bit} = 1248)



I2C refresh Hz	Φ 10^8 cm^{-2}	r	σ
Disabled	2.44±0.09	[3.4±0.5]x10^{-5}	[1.4±0.2]x10^{-13}
1(*)	2.42±0.03	[2.3±0.5]x10^{-5}	[9.2±2.1]x10^{-14}
10(*)	2.39±0.14	[2.2±0.6]x10^{-5}	[8.9±2.2]x10^{-14}
10	2.64±0.01	[6.2±0.7]x10^{-5}	[2.5±0.3]x10^{-13}
Disabled	2.57±0.61	[4.4±0.6]x10^{-5}	[1.8±0.2]x10^{-13}

Average of Day1Run4 & Day2Run12 : σ =[1.6±0.1]x10^{-13}

The refresh is not working properly and not reducing the SEU effect well. Higher frequency, shorter refresh pulse does not help.

Measured SEU cross section on I2C registers (The case of SEU on multiple cells)

r & σ calculation without taking into account the refresh.

CBC2 is tilted by 45 degree in day2

SEU 0->1 (N^{bit} = 1208)

Run	T_0	N^{read}	N^{SEU}	I2C refresh Hz	$\Phi\ 10^8\ cm^{-2}$	r	σ
Day1Run4	600	7	5	Disabled	2.44±0.09	$[9.9\pm4.4]\times10^{-7}$	$[4.0\pm1.8]\times10^{-15}$
Day1Run6	600	7	1	1(*)	2.42±0.03	$[2.0\pm2.0]\times10^{-7}$	$[7.9\pm7.9]\times10^{-16}$
Day1Run8	600	6	6	10(*)	2.39±0.14	$[1.4\pm0.6]\times10^{-6}$	$[5.6\pm2.3]\times10^{-15}$
Day1Run9A	600	4	5	10	2.64±0.01	$[1.7\pm0.8]\times10^{-6}$	$[6.9\pm3.1]\times10^{-15}$
Day2Run12	600	6	4	Disabled	2.57±0.61	$[9.3\pm4.6]\times10^{-7}$	$[3.7\pm1.9]\times10^{-15}$

Average of Day1Run4 & Day2Run12 : $\sigma=[3.9\pm1.3]\times10^{-15}$

SEU 1->0 (N^{bit} = 1248)

Run	T_0	N^{read}	N^{SEU}	I2C refresh Hz	$\Phi\ 10^8\ cm^{-2}$	r	σ
Day1Run4	600	7	11	Disabled	2.44±0.09	$[2.1\pm0.6]\times10^{-6}$	$[8.4\pm2.5]\times10^{-15}$
Day1Run6	600	7	5	1(*)	2.42±0.03	$[9.5\pm4.2]\times10^{-7}$	$[3.8\pm1.7]\times10^{-15}$
Day1Run8	600	6	4	10(*)	2.39±0.14	$[8.9\pm4.5]\times10^{-7}$	$[3.6\pm1.8]\times10^{-15}$
Day1Run9A	600	4	21	10	2.64±0.01	$[7.0\pm1.5]\times10^{-6}$	$[2.8\pm0.6]\times10^{-14}$
Day2Run12	600	6	16	Disabled	2.57±0.61	$[3.6\pm0.9]\times10^{-6}$	$[1.4\pm0.4]\times10^{-14}$

Average of Day1Run4 & Day2Run12 : $\sigma=[1.1\pm0.3]\times10^{-14}$

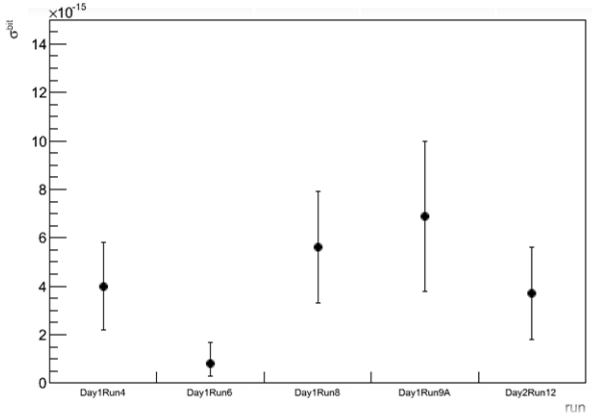
If the multiple cells flip, refresh does not restore the initial value, so in this case, it is understandable that there is no improvement with the refresh.

Measured SEU cross section on I2C registers (The case of SEU on multiple cells)

r & σ calculation without taking into account the refresh.

CBC2 is tilted by 45 degree in day2

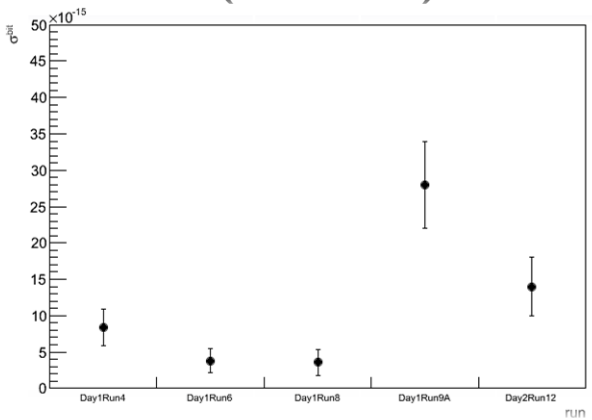
SEU 0->1 (N^{bit} = 1208)



I2C refresh Hz	$\Phi\ 10^8\ cm^{-2}$	r	σ
Disabled	2.44±0.09	[9.9±4.4]x10^{-7}	[4.0±1.8]x10^{-15}
1(*)	2.42±0.03	[2.0±2.0]x10^{-7}	[7.9±7.9]x10^{-16}
10(*)	2.39±0.14	[1.4±0.6]x10^{-6}	[5.6±2.3]x10^{-15}
10	2.64±0.01	[1.7±0.8]x10^{-6}	[6.9±3.1]x10^{-15}
Disabled	2.57±0.61	[9.3±4.6]x10^{-7}	[3.7±1.9]x10^{-15}

Average of Day1Run4 & Day2Run12 : σ=[3.9±1.3]x10^{-15}

SEU 1->0 (N^{bit} = 1248)

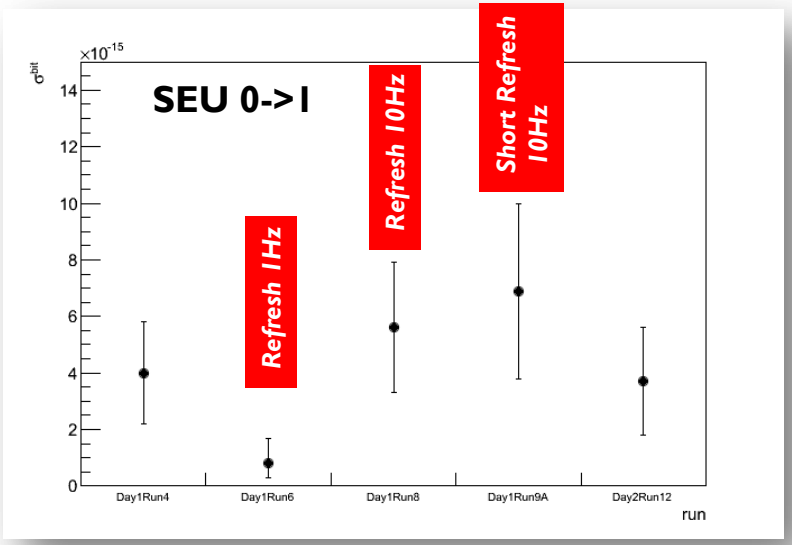


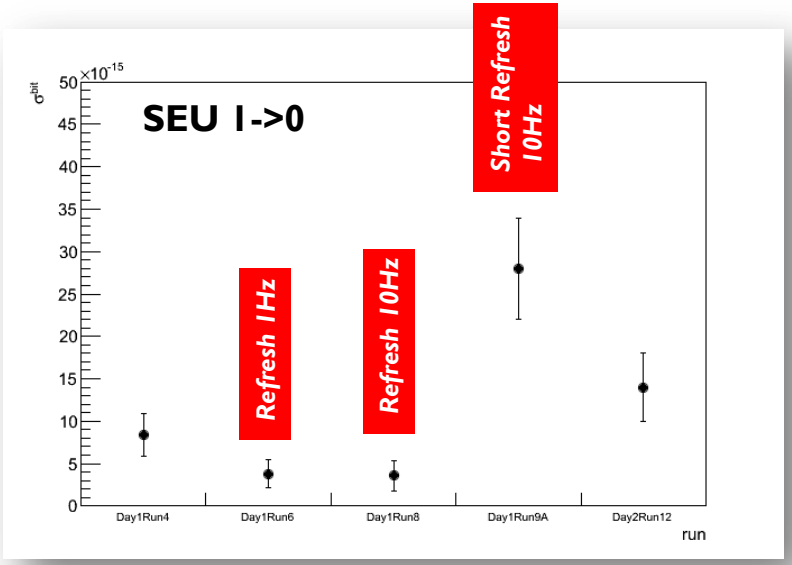
I2C refresh Hz	$\Phi\ 10^8\ cm^{-2}$	r	σ
Disabled	2.44±0.09	[2.1±0.6]x10^{-6}	[8.4±2.5]x10^{-15}
1(*)	2.42±0.03	[9.5±4.2]x10^{-7}	[3.8±1.7]x10^{-15}
10(*)	2.39±0.14	[8.9±4.5]x10^{-7}	[3.6±1.8]x10^{-15}
10	2.64±0.01	[7.0±1.5]x10^{-6}	[2.8±0.6]x10^{-14}
Disabled	2.57±0.61	[3.6±0.9]x10^{-6}	[1.4±0.4]x10^{-14}

Average of Day1Run4 & Day2Run12 : σ=[1.1±0.3]x10^{-14}

If the multiple cells flip, refresh does not restore the initial value, so in this case, it is understandable that there is no improvement with the refresh.

Measured SEU cross section on I2C registers (The case of SEU on multiple cells)





- If the multiple cells flip, refresh does not restore the initial value, so in this case, it is understandable that there is not very good improvement with the refresh.
- Short refresh in Day1Run9A does not look working well, but statistics is small.

LIF proton flux & CBC2 current vs. Time

- LIF proton flux in black, CBC2 current in red, filled area are the run periods, error timings are in orange triangles.
- LIF proton flux ~ 2.55±0.14x10^{8} p $cm^{-2}s^{-1}$ with the energy 62.0 MeV where *LET* = 8.39 MeVcm^{2}/mg.
- Total fluence : 1.1x$10^{13}cm^{-2}$
- Total radiation : Total fluence x *LET* = 1.5 MRad. <- large?
- CBC2 current drop seems to be correlated with hard reset. (Not always?)