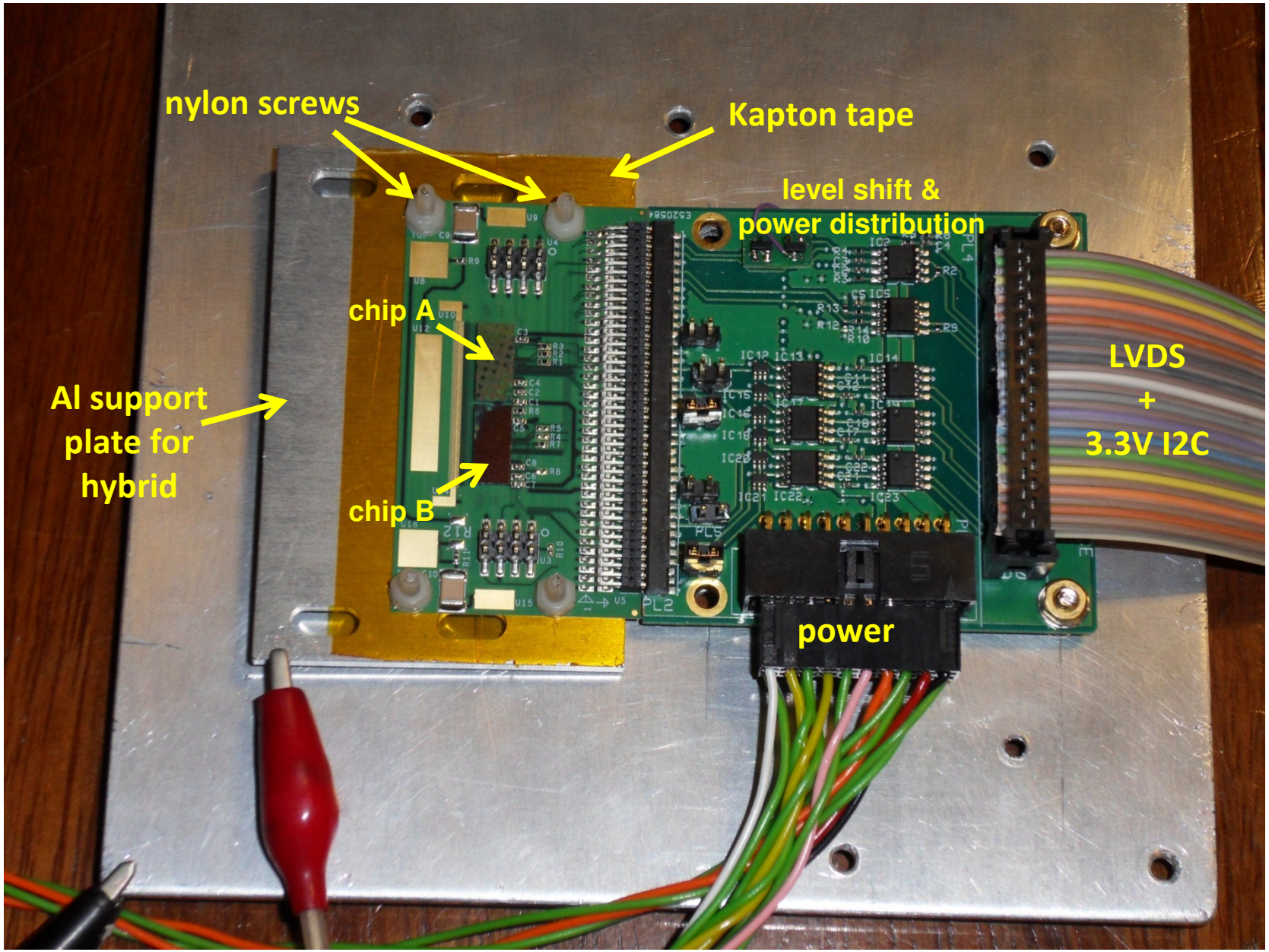
2xCBC2 hybrid functional test results

results from screening first 5 bump-bonded hybrids

objective to verify functionality - looking for anything that might indicate failure of bump-bonding process

hybrid test setup



measured power parameters

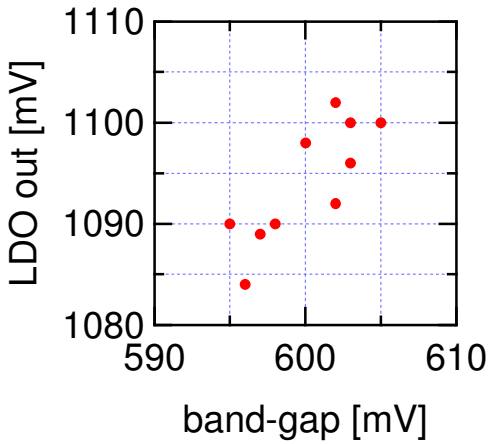
band-gap voltage accessible via on-chip analogue mux

LDO O/P voltage recorded for baseline set of bias parameters

powering measurements
- both chips powered from 1.2V VDDD rail
- analogue powered via LDO (VDDD in / VDDA out)
- current measured in VDDD rail

baseline current (digital + quiescent analogue) ~ 6mA / chip

LDO out vs. band-gap



total hybrid power supply current [mA]

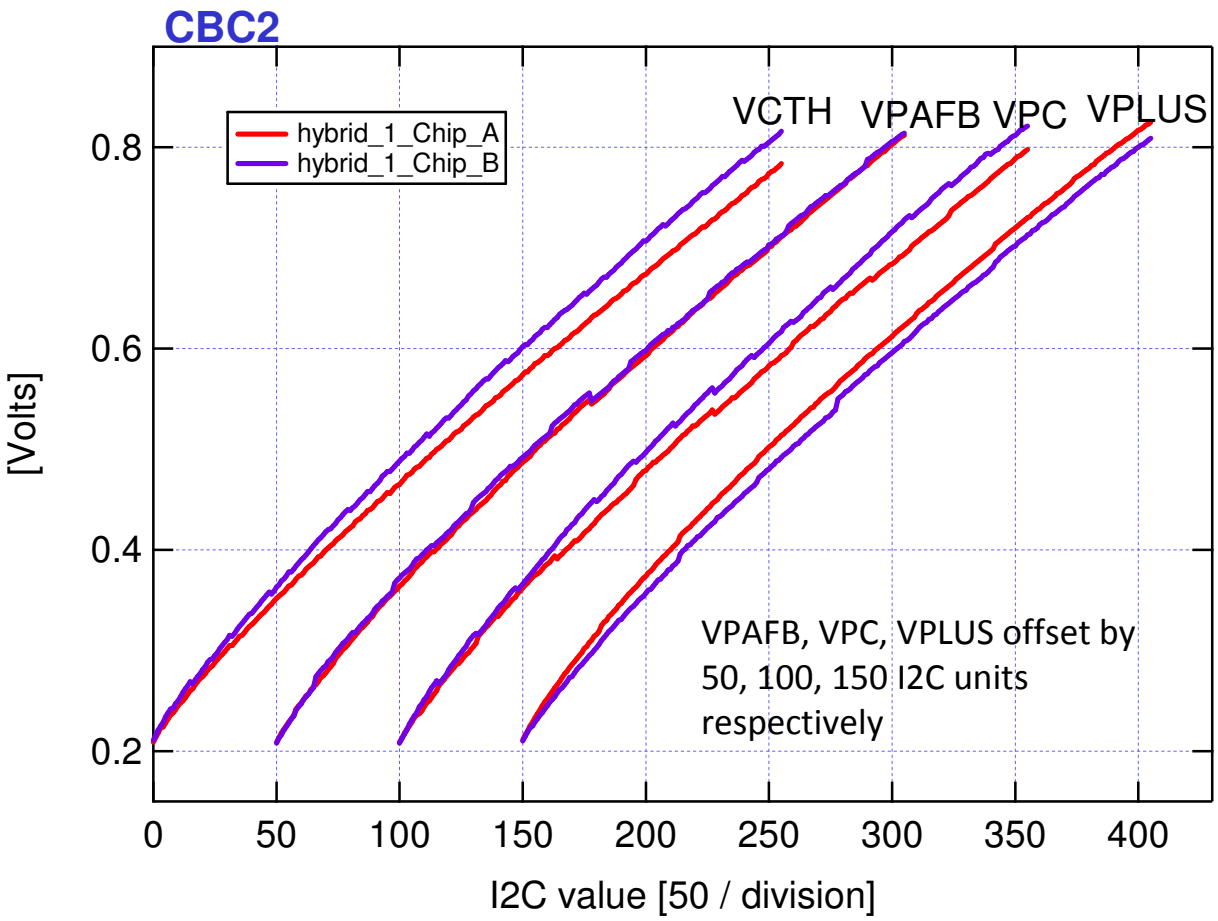
conditions	hybrid 1	hybrid 2	hybrid 3	hybrid 4	hybrid 5
all current biases zero, SLVS off, both chips	7.0	7.2	6.7	6.7	6.7
all current biases zero, SLVS on for one chip	9.5	9.9	9.3	9.2	9.5
all current biases zero, SLVS on, both chips	12.2	12.7	12.0	11.8	12.3
current biases to baseline values, chip A	39.6	40.1	39.9	41.9	41.1
current biases to baseline values, both chips	67.6	68.8	67.7	70.6	69.6

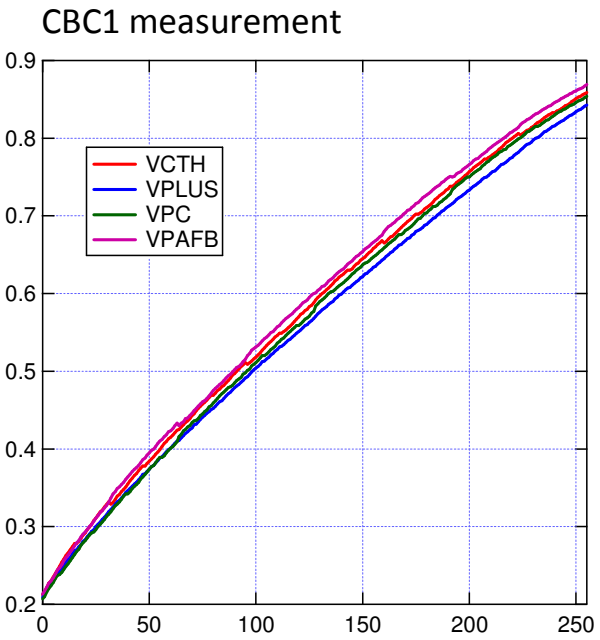
baseline
I2C bias values

IPRE1	35
IPRE2	20
IPSF	45
IPA	30
IPAOS	45
VPAFB	0
ICOMP	30
VPC	74
VPLUS	100

note: baseline I2C values chosen for no significant external capacitance
(IPRE1 needs to be chosen appropriately, depending on sensor capacitance)

voltage bias sweep measurements



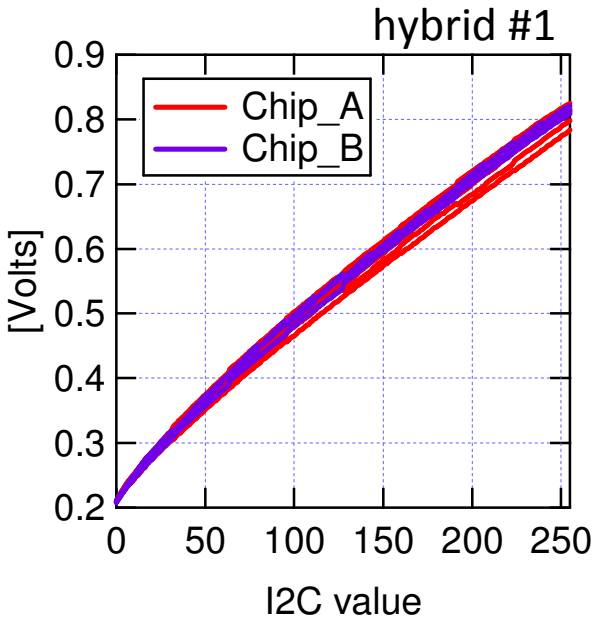


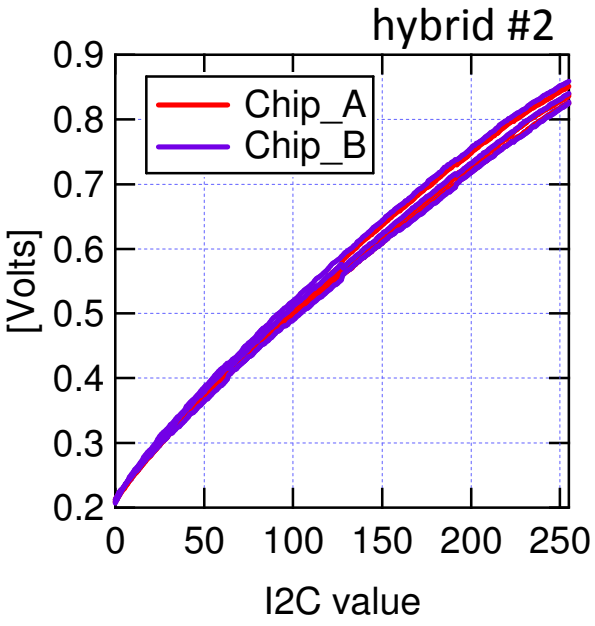
voltage biases externally accessible via on-chip analogue mux

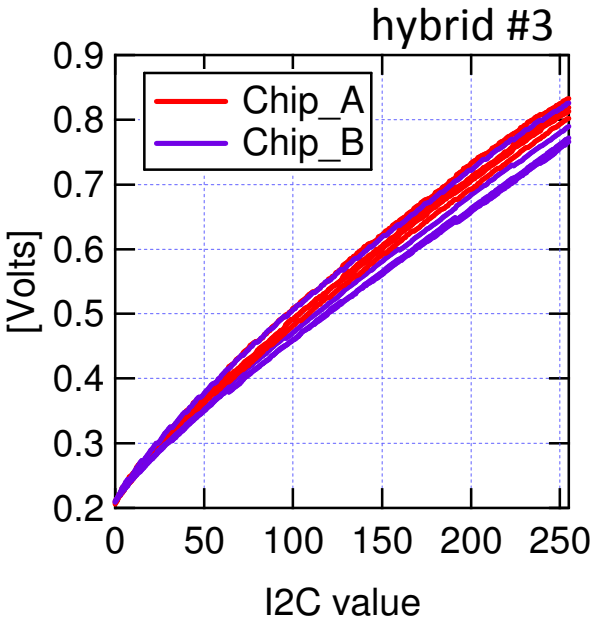
sweep the parameter of interest, all other I2C parameters set to baseline values

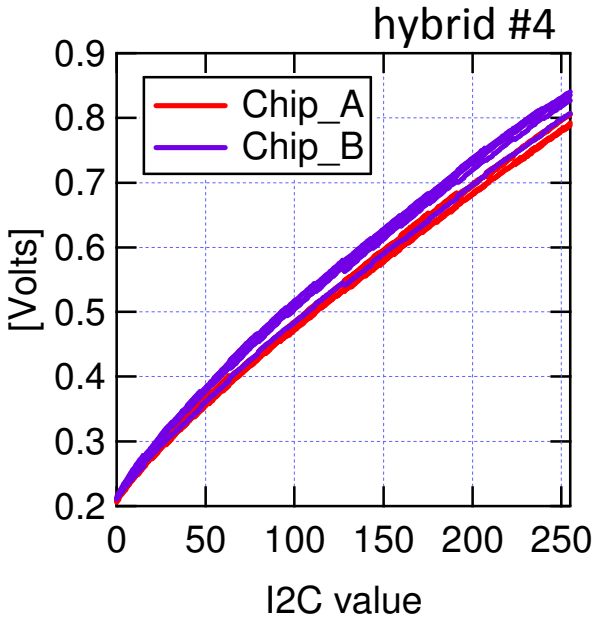
no surprises, behaviour as expected, and not significantly different to prototype measurements

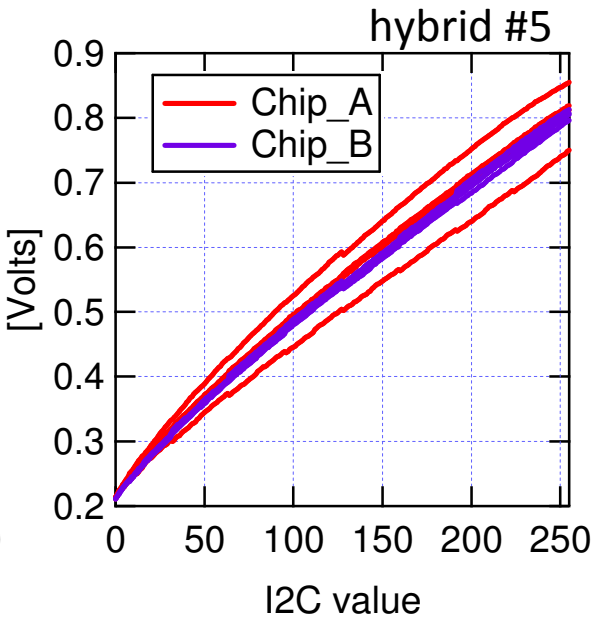
voltage bias sweep results - all hybrids



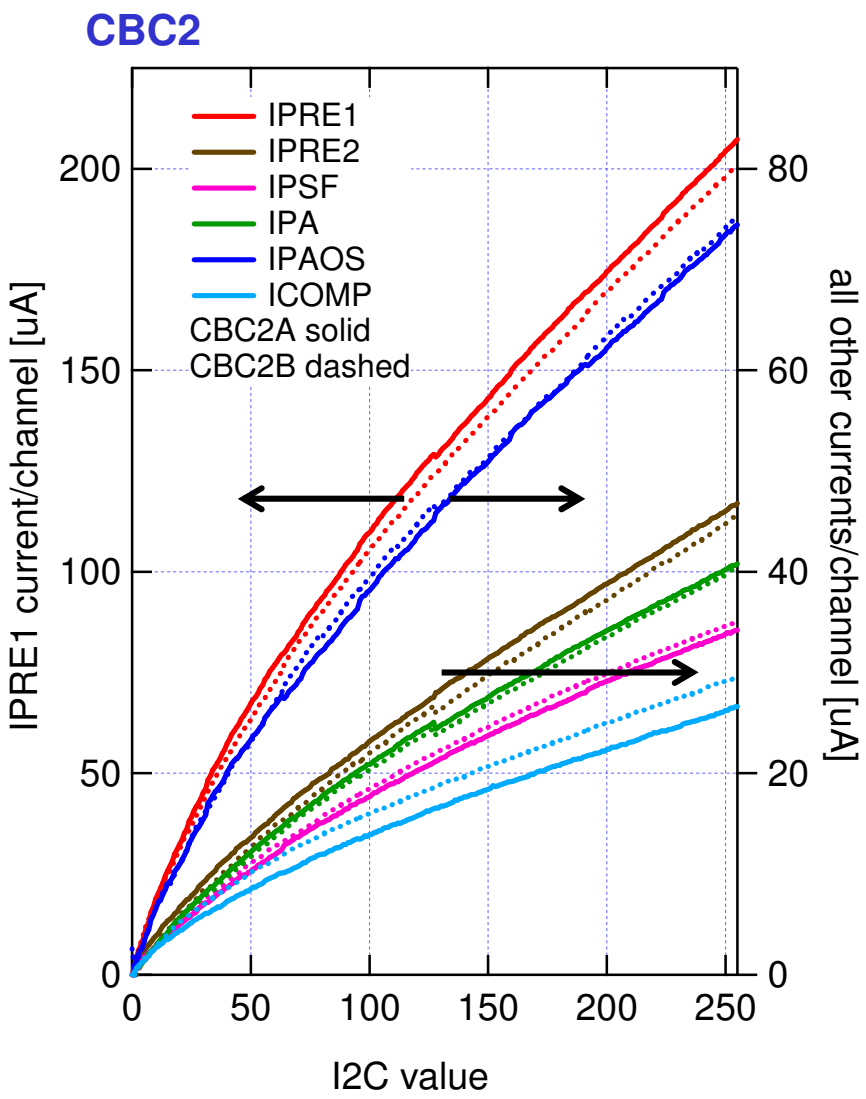




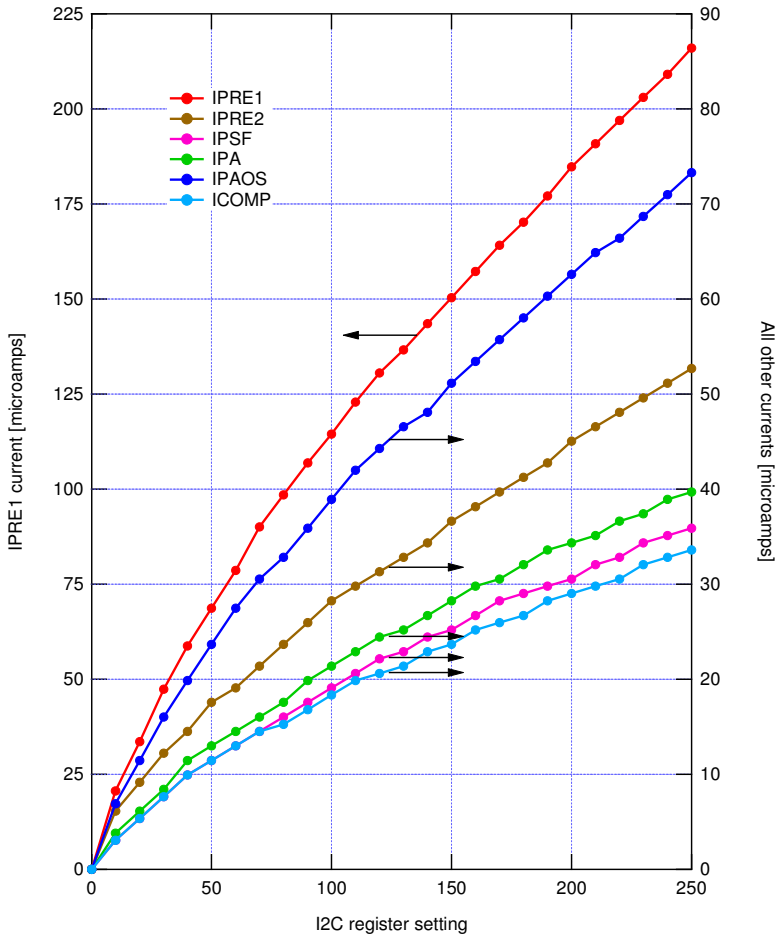




current bias sweep measurements



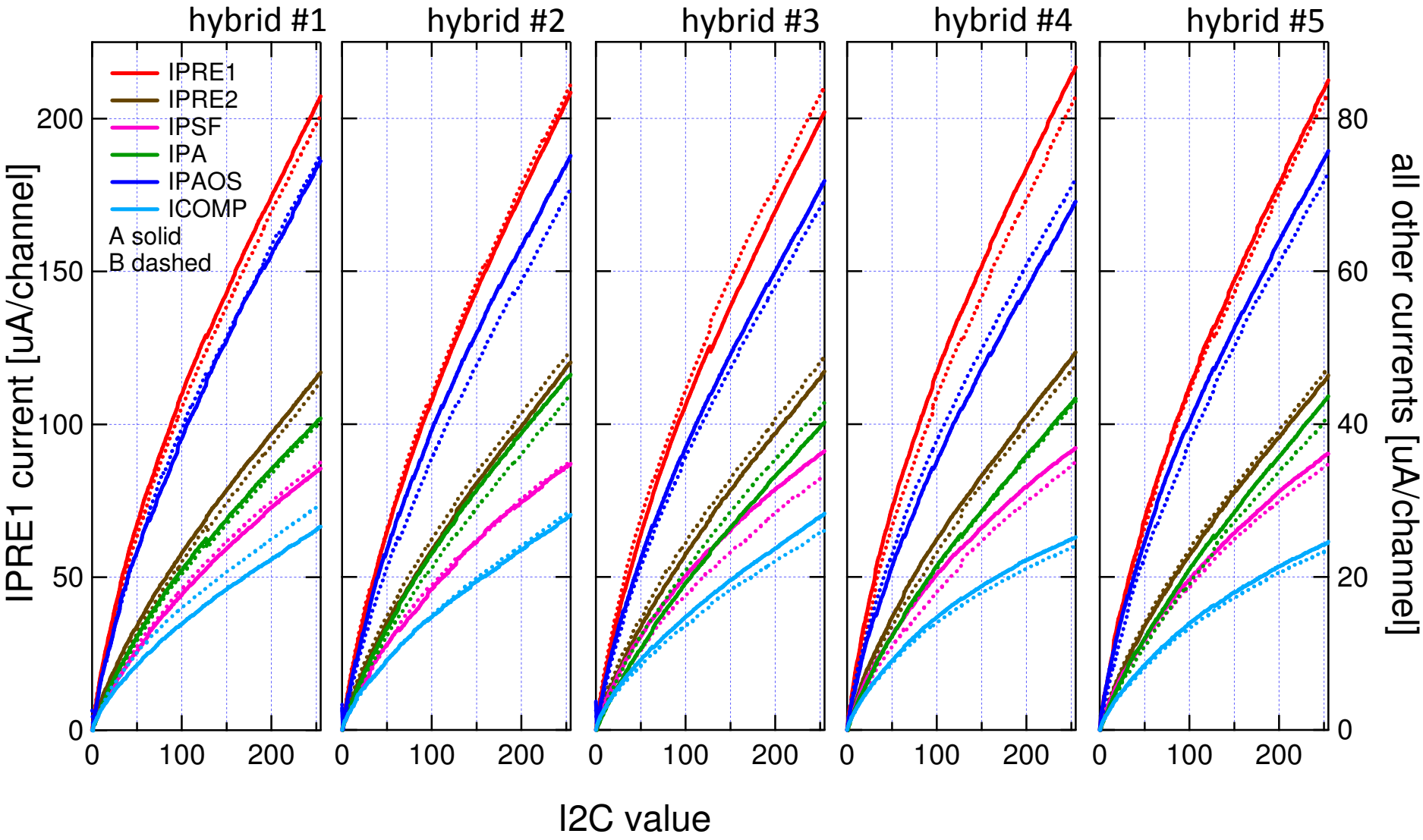
CBC1 measurement



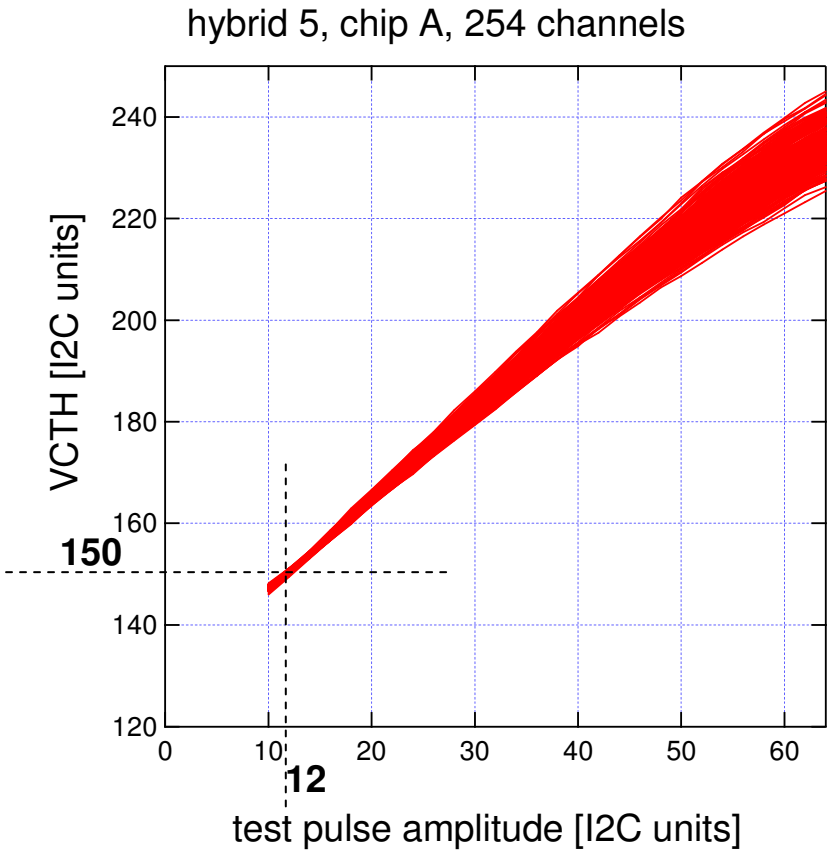
total current (all channels) measured in supply rail
subtract zero value and divide by 254

results as expected, and similar to prototype

current bias sweep measurements - all hybrids



gain measurements

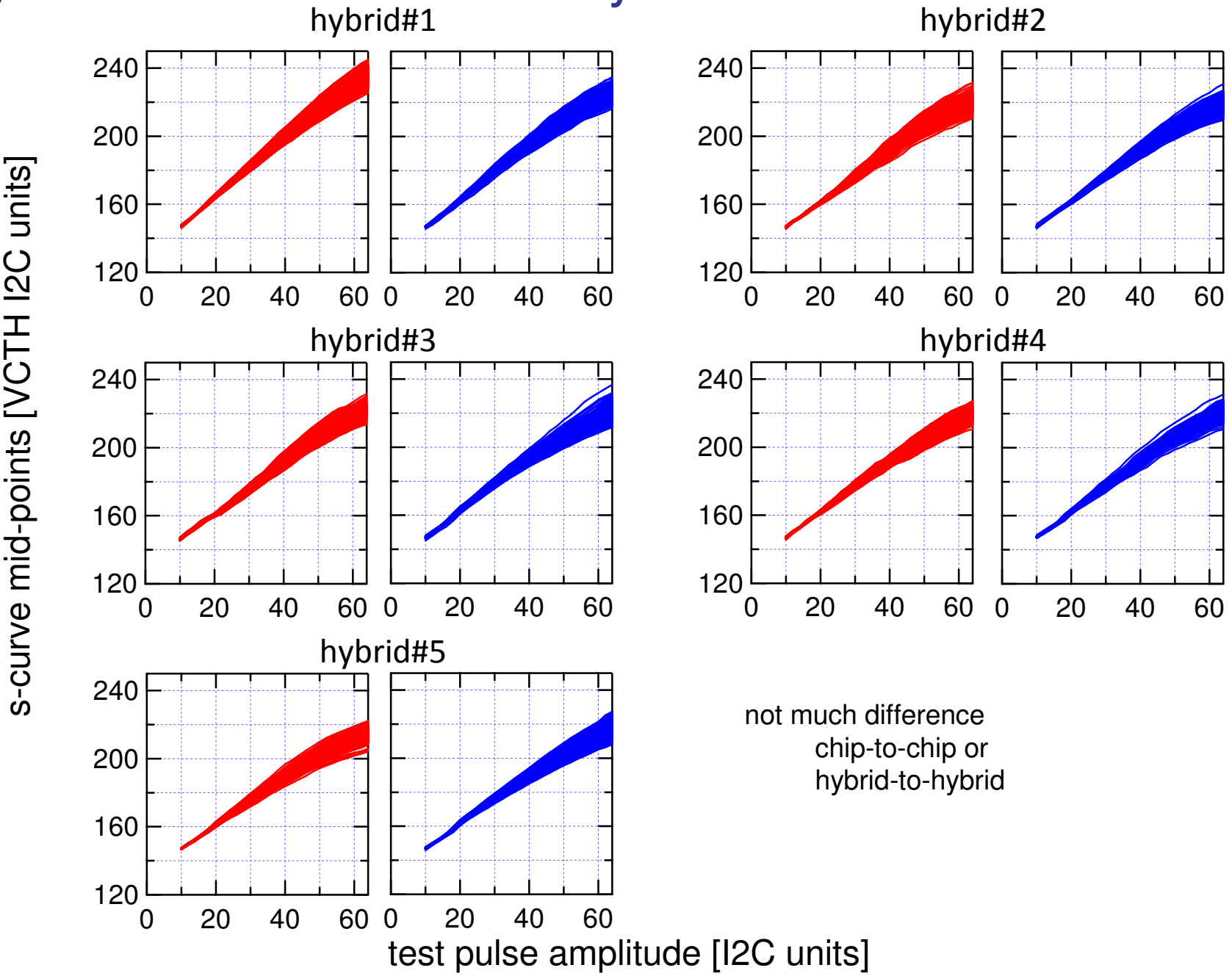


sweep test pulse amplitude and measure
s-curve mid-points by sweeping global comparator
threshold voltage VCTH

comparator offsets tuned to a VCTH vlaue of 150
at test pulse amplitude 12

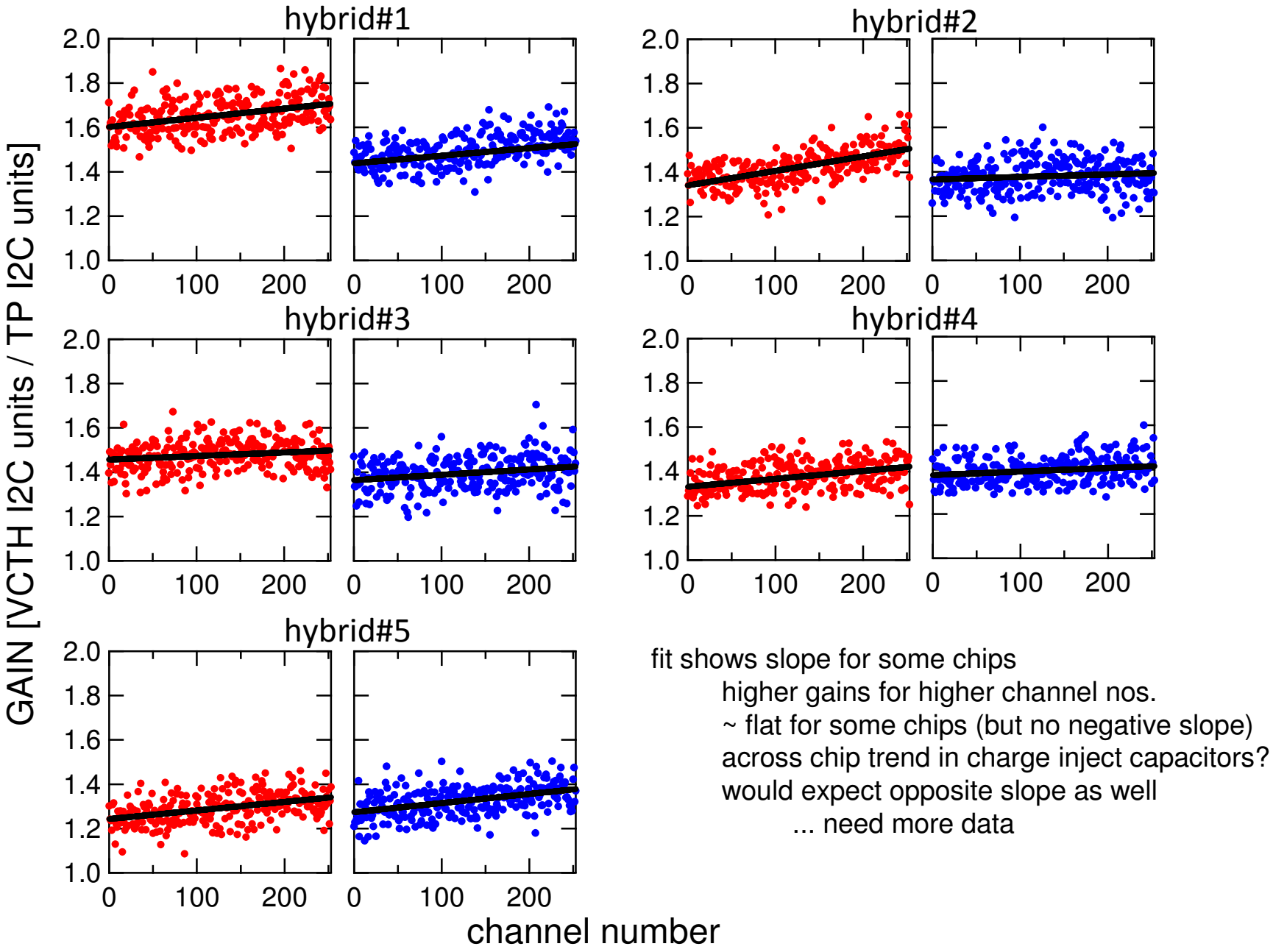
(12 corresponds to approximately 1 fC
assuming 20fF charge injection capacitance)

gain measurements - all hybrids



not much difference
chip-to-chip or
hybrid-to-hybrid

gain vs. channel number



fit shows slope for some chips

higher gains for higher channel nos.

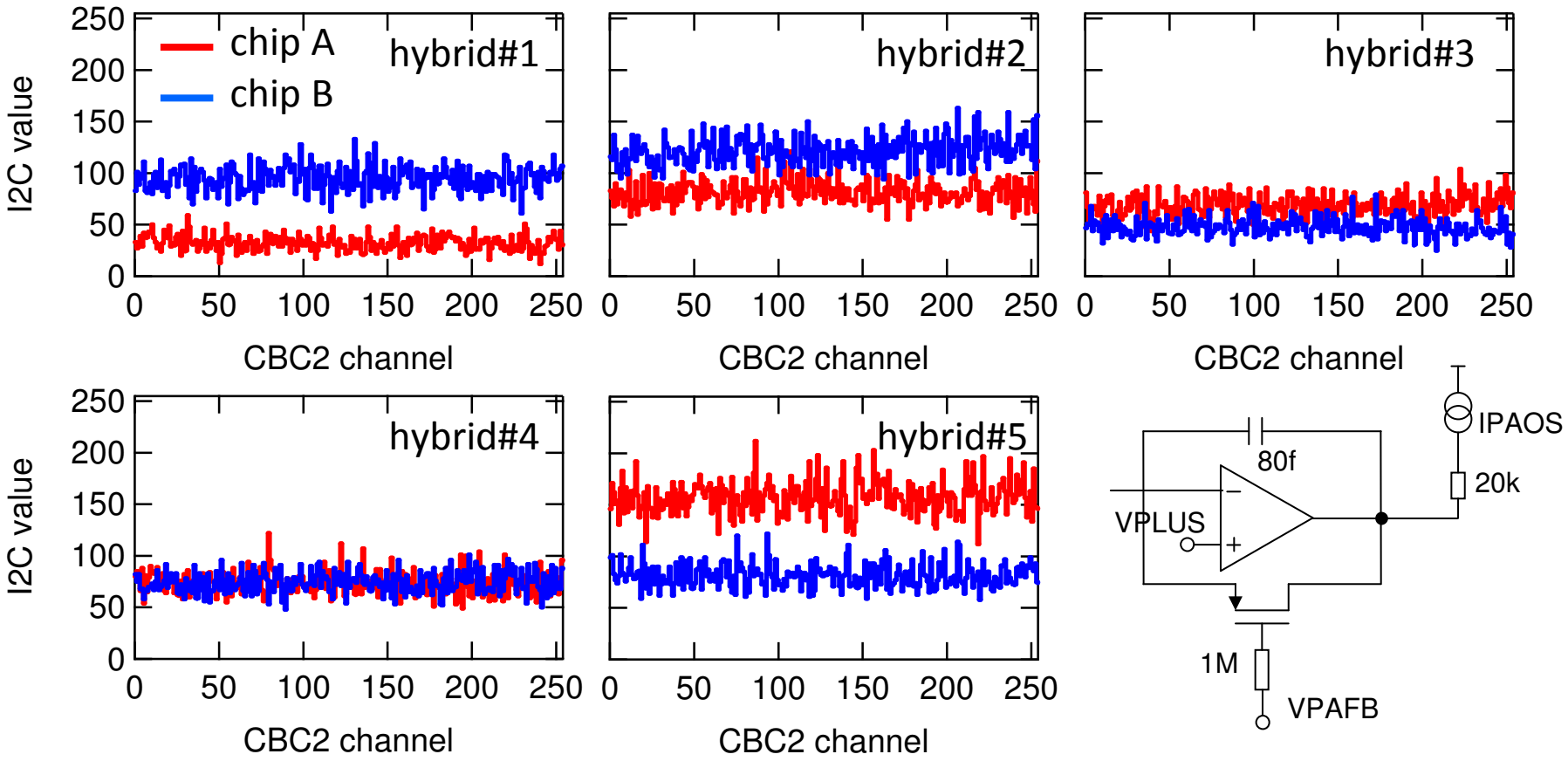
~ flat for some chips (but no negative slope)

across chip trend in charge inject capacitors?

would expect opposite slope as well

... need more data

individual comparator channel offset tuning - all hybrids

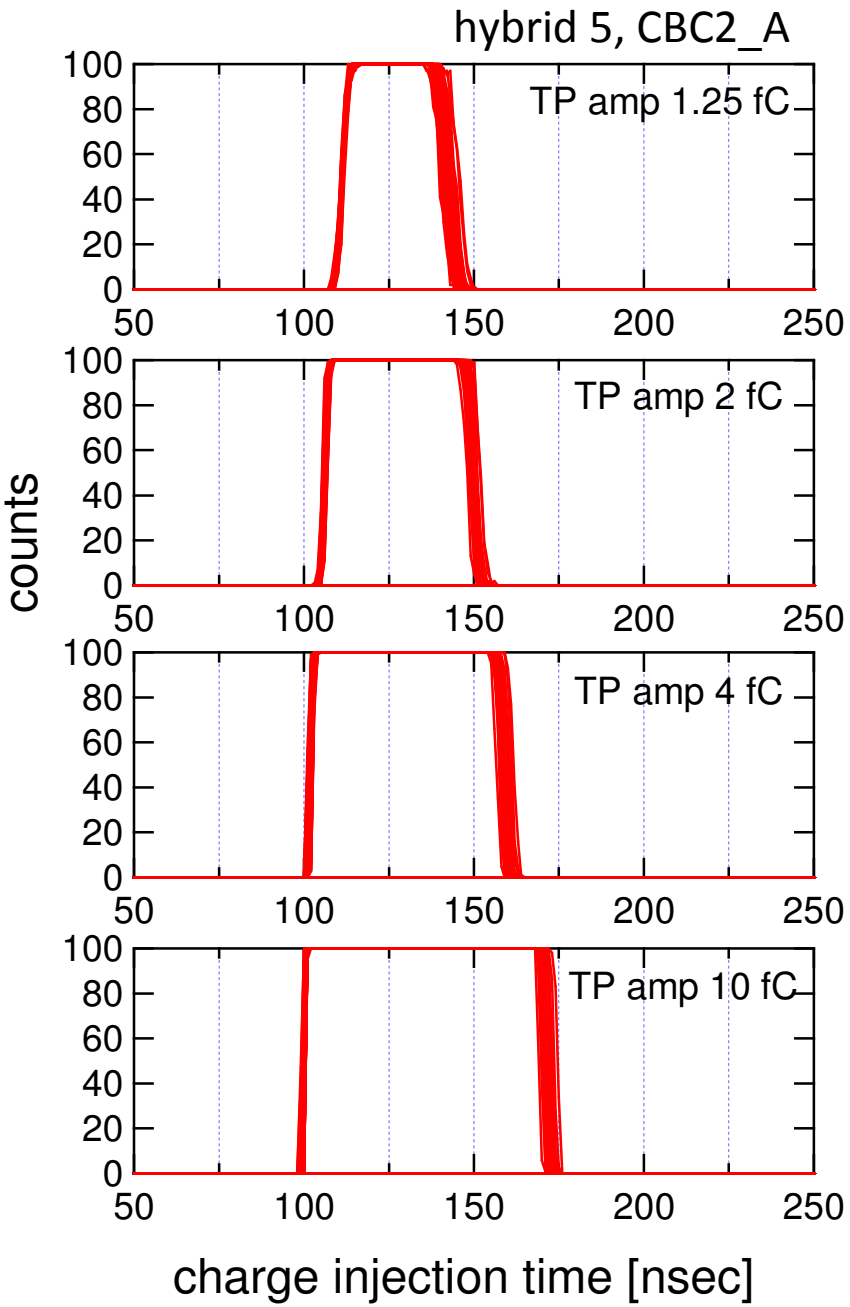


all channels tuned to position S-curve midpoints at **same** value of global comparator threshold VCTH

chip-to-chip variation in average level and channel-to-channel spread within tuning range

not necessary to adjust any other parameter

test pulse injection time sweep

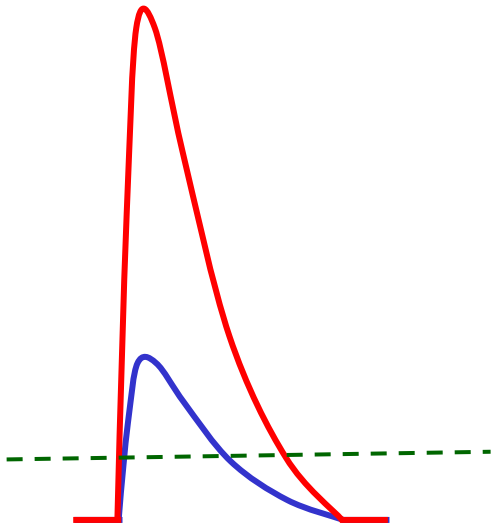


using on-chip test pulse

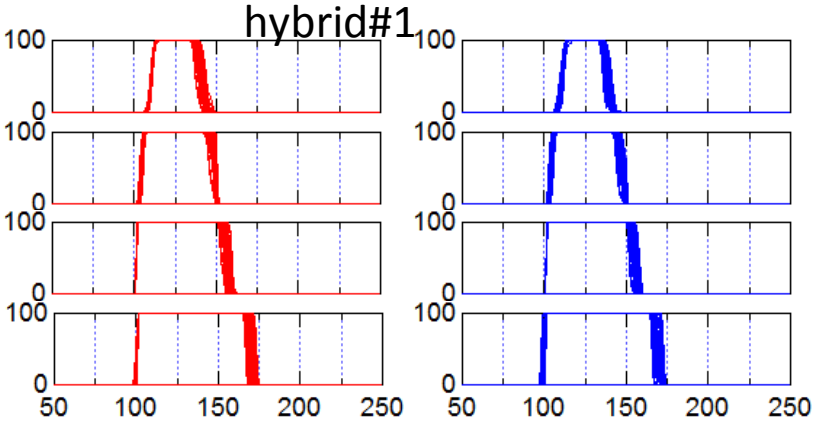
sweep time of charge injection for range of test pulse amplitudes

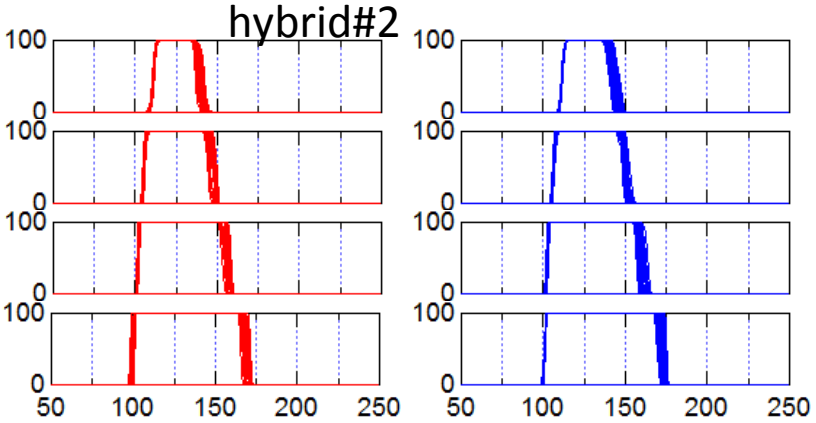
comparator threshold at 1 fC

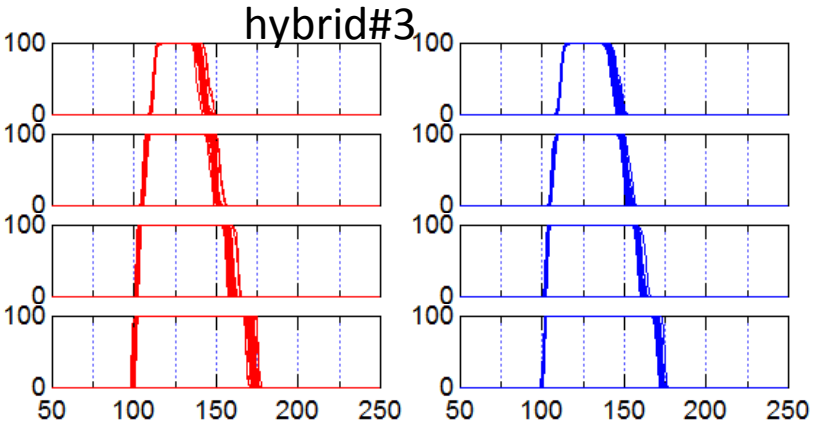
test pulse amplitudes 1.25, 2, 4, 10 fC

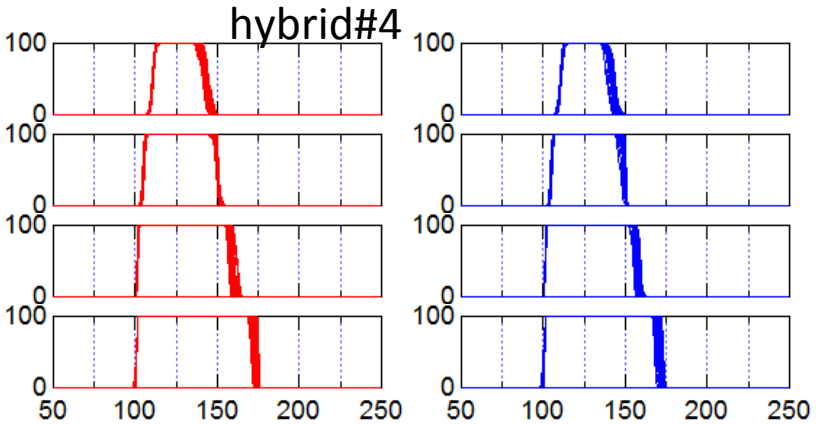


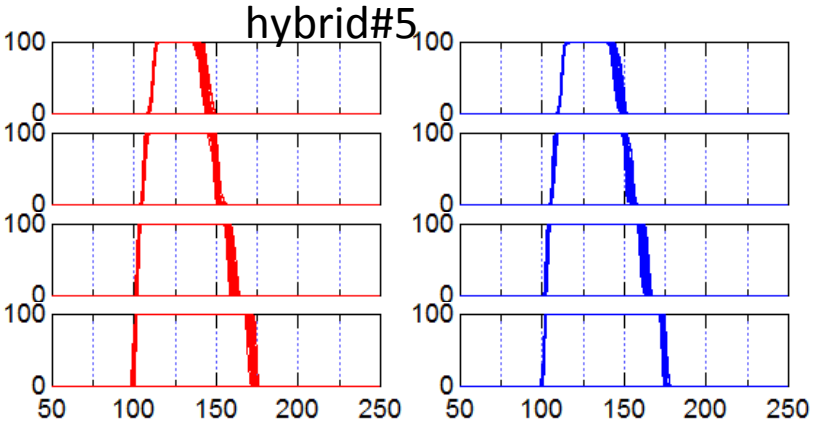
test pulse injection time sweep - all hybrids











not much difference
chip-to-chip or
hybrid-to-hybrid

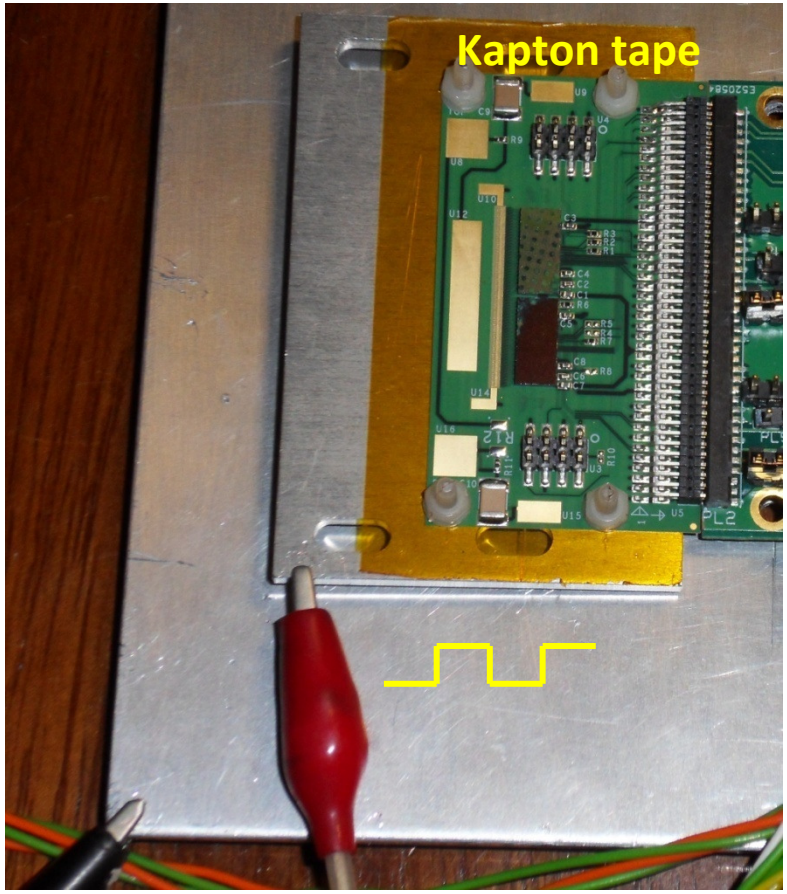
input channel connectivity testing

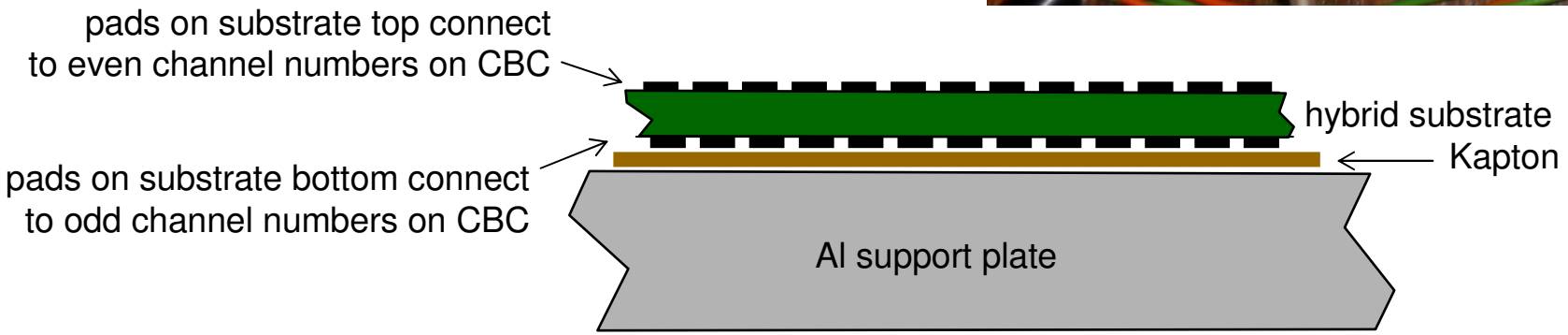
asynchronous squarewave applied to hybrid support plate

capacitively couples to hybrid input sensor traces

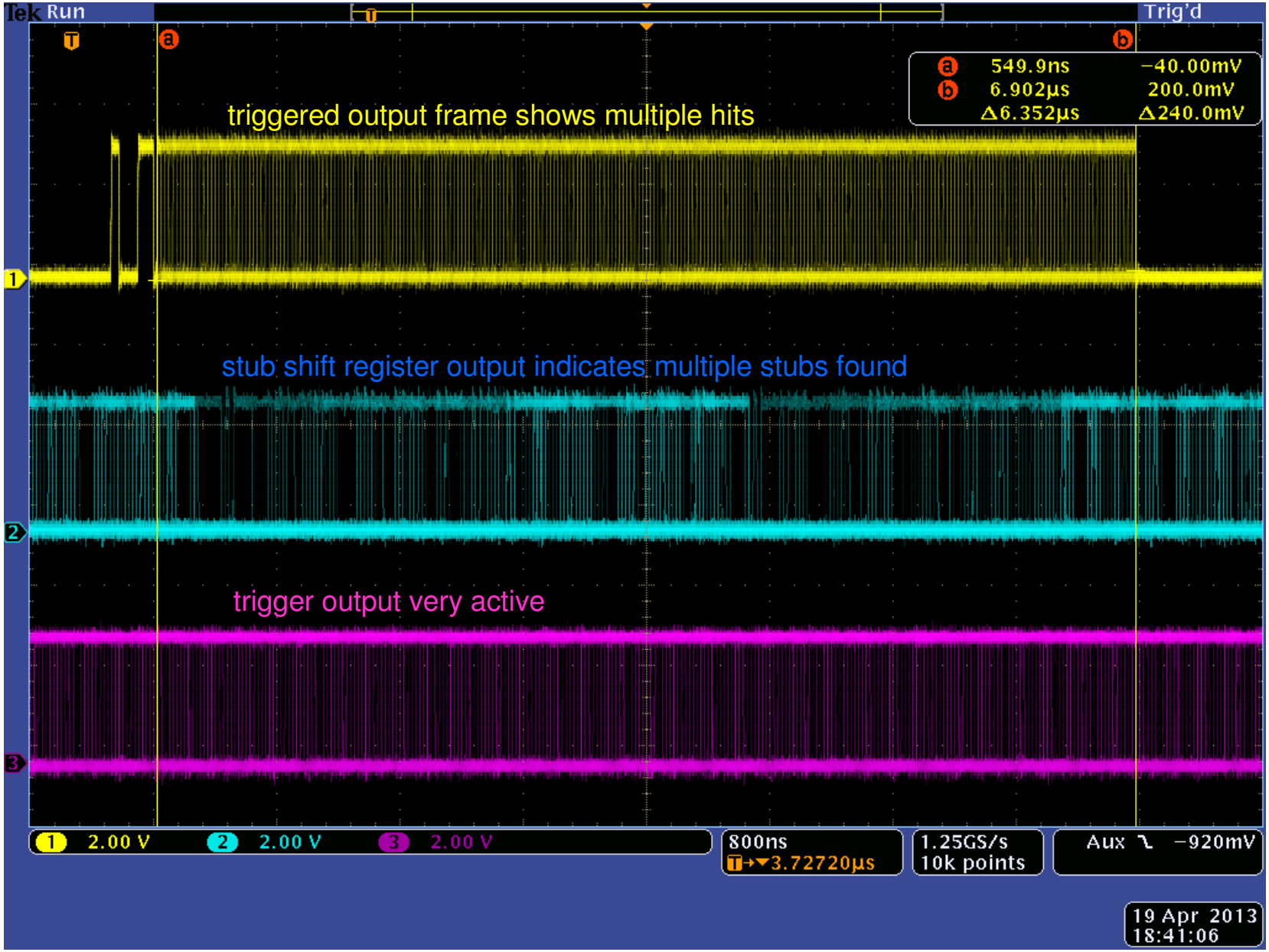
repetitively trigger chip and count hits

expect more hits in channels on bottom of substrate

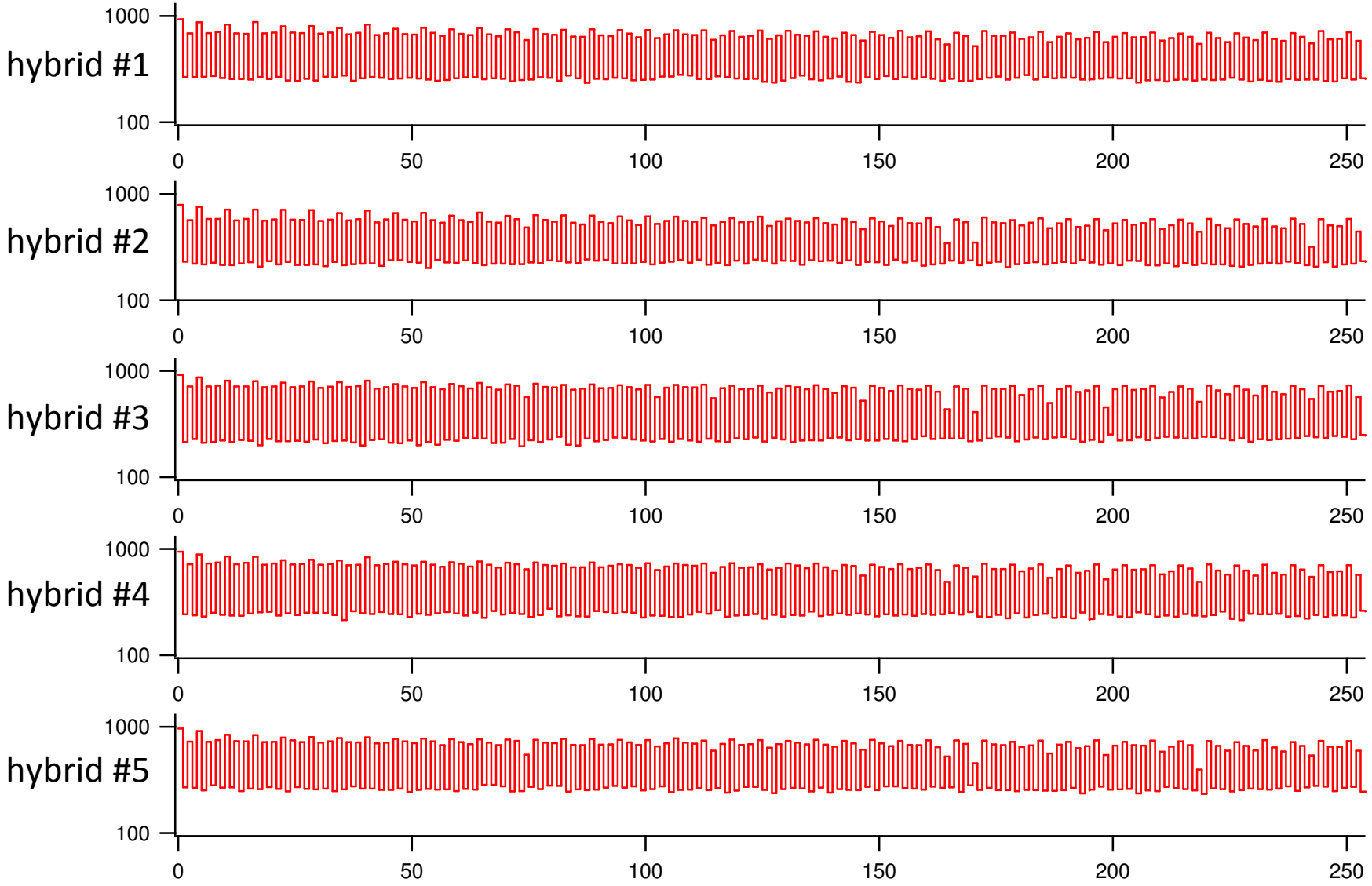




input channel connectivity testing

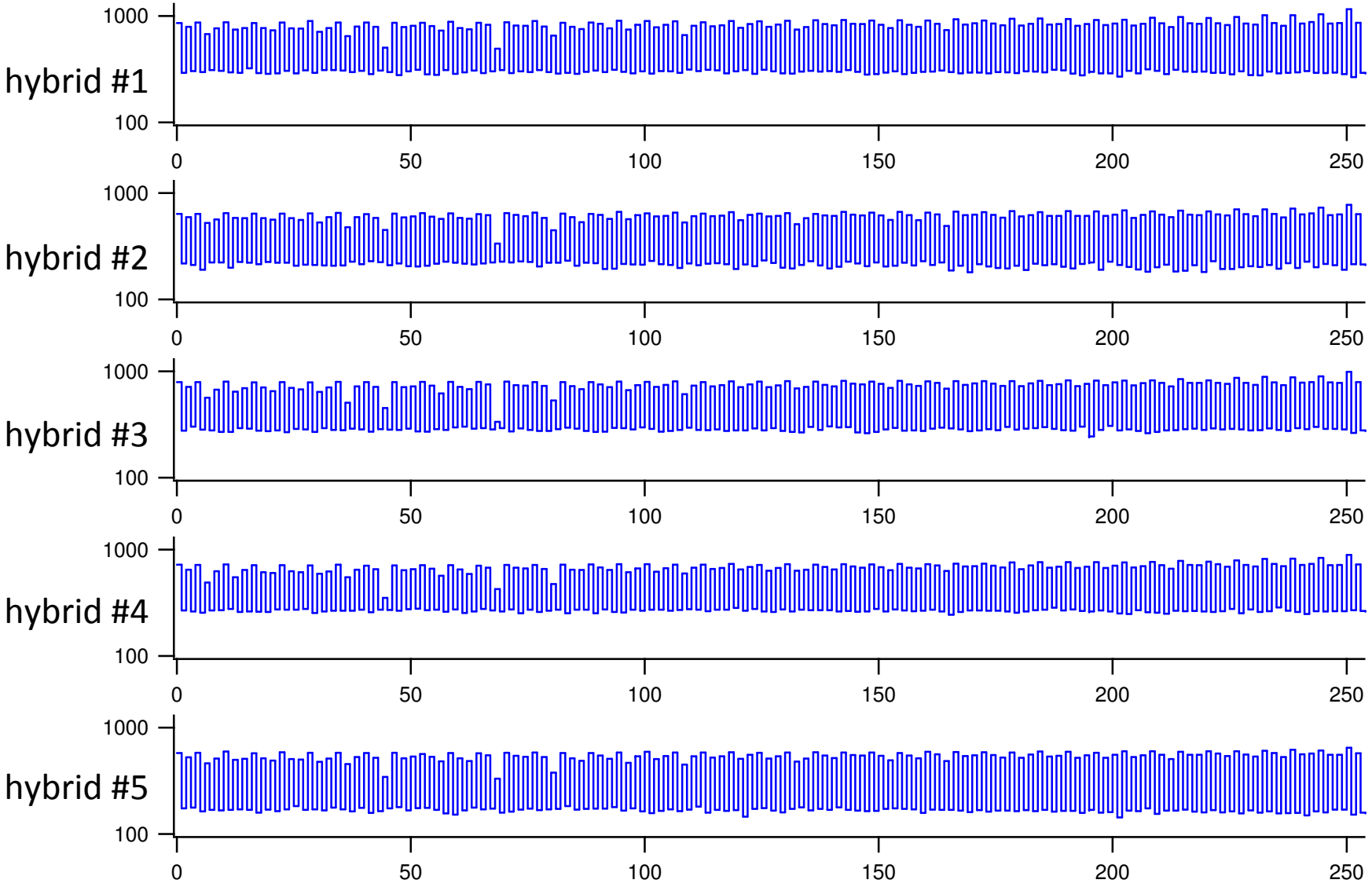


input channel connectivity testing - chip position A



=> all channels connected

input channel connectivity testing - chip position B



=> all channels connected

summary

1st run of five 2xCBC2 hybrid assemblies successful from electrical viewpoint

all chips functional, good uniformity of performance

strong evidence of very high yield of bump-bond connectivity

some redundancy in back end pads
but 100% yield of input channel bonds (254 bonds per chip)