# 8CBC2flex hybrid functional test results

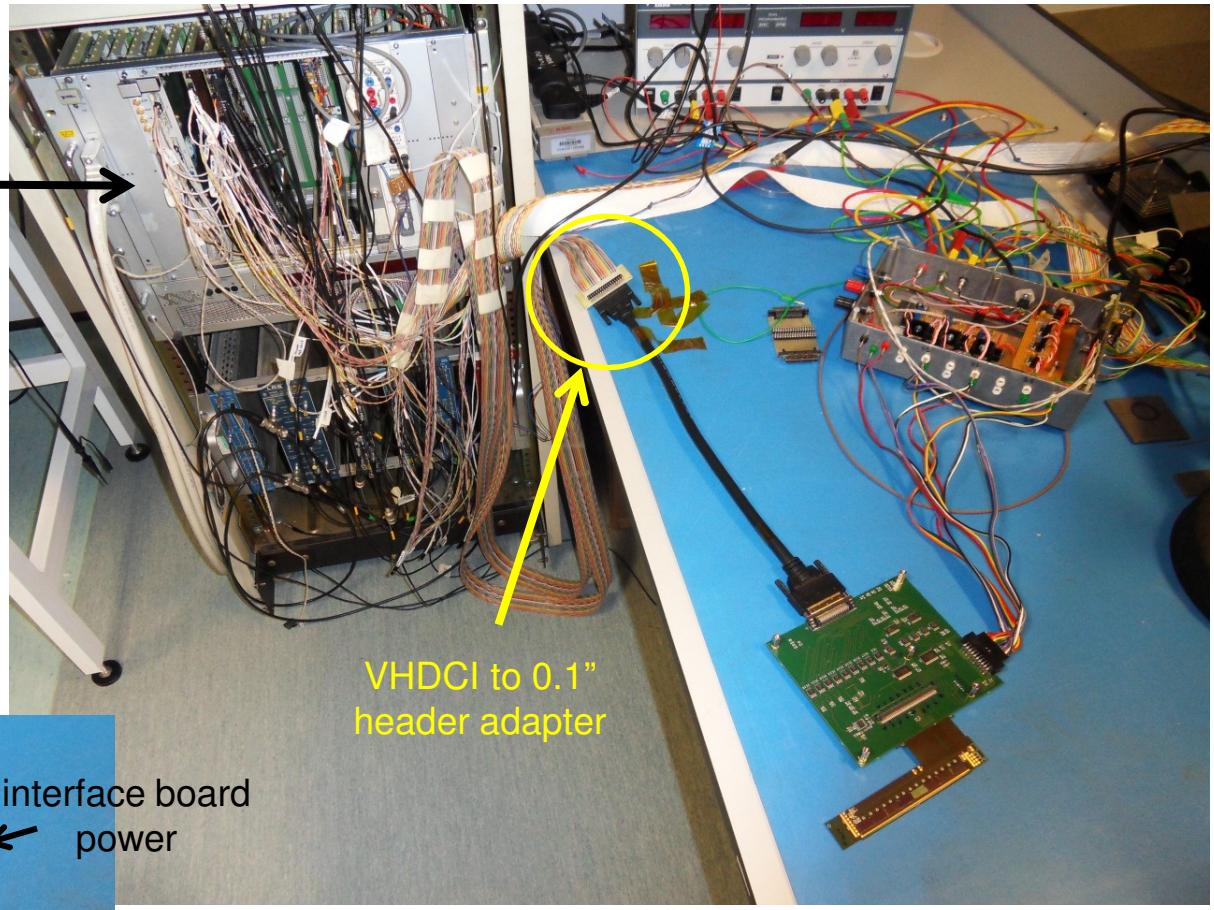
results from screening 2 bump-bonded hybrids
    1 underfilled, 1 not

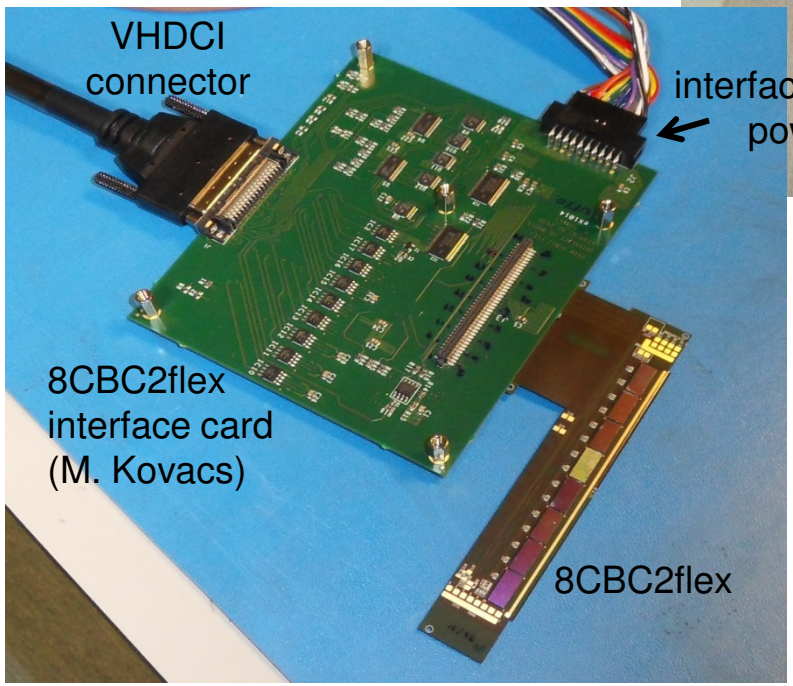
main objective to verify functionality - looking for anything that might
    indicate failure of bump-bonding process

# hybrid test setup

**VME based DAQ**

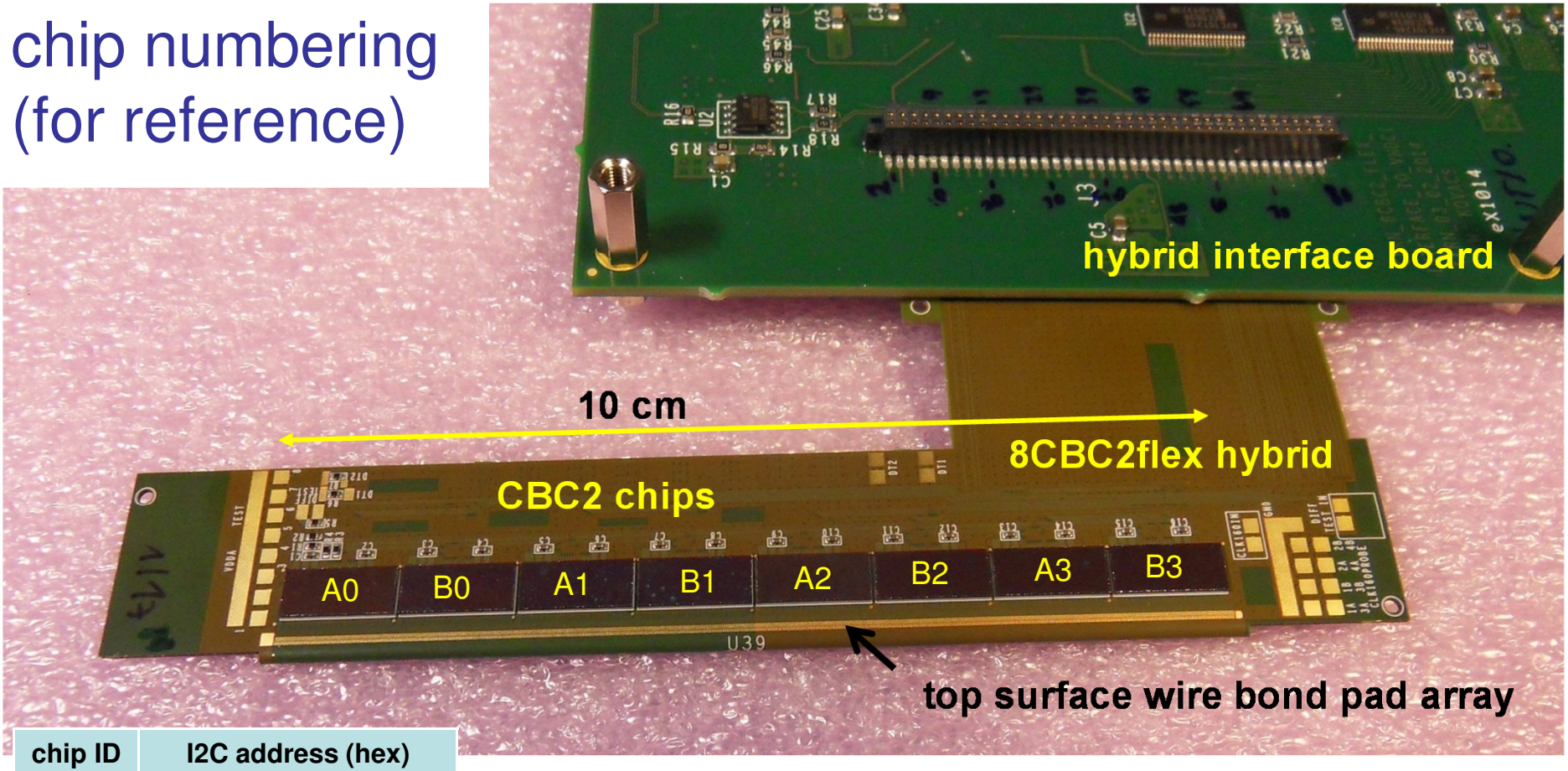
digital pattern generator
I2C interface
digital CBC frame capture




LabVIEW based DAQ software

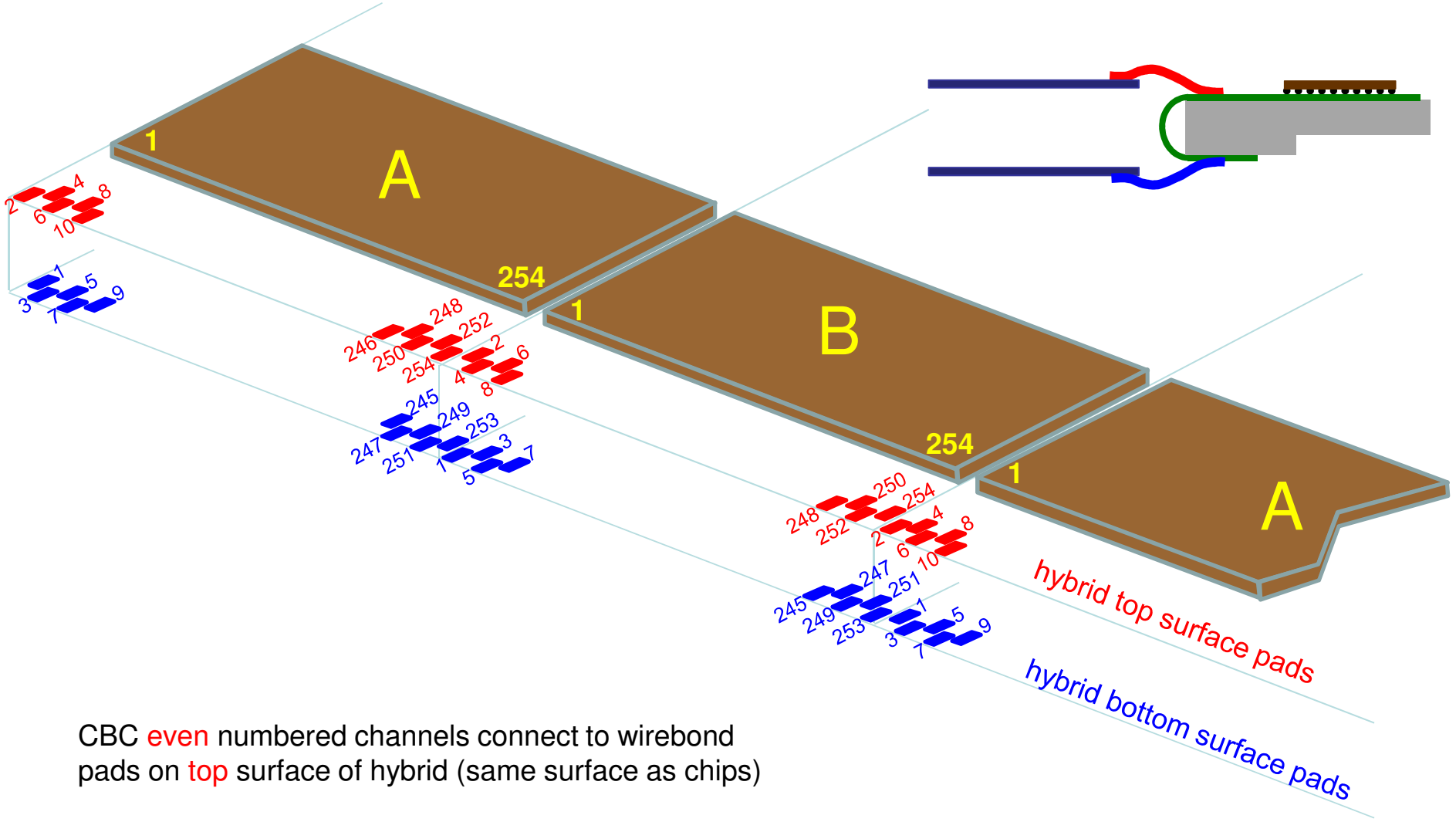
# chip numbering (for reference)




| chip ID | I2C address (hex) |
|---|---|
| A0 | 0x41 |
| B0 | 0x42 |
| A1 | 0x43 |
| B1 | 0x44 |
| A2 | 0x45 |
| B2 | 0x46 |
| A3 | 0x47 |
| B3 | 0x48 |

chips identified as pairs A/B, like 2CBC2 hybrid

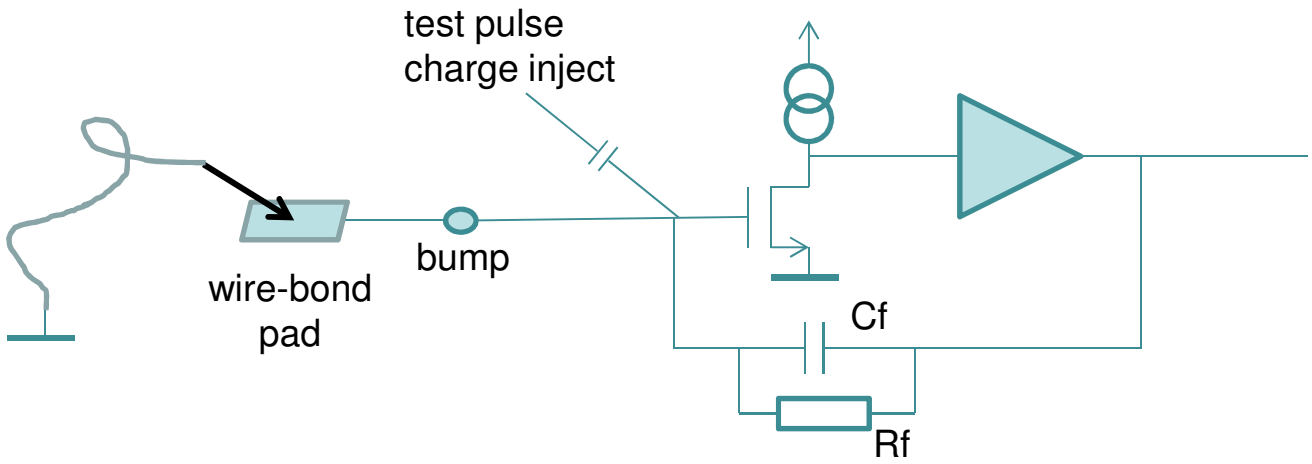
# CBC channel number mapping (for reference)




CBC even numbered channels connect to wirebond pads on top surface of hybrid (same surface as chips)

CBC odd channels come from bottom surface
=> longer tracking distance from wirebond pad to CBC input

# input channel connectivity testing




goal is to verify all channels connected via bump to wire-bond pad array

important given experience with 2CBC2 hybrids

inject charge using on-chip test pulse

=> look at output data frame => verify channel is working

place grounded probe needle on wire-bond pad

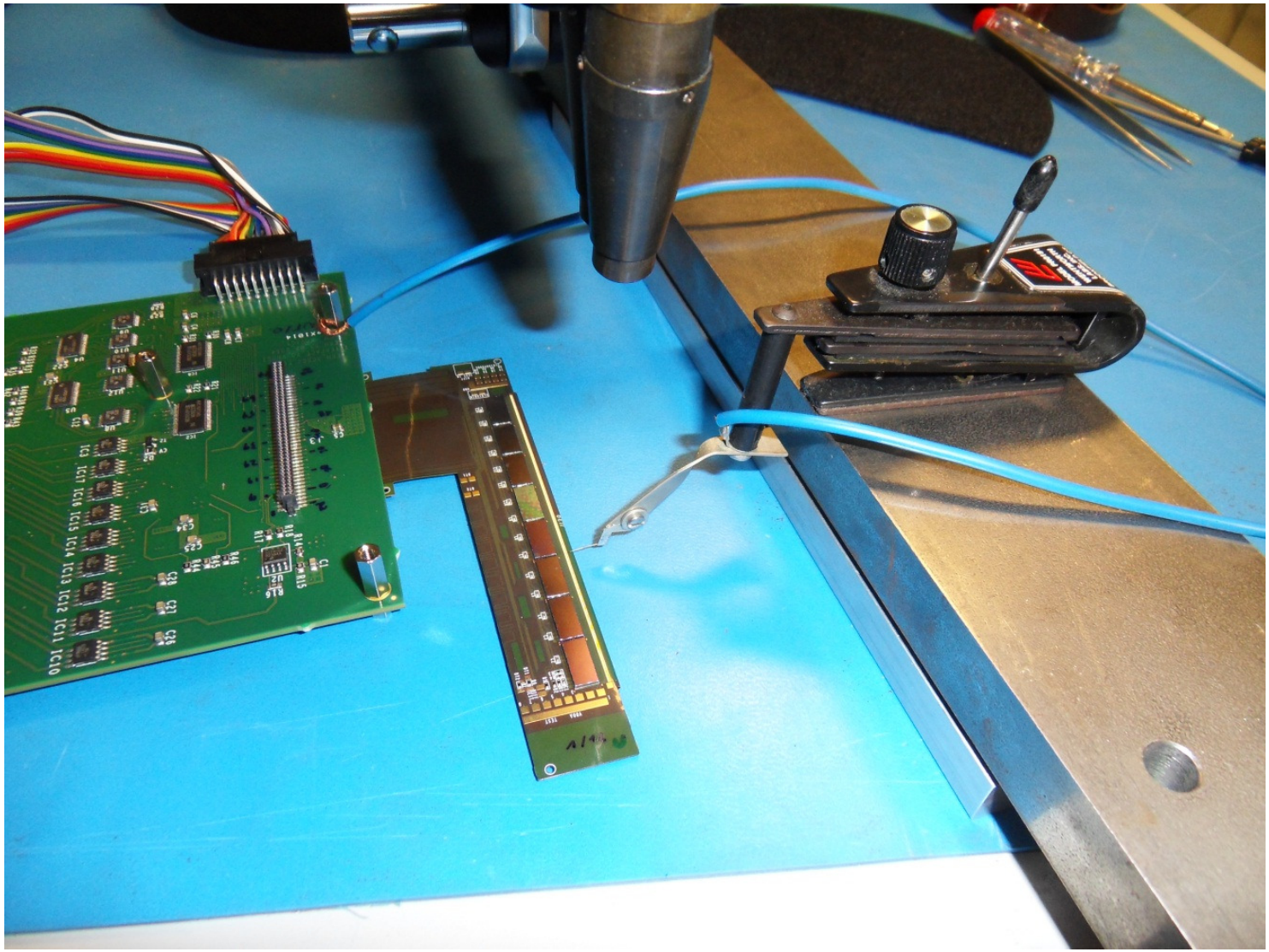
if connection good then input FET turned off and output signal disappears

repeat for all 2032 channels on hybrid!

# input channel connectivity testing

**results**

all channels on both hybrids alive and connected to wire- bond pads arrays



# measured power parameters

all chips powered from digital 1.2V VDDD rail

analogue powered via LDO
1.2 V VDDD in / 1.1 V VDDA out
current measured in VDDD rail

if clock chip but set all analogue bias values to zero
baseline current ~ 6mA / chip (~ 50mA total)
(digital + quiescent analogue)

now program analogue biases to nominal values

IPRE1 = 35 (suitable for no external capacitance)
IPRE1 = 240 (appropriate for 5 cm strips)

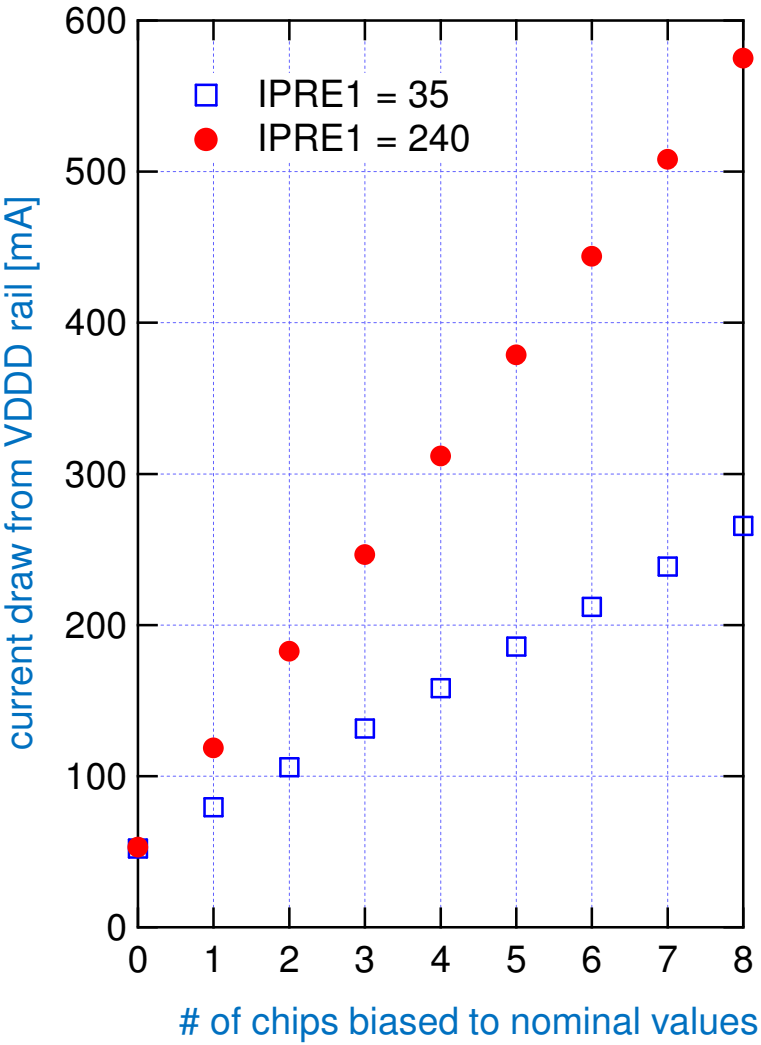
| nominal I2C bias values | |
|---|---|
| IPRE1* | 35/240 |
| IPRE2 | 20 |
| IPSF | 45 |
| IPA | 30 |
| IPAOS | 45 |
| VPAFB | 0 |
| ICOMP | 30 |
| VPC | 74 |
| VPLUS | 100 |

current ~ 34 mA / chip for IPRE1=35
~ 70 mA/ chip for IPRE1=240

**no surprises and no problems**
only ~10 mV droop in VDDD
across hybrid for IPRE1=240

(*IPRE1 needs to be chosen appropriately, depending on sensor capacitance)

**hybrid current vs. # of chips biased**



# s-curves

individual channel comparator offsets tuned (electrons mode) using recommended procedure

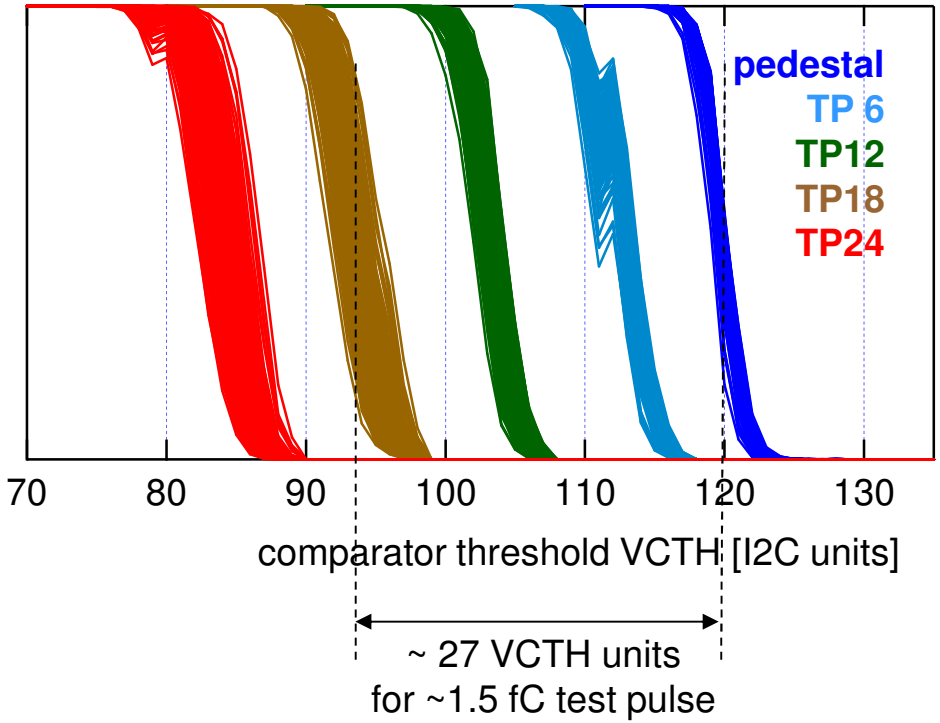
(see Kirika's talk)

=> pedestal s-curves mid-points at VCTH = 120

s-curves taken using internal test pulse gives approximate gain measurement

test pulse amplitude [I2C units] ~ 12 / fC
~ 2.5 mV / VCTH I2C unit
=> gain ~ 45 mV / fC

**s-curves raw data**
**all channels for 1 chip, different test pulse amplitudes**

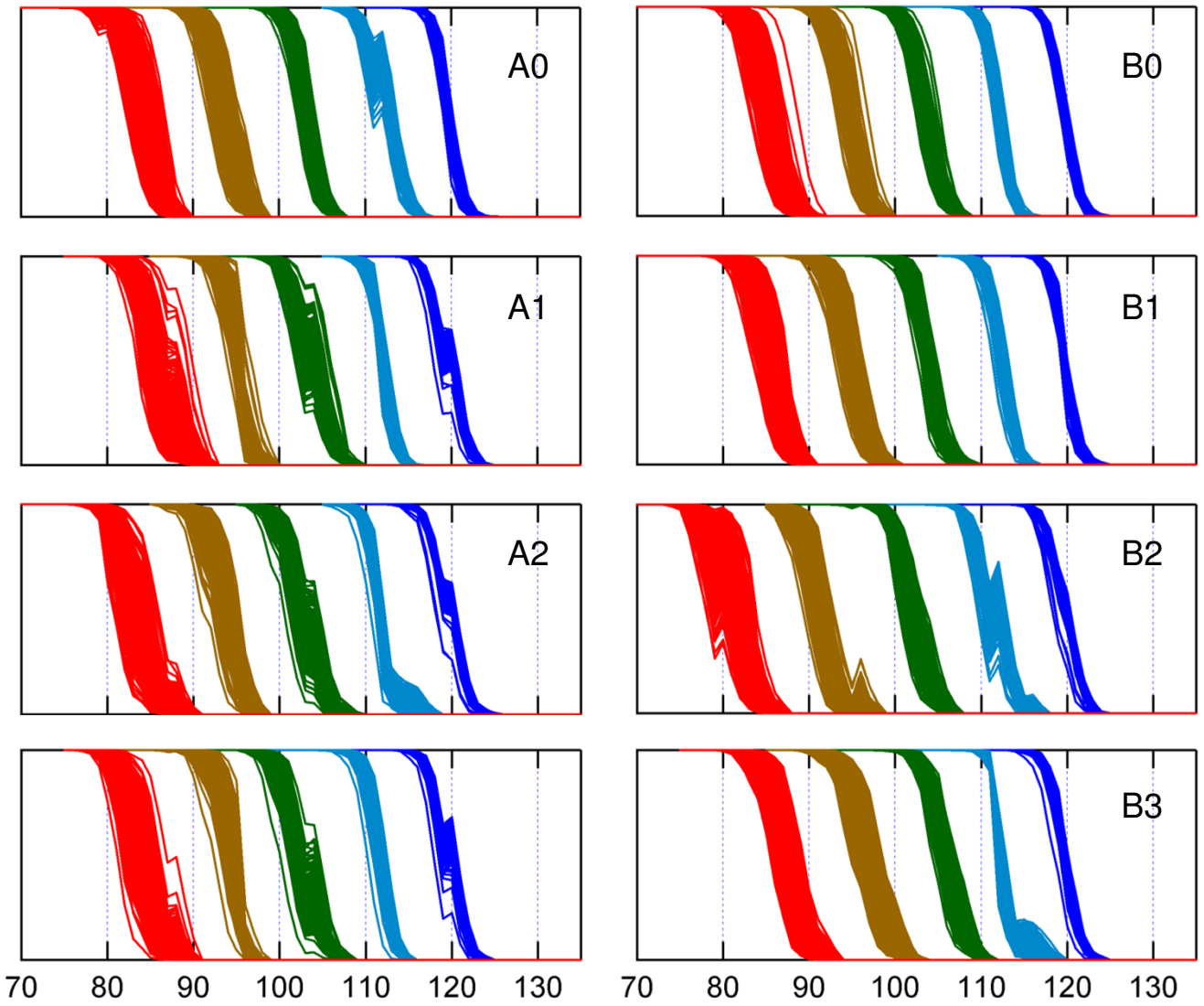



raw s-curve data shows effects of comparator threshold non-linearities

particularly obvious for test pulse amplitude 6 in this example

plan to improve VCTH linearity in next version of chip

# s-curves raw data: all chips




**pedestal**
**TP 6**
**TP12**
**TP18**
**TP24**

all chips functioning

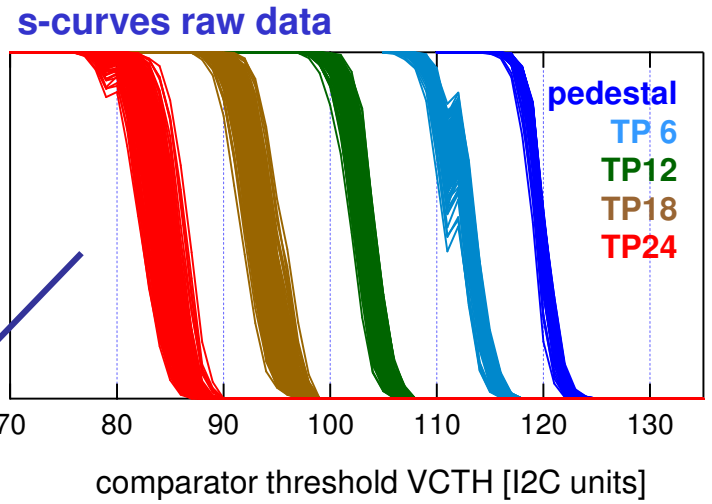
(both hybrids)

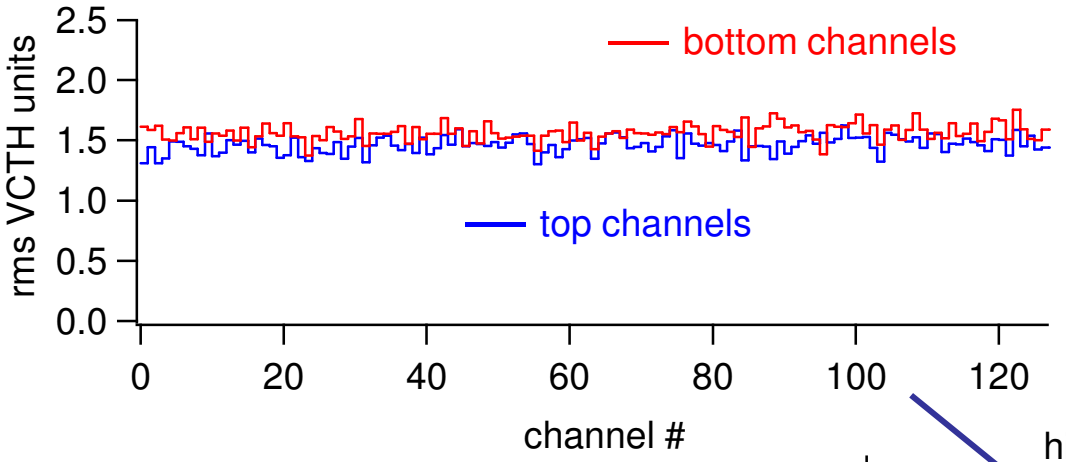
gains ~ similar

# noise

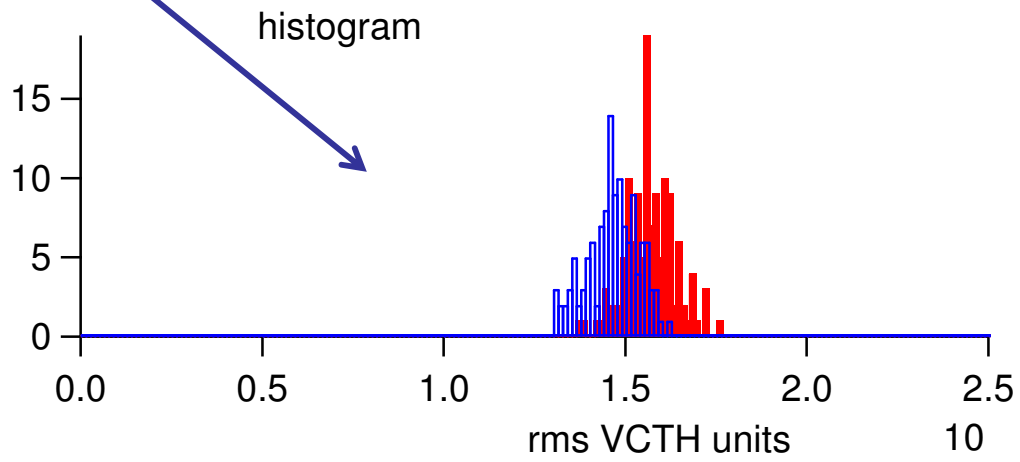
noise obtained from erfc fit to raw s-curve data

interesting to sort into channels corresponding to top and bottom wire-bond pad arrays

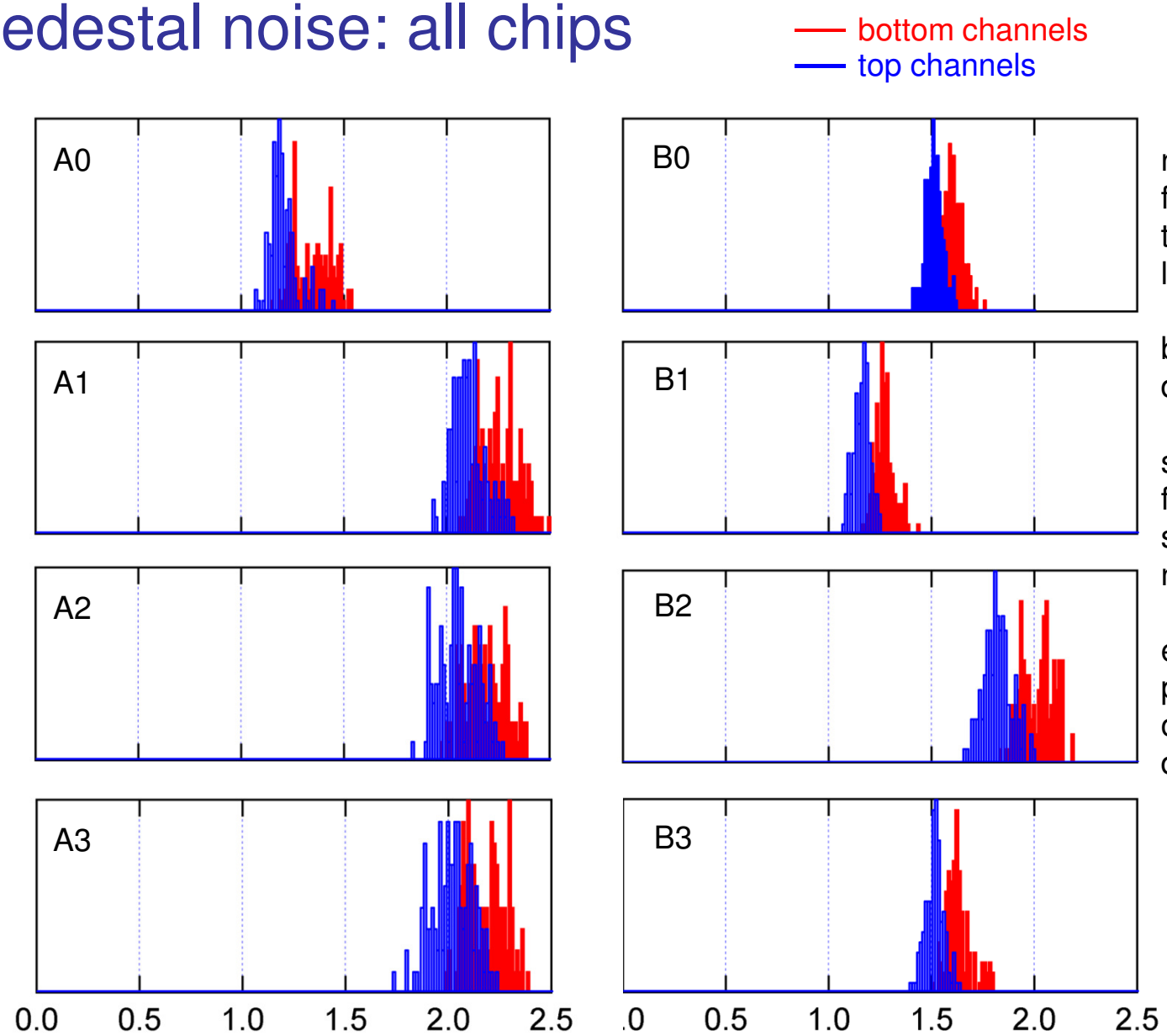



slightly nigher noise observed for channels on bottom surface of hybrid



# pedestal noise: all chips




noise consistently higher for channels connected to wirebond pads though longer tracks

big chip to chip variations due to VCTH non-linearity

s-curves span only a few VCTH units so very sensitive to differential non-linearity

e.g. A1, A2, and A3 pedestal s-curves sit on a significant VCTH discontinuity (see slide 9)

# summary

2 8BCB2flex hybrids tested: 1 underfilled, 1 not

no functionality problems found, 100% channels working

100% connectivity verified between chip inputs and wire-bond pads

good prospects for constructing full size module prototypes