CBC2: test results & plans

OUTLINE

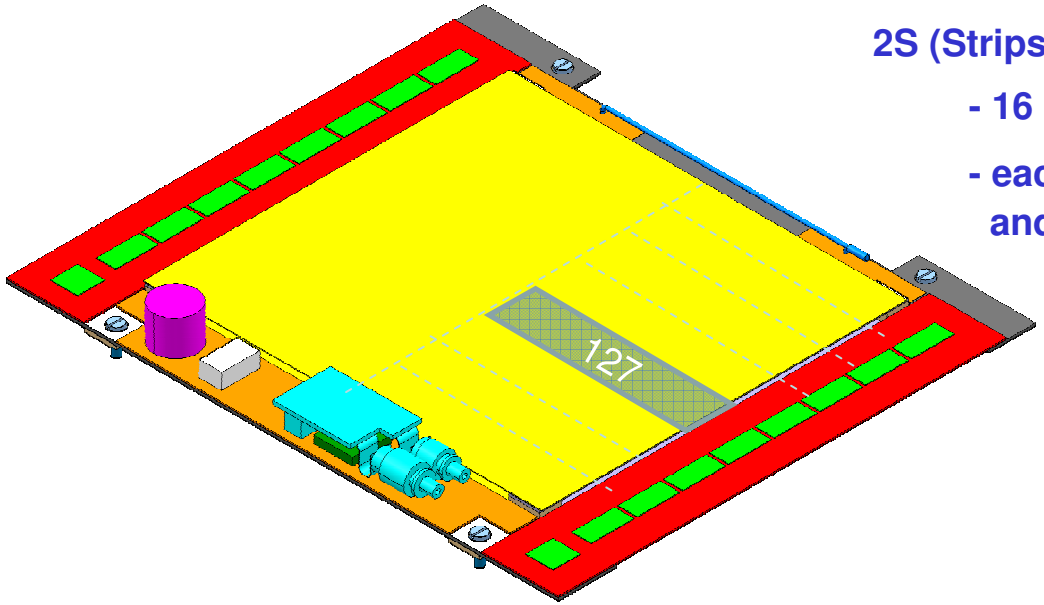
reminder of CBC2 layout and architecture

test results so far
- front end performance
- pT stub logic functionality
- wafer test

summary and further test plans

for more details see Outer Tracker Review talk:
https://indico.cern.ch/getFile.py/access?contribId=2&sessionId=0&resId=1&materialId=slides&confId=234886
and Tracker Phase II electronic system design meeting talk:
https://indico.cern.ch/getFile.py/access?contribId=0&sessionId=0&resId=1&materialId=slides&confId=246815

CBC2 for 2S-Pt module



2S (Strips-Strips) module

- 16 readout chips

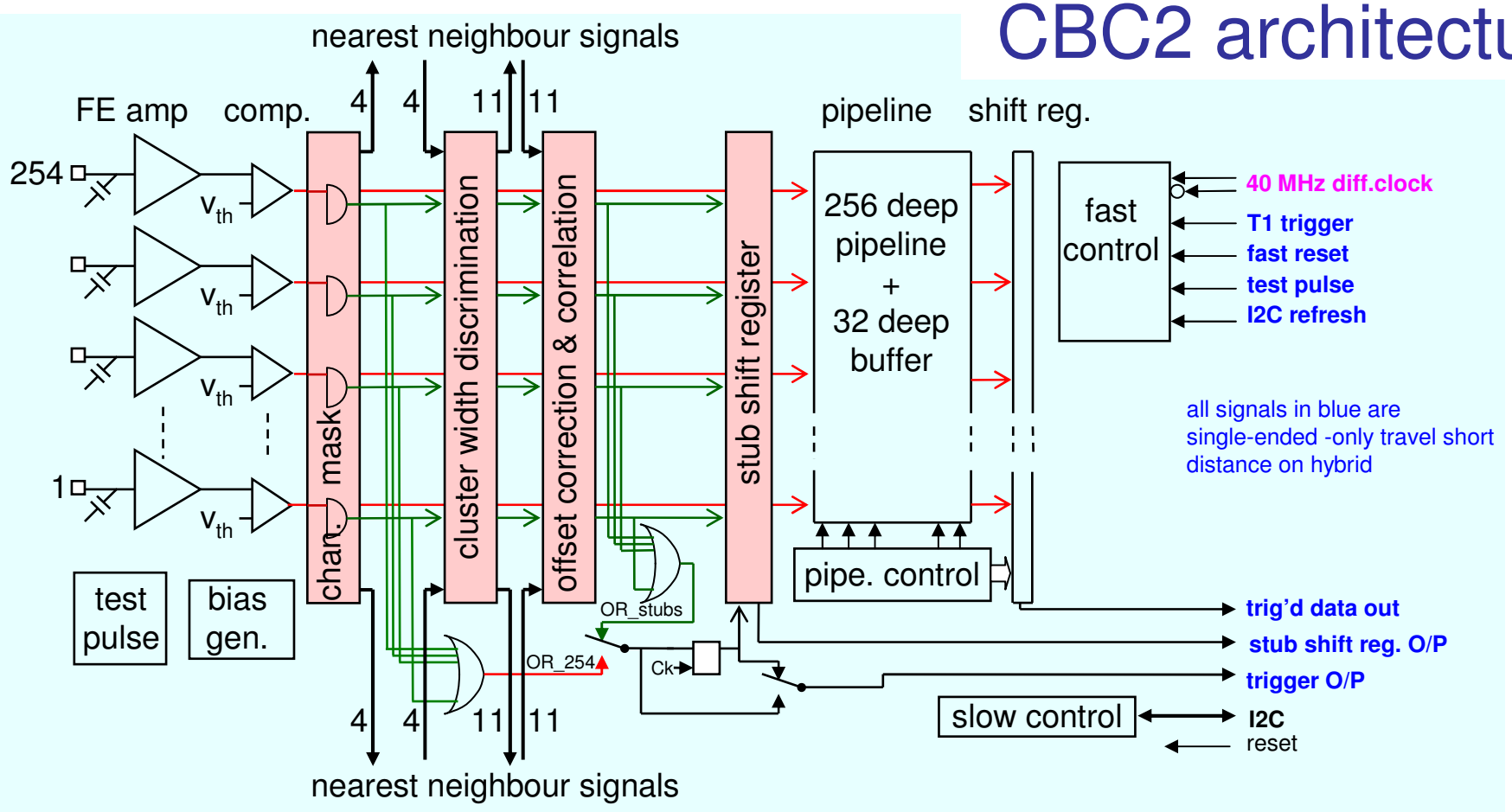
- each reads 127 strips from bottom sensor and 127 from top

CBC2

bump-bond chip, brings signals from 2 sensor layers in 1 chip (254 channels total)
provides L1 triggered readout data as in prototype
also performs cluster correlations to identify high Pt stub
positive correlation produces trigger output pulse

=> functionality required to construct and evaluate prototype 2S-Pt module

CBC2 architecture



front end, pipeline, L1 triggered readout, biasing

~ same as prototype (some bug fixes) twice as many channels

new blocks associated with Pt stub generation

channel mask: block problem channels (not from L1 pipeline)

cluster width discrimination: exclude wide clusters > 3

offset correction and correlation: correct for phi offset across module and correlate between layers

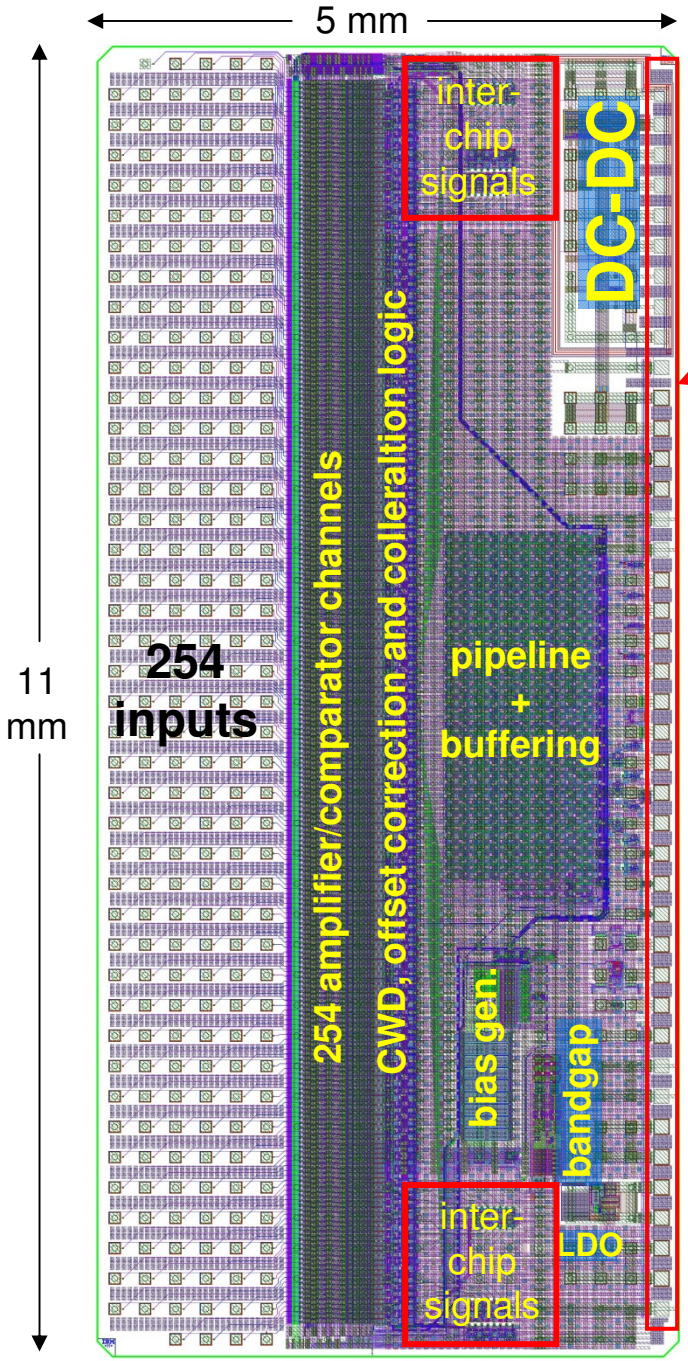
stub shift register: test feature - shift out result of correlation operation at 40 MHz

trigger O/P: in normal operation 1 bit per BX indicates presence of high Pt stub

test pulse

charge injection to all channels (8 groups of ~32), programmable timing and amplitude

CBC2 layout



C4 layout, 250um pitch, 19 columns x 43 rows

30 inter-chip signals (15 in, 15 out), top and bottom gives continuity across chip boundaries

right-most column wire-bond (for wafer probe test)
- access to:
  - power
  - fast control
  - I2C
  - outputs

prototype powering features retained
- CERN bandgap, LDO for analog powering, same as prototype
- improved DC-DC switched capacitor circuit (CERN)
  - slower switching edges & rad-hard layout

chip submitted for fabrication July 2012

- wafers back January 2013
- wire-bondable (other users) and C4 processed (CBC2)

Davide Braga,
Mark Prydderch,
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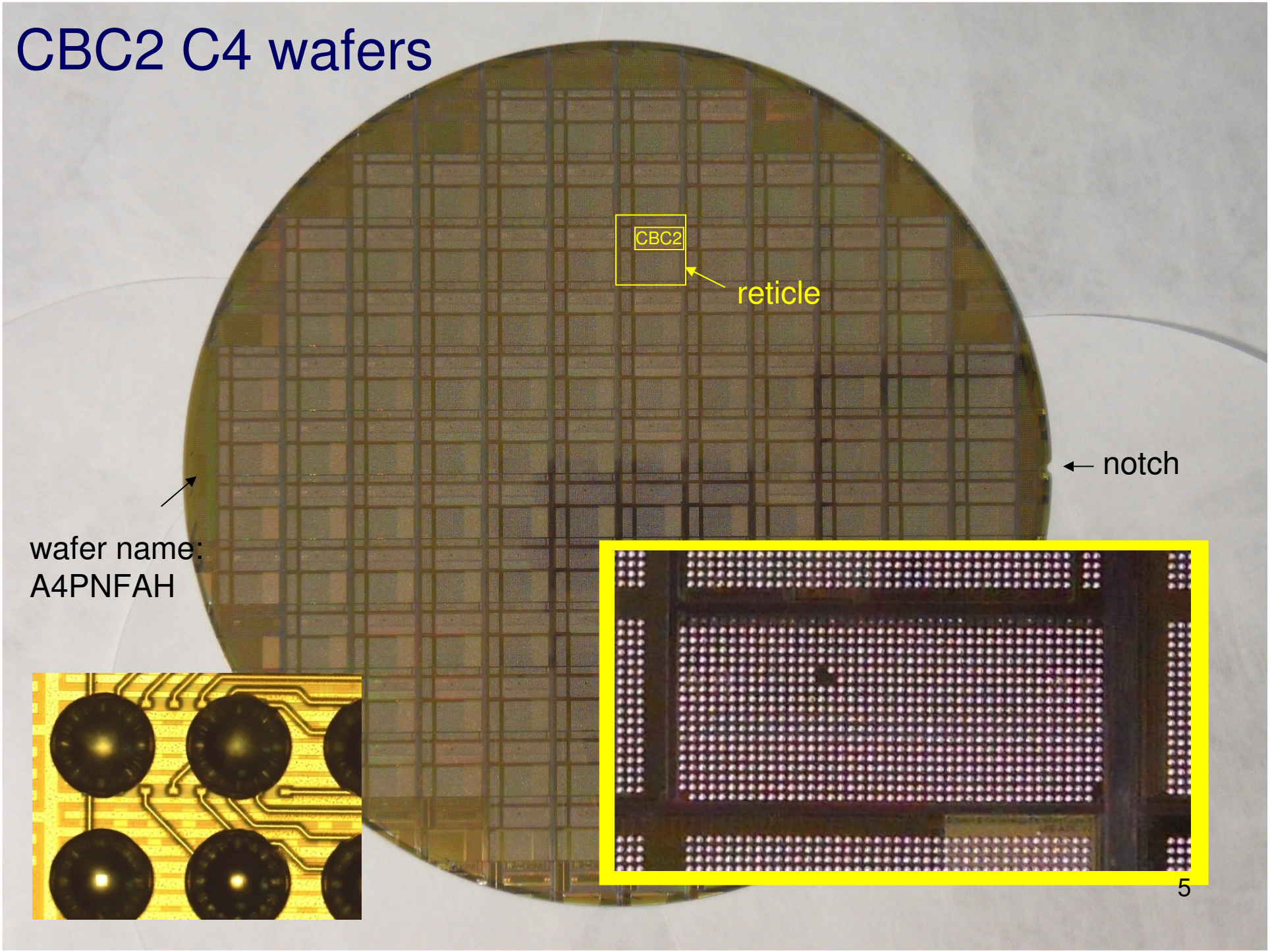
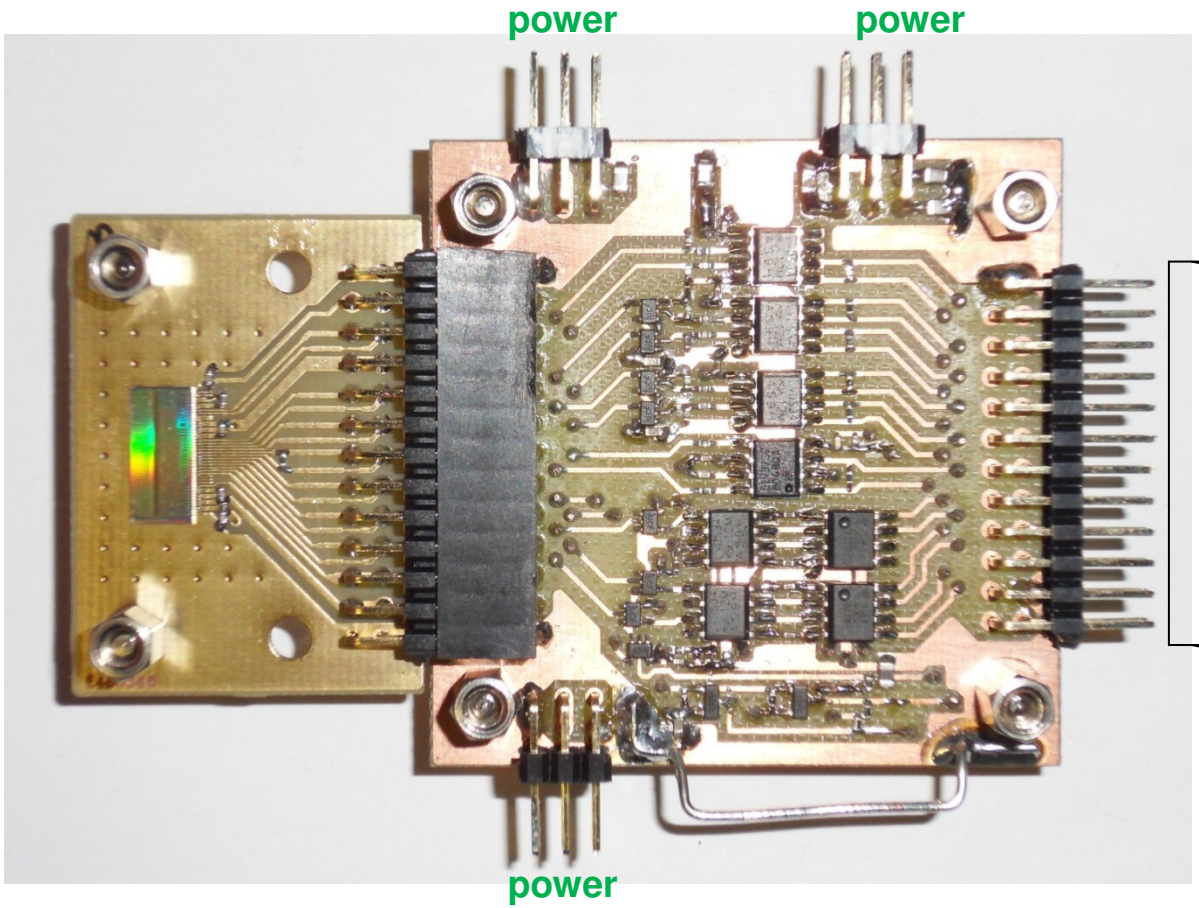
(RAL)

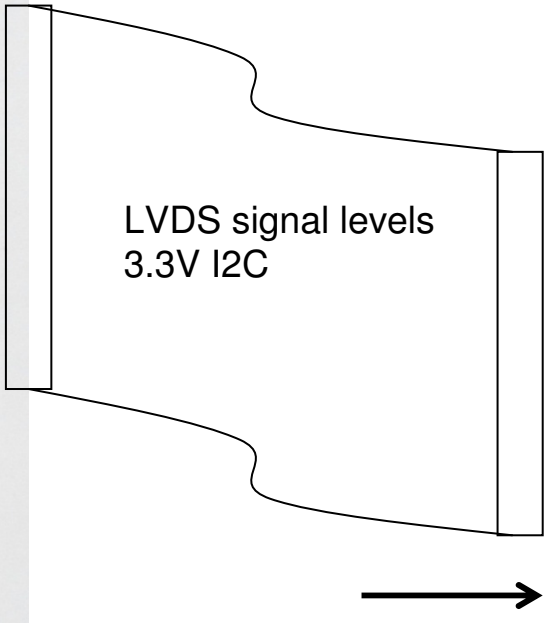
CBC2 C4 wafers



front end performance

wire-bond CBC2 test setup





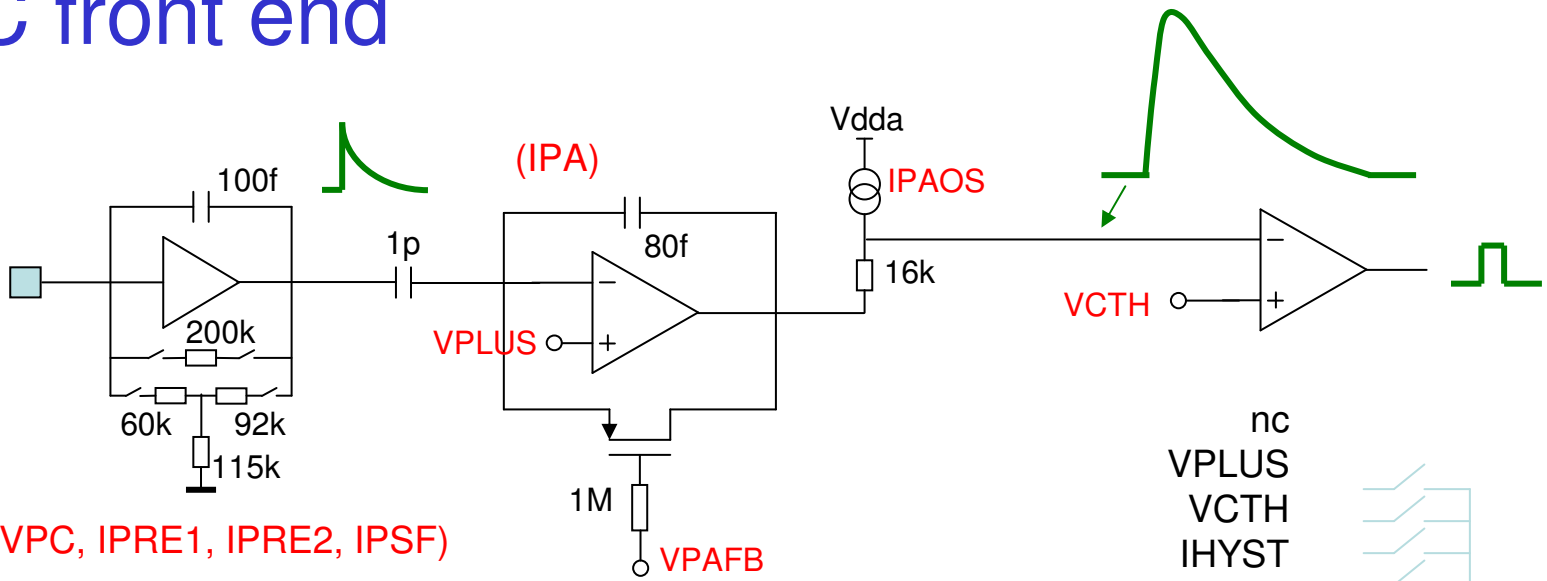
VME based DAQ

use wafer probe pads to wirebond single CBC2 die to carrier
(CBC2 chips from diced wire-bond (XFEL) wafer)

convenient setup for developing wafer probe procedures

all testing performed using 1.2V VDDD supply only
VDDA provided by LDO on CBC2

CBC front end

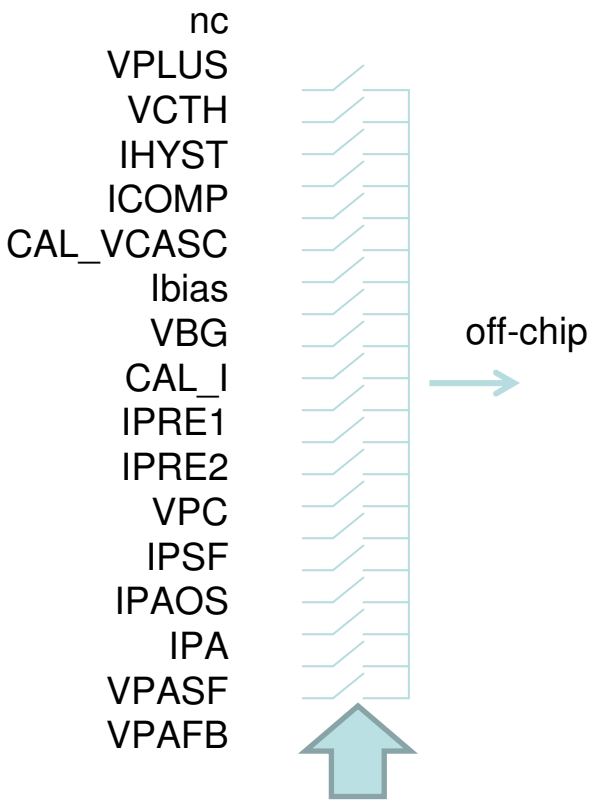


bias studies

currents and voltages required to set front end operating conditions

accessible outside using analog mux output (test feature)

most useful for voltages
e.g. VCTH - global comparator threshold



bias voltages

shape as expected
simulation and CBC1

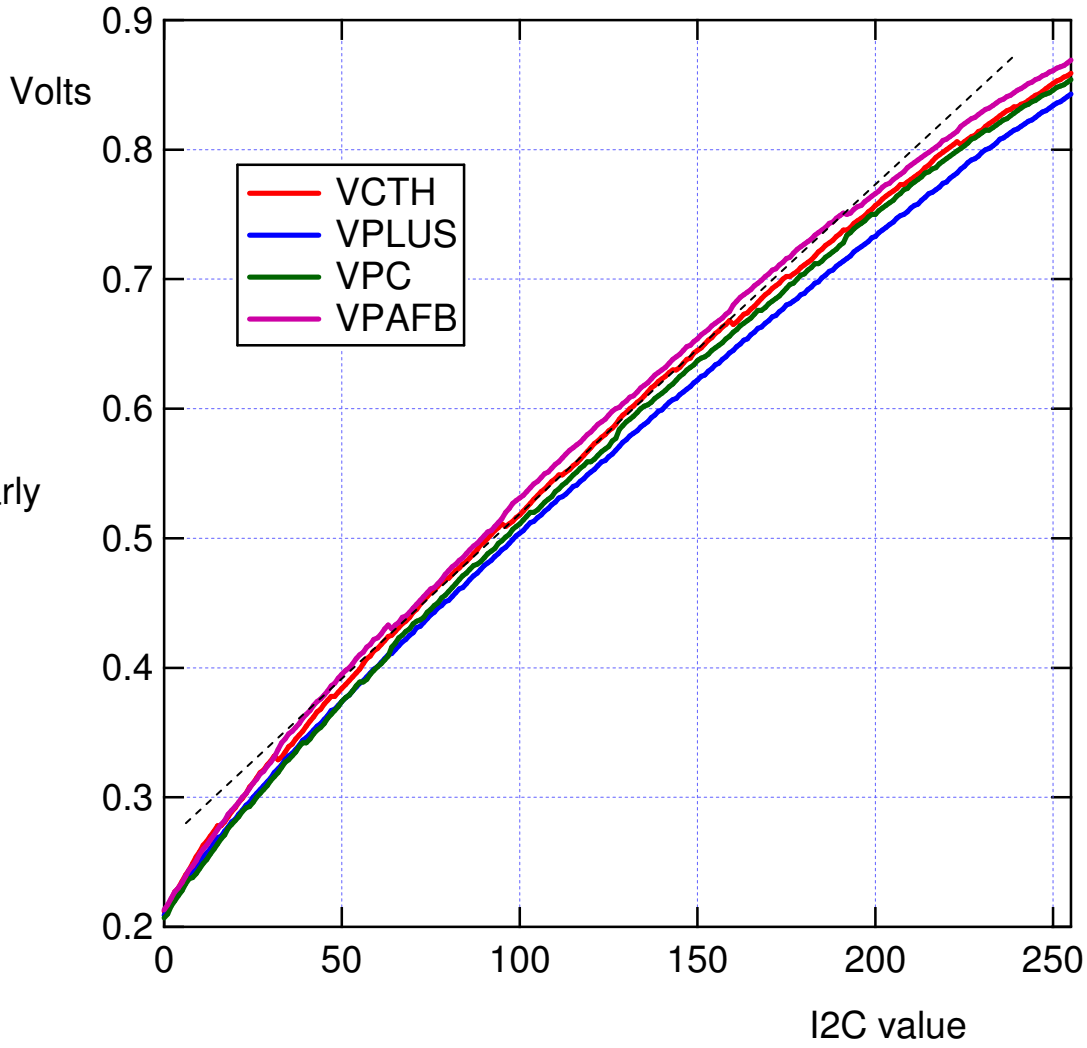
linearity not important

discontinuities (diff. non-linearity), particularly for global comparator threshold VCTH causes some difficulties

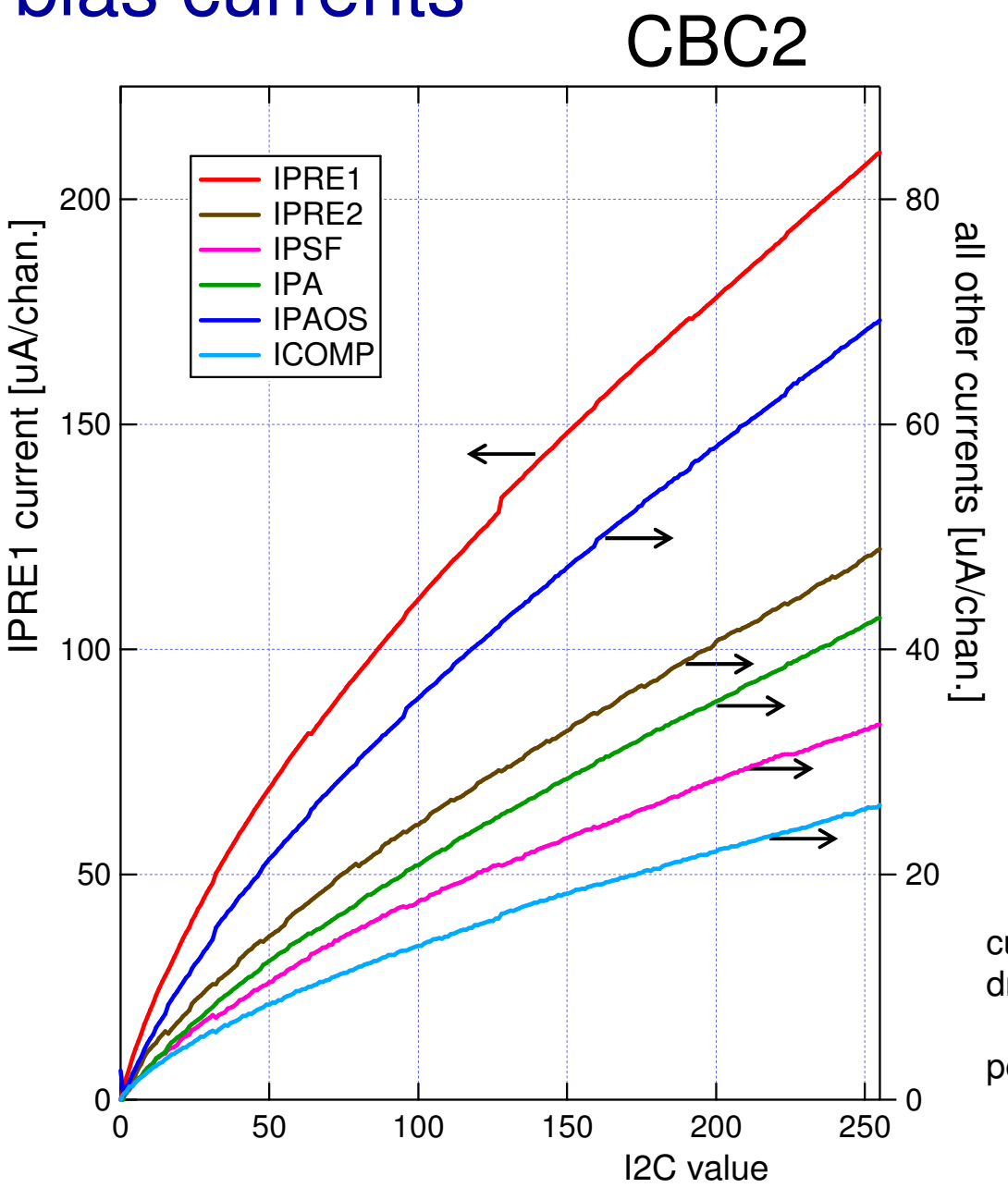
will see why later

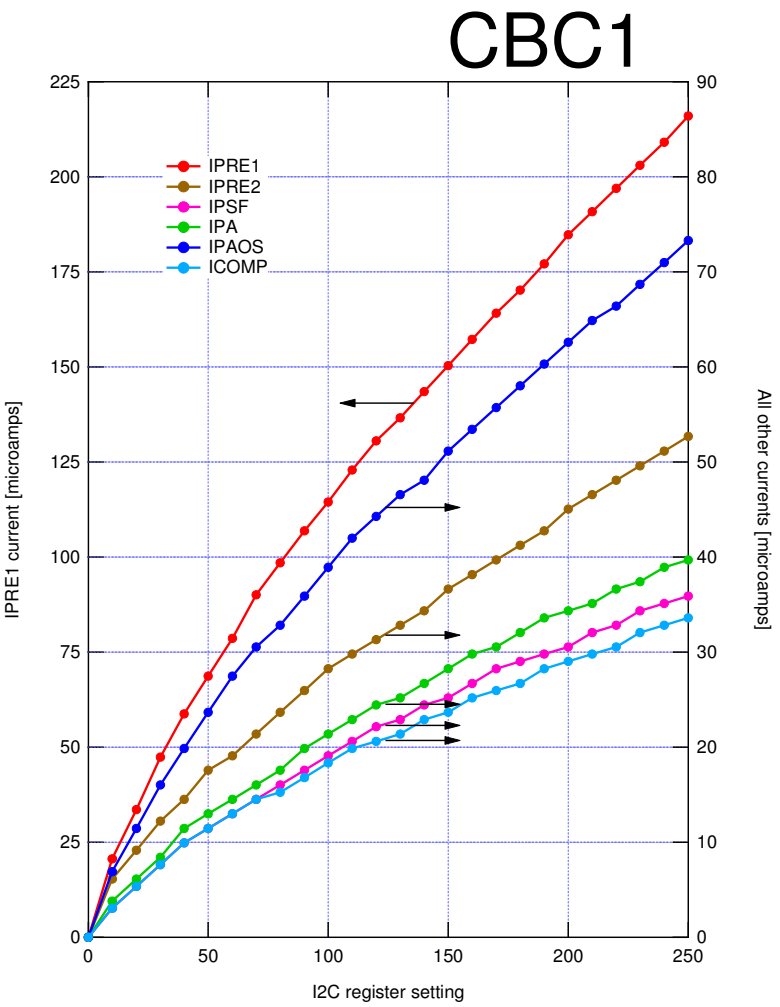
(can try and improve in future)

rough fit -> 2.5 mV / I2C unit



bias currents

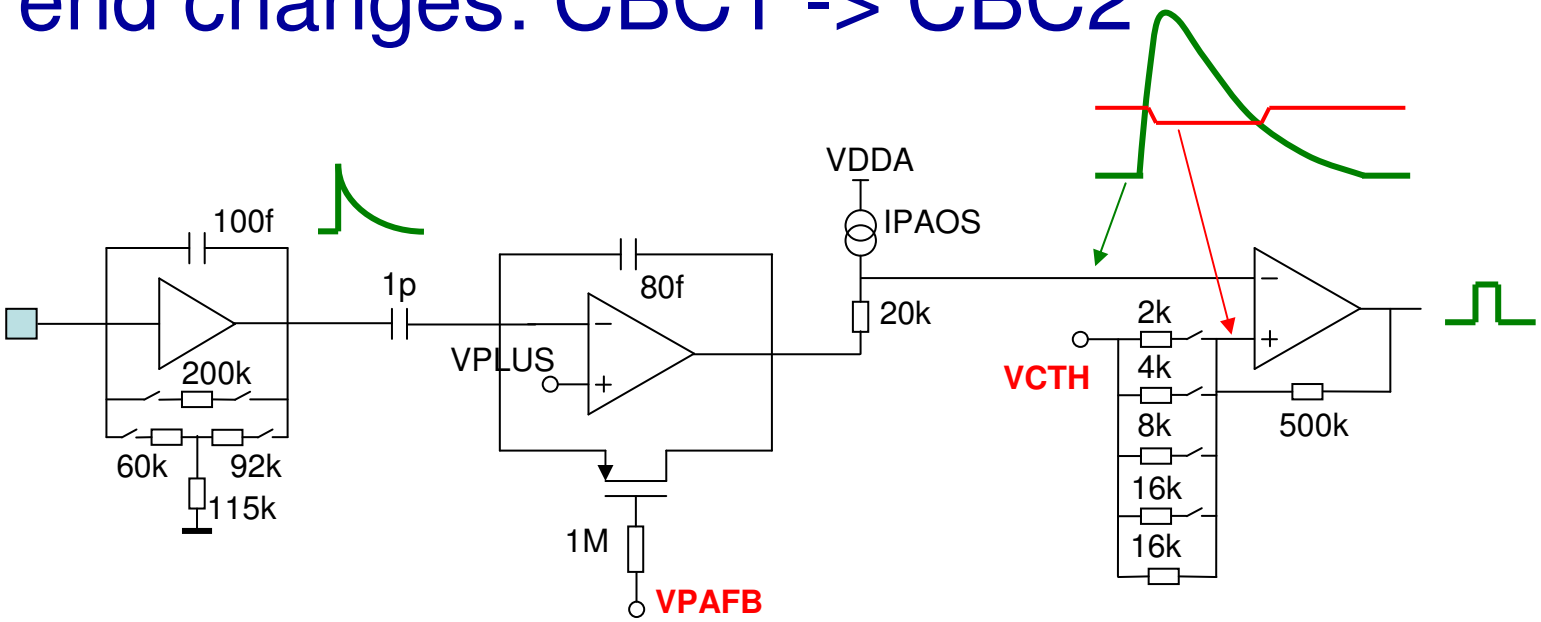




currents/channel deduced from current drawn from VDD as register value swept

performance v. similar to CBC1

front end changes: CBC1 -> CBC2



2 significant problems with prototype chip version

postamp: VPAFB susceptible to CM effects
needed external decoupling for stability
solution: VPAFB buffered by source follower on very channel

comparator: VCTH affected by external hysteresis network
external overdriving solved the problem
solution: hysteresis implemented differently - no load on VCTH

measurements show both these solutions have worked for CBC2

on-chip test pulse

test capacitors present on CBC1 but no on-chip circuit to drive

DLL circuit on CBC2 allows to inject charge with programmable phase relative to 40 MHz clock (25 steps of 1 nsec)

test pulse amplitude provided by resistor string between 1.1V & GND (256 steps)

charge inject polarity depends on which switch closed

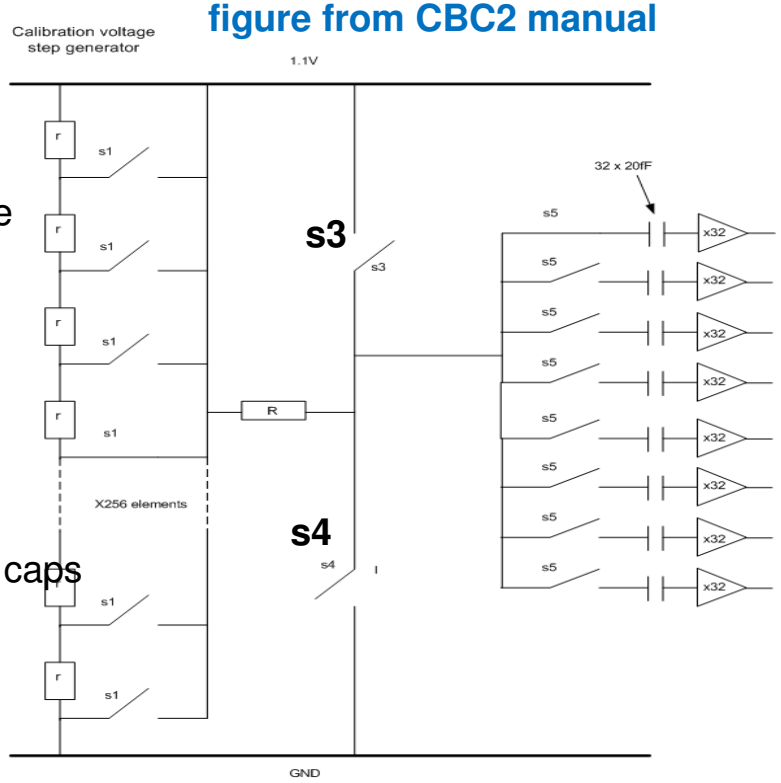
charge injected into 32 channels simultaneously through 20 fF caps

20fF x (1.1V / 256) = 0.086 fC step resolution

e.g. value of 12 corresponds to ~ 1 fC (+/- 10%)

(20fF largest source of uncertainty)

figure from CBC2 manual



some evidence (during testing) of DLL losing lock occasionally

can restart by disabling and re-enabling via I2C - but needs further investigation

test pulse sweep

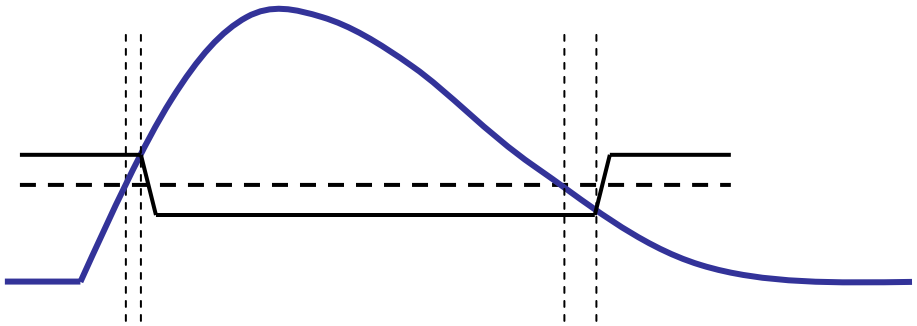
sweeping charge injection time allows to study comparator behaviour

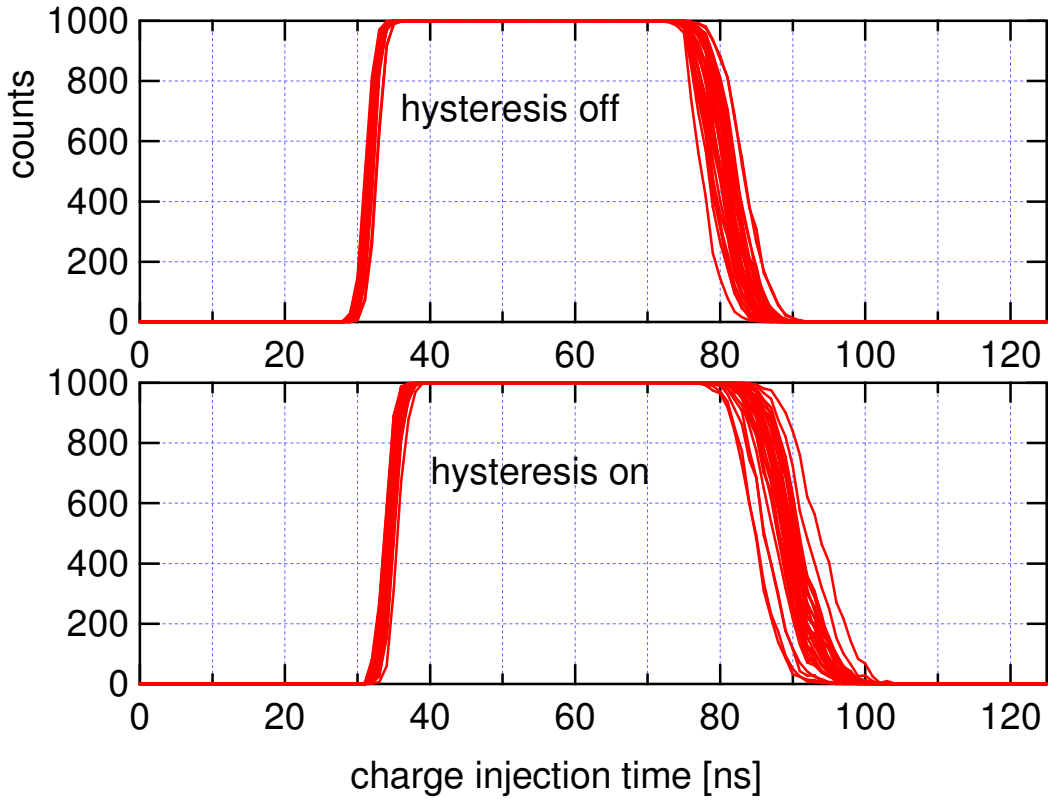
count the number of times hit
observed for fixed number of triggers,
for each timestep

get coarse steps of 25 nsec by moving test trigger fast control pulse

get 1 nsec resolution using DLL steps

hysteresis circuit working as expected (new method of implementing in CBC2)



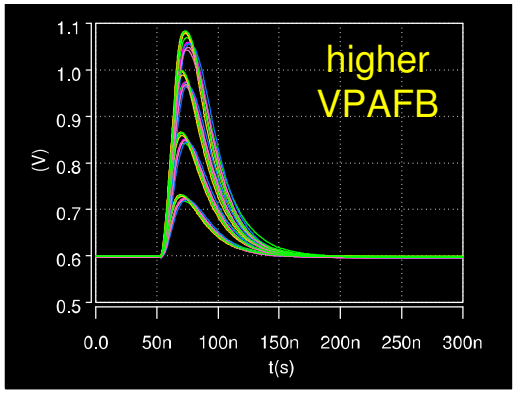


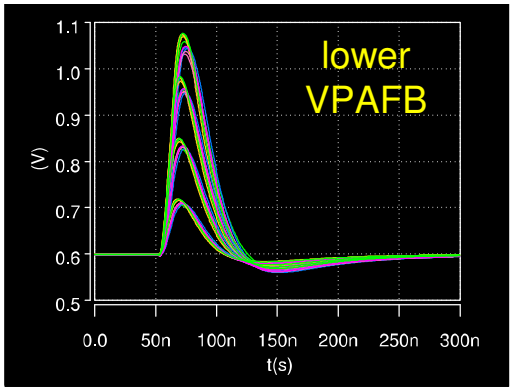
post-amp feedback resistor control

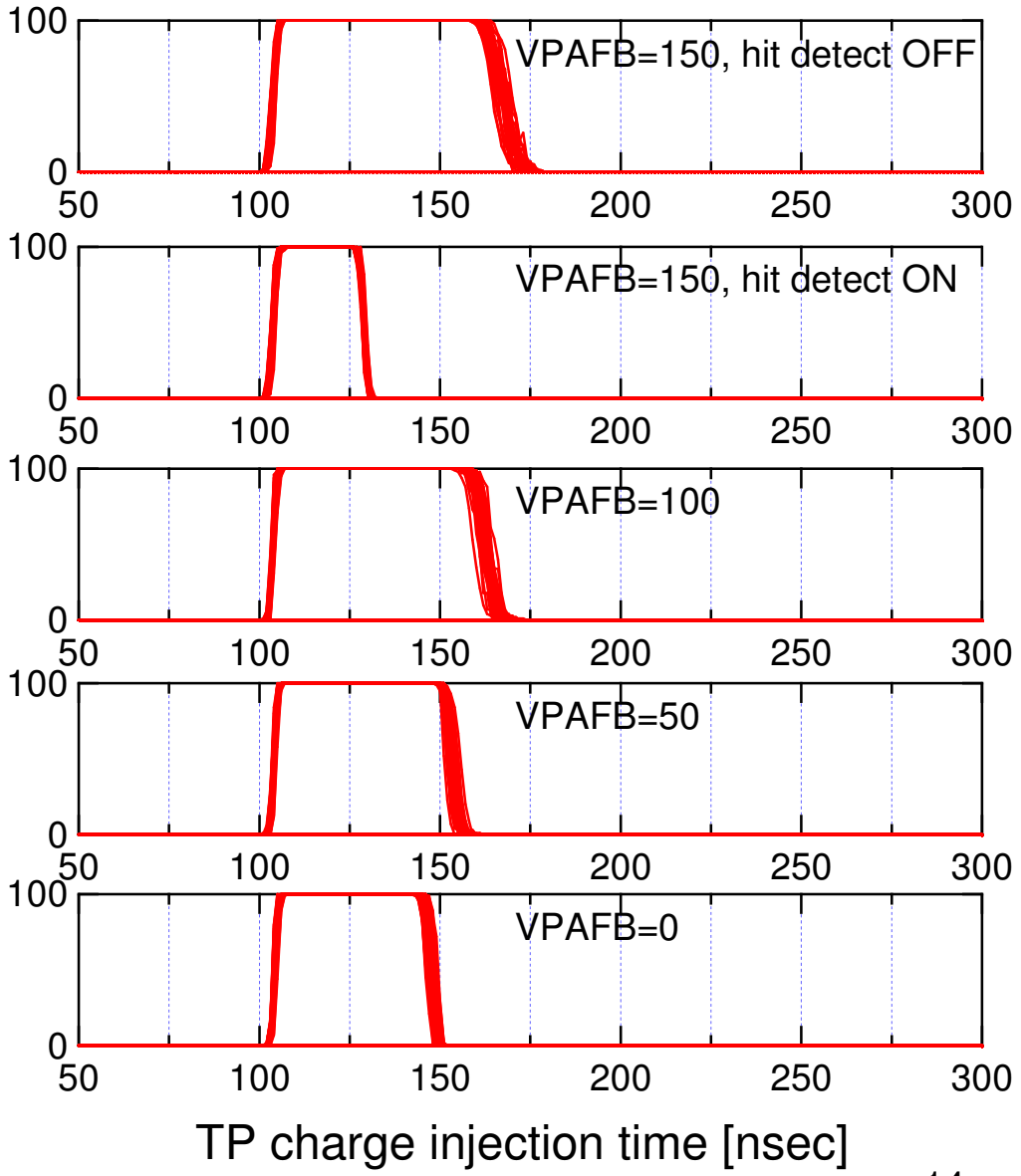
can see effect of VPAFB using test pulse sweep - smaller values give shorter pulse length

hit detect circuit works - only single hit in pipeline irrespective of how long comp O/P stays high

~ 2 fC signal
1 fC comp. thresh







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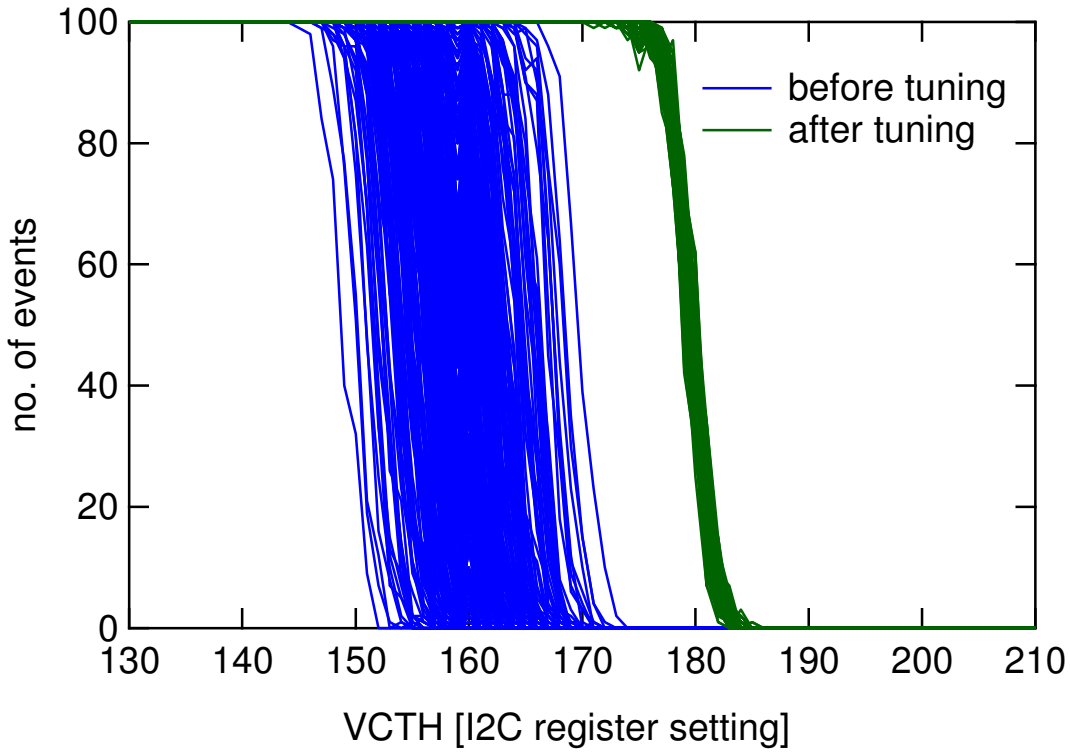
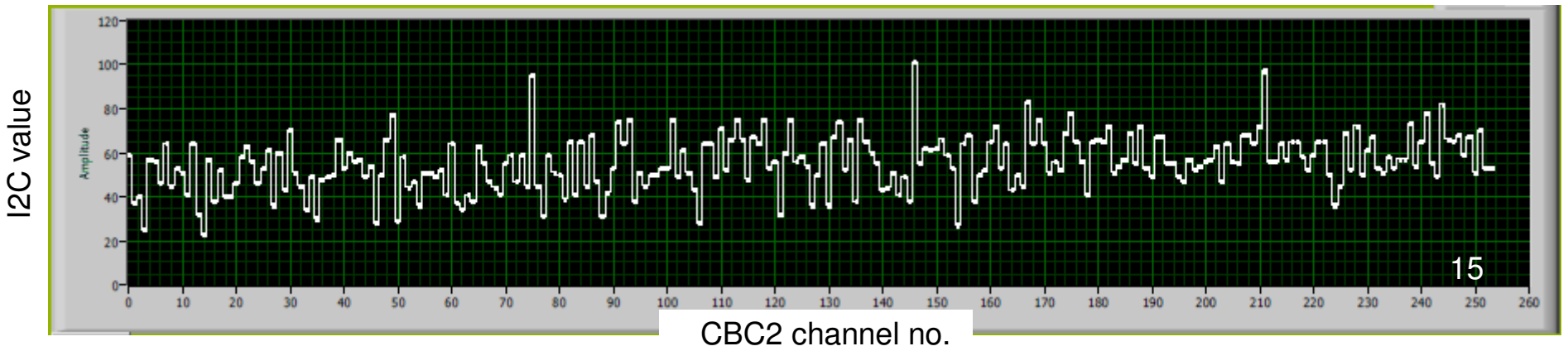
S-curves and tuning



254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to VCTH setting of 180 in this example

254 offset values after tuning



gain

sweep global comparator threshold VCTH
to get s-curves for range of test pulse amplitudes

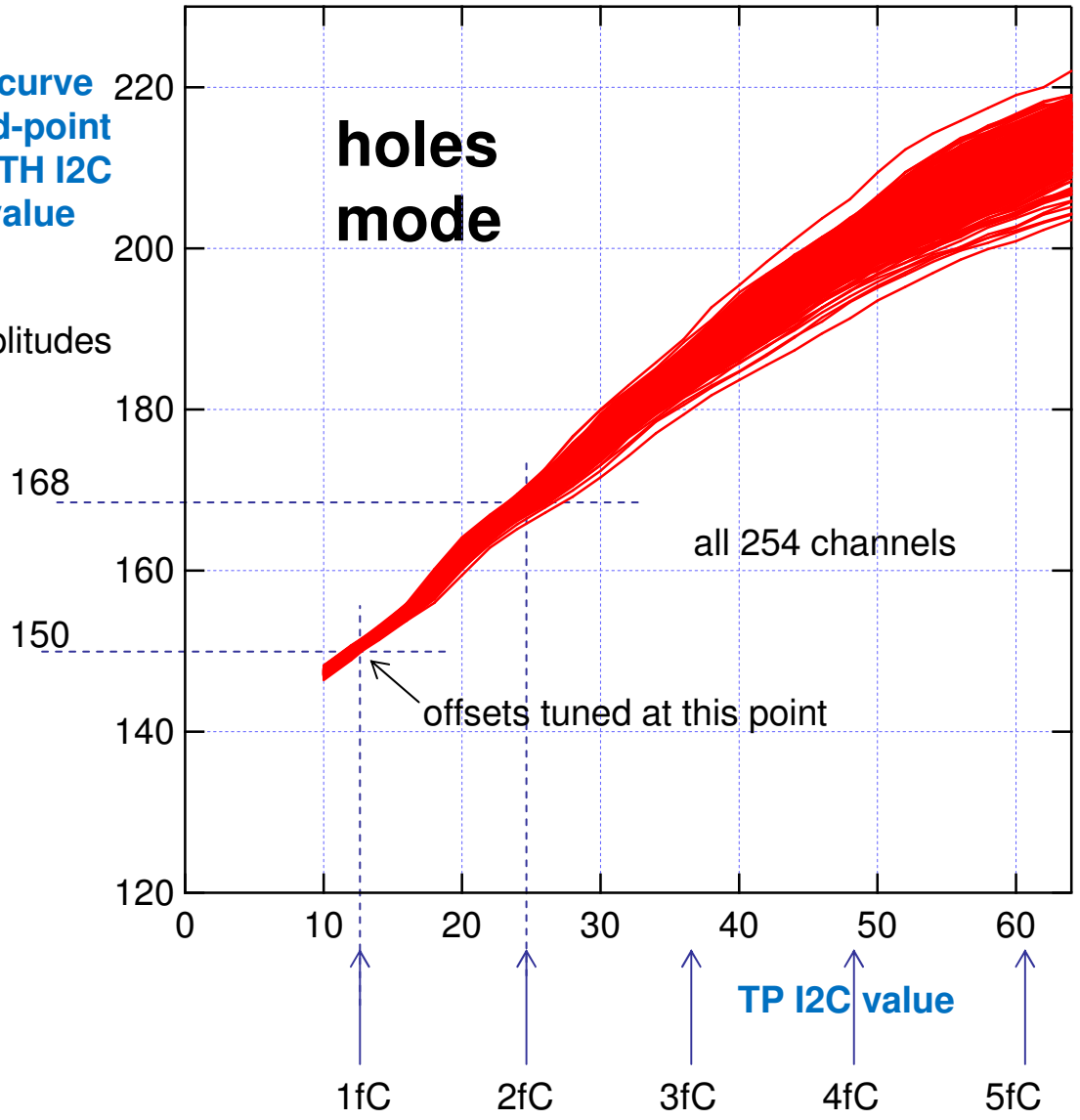
plot s-curve mid-points vs. TP amp →

rough calculation
(assumes TP value of 12 / fC)

(168 - 150) x 2.5 mV*

= 45 mV / fC

note: “wavy” nature of characteristic



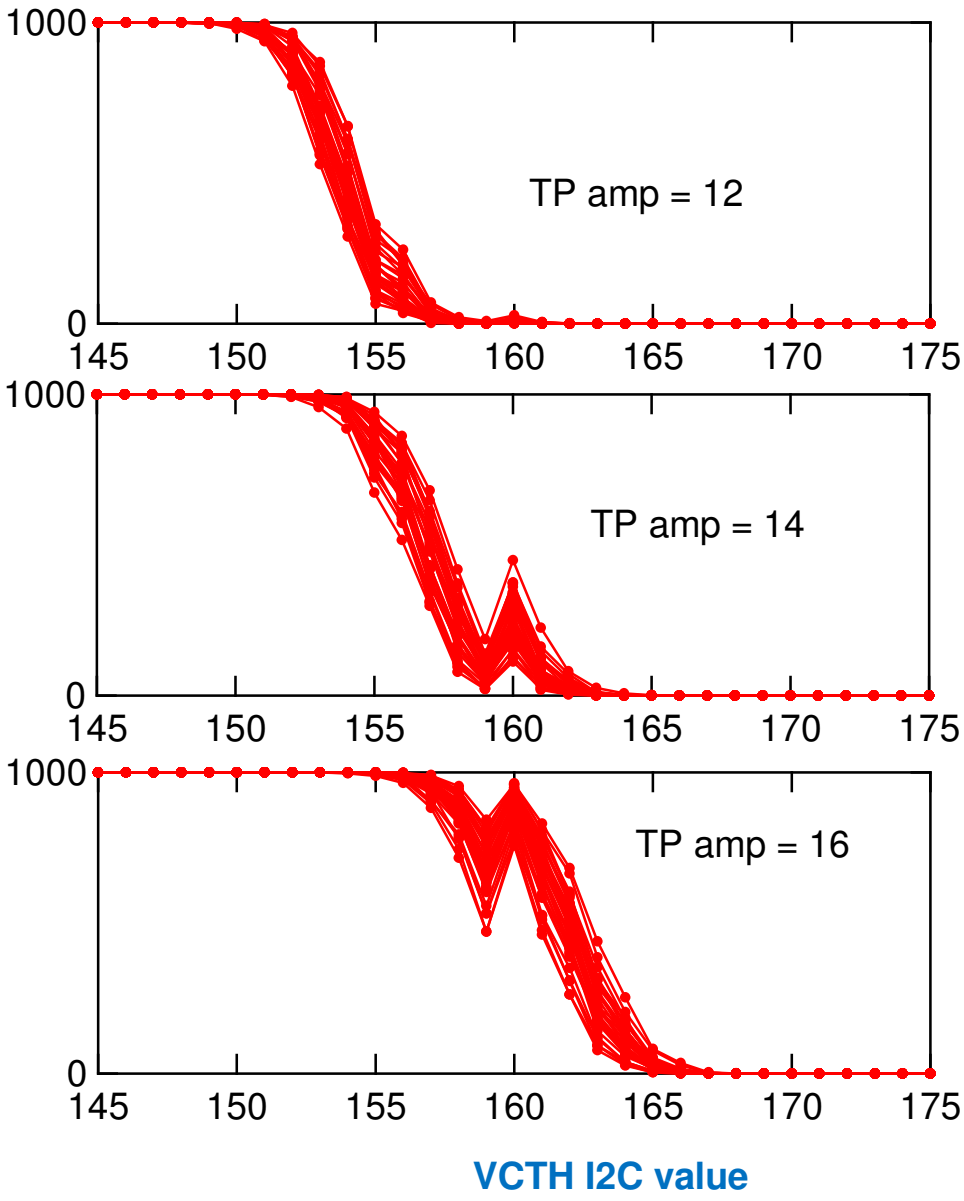
(* from VCTH bias sweep measurements - slide 9)

s-curve skew

s-curve mid-points obtained by fitting raw data with erfc function

value gets skewed by non-linearity of VCTH

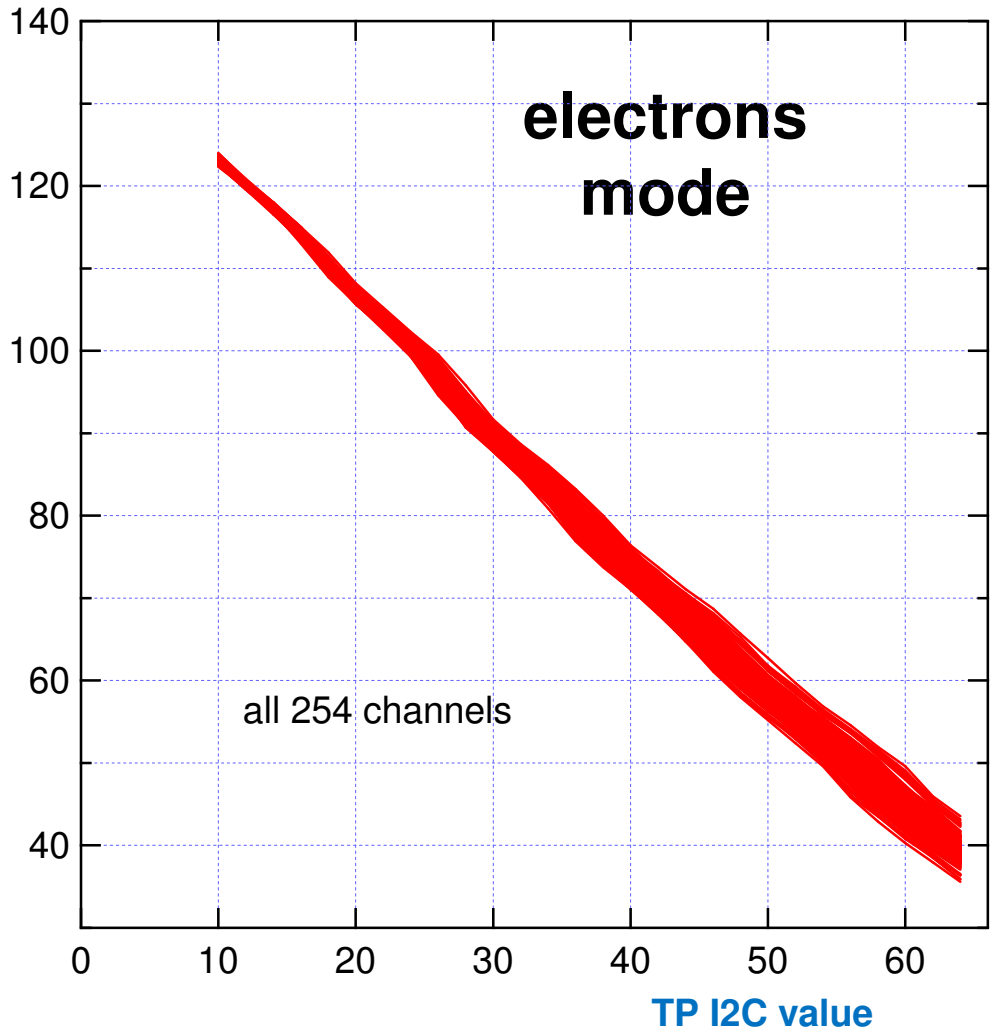
not a big problem, but worth trying to improve



gain - electrons mode

have concentrated on results in holes mode, but electrons mode ok too

all results and characteristics similar



stub logic functionality

stub finding logic

cluster width discrimination (CWD) logic

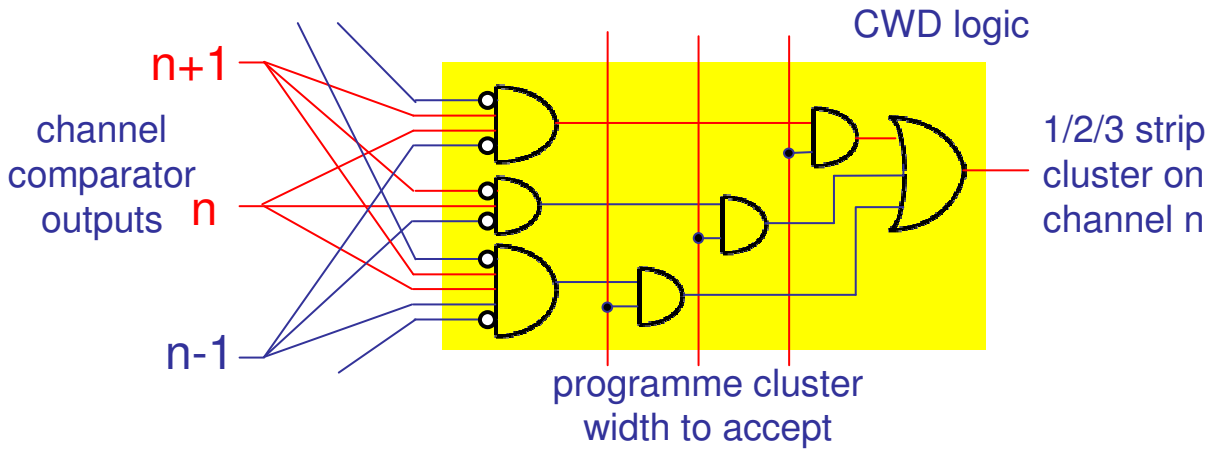
exclude clusters with hits in >3 neighbouring channels
wide clusters not consistent with high pT track

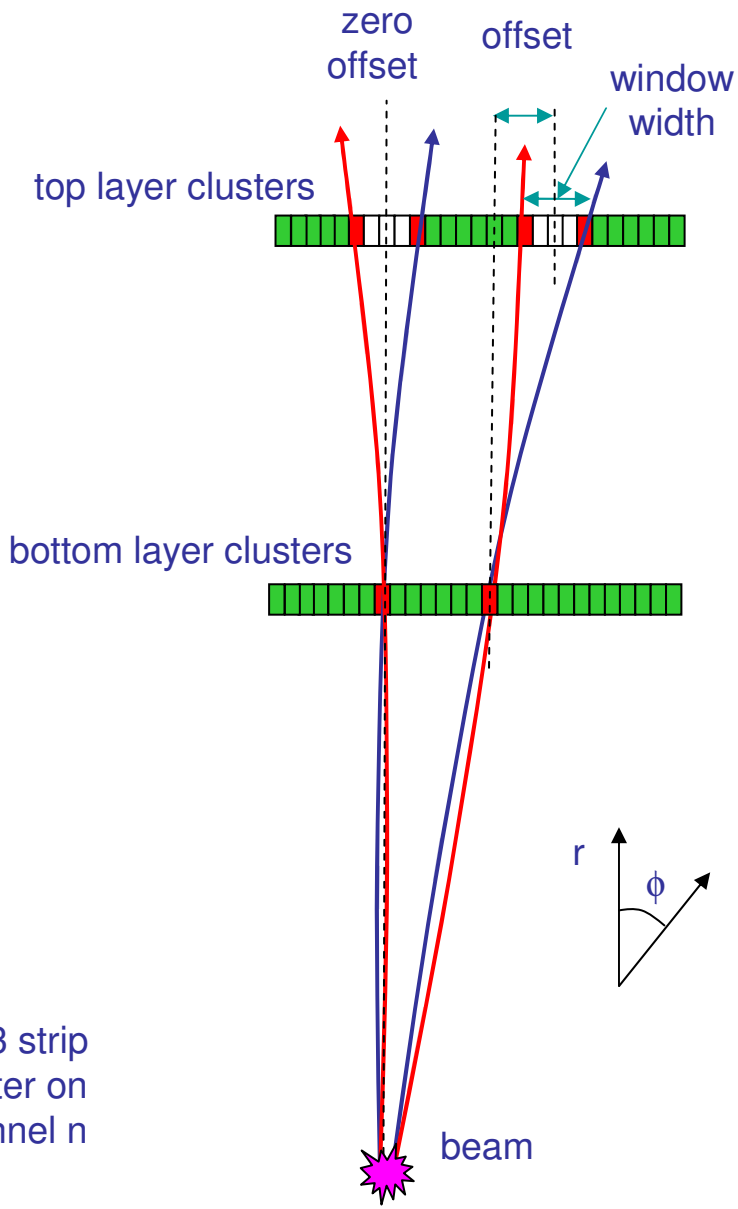
offset correction & correlation logic

for a cluster in bottom layer, look for correlating cluster occurring in window in top layer

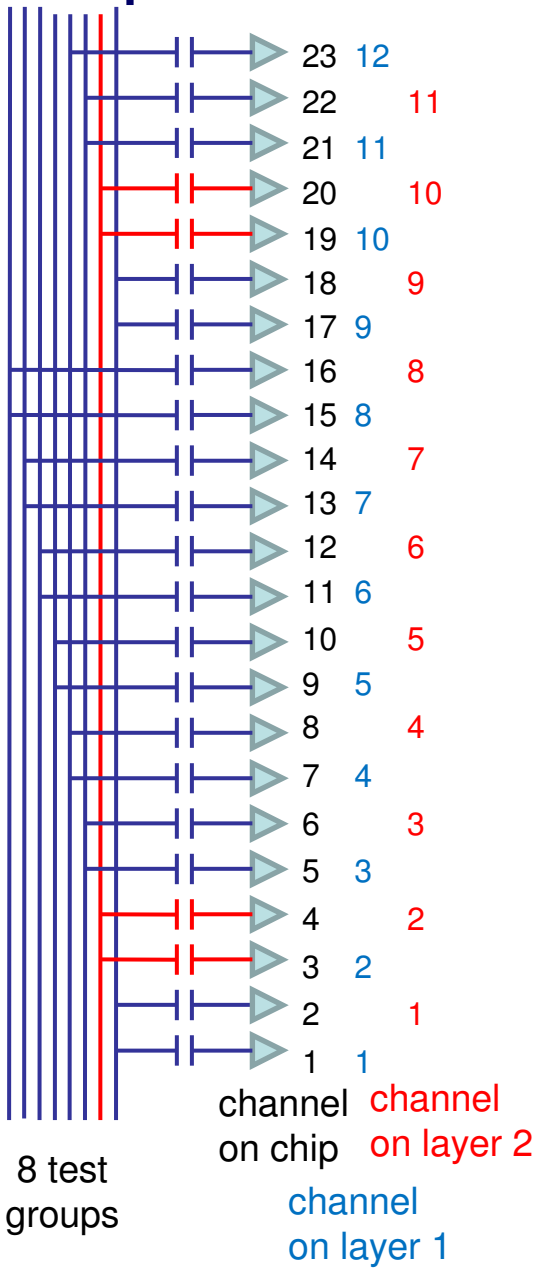
window width controls pT cut
stub found if cluster in bottom layer corresponds to cluster within window in top layer
window width programmable up to **+/- 8** channels

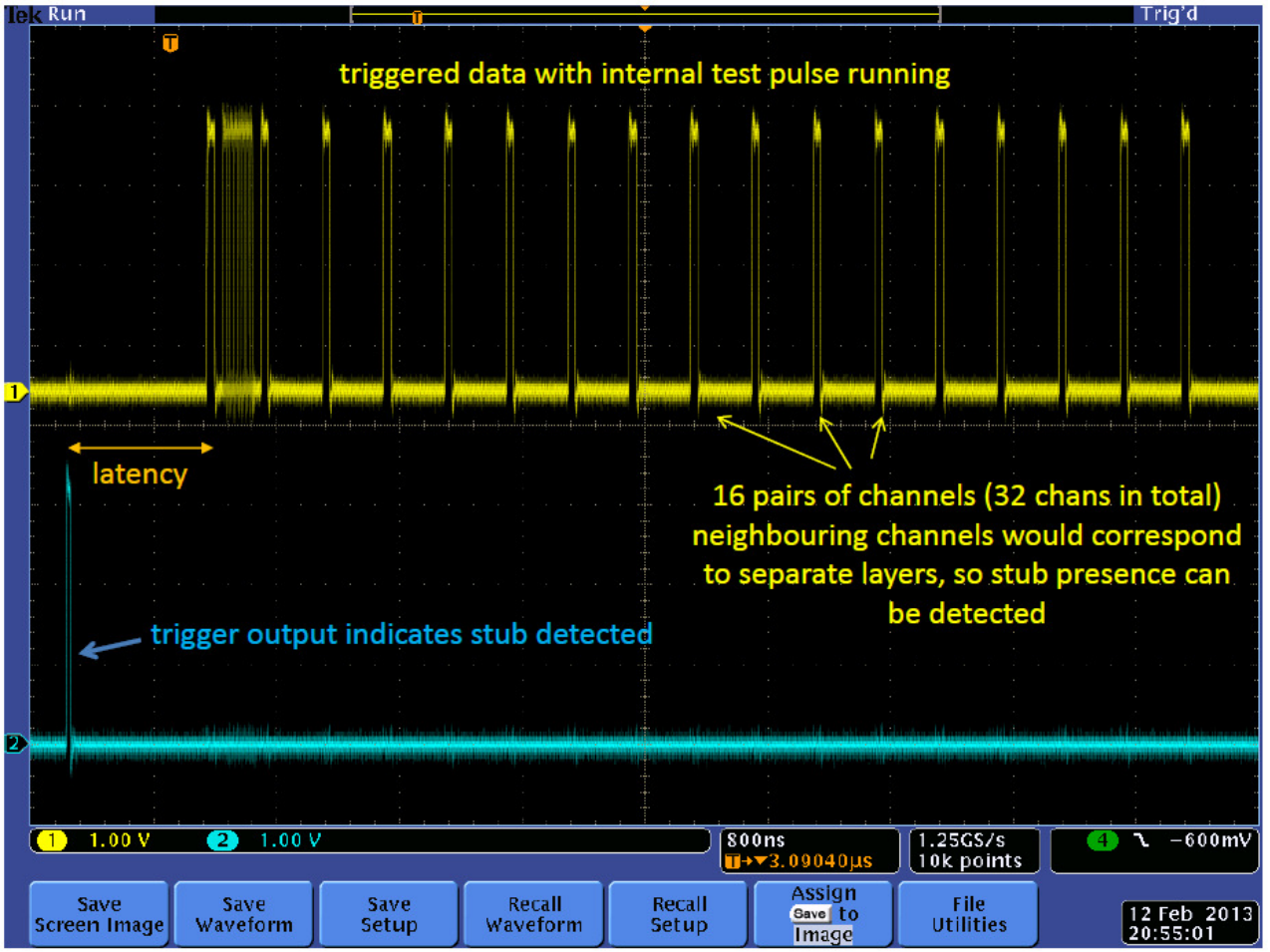
offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels





test pulse result



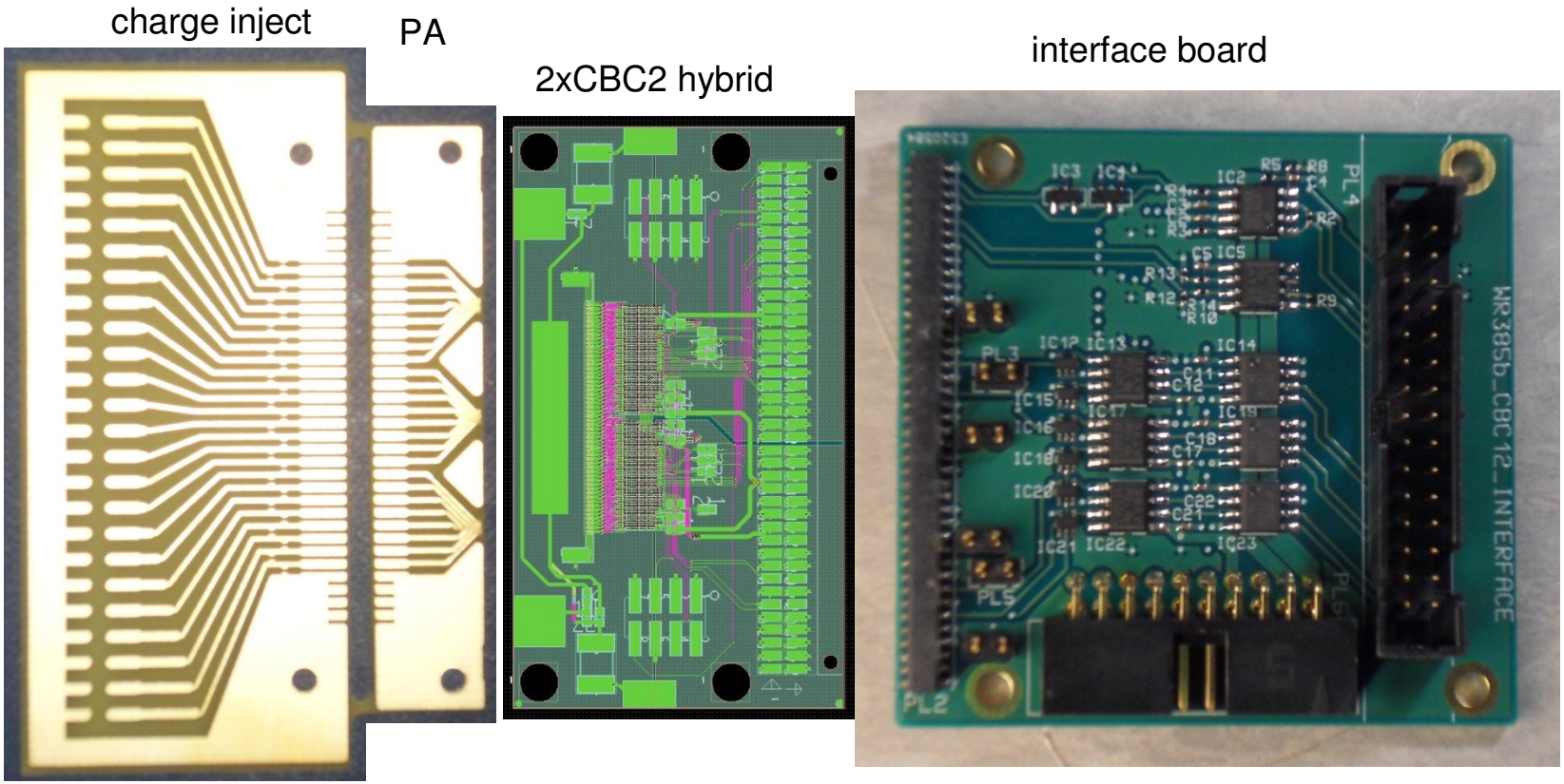


arrangement of 8 groups of test pulse connections allows to simulate signals from different layers and therefore exercise correlation logic

=> stub finding logic is working, but can't prove much with single chip and internal test pulse only

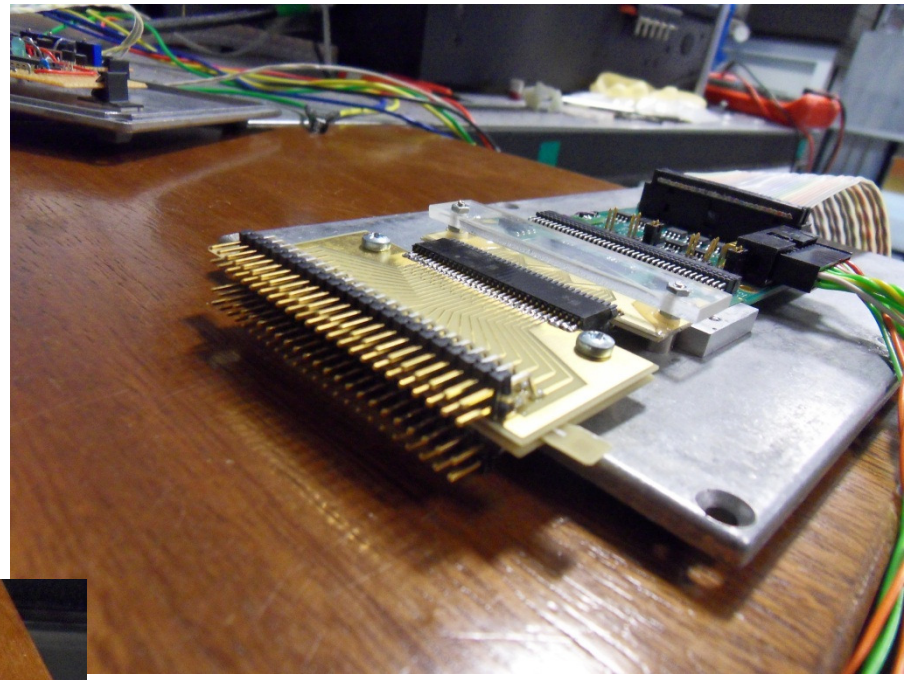
=> need 2xCBC2 hybrid

2xCBC2 hybrid test setup



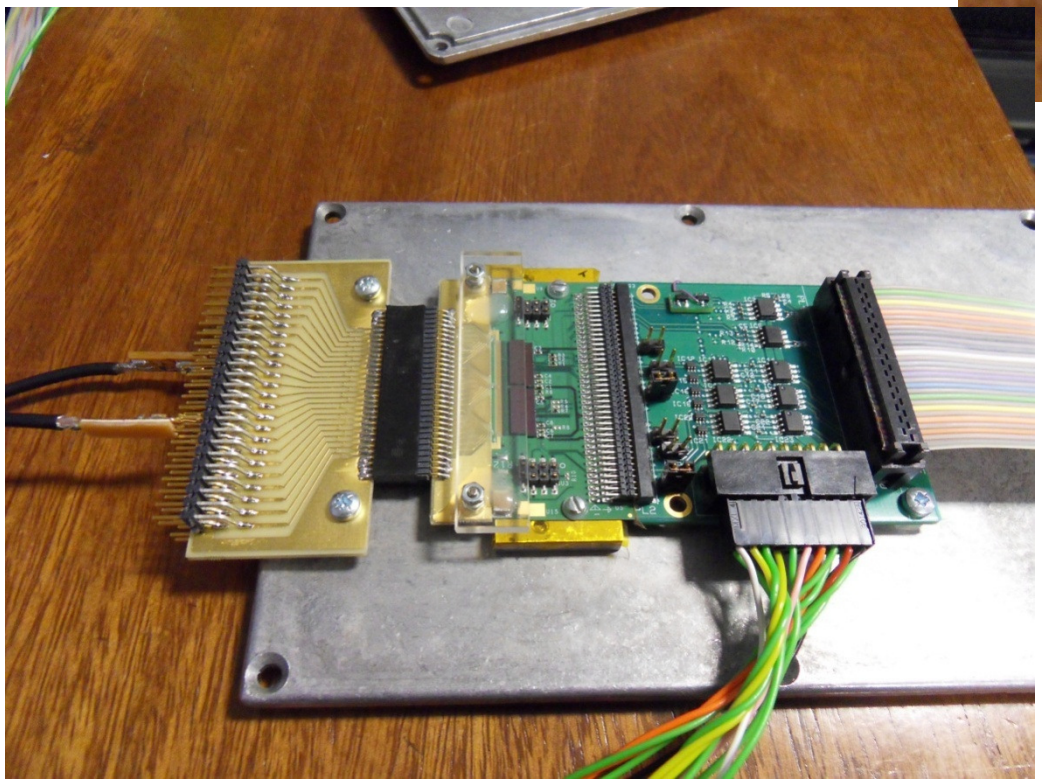
2xCBC hybrid + PA (both sides) becomes device under test
pluggable charge inject board allows different external capacitance
bonding arrangement allows to study region where signals exchanged between chips

2xCBC2 substrate test setup



wire-bonding on both sides of hybrid non-trivial

needs dedicated jigs to provide as much support as possible

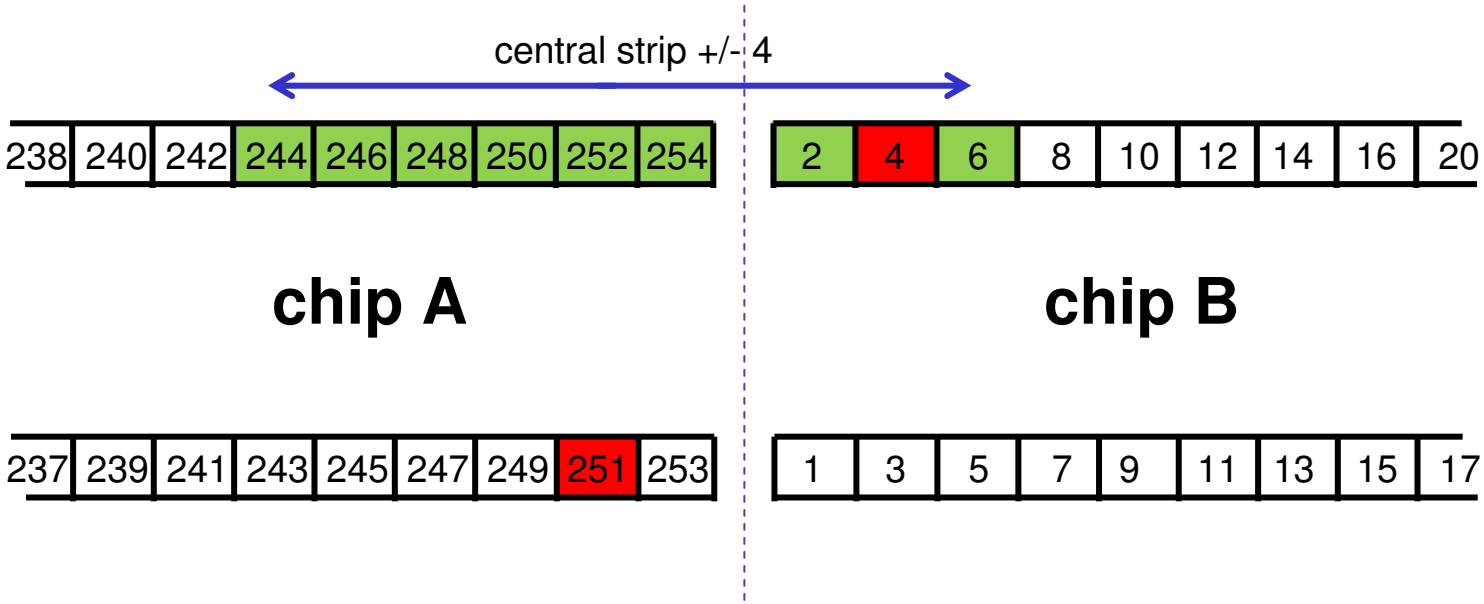


can now inject signals in both sensor layers electrically

with accurately known values of test charge

setup only recently available - so far have only had time to verify all wire-bonded channels working and basic functionality

looking at inter-chip region



2xCBC2 hybrid allows to verify correct transfer of CWD output signals between chips

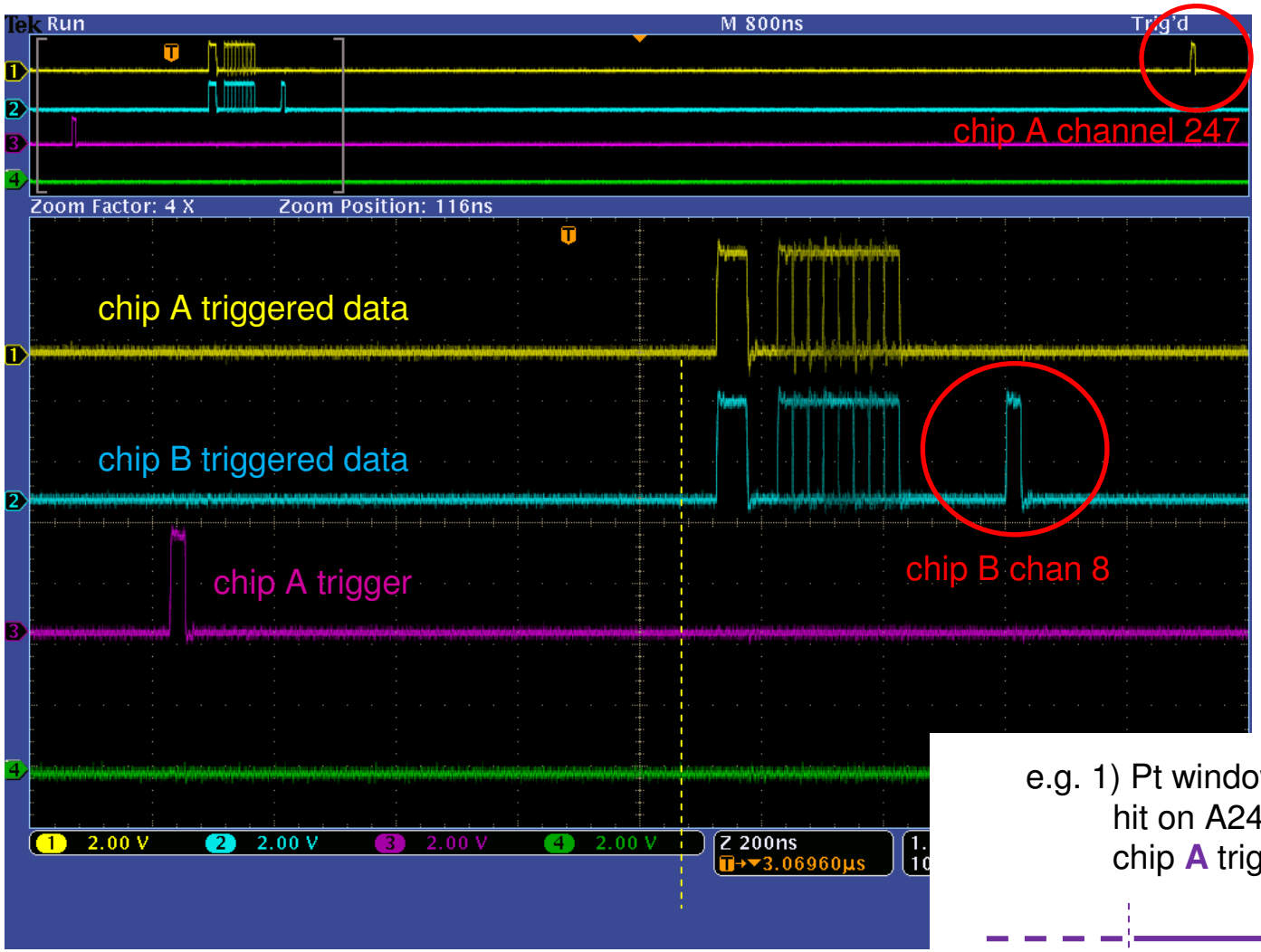
above example

- cluster in chan 251 in lower layer chip A
- cluster in chan 4 in upper layer chip B
- window width set at central strip +/- 4

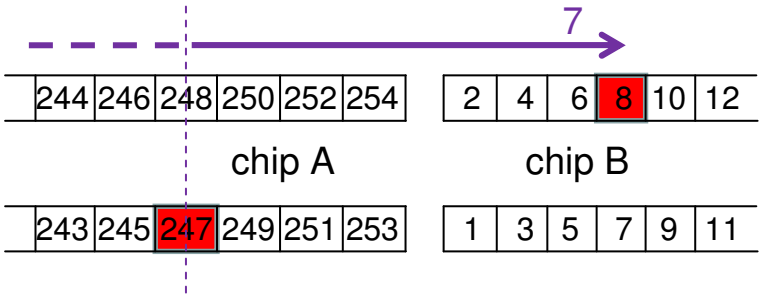
so above example will produce a positive correlation and a trigger from chip A

example 1

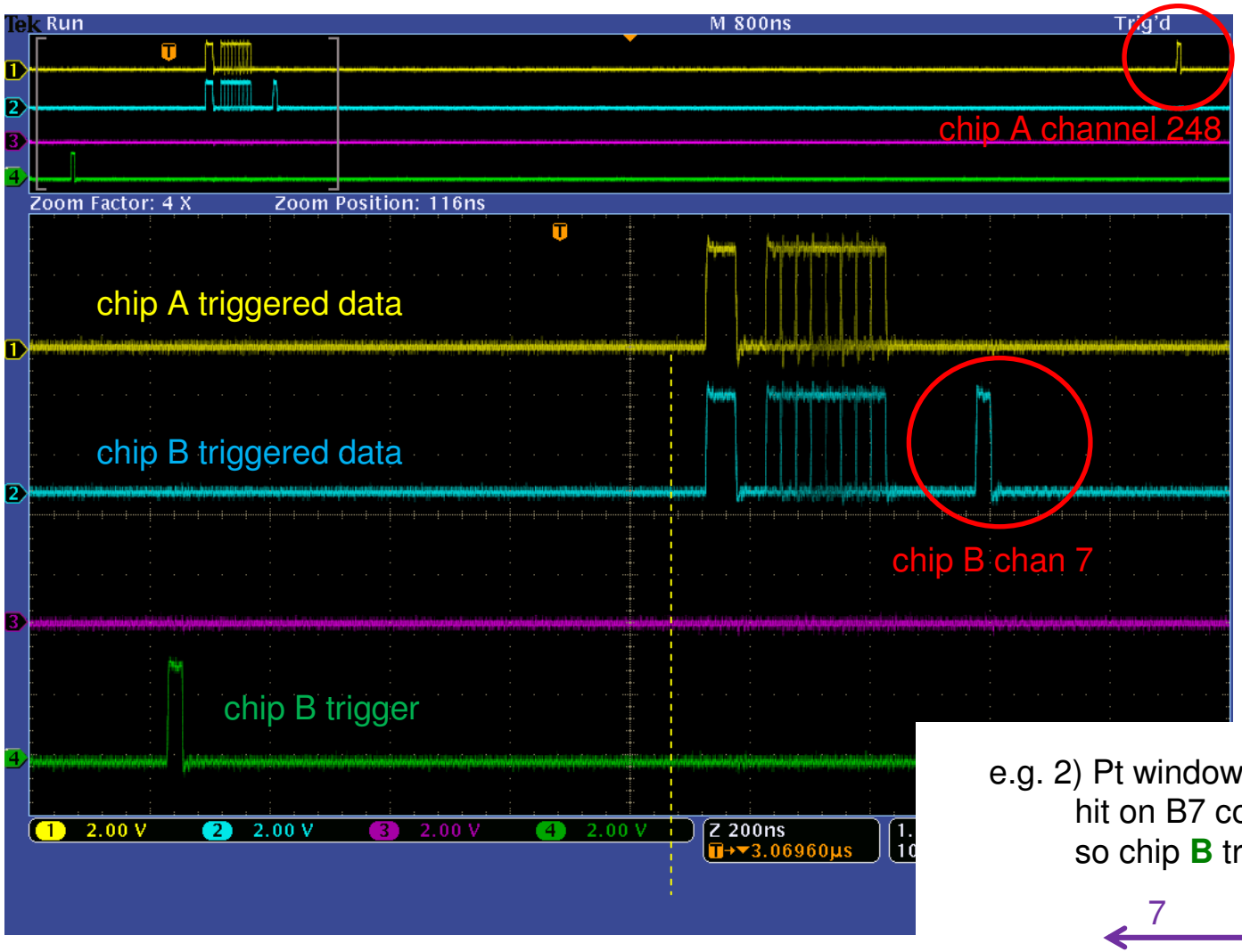
(from 2xCBC2 hybrid with external charge injection)



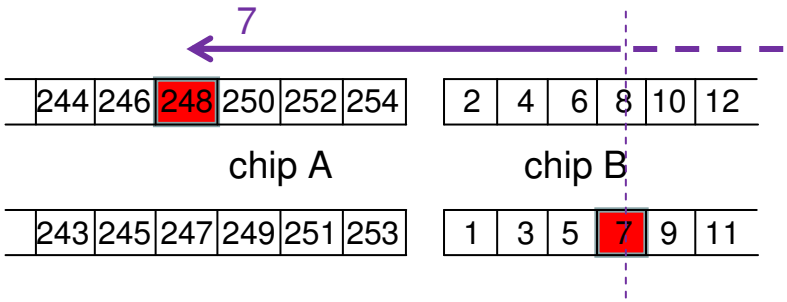
e.g. 1) Pt window width +/- 7
hit on A247 correlates with B8
chip **A** trigger output active



example 2

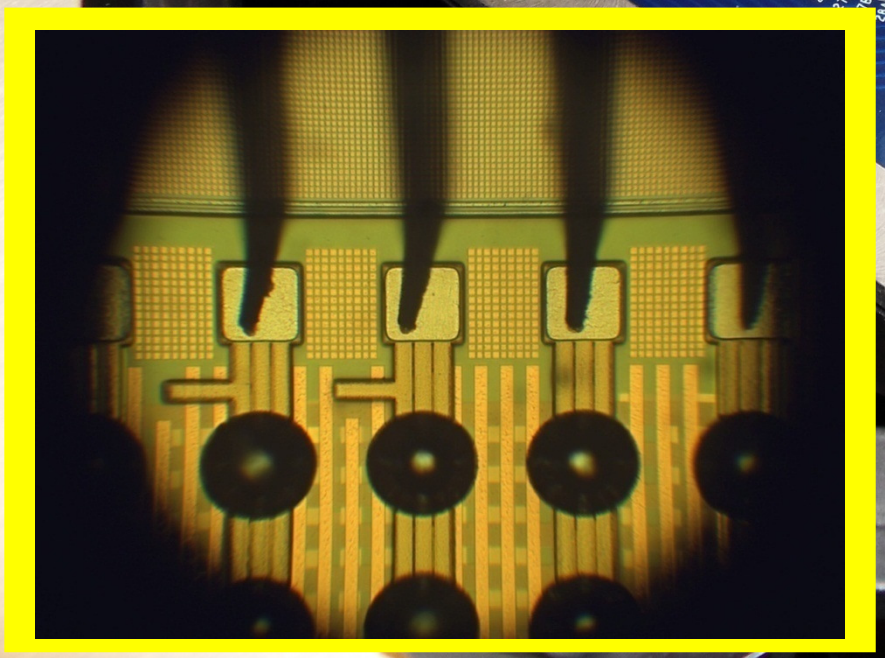


e.g. 2) Pt window width still +/- 7
hit on B7 correlates with A248
so chip **B** trigger output active



wafer test

first wafer probed manually



wafer test procedure

chip clocked at 40MHz
I2C parameters downloaded

not an exhaustive test - but enough to differentiate bump-bond assembly problems from chip problems

power consumption recorded

power consumption dependence on I2C value for some bias currents swept

check all channels respond to test pulse

final yield for 1st wafer

112 reticles
108 good chips
4 bad chips

bad chips due solely to physical damage from probe card

bad chip

CBC2

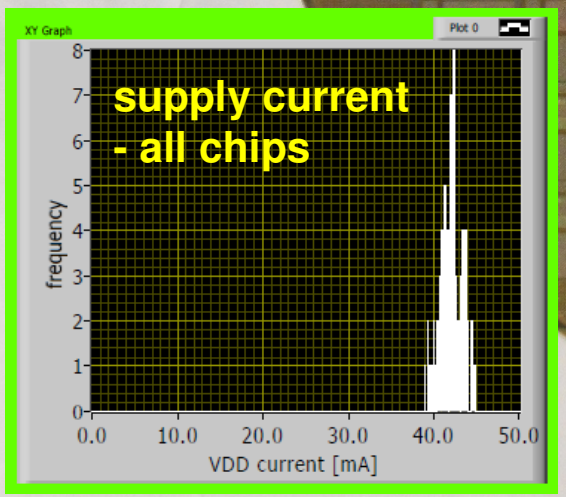
reticle

no defective channel found on any of 112 chips tested on this first wafer

=> 100% yield

perhaps not too surprising if overall wafer yield high

CBC2 is relatively small area of reticle & significant fraction of CBC2 area not occupied by active circuitry



summary & plans

- now clear that CBC2 working well enough to allow module development to progress

  front end performance similar to CBC1, bugs fixed
  stub finding logic functioning
  power features: LDO and switched capacitor DC-DC circuits operational

- short term plans

  for wire-bonded chip setup

    will use to refine wafer probe procedure
      plan to probe remaining 7 C4 wafers soon (depending on requirements)
      likely high yield => ~750 more chips

    could also be useful for ionising radiation studies using X-rays

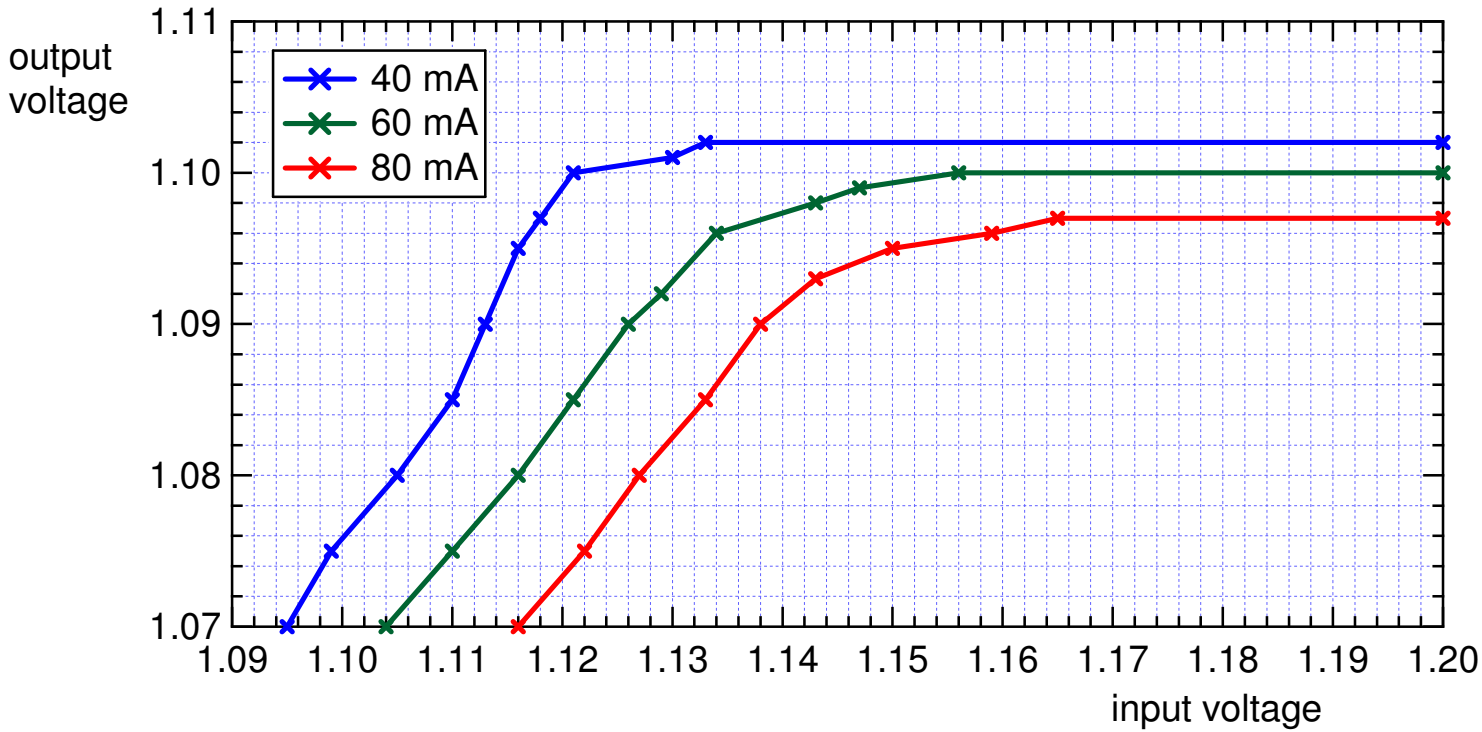
- longer term

  in-depth chip characterisation studies better suited to 2xCBC2 hybrid
    electrical test setup now available

  mini-pT module studies
    2xCBC2 hybrid + sensors

extra

LDO performance



LDO

load currents 40, 60, 80 mA
dropouts ~ 30, 55, 70 mV (approx.)
DC shift due to series resistance
50 mOhm on-chip + wire-bond resistance (which will go away when bump-bonded)

other power related measurements

measured band-gap voltage: 0.604 (for this chip)
quiescent power consumption from VDDD
all bias currents set to zero, SLVS off ~4.4mA
all bias currents set to zero, SLVS ON ~6.7mA

pulse length vs. amplitude

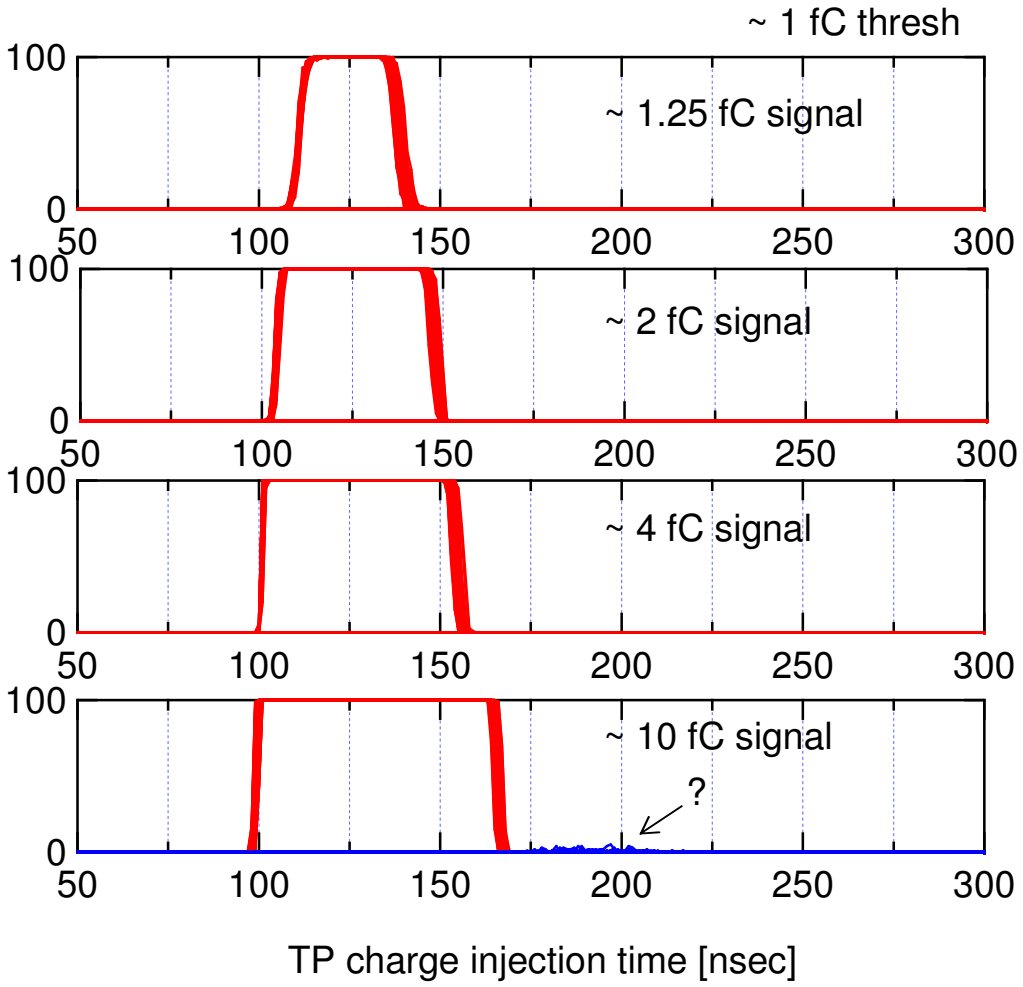
ideally (to address dead-time issue) want comparator high for less than 50 ns

not case for signals > ~ 2 fC

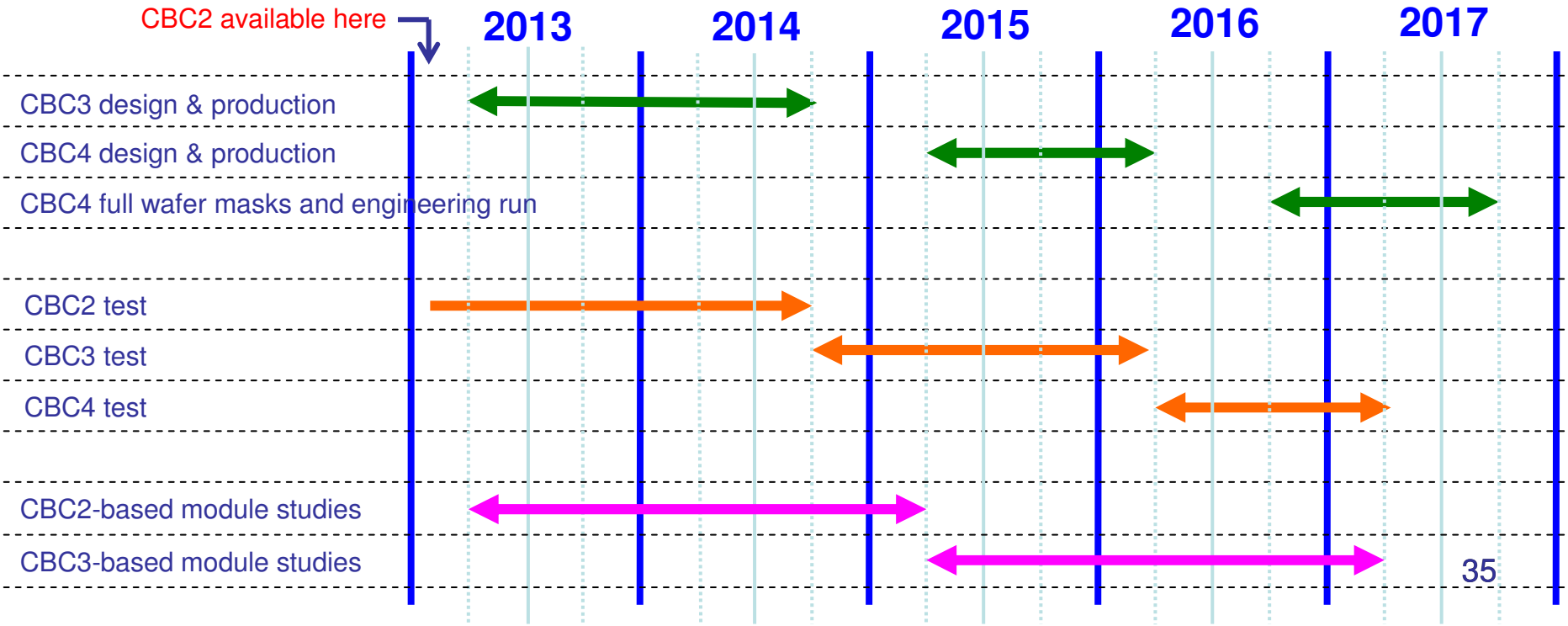
=> can study dead-time vs. pulse length using CBC2 but postamp feedback FET will probably need tweaking for CBC3

note: all plots contain 254 channels data
10 fC plot shows activity in channels not being driven by test pulse

crosstalk? power supply disturbance?



future plans



CBC2 (and modules based on CBC2) will dominate test activity over next ~ 2 years

next prototype, **CBC3**, should be very close to final chip – available towards end 2014

incorporate functionality to generate and transmit stub addresses

… new features

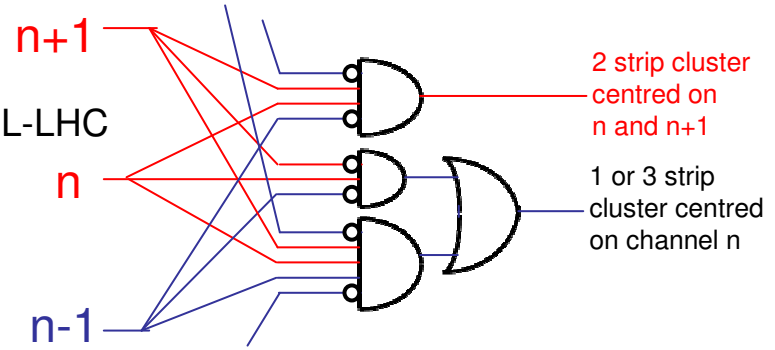
CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017

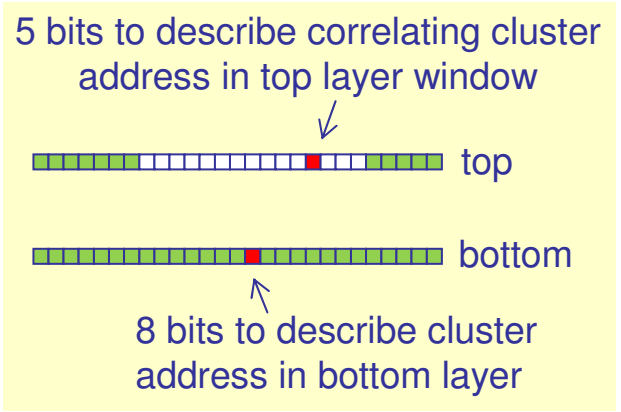
~ 5 years assumed for large scale production, module construction, integration, commissioning, …

CBC3 - the “final prototype”

next version of chip should incorporate all features required for HL-LHC

- **final choices for front end**
  - ½ strip cluster resolution
    - 2 strip cluster position assigned to mid-point
- **stub data definition**
  - 8 bits address (for ½ strip resolution) of cluster in bottom layer
  - 5 bit bend information
    - address of correlating cluster in top layer
- **stub data formatting & transmission to concentrator**
  - 13 bit / stub, up to 3 stubs/BX => 39 bits
  - +1 bit unsparsified L1 triggered readout data
  - => 40 bits / 25 nsec
    - e.g. 10 lines at 160 Mbps (per chip)
- **other useful features**
  - e.g. slow ADC to monitor bias levels
  - …

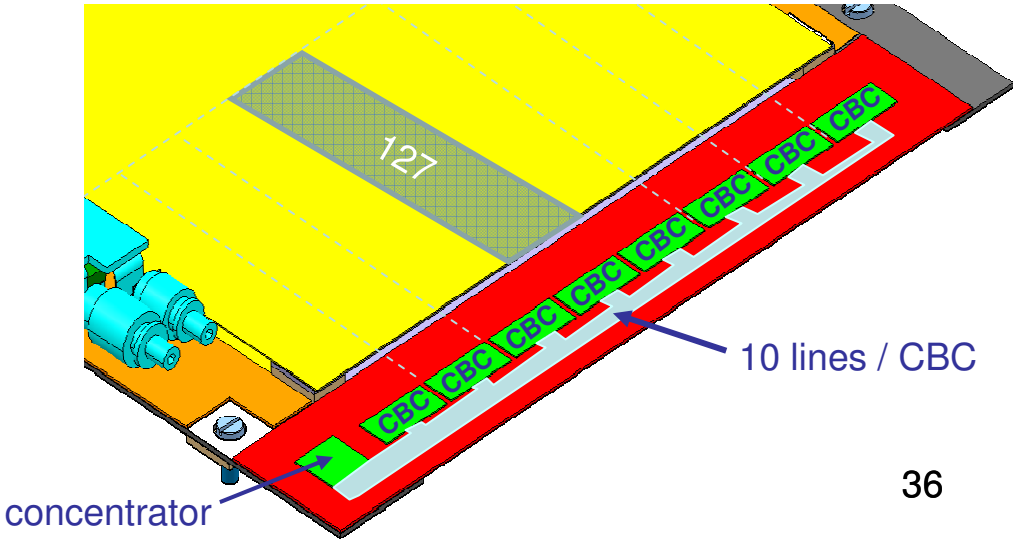




CBC data to concentrator

25 ns

S1	S1	S1	S1	S1	S1	S1	S1	B1	B1
B1	B1	B1	S2	S2	S2	S2	S2	S2	S2
S2	B2	B2	B2	B2	B2	S3	S3	S3	S3
S3	S3	S3	S3	B3	B3	B3	B3	B3	**R**



neighbour chip signals - comparator O/Ps

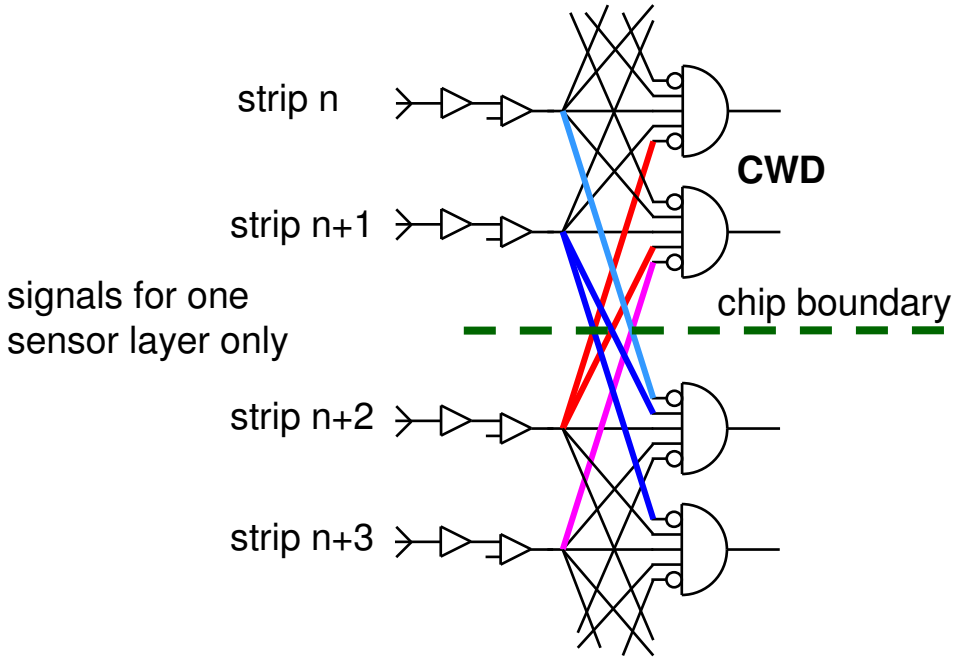
need to transfer signals across chip boundaries

for cluster width < 3 need (for each sensor layer)

to pass comp. O/Ps from 2 edge channels to neighbour
to receive comp. O/Ps from 2 edge channels on neighbour

=> 4 signals for single sensor layer

=> 8 signals for both layers



neighbour chip signals - CWD O/Ps

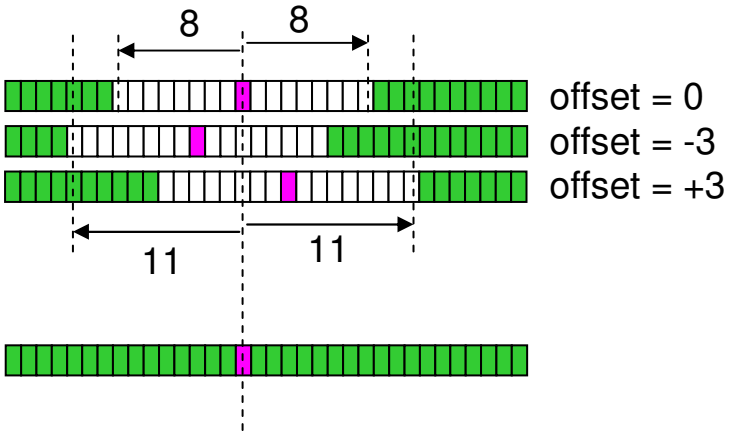
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

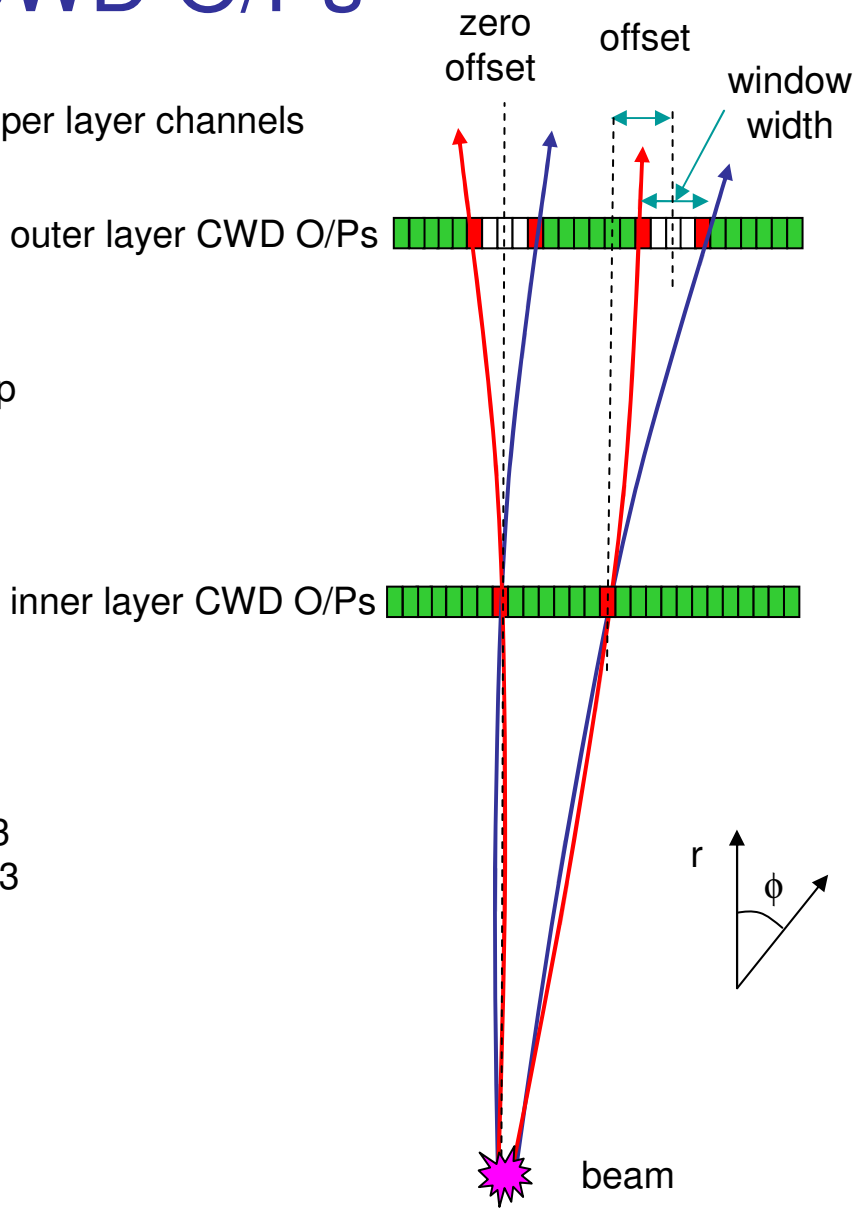
window defines Pt cut
width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
11 to receive from neighbouring chip

= 22 signals





adding comp O/Ps -> 30 signals altogether, top and bottom of chip

CBC1

features

- designed for short strips, 2.5 – 5cm, < ~ 10 pF
- full size prototype - 128 channels
  - 50 μm pitch wirebond
- binary un-sparsified **triggered** readout only
- powering test features
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analog FE

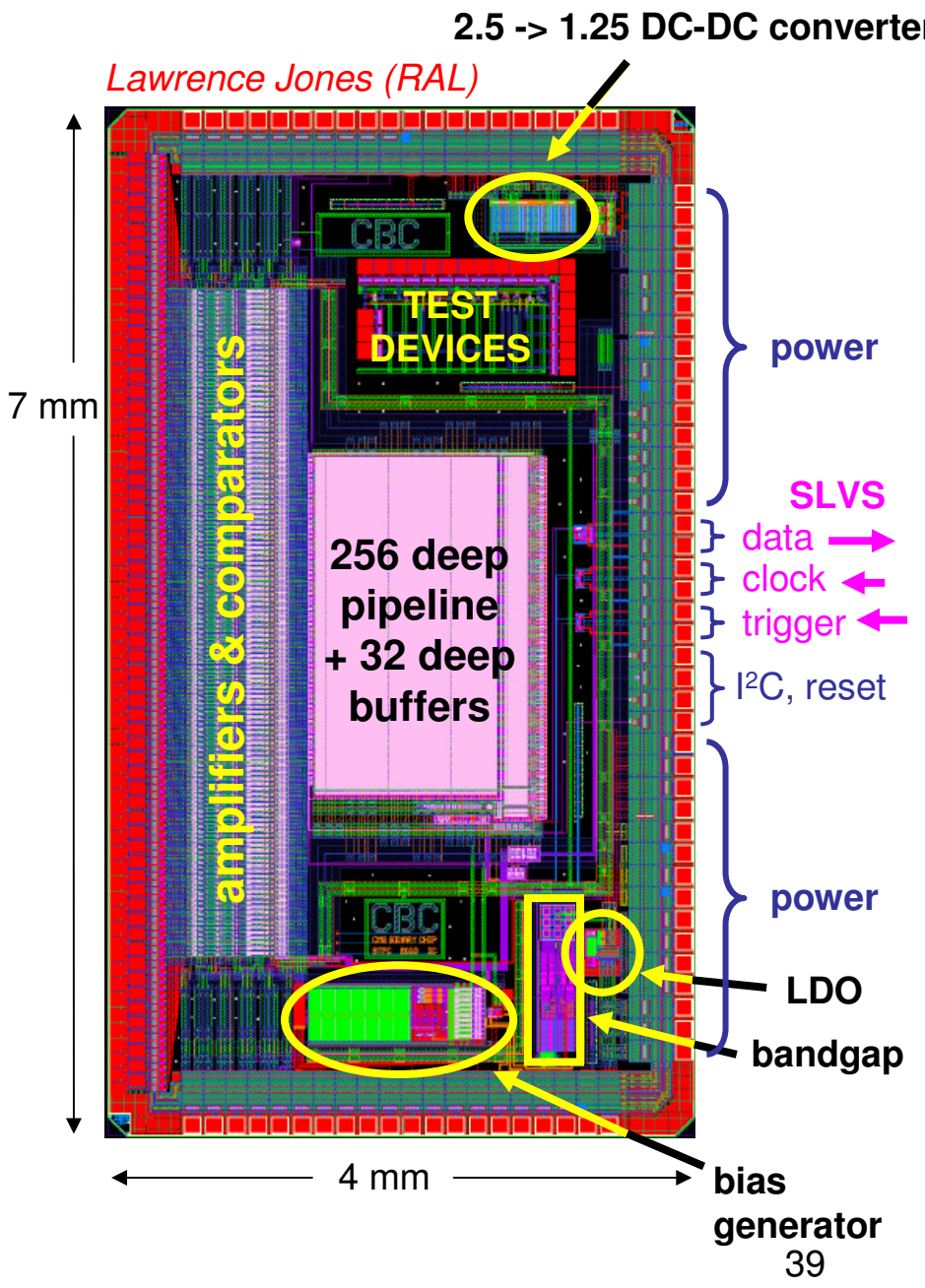
main functional blocks

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- fast (SLVS) and slow (I2C) control interfaces

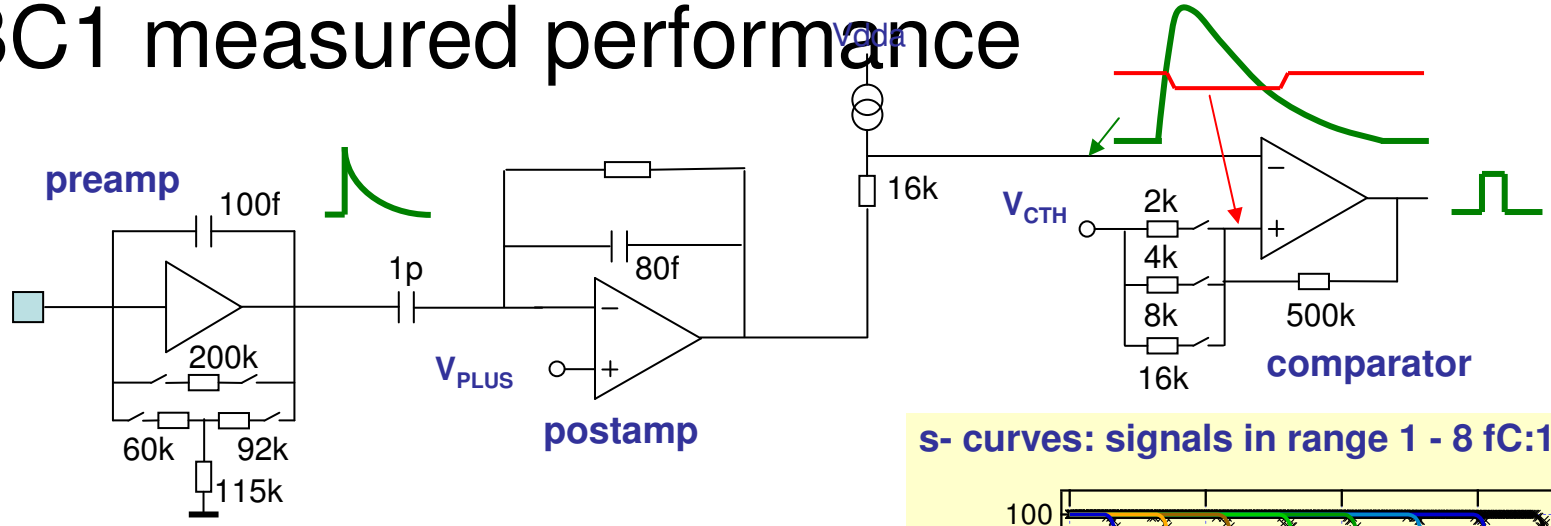
some target specs

- both signal polarities
- DC coupled to sensor – up to 1 uA leakage
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  - < 0.5 mW/channel for C_{SENSOR} ~ 5 pF

first chips received Feb. 2011



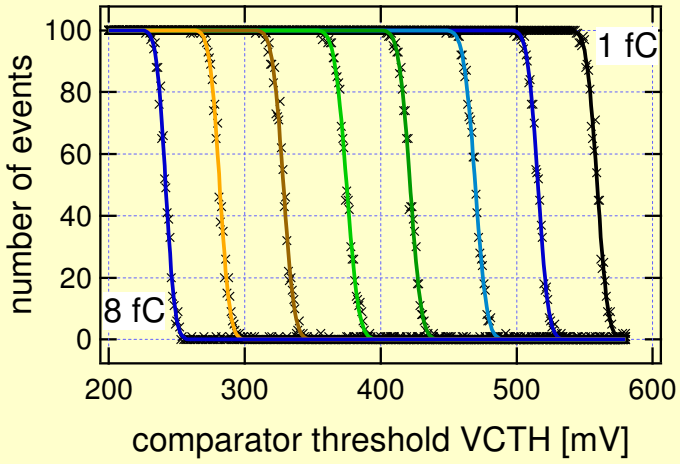
CBC1 measured performance



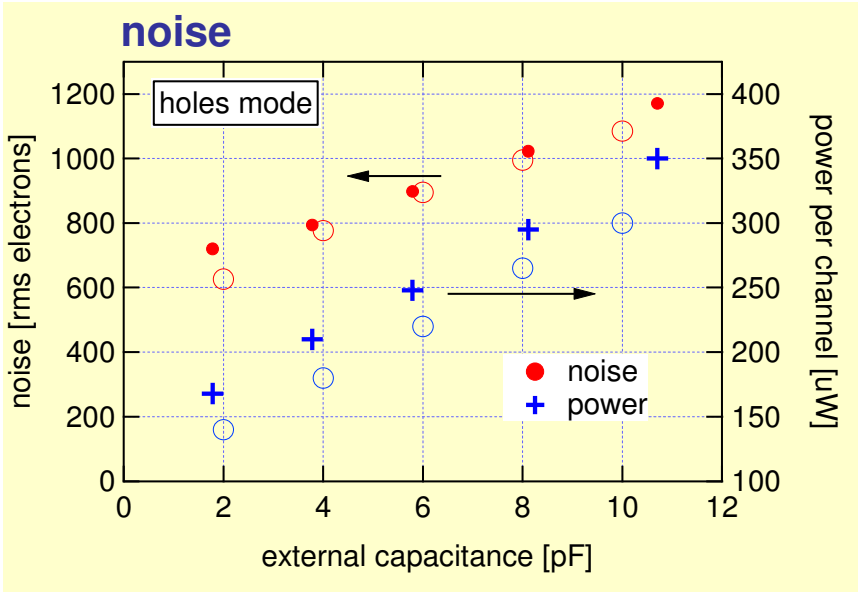
preamp: leakage tolerance 1µA verified, both polarities

postamp: gain: ~ 50 mV / fC

s- curves: signals in range 1 - 8 fC:1 fC steps



noise



noise dependence on external C

vary current in input device

=> pulse shape independent of C

e.g. for C_{SENSOR} ~ 8 pF (~ 5 cm strips)

~ **1000e** achievable for

~ **350 uW** tot. power/chan. (incl.digital)

CBC1 comparator

thresholds

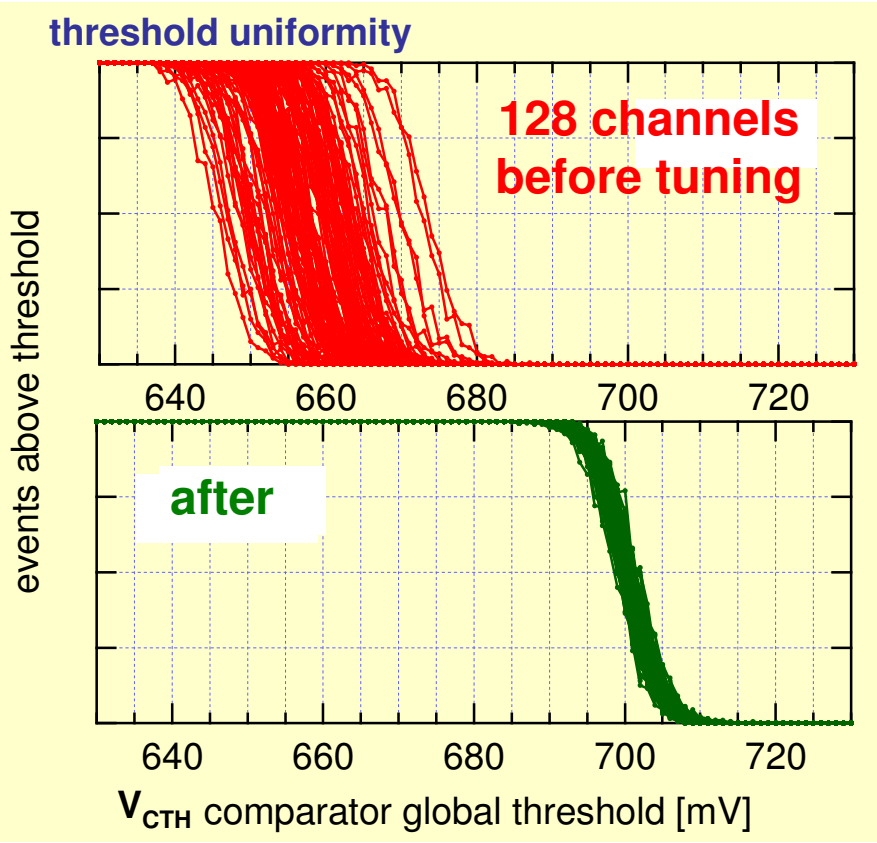
before tuning pk-pk threshold spread ~30 mV (~ 0.6 fC)

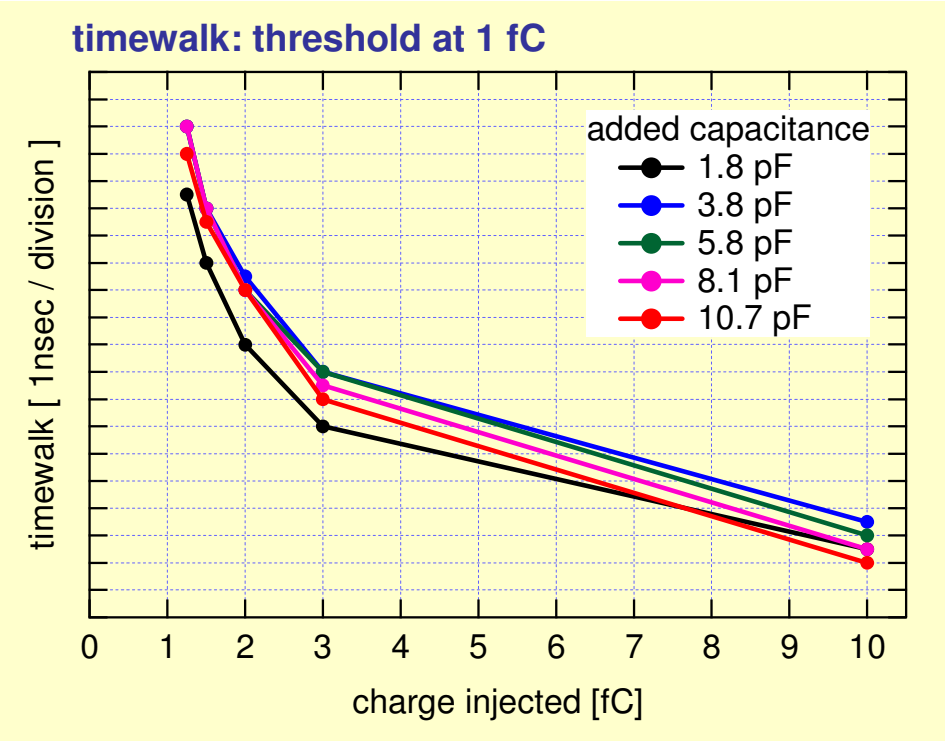
tuning reduces spread to ~ mV level

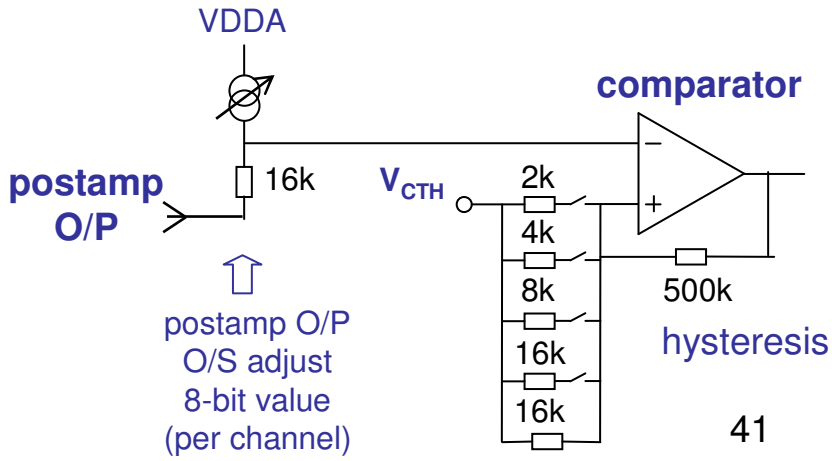
timewalk

timewalk spec.: < 16 ns between 1.25 and 10 fC signals, with comp. threshold set to 1 fC

measurements just within spec.







CBC1 power features

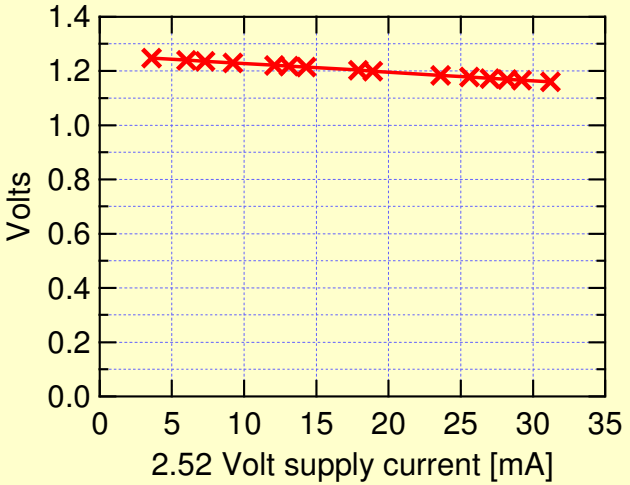
DC-DC switched capacitor converter (CERN)

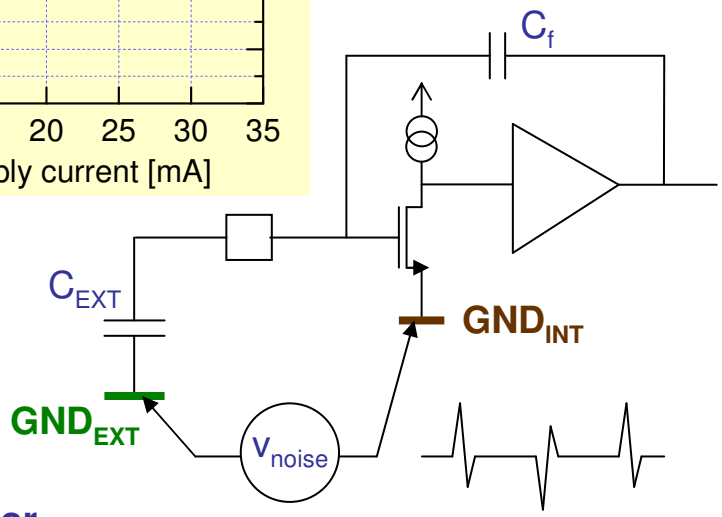
converts 2.5 -> ~ 1.2
works well: ~ 90% efficiency

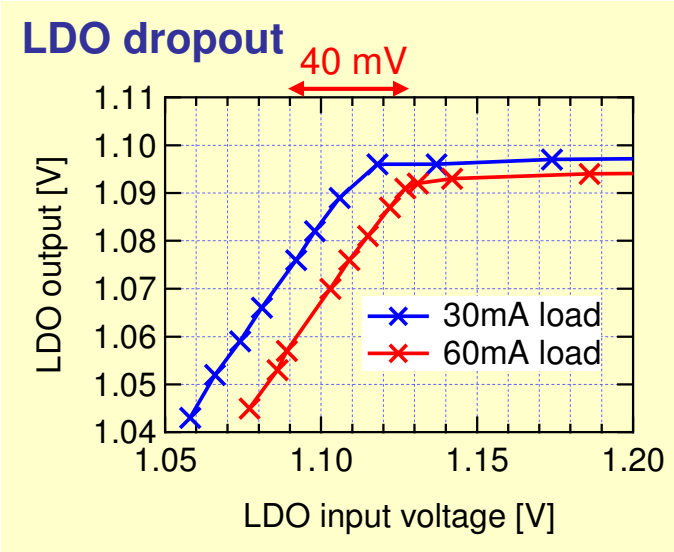
but switch noise produces difference between internal and external grounds

=> interference depending on C_{EXT}

improved circuit on CBC2, and bump-bonding should help







LDO linear regulator

provides clean, regulated rail to analog FE
(uses CERN 130 nm bandgap)

~ 1.2 Vin, 1.1 Vout

dropout ~ 40 mV for 60 mA load

provides > 30dB supply rejection up to 10 MHz