CBC3 specifications

now in middle of CBC3 design phase

specifications agreed and document available here:

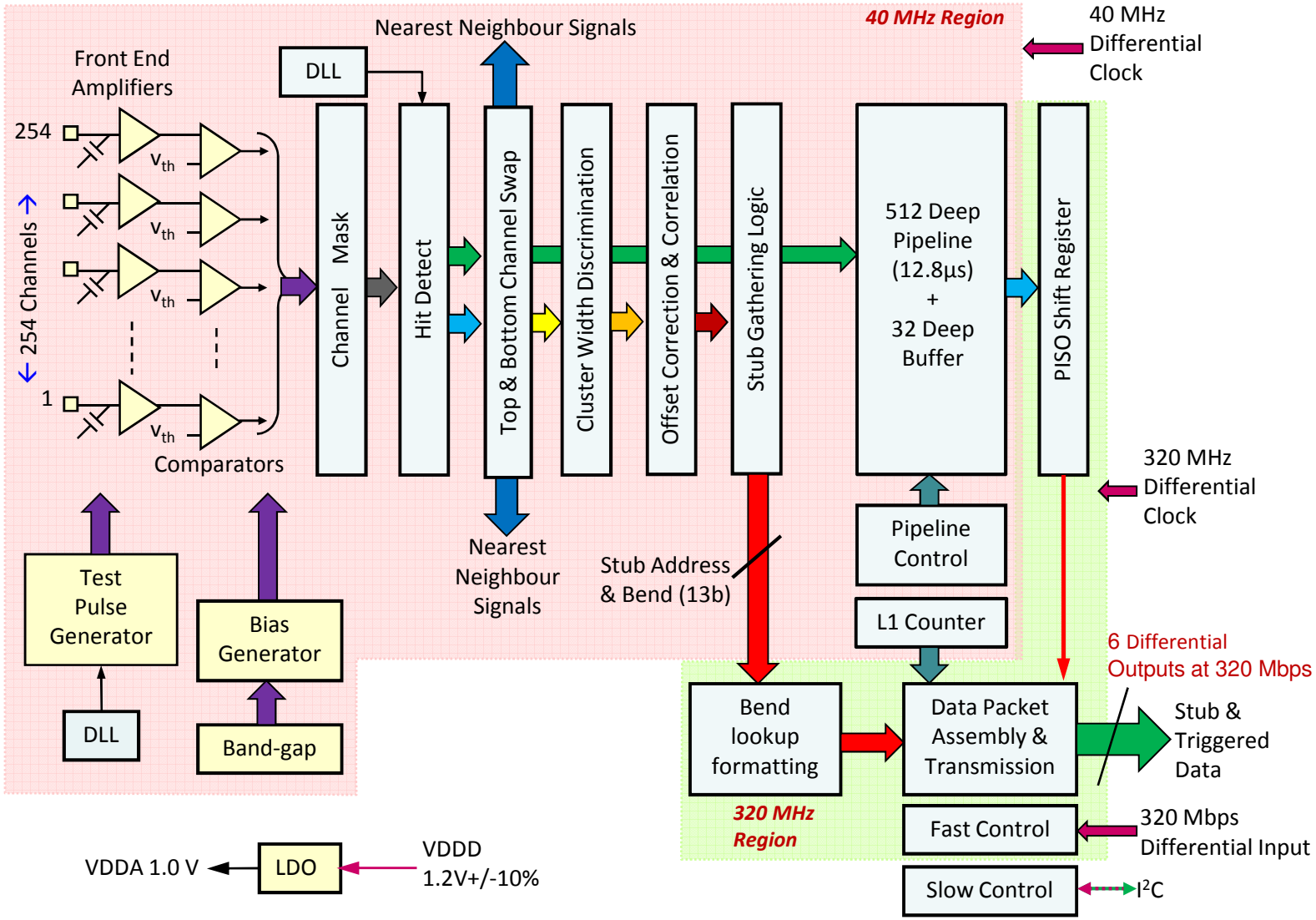
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p03.doc

will summarise today

(some repetition of previous presentations, but worth it now specs finalised)

Mark Raymond, CMS Tracker Week, Tracker Phase 2 Electronics, May 2015

CBC3 block diagram



will go through each block in turn, explaining functionality and quoting specs.

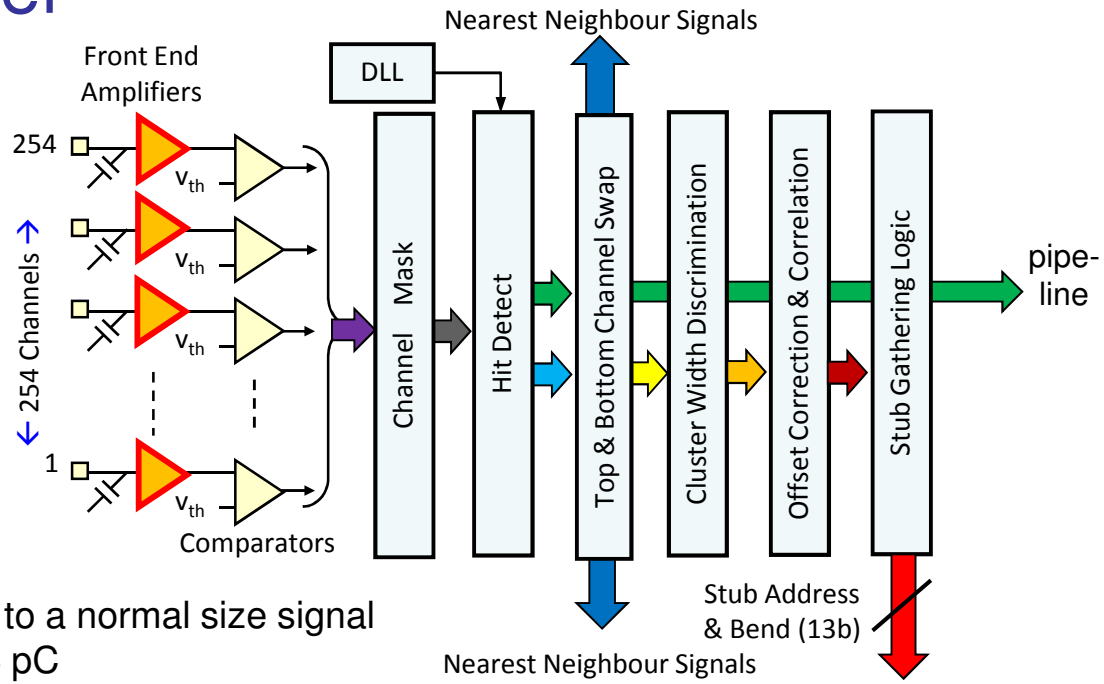
CBC3 front end amplifier

front end will be optimised **specifically**
for n-on-p sensor polarity
- AC coupled
  - no DC current tolerance required
- strip length 5 cm (~8 pF)

pulse shaping
- peaking time <20 nsec
- return to baseline within 50 nsec

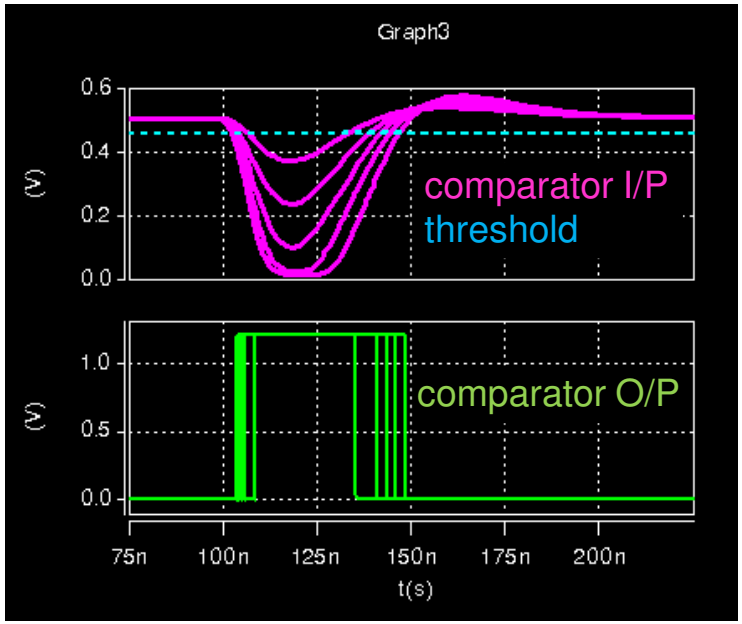
overload recovery (hips response)
- an individual channel should respond to a normal size signal < 2.5 usec following hip signal up to 4 pC (spec. based on what is achievable)

noise
- target ENC < 1000e



front end optimisation progressing

simulation shows signals in comparator
- 2.5 fC -> 12.5 fC, 2.5 fC steps
- comparator threshold at 1 fC
- overall pulse length < 50 nsec



comparators and channel mask

comparator

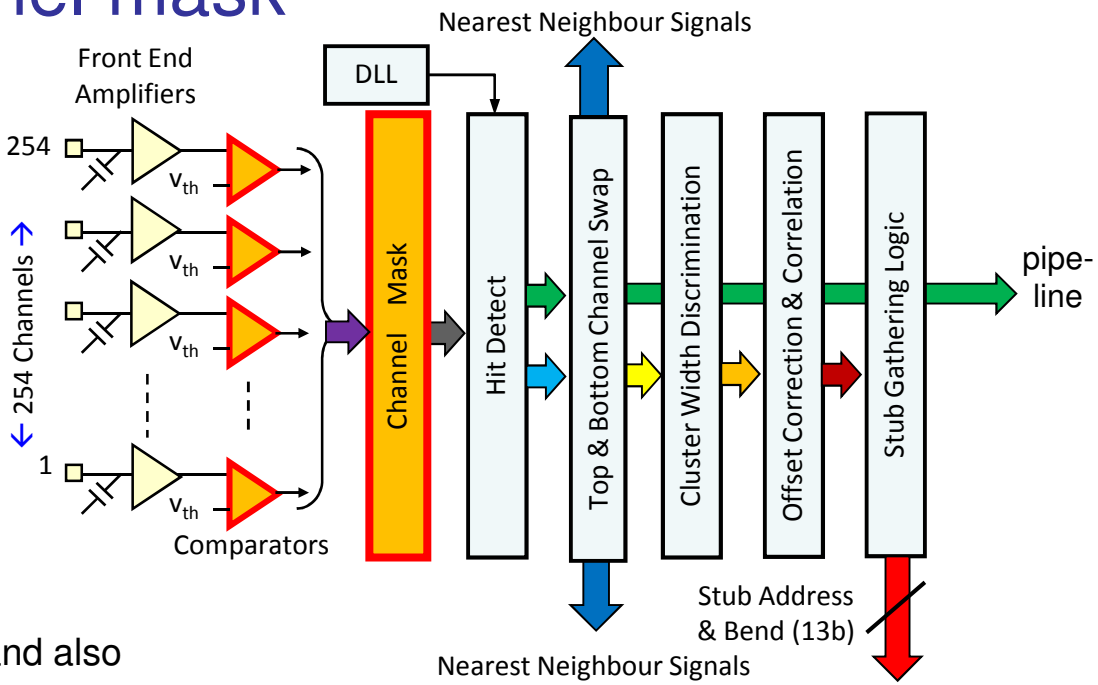
individually tunable offset

improved (10-bit) resolution
for global threshold

=> 1 mV LSB (~125e)

channel mask

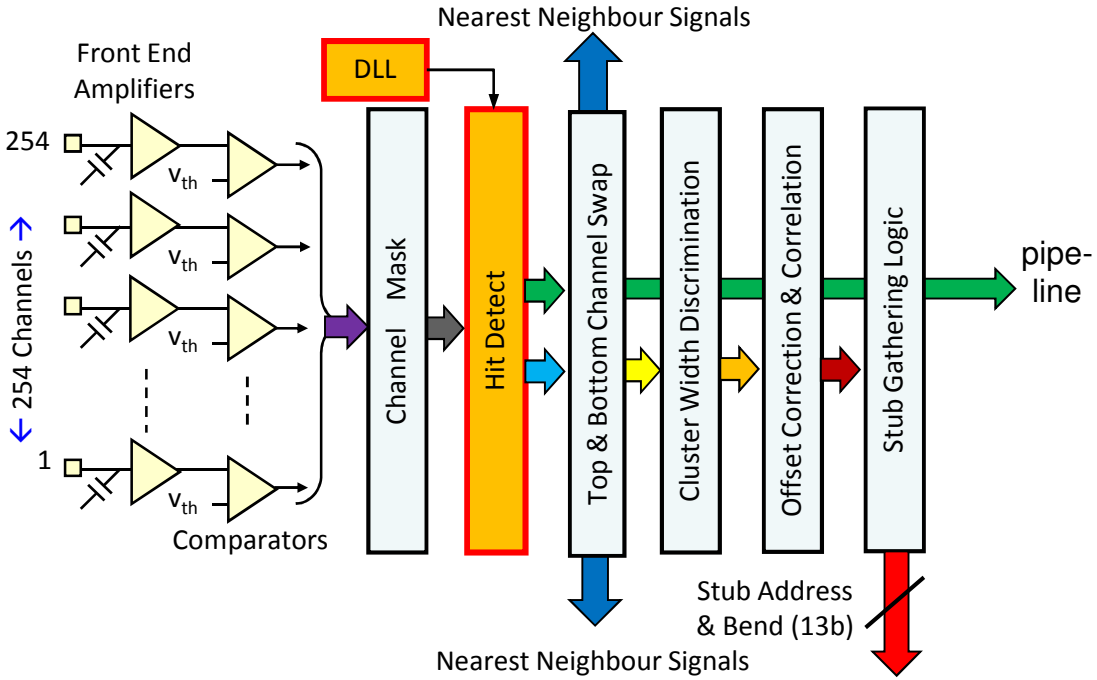
important to suppress fake triggers and also
to limit occupancy after sparsification



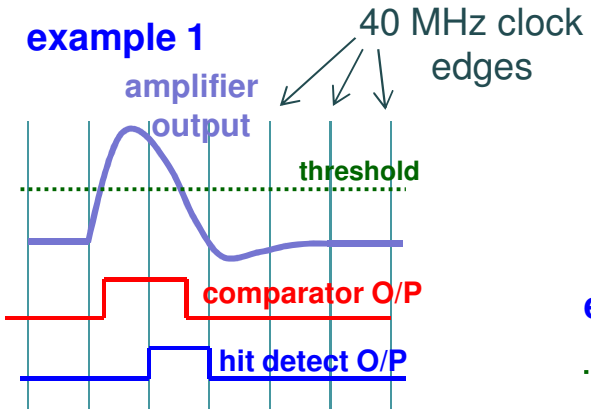
hit detect

samples output from comparator using programmable phase 40 MHz clock from DLL (1 nsec resolution)

needs to be sensitive to variety of input conditions

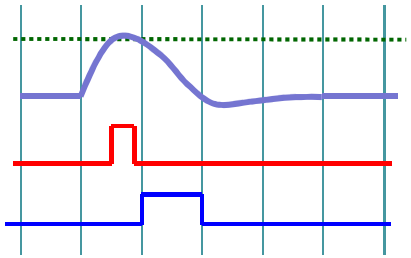


example 1



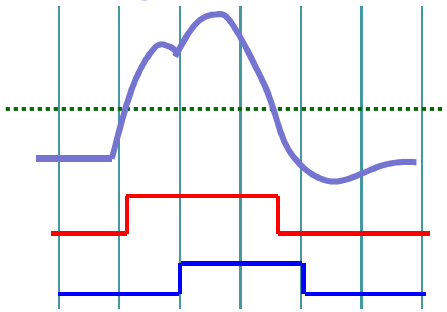
single pulse at amp. O/P.
Comparator O/P fires.
Hit detect produces output at next 40 MHz clock edge

example 2



single pulse only just exceeds threshold. Comp O/P rises and falls between clock edges, but hit detect still "detects" and produces an output

example 3



two consecutive pulses piled up.
Comp O/P stays high for 2 clock edges.
=> hit detect output stays high for two clock cycles

top & bottom channel swap

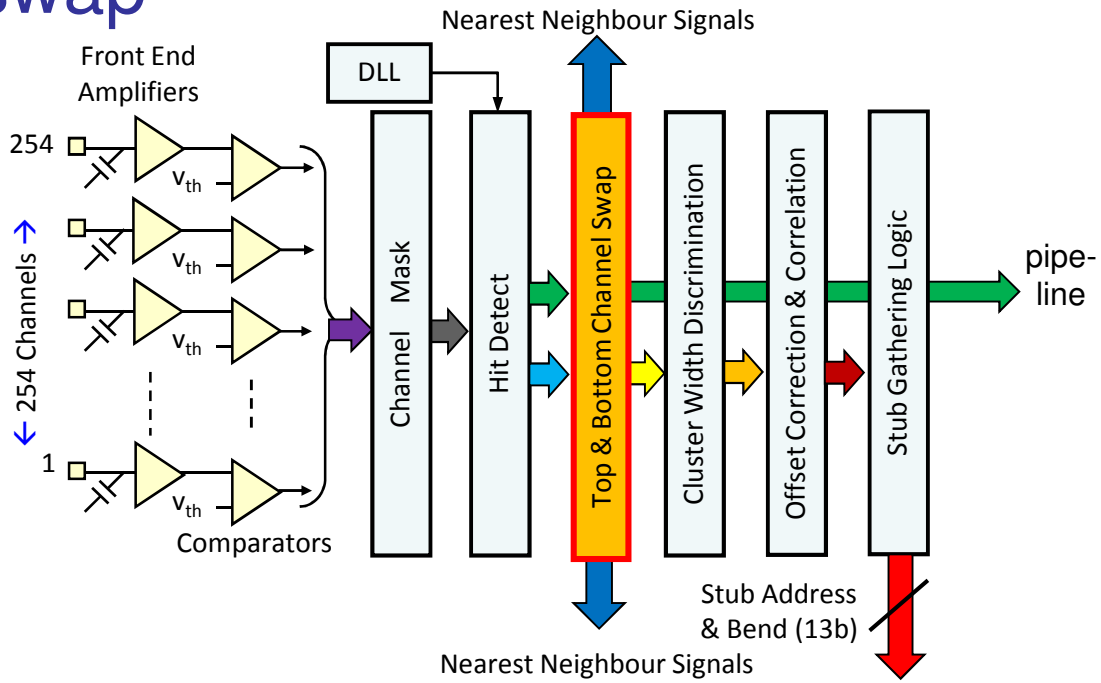
modules mounted above and below support structure will be flipped (probably)

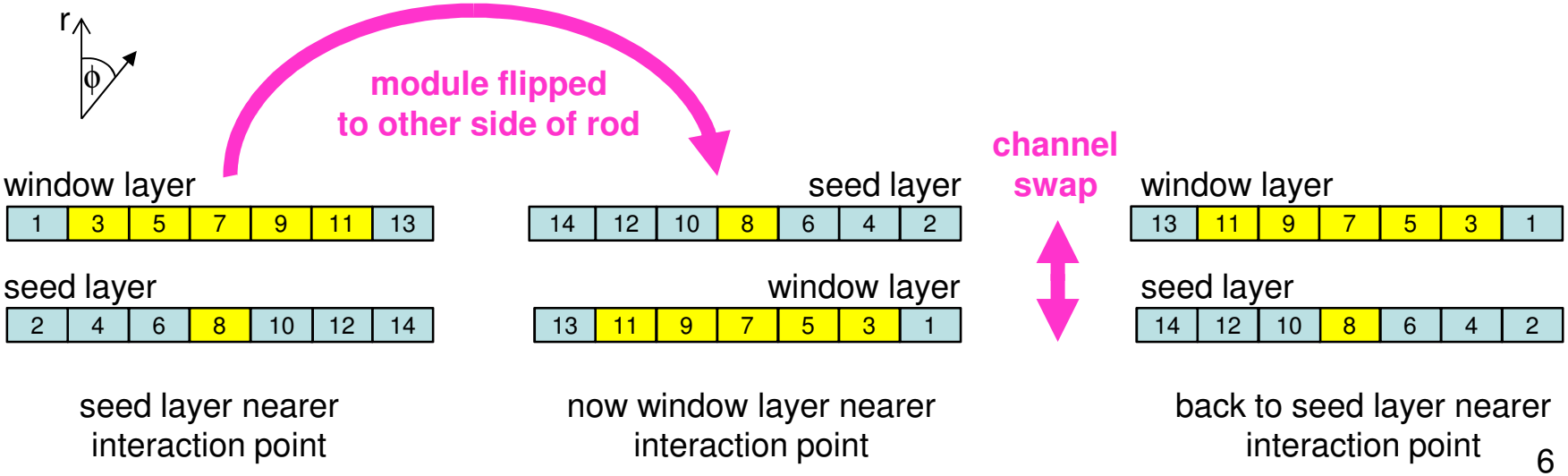
=> seed and window layers will also be flipped unless do something about it

(expect lower efficiency when seeding from outer layer because of scattering and conversions -> more hits in outer layer which don't correspond to valid stub)

simplest thing is to swap channels on chip

1<->2, 3<->4, 5<->6,…..





cluster width discrimination

CBC2: clusters ≤ **3** strips accepted

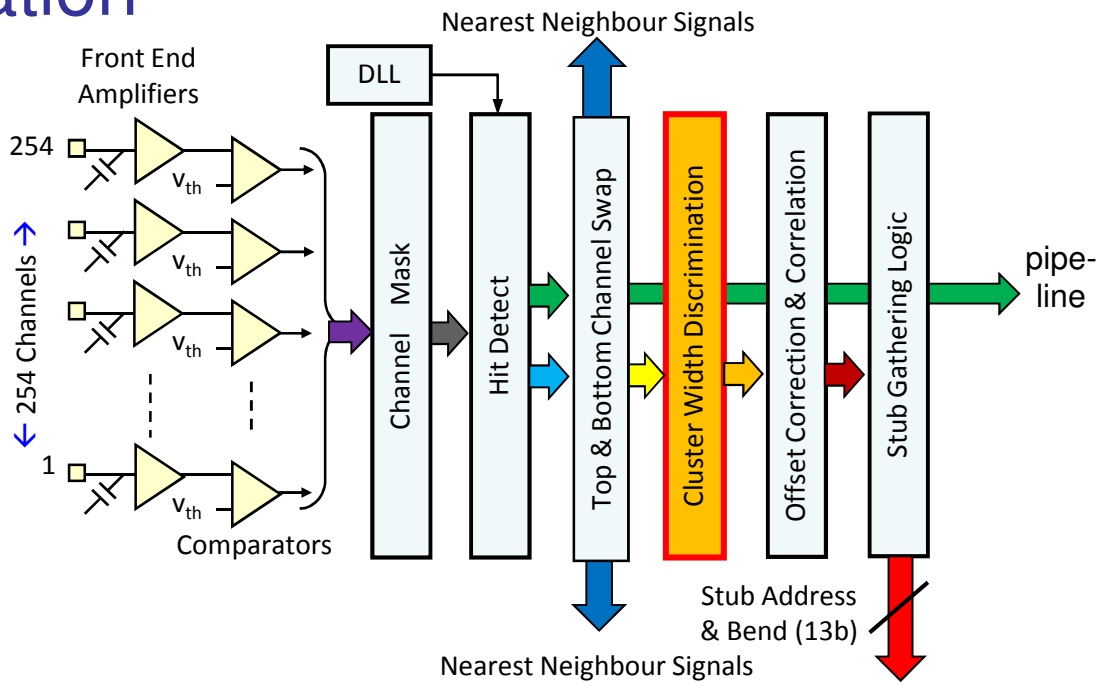
2 strip cluster assigned to one of the strips involved

CBC3: clusters ≤ **4** strips accepted

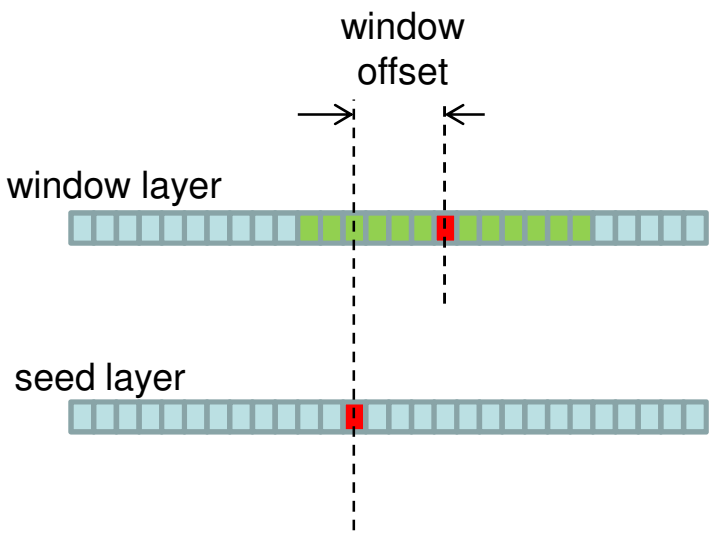
2 & 4 strip clusters assigned to mid-position

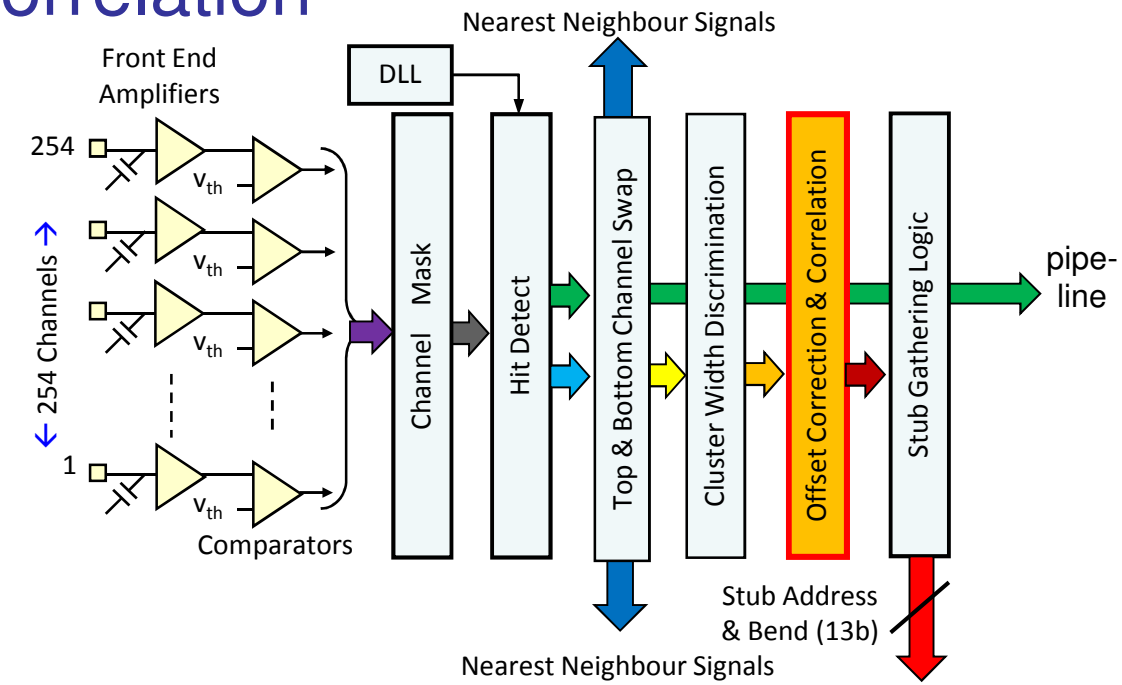
=> ½ strip cluster position resolution

=> 8-bit cluster address



offset correction and correlation





CBC3 stub generated if cluster in seed layer corresponds to cluster found within window in other layer

window width programmable up to ± 7 strips (± 14 half strips)

window can be offset, 4 domains / chip (=> 32 across module)

offset programmable up to ± 3 strips (± 6 half strips)

position of cluster in window indicates direction of stub -> this is the **bend** information

5 bits bend info locates cluster to individual ½ strip position if widest window selected

stub gathering logic + bend lookup formatting

up to 3 stub addresses + associated bend info can be passed to **bend lookup formatting** block every BX

no priority logic - 1st 3 stubs only

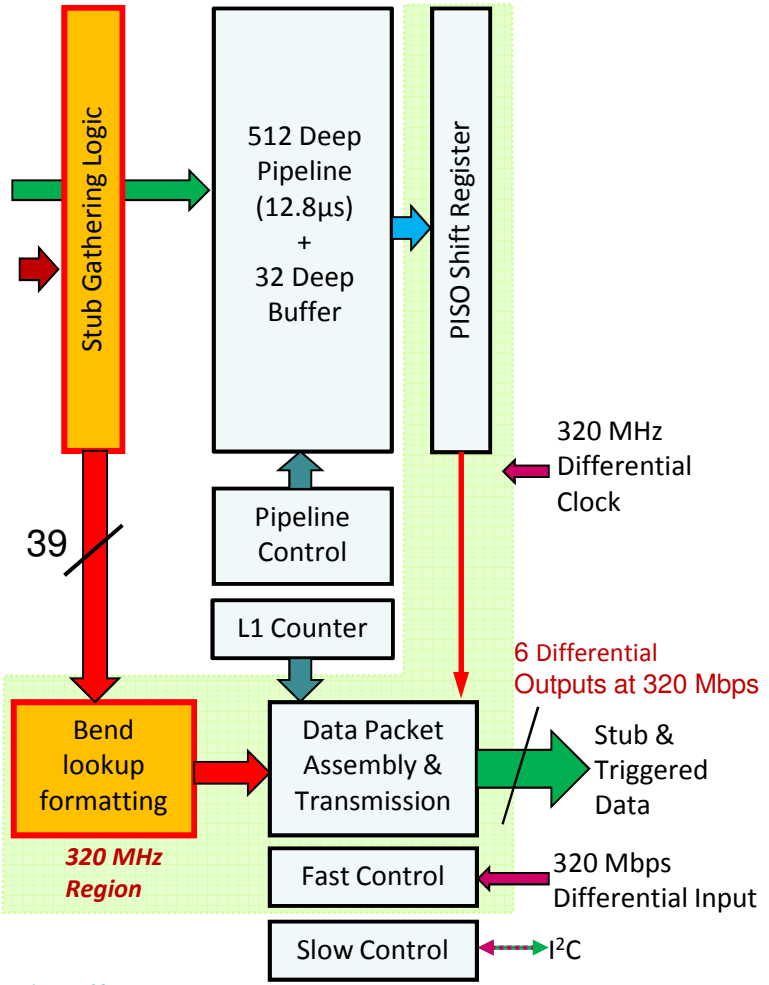
more than 3 -> stubs overflow bit set in O/P data packet

13 bits / stub => 39 bits total

5 bits bend info reduced to 4 bits using programmable lookup table (mapping depends on location in tracker)

stubs gathering logic and bend lookup formatting logic described in more detail last time:

https://indico.cern.ch/event/360684/session/0/contribution/1/material/slides/1.pdf



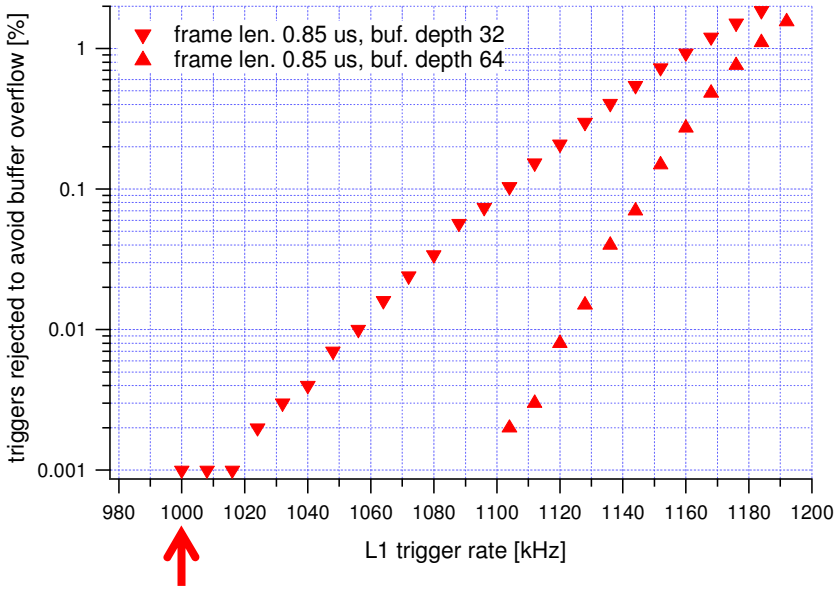
pipeline & PISO shift register

512 deep pipeline => up to 12.8 usec latency

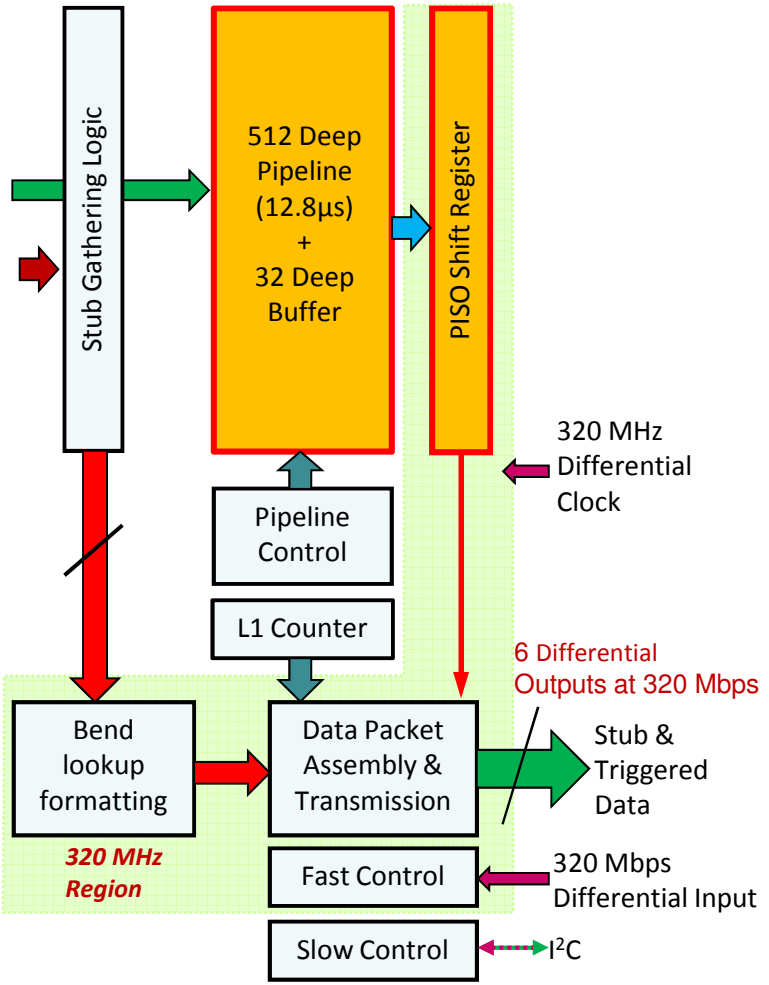
32 deep buffer for triggered events awaiting readout

=> very low inefficiency for trigger rate up to 1MHz

triggers rejected to avoid buffer overflow vs. trigger rate



< 0.001% triggers rejected @ 1 MHz for buffer depth 32

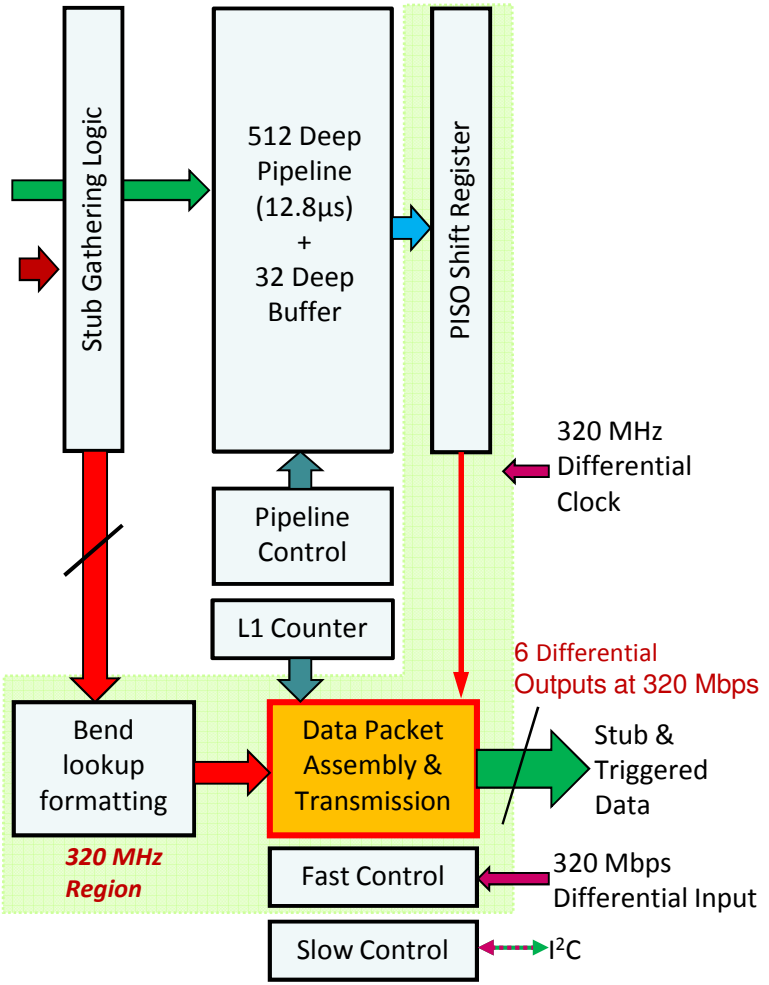


data packet assembly & transmission

6 differential outputs running at 320 Mbps

25 ns

S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	SoF	**R**
S1	S2	S3	B2	OR254	**R**
S1	S2	S3	B2	Error	**R**
S1	S2	S3	B2	**Sync**	**R**



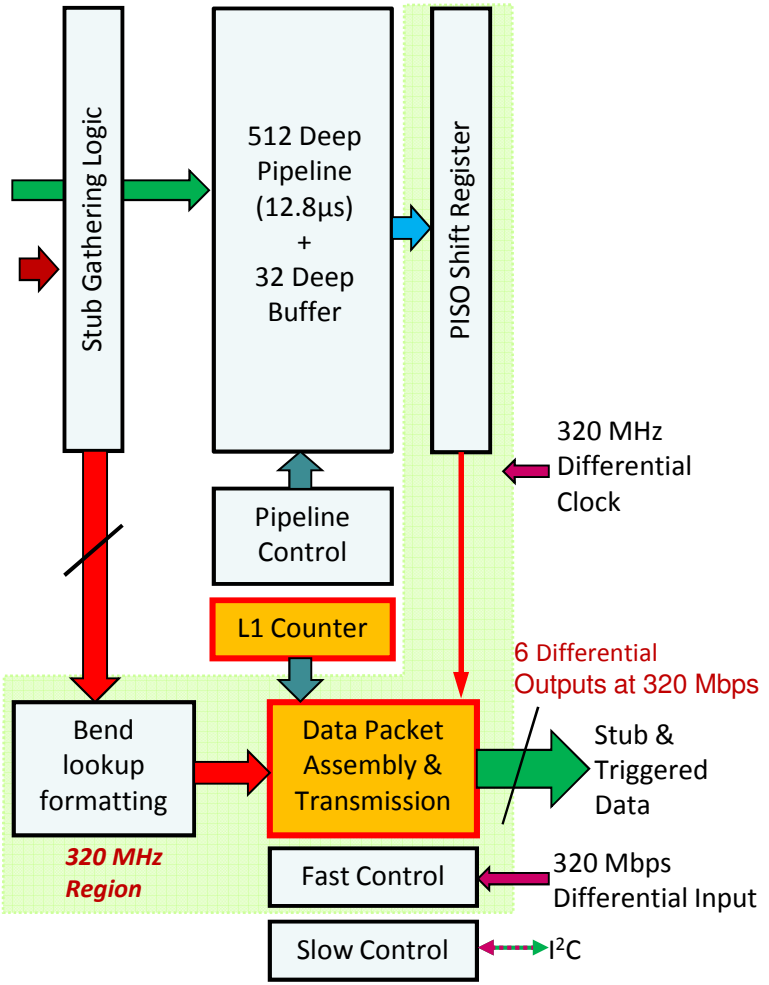
S = Cluster address, B = Bend data
SoF = Stub Overflow (>3 Stubs)
OR254 = any unmasked channel over threshold
Error = latency OR FIFO overflow error
Sync = For synchronisation with CIC
R = Triggered readout data (remains unsparsified)

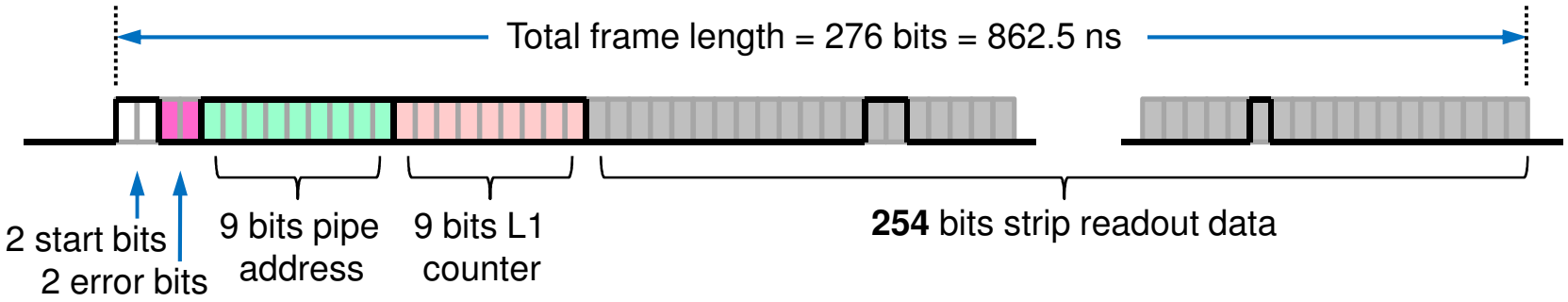
data packet assembly & transmission

trigger rate capability to 1 MHz

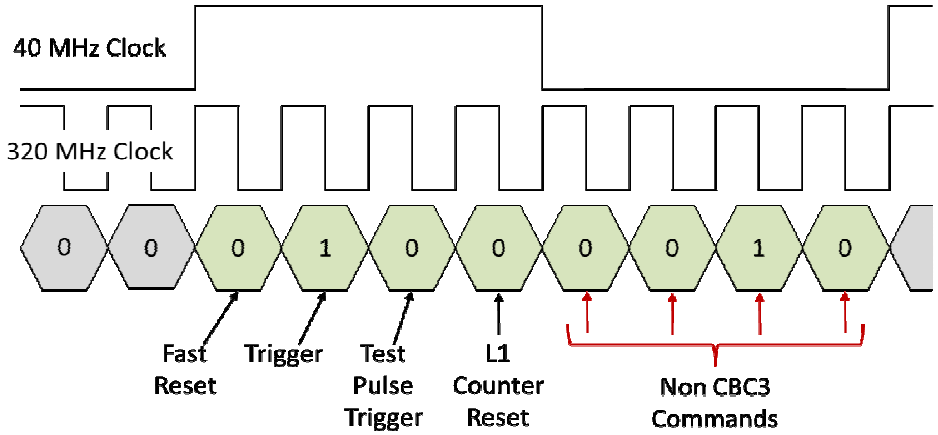
data frame comprises

2 start bits
2 error bits (latency & FIFO overflow)
9 bits pipe address (triggered pipeline location)
9 bits L1 counter
reset by fast reset OR dedicated reset
e.g. every orbit
254 bits strip readout data





fast and slow control



fast control

320 Mbps differential stream

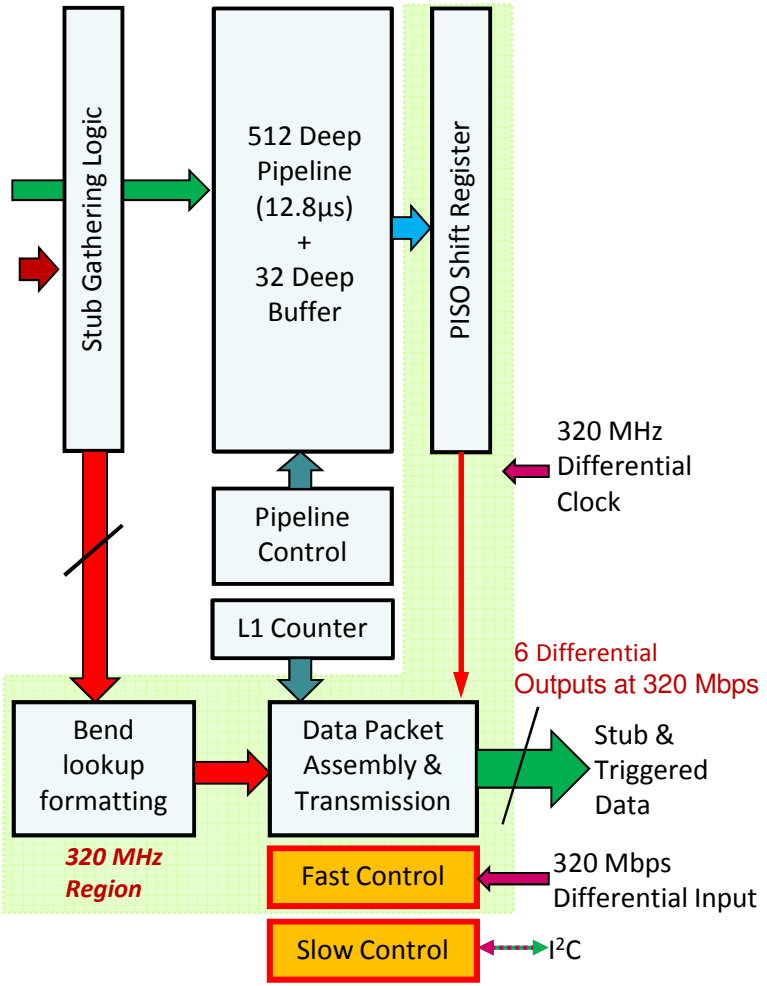
not decoded - pos'n within 40 MHz ck period determines function

commands are:

- fast reset
- trigger
- test pulse trigger
- L1 counter reset

slow control

I2C @ 1 MHz



CBC3 miscellaneous

clocks
- 40 MHz and 320 MHz differential

test pulse feature
- same as CBC2

SEU immunity
- I2C register immunity to be improved by using Whitaker cells
  - for results see http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_SEU_Kirika_Nov_14.pdf

ionizing radiation tolerance
- pipeline cell design to be modified to eliminate leakage effect at low doses
  - for results see http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_TID_Davide_Nov_14.pdf

power
- 1.2 V ± 10%
- on-chip LDO to generate analogue power rail
- **target** power consumption for 5 cm strips 450 uW/channel

pads
- 250 um pitch, same as CBC2
- wire-bondable column for probing and other tests

summary

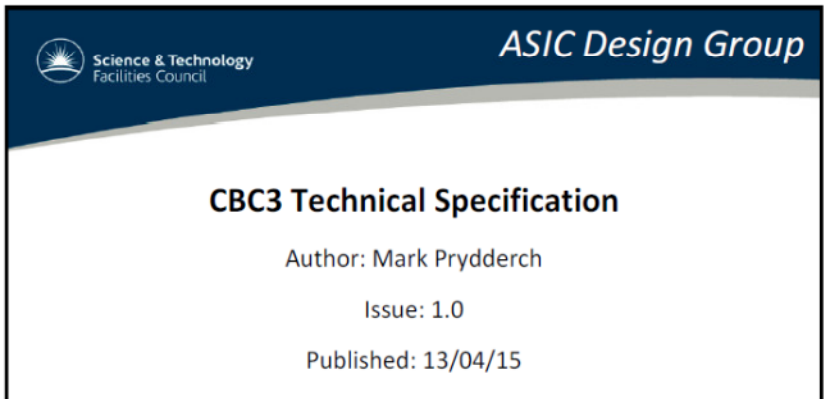
CBC3 design underway

specs are defined and a document is available

have summarised most of contents here

MOSIS submission planned for February 2016

=> chips in hand ~ May

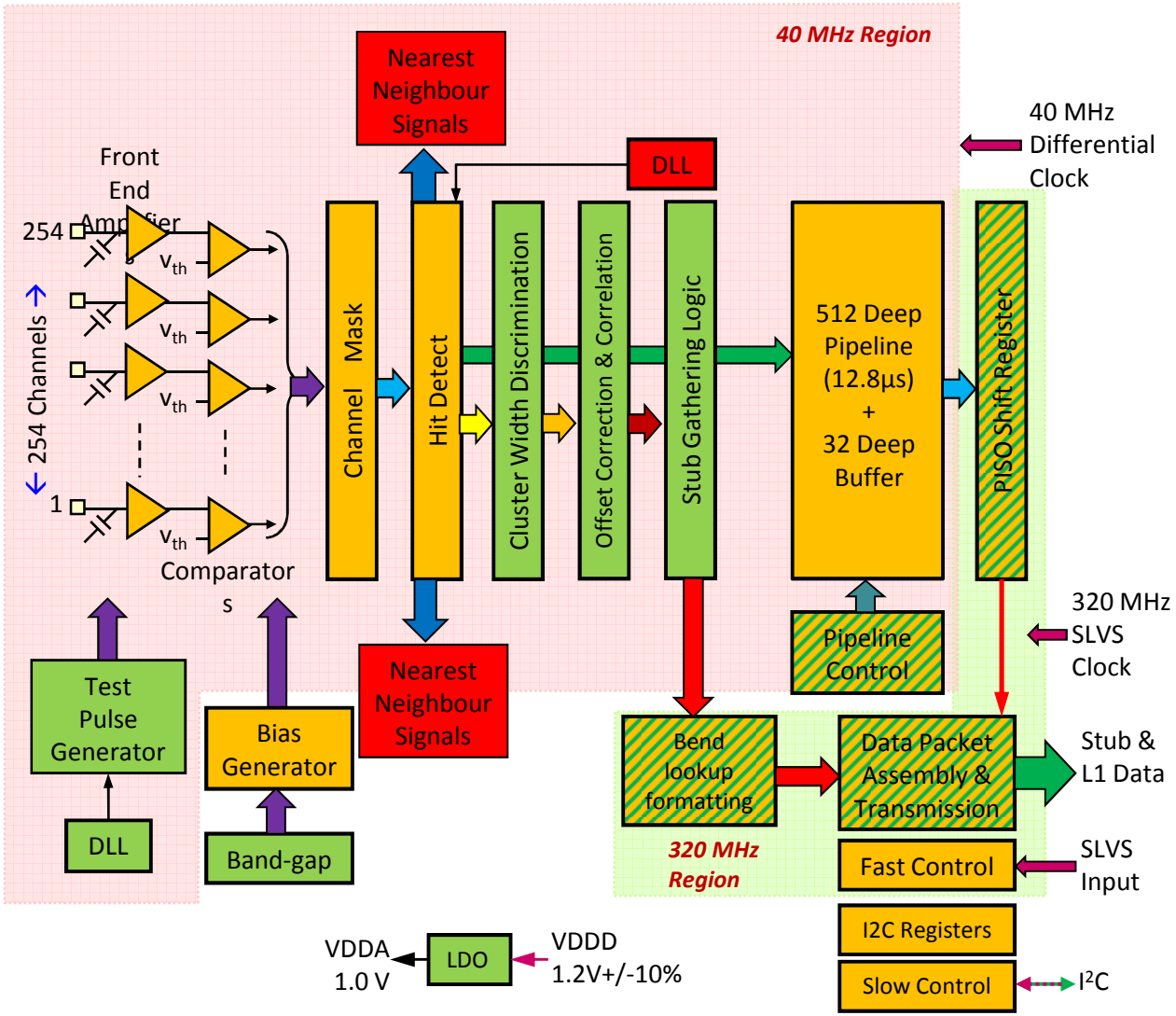


http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p03.doc

EXTRA

CBC3 status

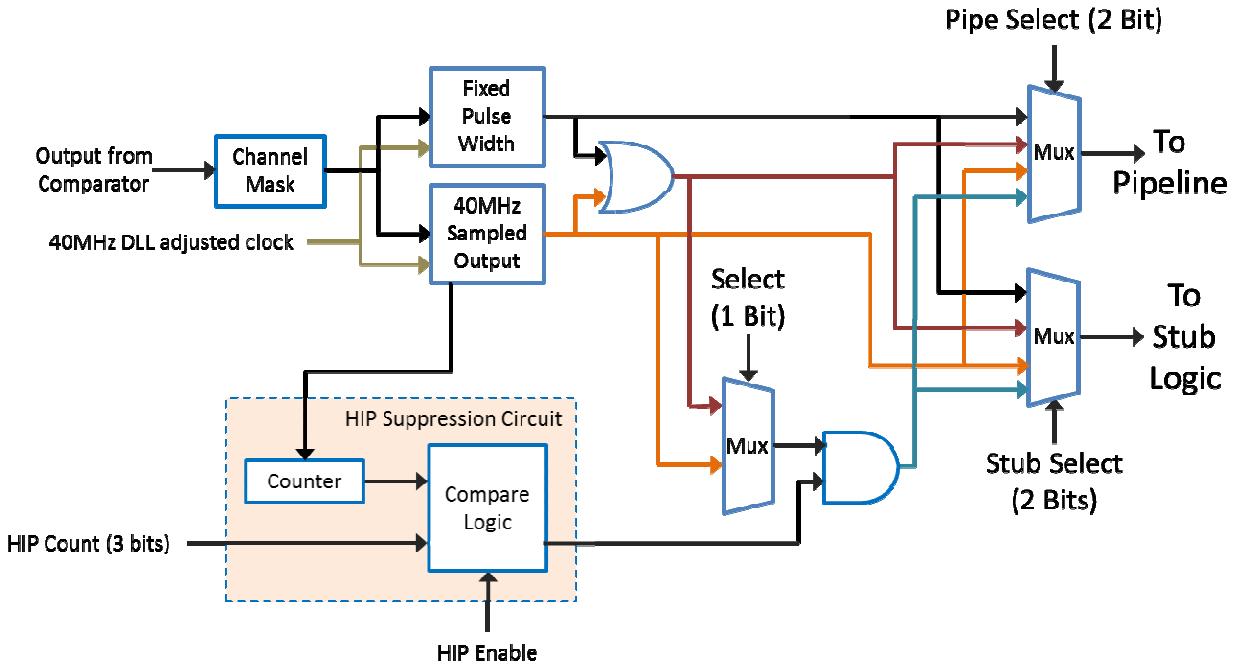
M.Prydderch



- Analogue front end re-designed. Needs layout & further simulation.
- Hit Detect Schematic & simulations complete. Needs layout.
- Channel Mask incorporated in Hit Detect. I2C registers need to be added.
- Stub finding logic blocks complete.
- Bend look-up table completed to preliminary layout. I2C registers need to be added.
- Data assembly blocks are completed to preliminary layout.
- Serial Fast Control designed and simulated. Needs layout.
- Pipeline SRAM cell modified. Pipeline needs extending & drivers checked.
- I2C register cell redesigned. Layout in progress. Needs further simulation.
- Ibias current reference redesigned. Layout in progress. Needs further simulation.
- New 10 bit DAC for VCTH not started.
- Nearest Neighbour pads not started (Top level layout exercise)
- 2nd DLL not yet investigated.
- Top level layout assembly & verification not yet started.

Complete | Preliminary Layout | In progress | To do

hit detect logic



flexibility included to allow choice of output to following logic
mainly for diagnostic purposes

also includes HIP suppression circuit to block output if comparator high for longer than N clock cycles
N programmable up to 7

CBC2 issues to address (in CBC3)

- leakage current in pipeline at low ionizing doses
  http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_TID_Davide_Nov_14.pdf
  enclosed NMOS devices now implemented

- I2C register SEU immunity could be better
  http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_SEU_Kirika_Nov_14.pdf
  now plan to use Whitaker cells for registers

- CM effect in electrons polarity mode
  shows up when threshold low and many channels firing
  traced to postamp feedback FET biasing
  http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC2_CM_systems_Jan2015.pdf
  a new method for biasing the feedback FET has been found

- so-called “shadow effect”
  when signal injected into many channels, other channels fire, but ~50ns later
  traced to coupling through preamp cascode bias
  http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC2_shadow_effect_Apr_2015.pdf
  preamp cascode now individually biased using regulated cascode circuit