CBC2 status

OUTLINE

recent CBC1 + Infineon sensor test beam

CBC2 layout and architecture

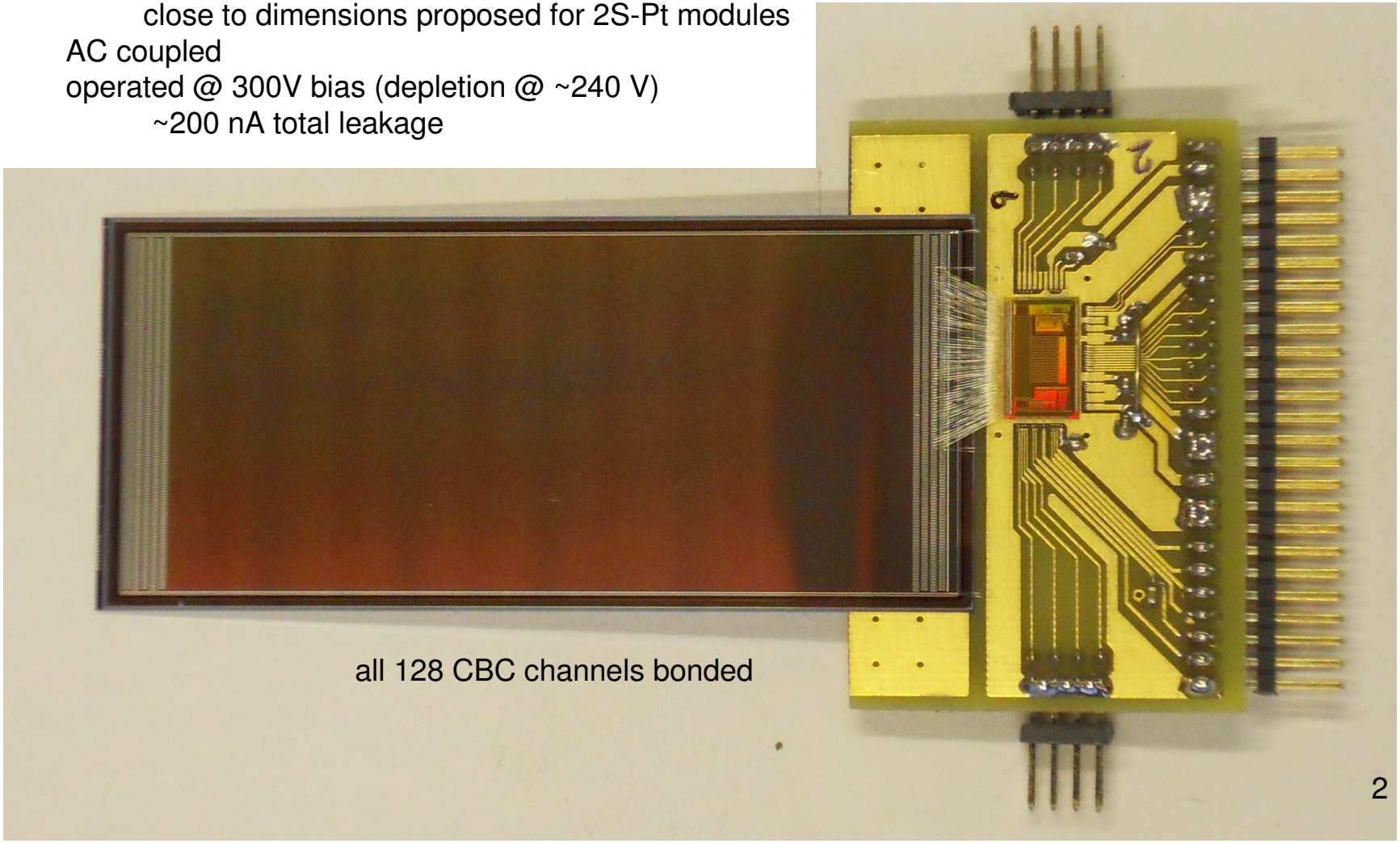
CBC2 test plans

CBC1 test beam 8th – 22nd October

CBC prototype + Infineon sensor

Infineon sensor provided by Vienna (Marko Dragicevic)

- 300 um thick, p-on-n
- 5cm long strips (256), 80 um pitch
  - close to dimensions proposed for 2S-Pt modules
- AC coupled
- operated @ 300V bias (depletion @ ~240 V)
  - ~200 nA total leakage



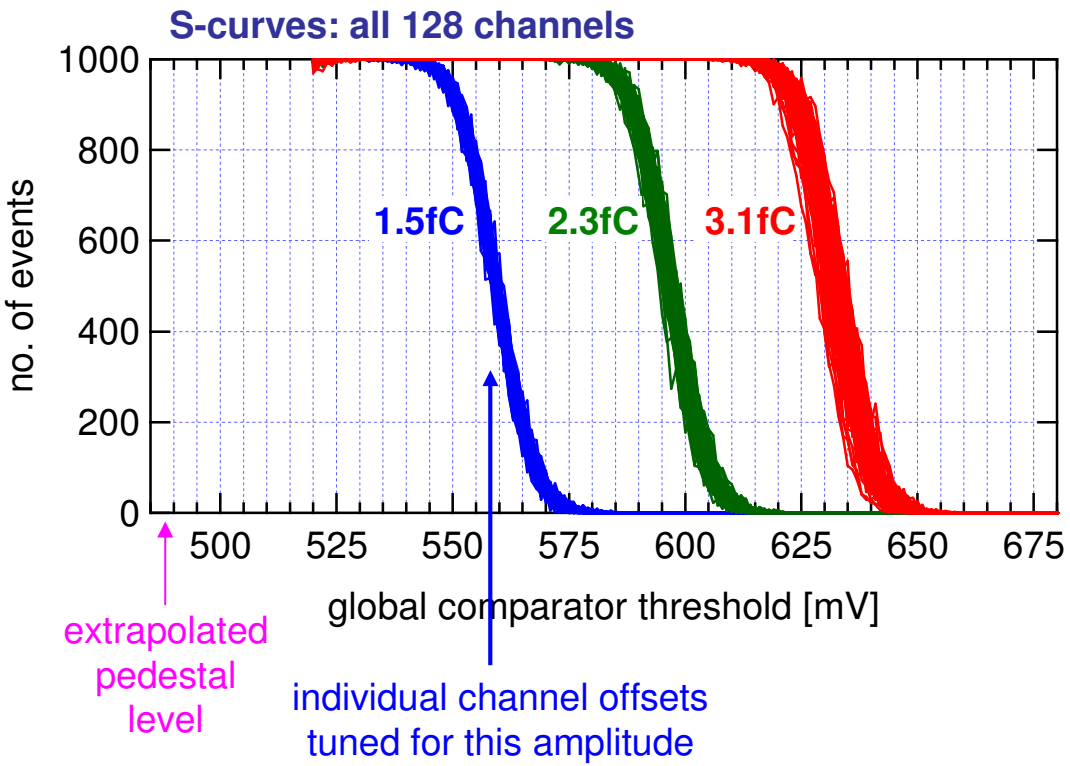
all 128 CBC channels bonded

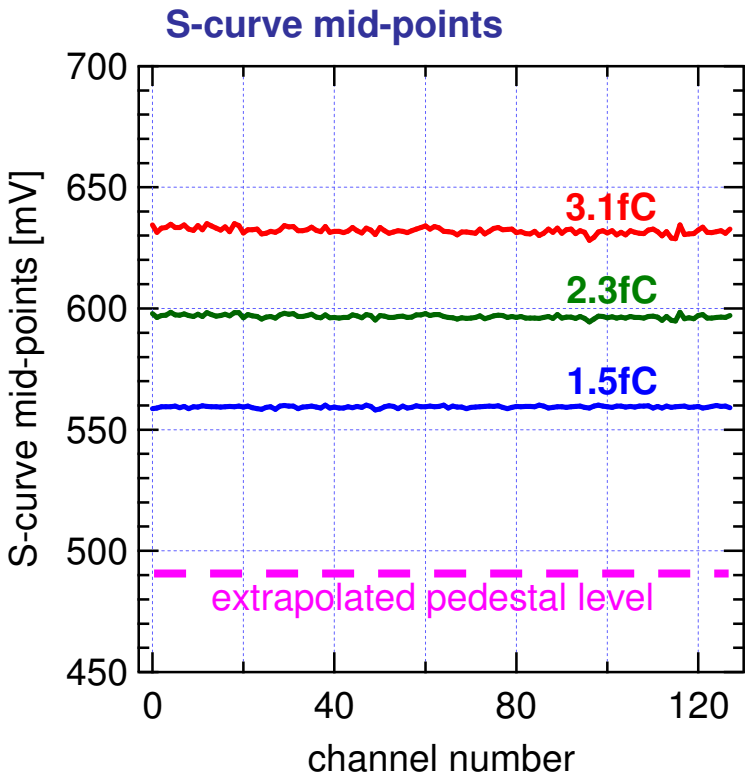
lab measurements

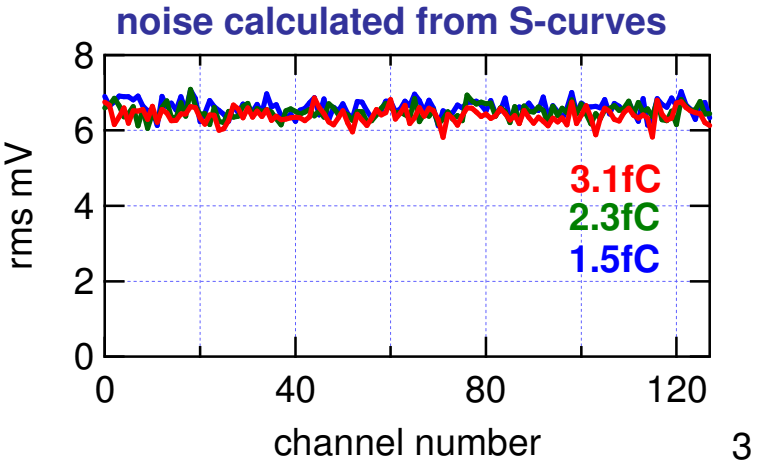
s-curves measured using test-pulse system
only 3 amplitudes used

noise and gain extracted from s-curves
gain 47 mV / fC (assumes 20 fF Cinj)
noise ~ 6.5 mV => 870 electrons

response flat across channels
no edge effects







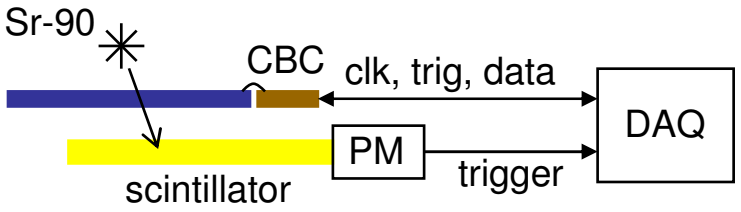
lab measurements - beta source

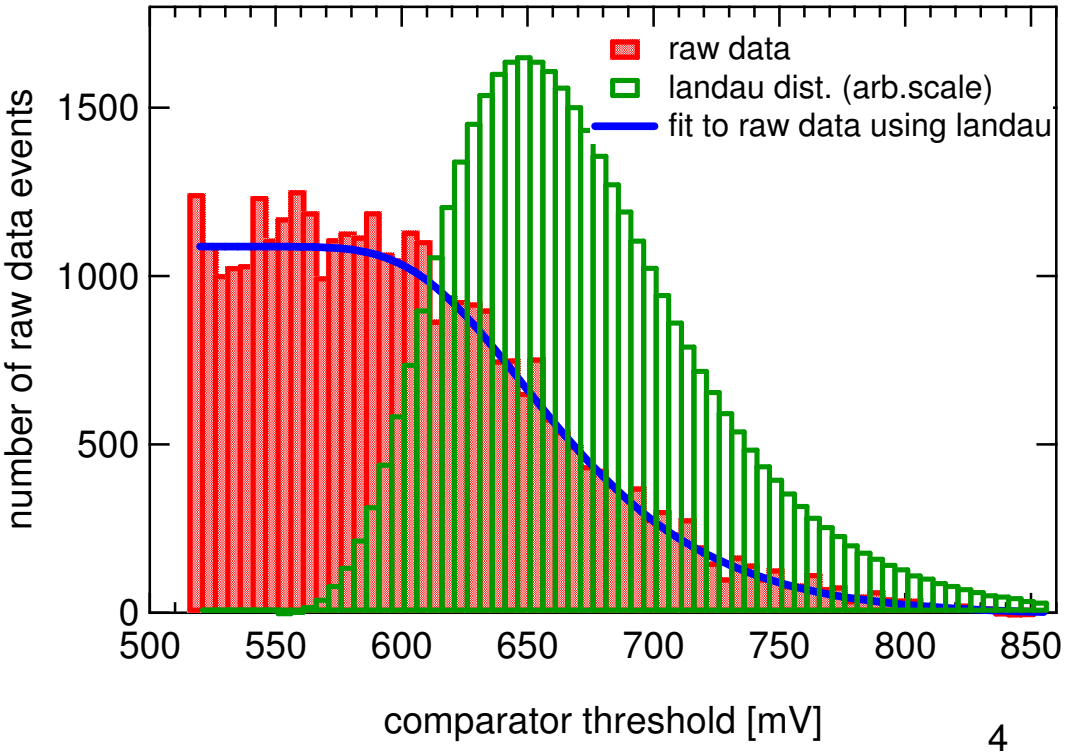
count clusters in CBC for fixed number of scintillator triggers

sweep comparator threshold in 5 mV steps -> raw data

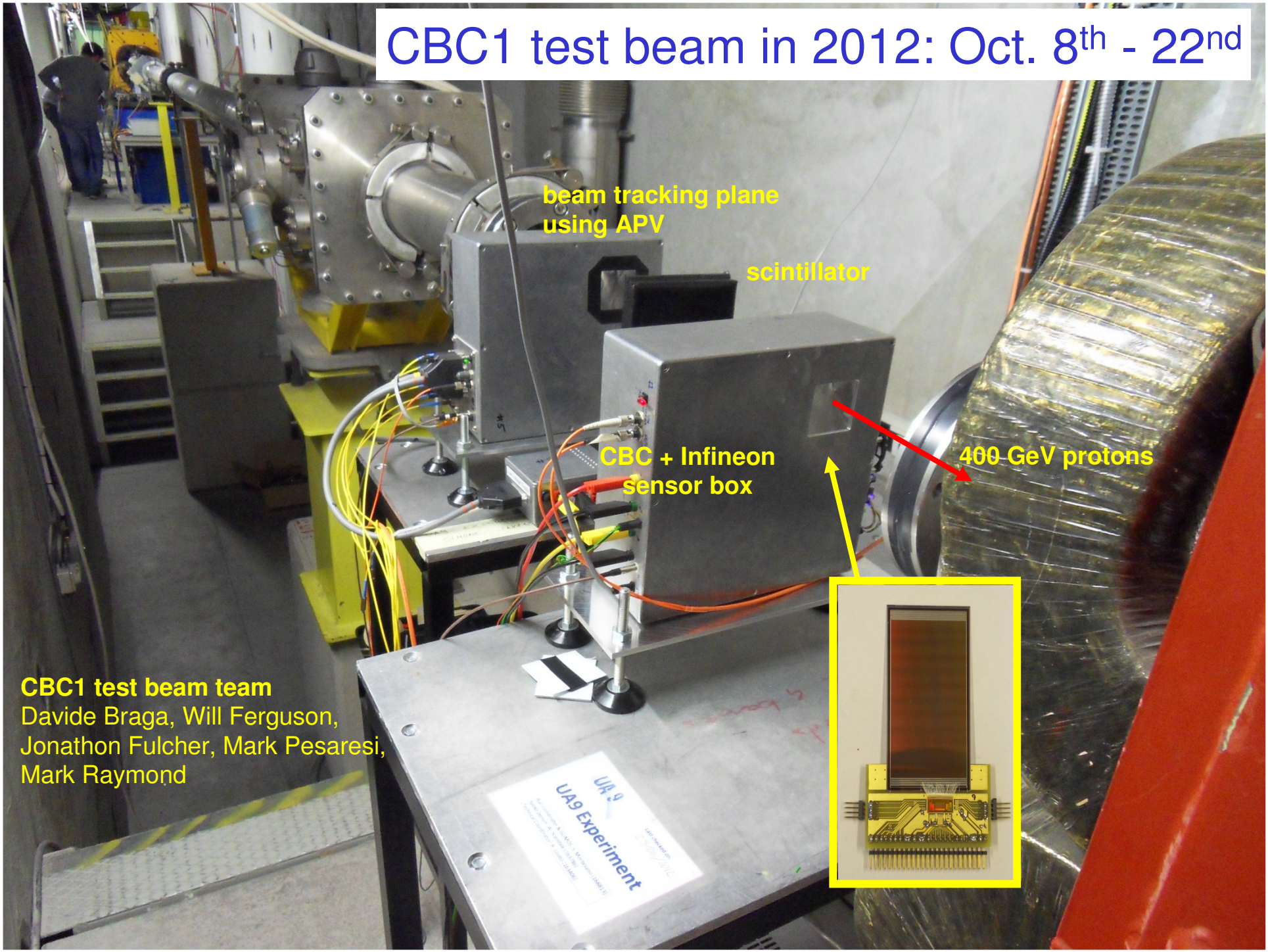
fit raw data with curve generated from Landau

-> most probable signal value ~ 3.4 fC (21,000 e)



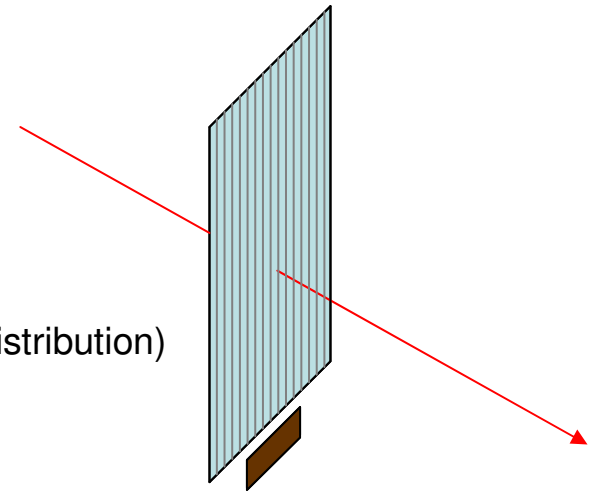


CBC1 test beam in 2012: Oct. 8th - 22nd



CBC1 test beam team
Davide Braga, Will Ferguson,
Jonathon Fulcher, Mark Pesaresi,
Mark Raymond

measurement programme



2 week UA9 test period (parasitic operation) - 400 GeV protons

CBC+Infineon sensor system in operation throughout

global comparator threshold scans (can use to extract pulse height distribution)

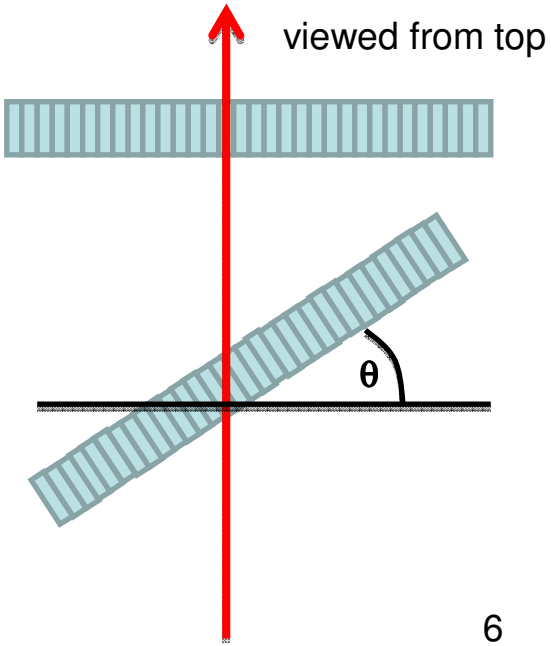
520 -> 900 mV (~ 0.75 -> ~ 9 fC)
600k triggers / threshold setting

data taken at 0, 10, 20, 30 deg. angle to beam

more data acquired at thresholds down to 510 mV (~0.55 fC, ~3000 e)

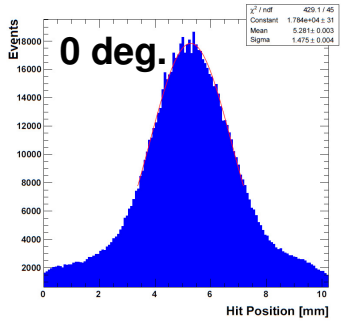
data analysis only just begun

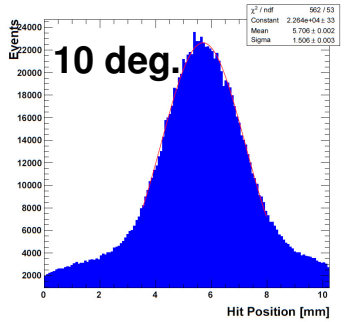
CBC data also successfully passed to and acquired by GLIB system

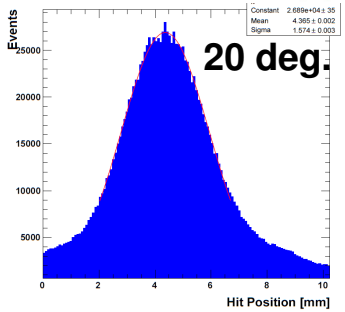


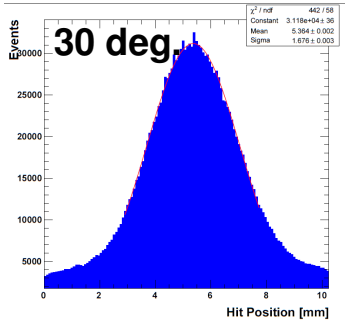
early results – beam profiles

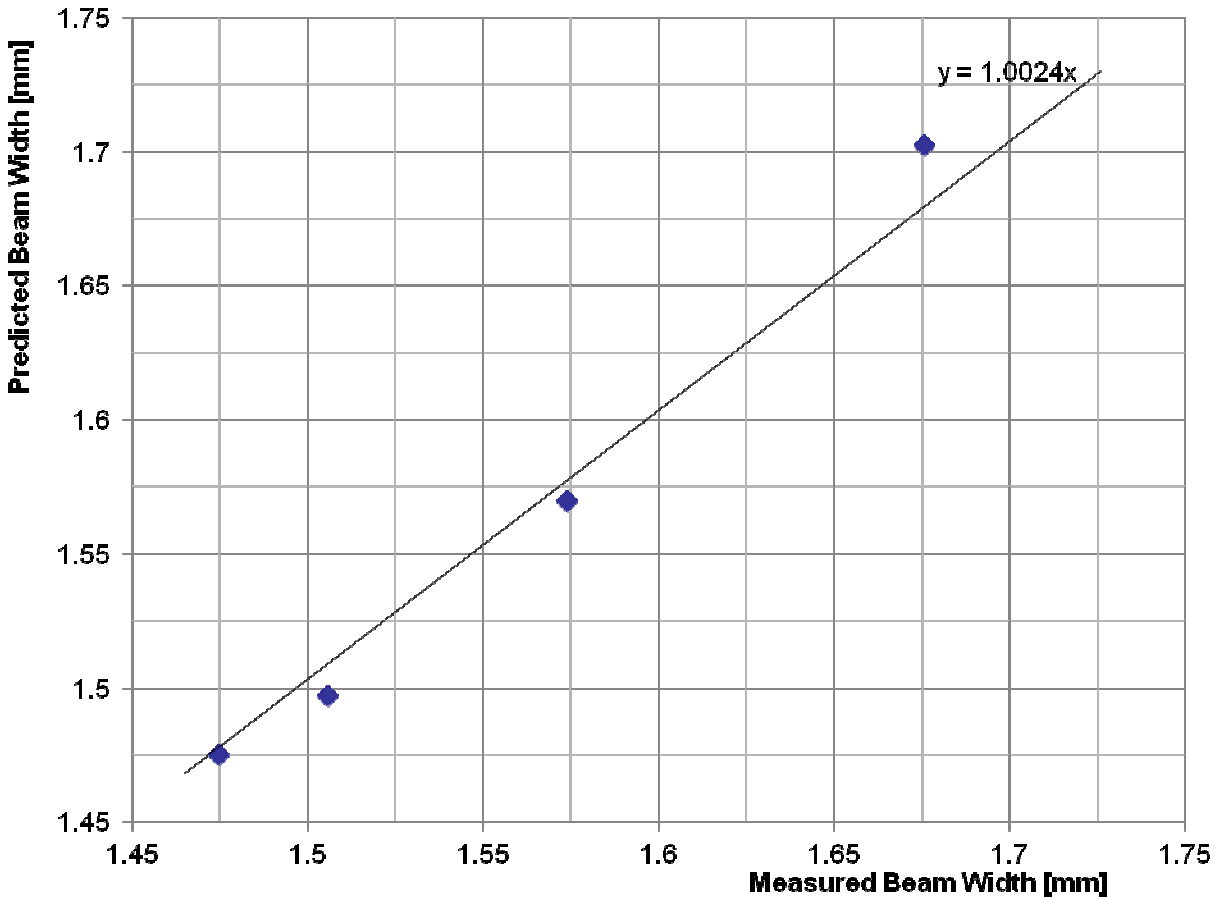
Mark Pesaresi









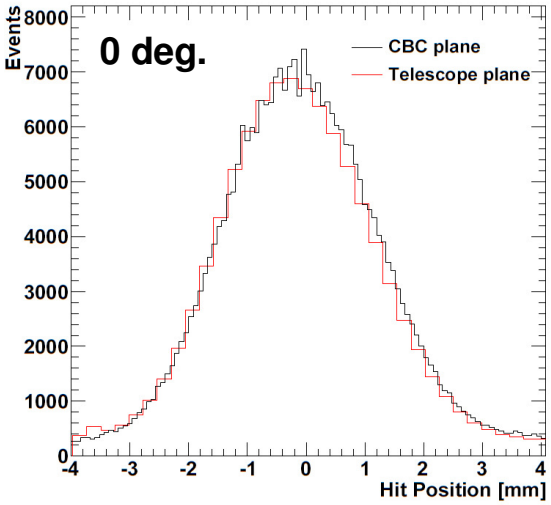


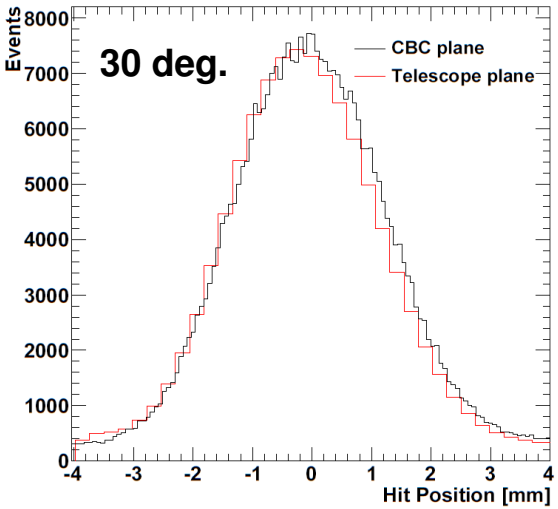
predicted beam width = normal incidence beam width / cos θ

more early results

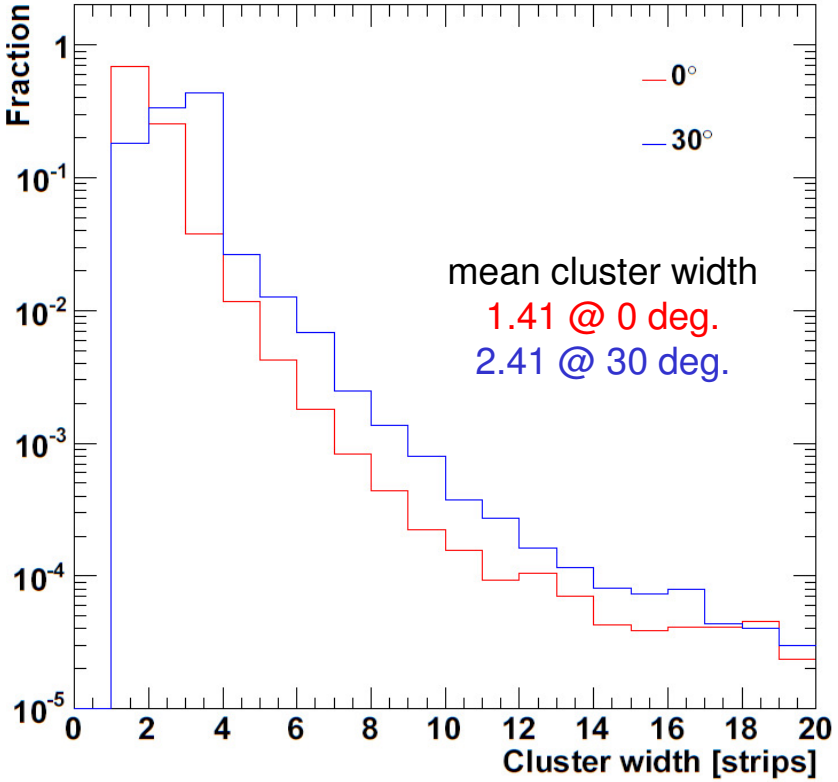
Will Ferguson

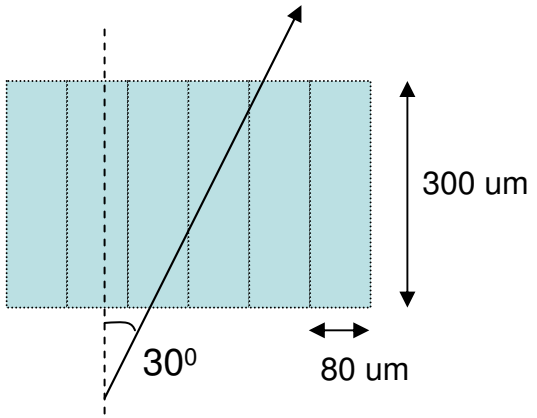
APV plane vs. CBC plane





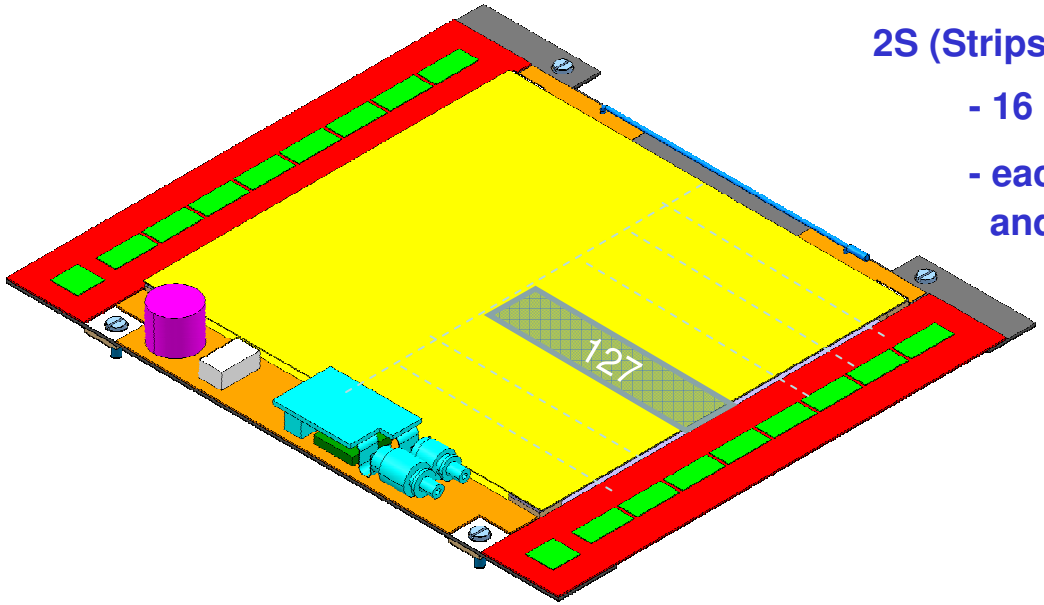
cluster width





CBC2

CBC2 for 2S-Pt module



2S (Strips-Strips) module

- 16 readout chips

- each reads 127 strips from bottom sensor and 127 from top

CBC prototype (CBC1)

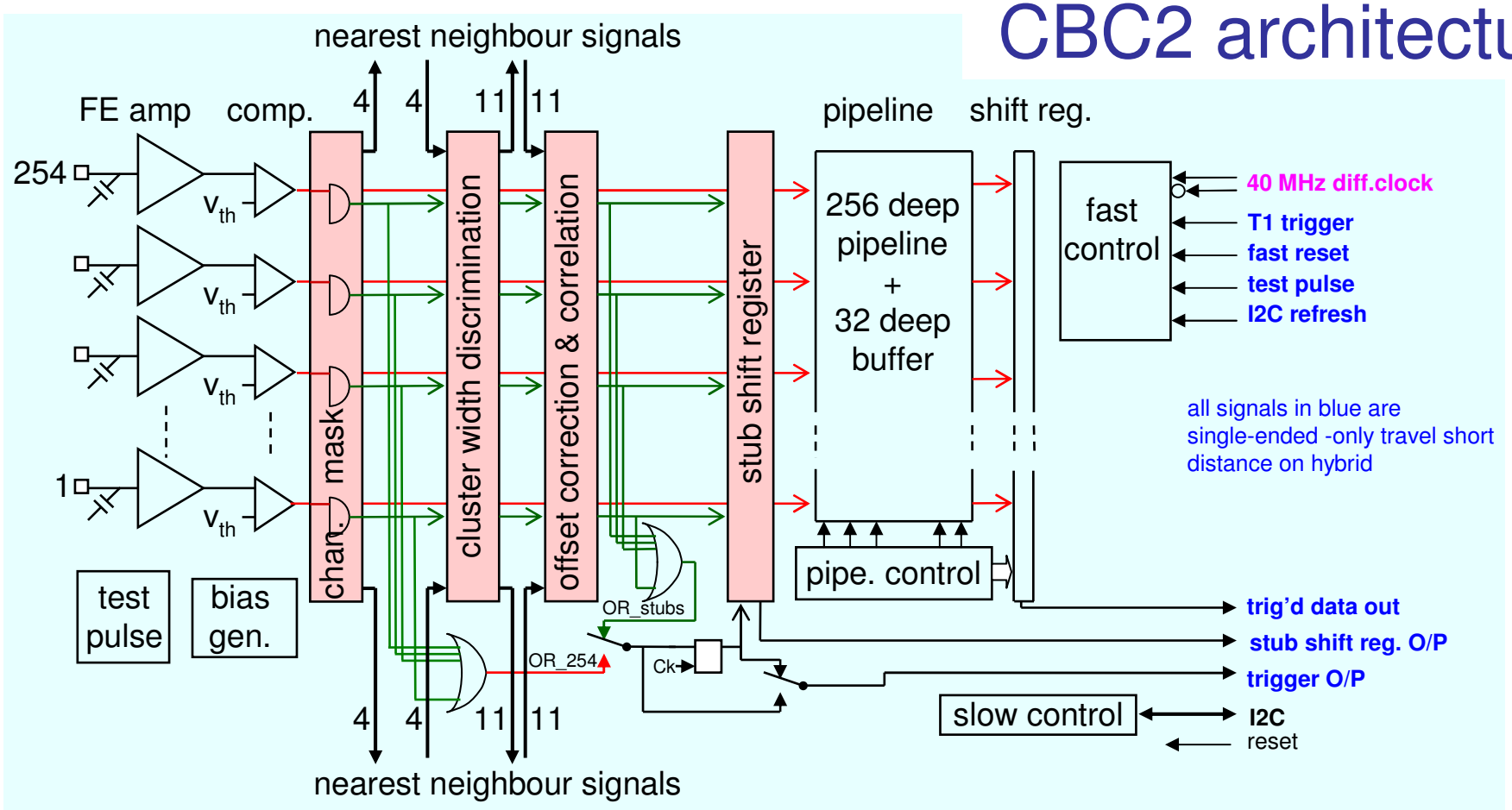
128 channel wire-bond chip, provides L1 triggered readout data only

CBC2

bump-bond chip, brings signals from 2 sensor layers in 1 chip (254 channels total)
provides L1 triggered readout data as in prototype
also performs cluster correlations to identify high Pt stub
positive correlation produces trigger output

=> functionality required to construct and evaluate prototype 2S-Pt module

CBC2 architecture



front end, pipeline, L1 triggered readout, biasing

~ same as prototype (few bug fixes) just more channels

new blocks associated with Pt stub generation

channel mask: block problem channels (not from L1 pipeline)

cluster width discrimination: exclude wide clusters > 3

offset correction and correlation: correct for phi offset across module and correlate between layers

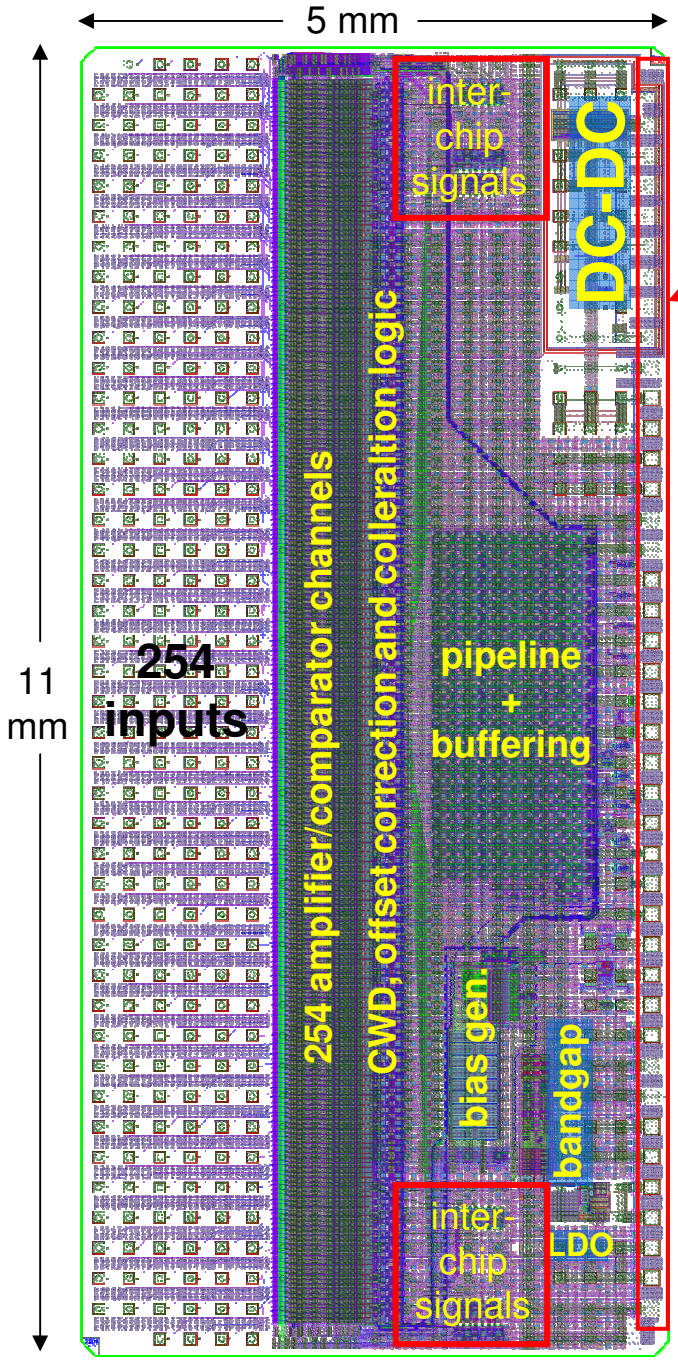
stub shift register: test feature - shift out result of correlation operation at 40 MHz

trigger O/P: in normal operation 1 bit per BX indicates presence of high Pt stub

test pulse

charge injection to all channels (8 groups of ~32), programmable timing and amplitude

CBC2 layout



C4 layout, 250um pitch, 19 columns x 43 rows

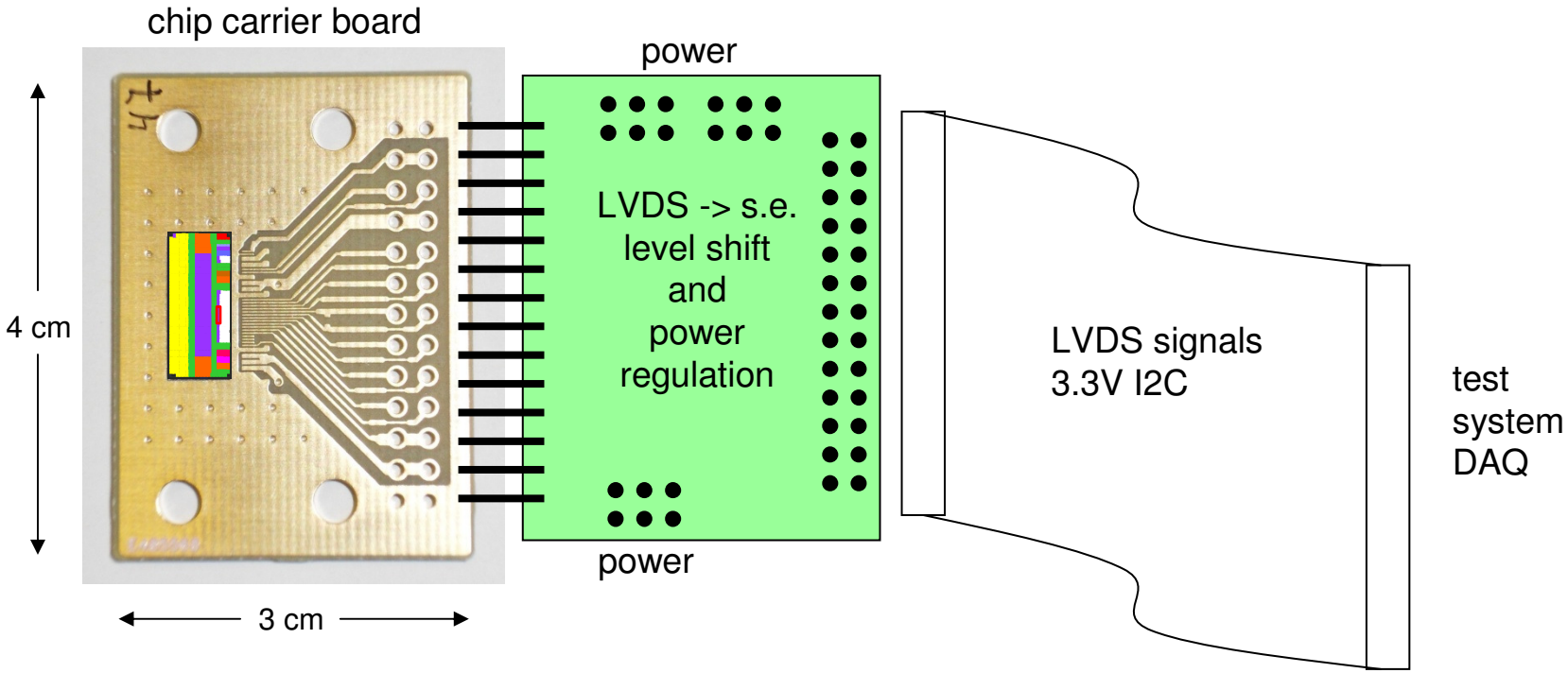
right-most column wire-bond (for wafer probe test)
- access to:
  - power
  - fast control
  - I2C
  - outputs

prototype powering features retained
- bandgap, LDO for analogue powering, same as prototype
- improved DC-DC switched capacitor circuit
  - slower switching edges & rad-hard layout

chip submitted for fabrication July 2012

test plans

wirebond test setup



use probe pads to wire-bond chip to simple carrier board

won't get best performance, but should be able to verify functionality

useful vehicle for wafer probe test development, radiation tests, …

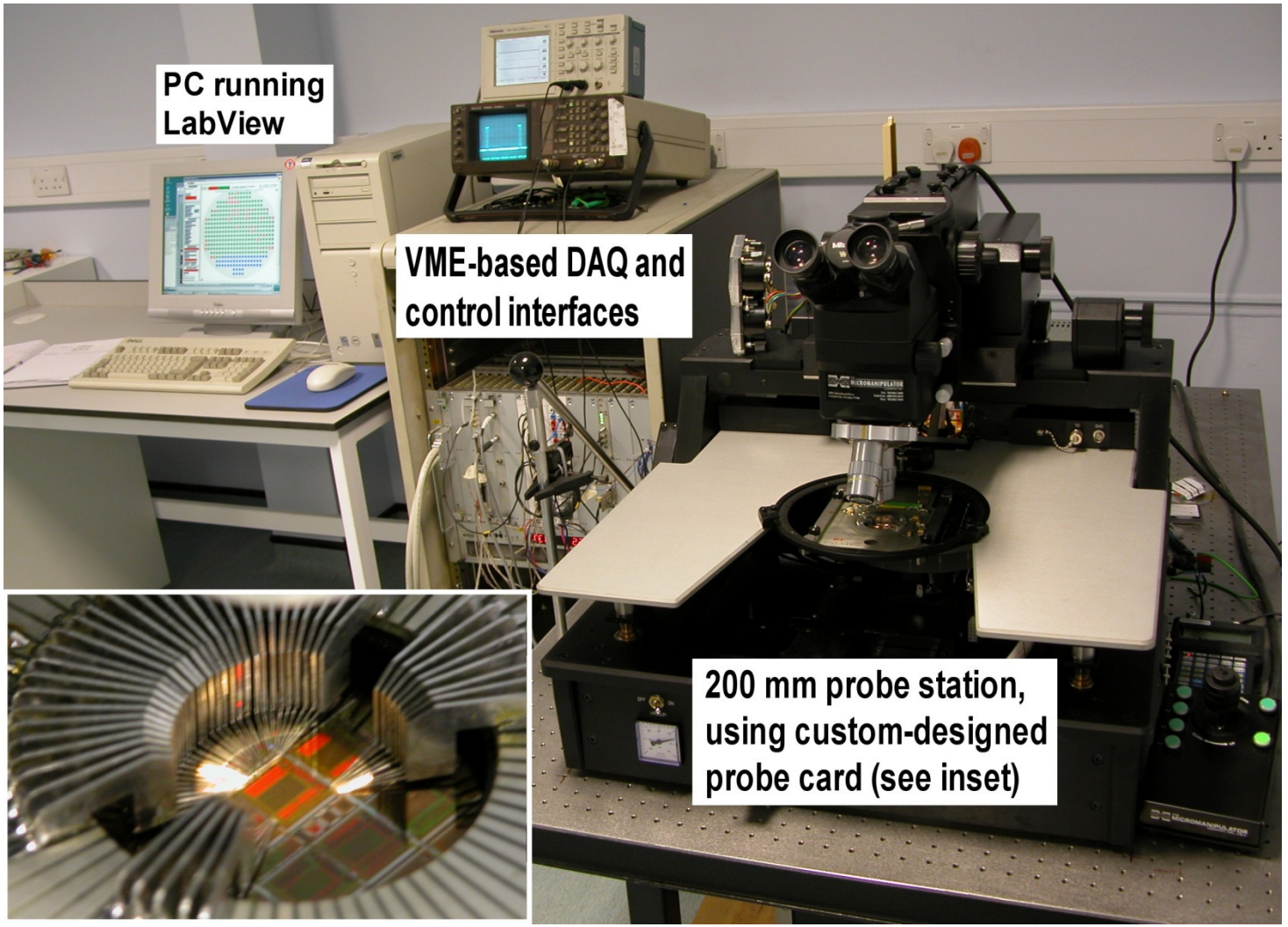
chip carrier board already exists, simple interface board design finished, production soon

wafer test system

need to screen chips for high multi-chip substrate yield
(also need to discriminate between chip and substrate problems)

re-use APV screening system

propose to use simple probe card to screen first wafers (check power consumption, maybe basic functionality)



Micromanipulator
8 inch semi–automatic
probe station

VME based
- ADC (8 bits)
- RAL SeqSi
  - 40 MHz CK/T1
- CERN VI2C I/F

PC controls both
DAQ (VME)
& probe-station (RS232)

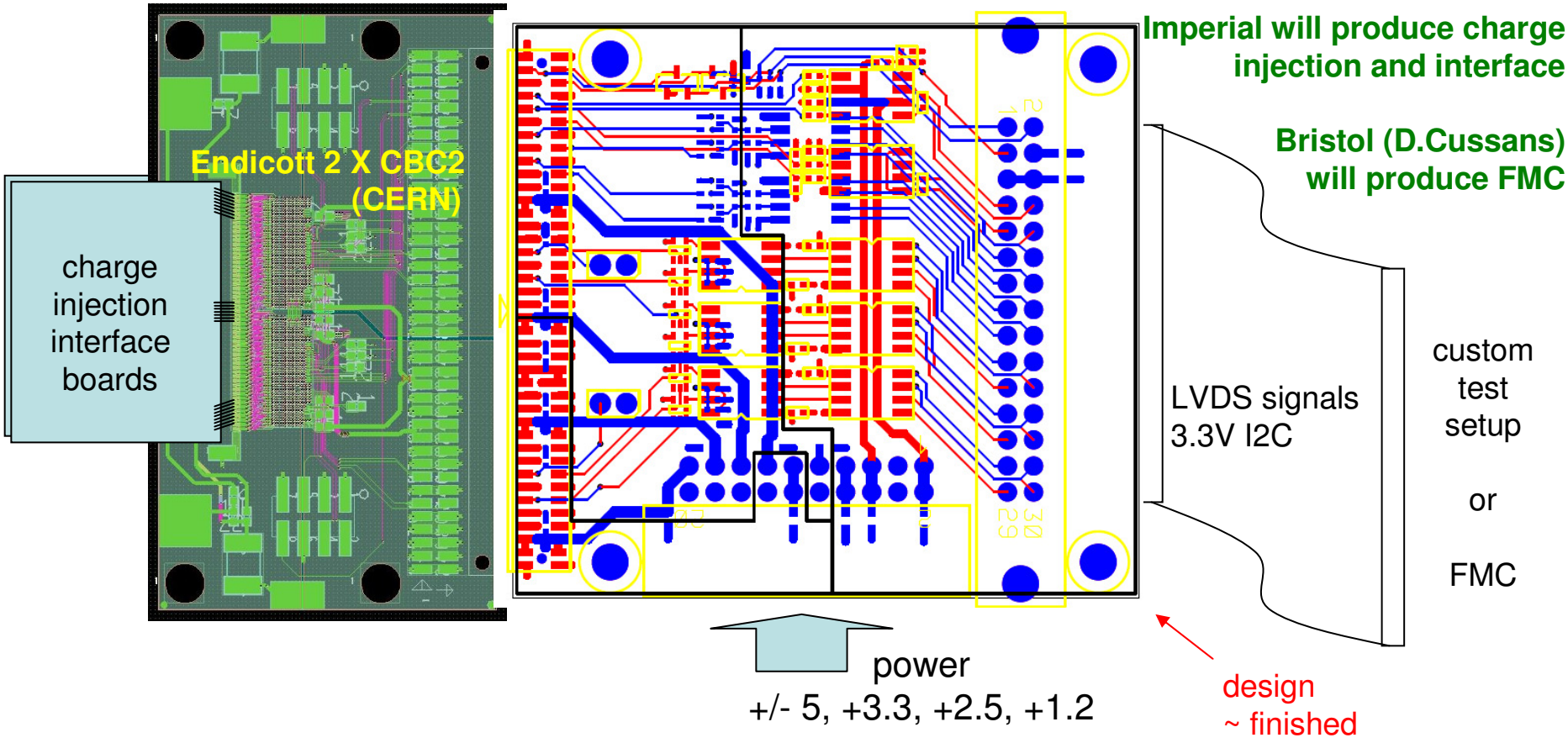
2xCBC2 substrate test setup

this will be the platform for detailed performance measurements

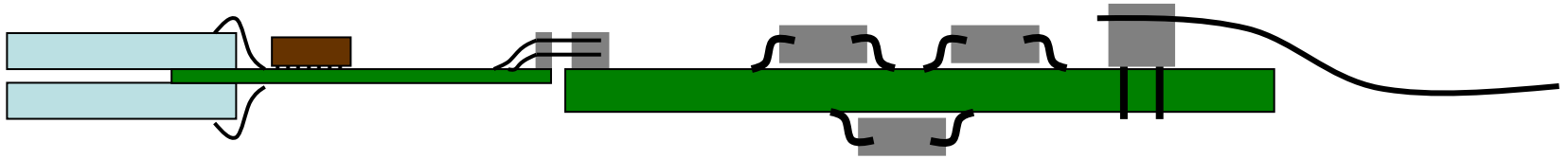
CERN (G.Blanchot) will look after 2xCBC2 substrate

Imperial will produce charge injection and interface

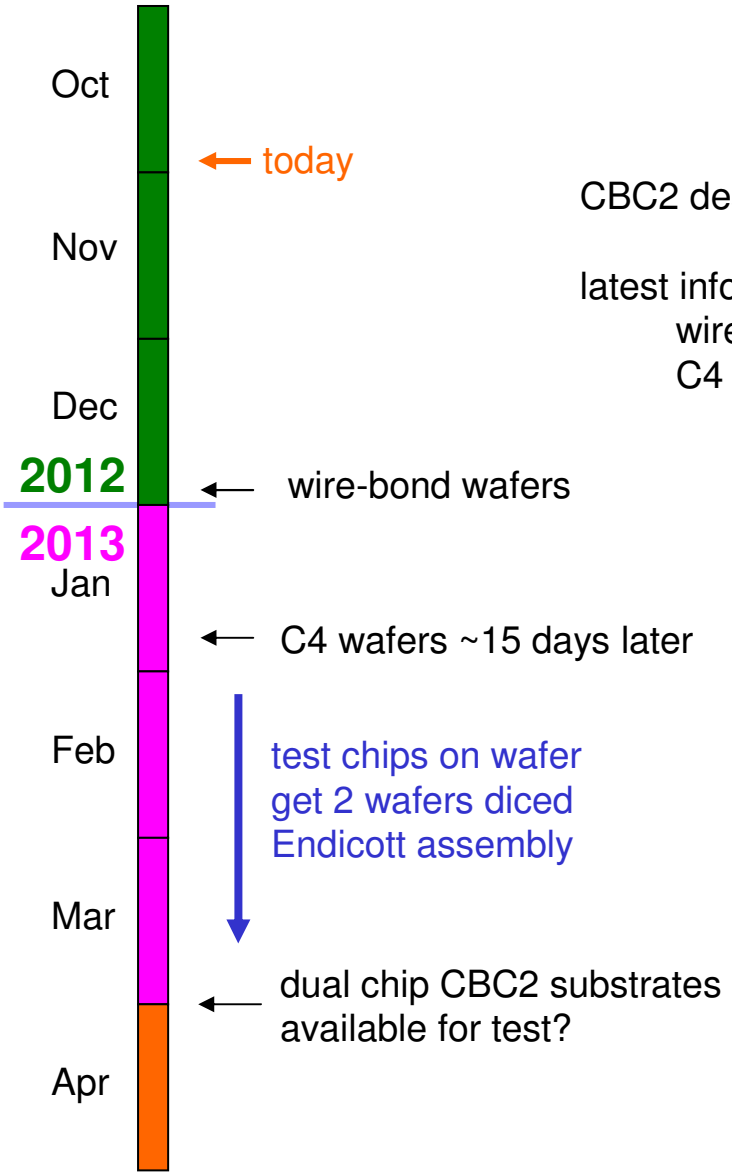
Bristol (D.Cussans) will produce FMC



Infineon sensors can be used to produce mini 2S-Pt module



timeline for next ~ 6 months



CBC2 design submitted in July – sharing wafer area with wire-bond chips

latest info:

wire-bond wafers scheduled to leave foundry Dec. 17th

C4 wafers ~ 15 days later

plan to perform wafer probe tests on C4 wafers

power consumption, maybe basic functionality

should give high yield of 2xCBC2 substrates

allows to discriminate between chip and bonding failures

Endicott require diced chips for 2xCBC2 substrate assembly

allowing for shipment delays, wafer testing and cutting, assembly, …

- hard to see bump-bonded 2xCBC2 substrates available before 2nd quarter 2013

summary

CBC1 test beam

CBC + Infineon sensor test beam looks like a success so far

stable behaviour - lots of data to study in detail
cluster width, efficiency vs. threshold, …

data transmitted successfully to GLIB based DAQ

CBC2

bump-bond chip for 2S-Pt module submitted in July - first wafers expected end of year

test setups in preparation

assembled 2xCBC2 substrates for detailed chip performance characterization
anticipated ~ 2nd quarter 2013

extra

CBC prototype summary

features

- designed for short strips, ~2.5–5cm, < ~ 10 pF
- full size prototype - 128 channels
  - 50 μm pitch wirebond
- binary un-sparsified readout
- powering test features
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analog FE

main functional blocks

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- fast (SLVS) and slow (I2C) control interfaces

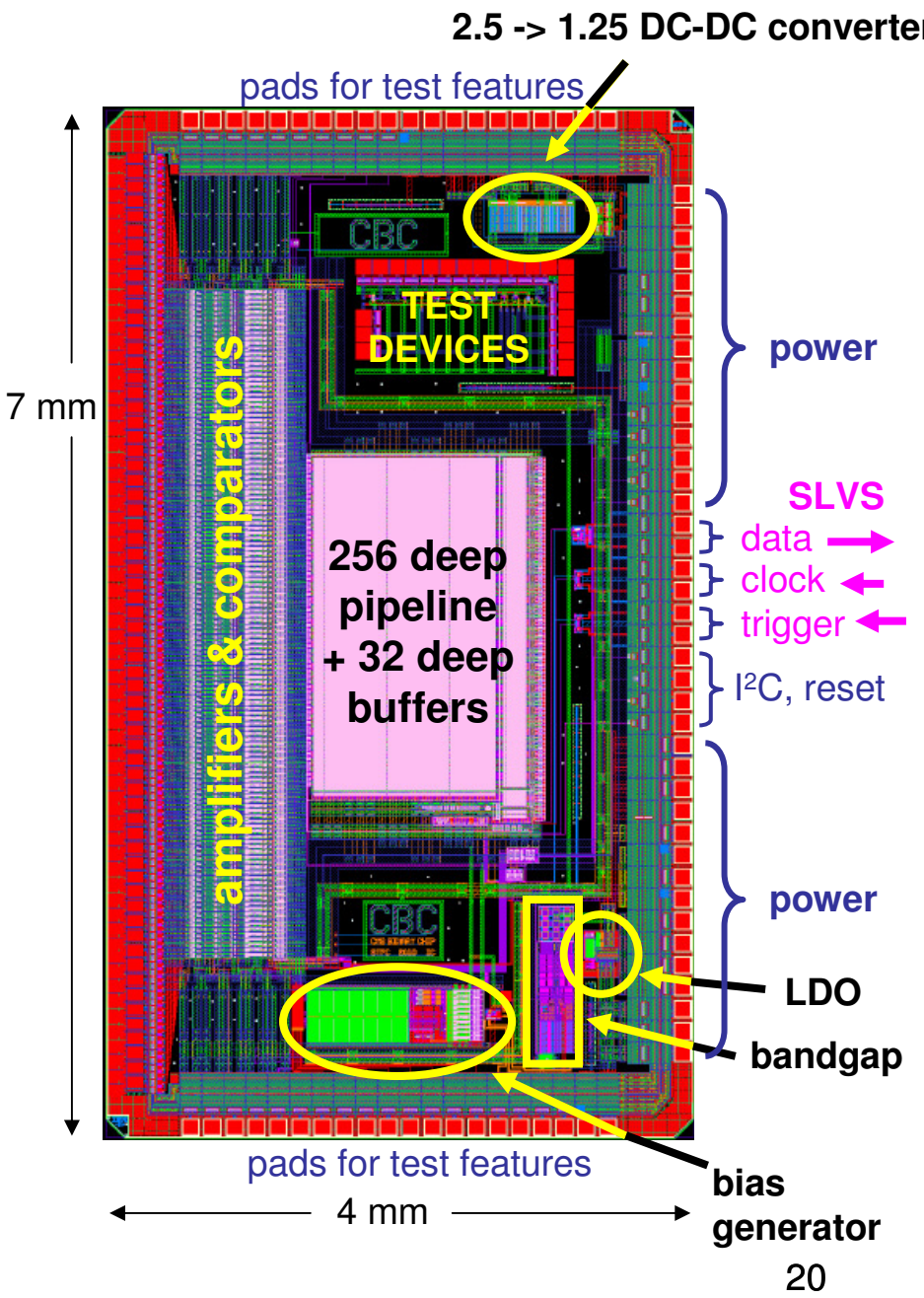
front end

- DC coupling to sensor – up to 1 uA leakage
- can be used for both sensor polarities

for 5 pF input capacitance

noise ~800e

power ~300 μW / chan.



neighbour chip signals - comparator O/Ps

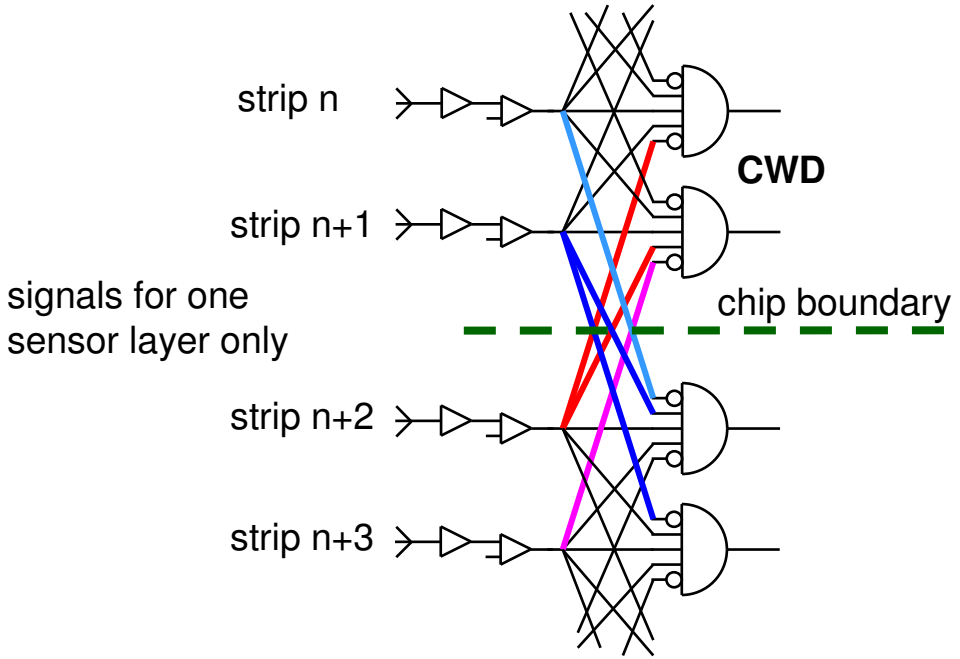
need to transfer signals across chip boundaries

for cluster width < 3 need (for each sensor layer)

to pass comp. O/Ps from 2 edge channels to neighbour
to receive comp. O/Ps from 2 edge channels on neighbour

=> 4 signals for single sensor layer

=> 8 signals for both layers



neighbour chip signals - CWD O/Ps

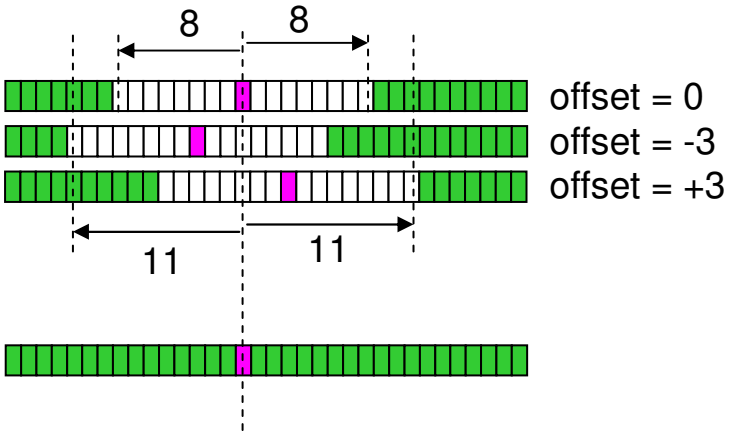
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

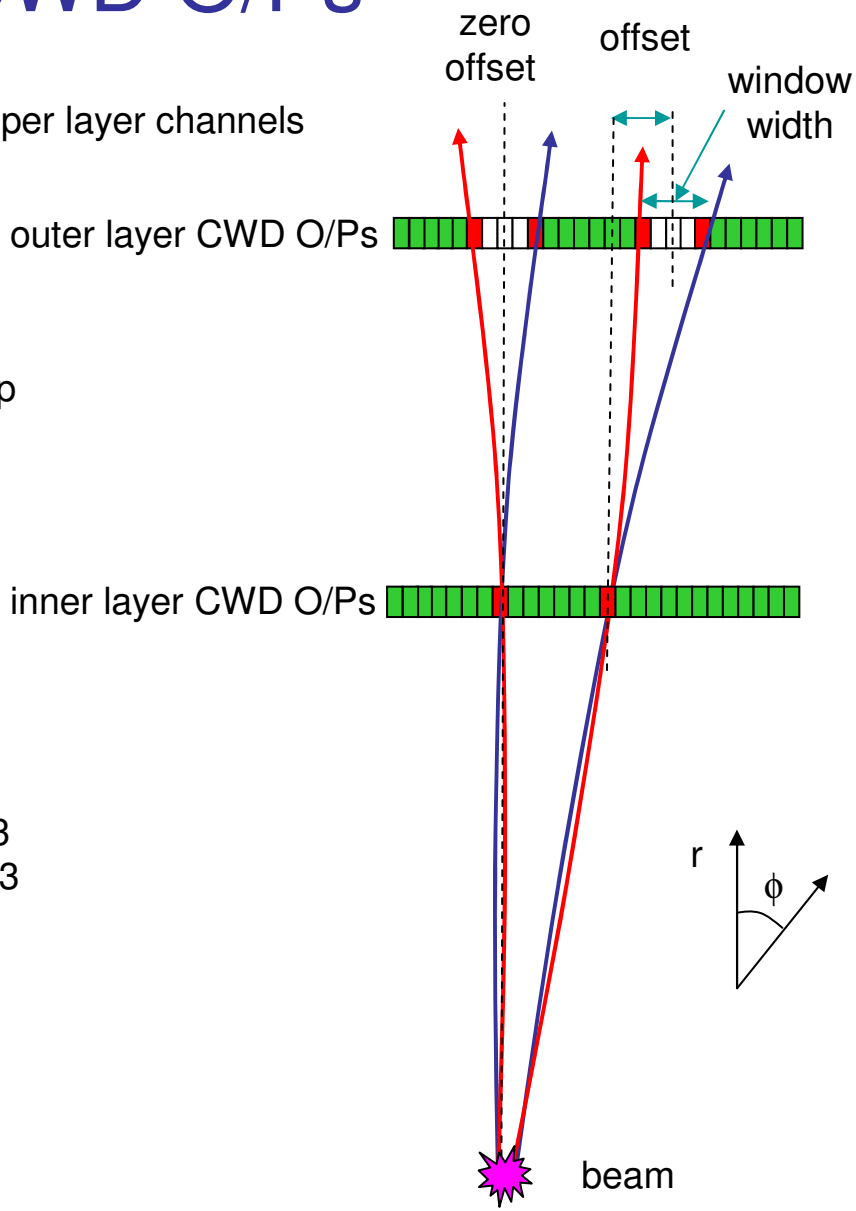
window defines Pt cut
width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
11 to receive from neighbouring chip

= 22 signals





adding comp O/Ps -> 30 signals altogether, top and bottom of chip