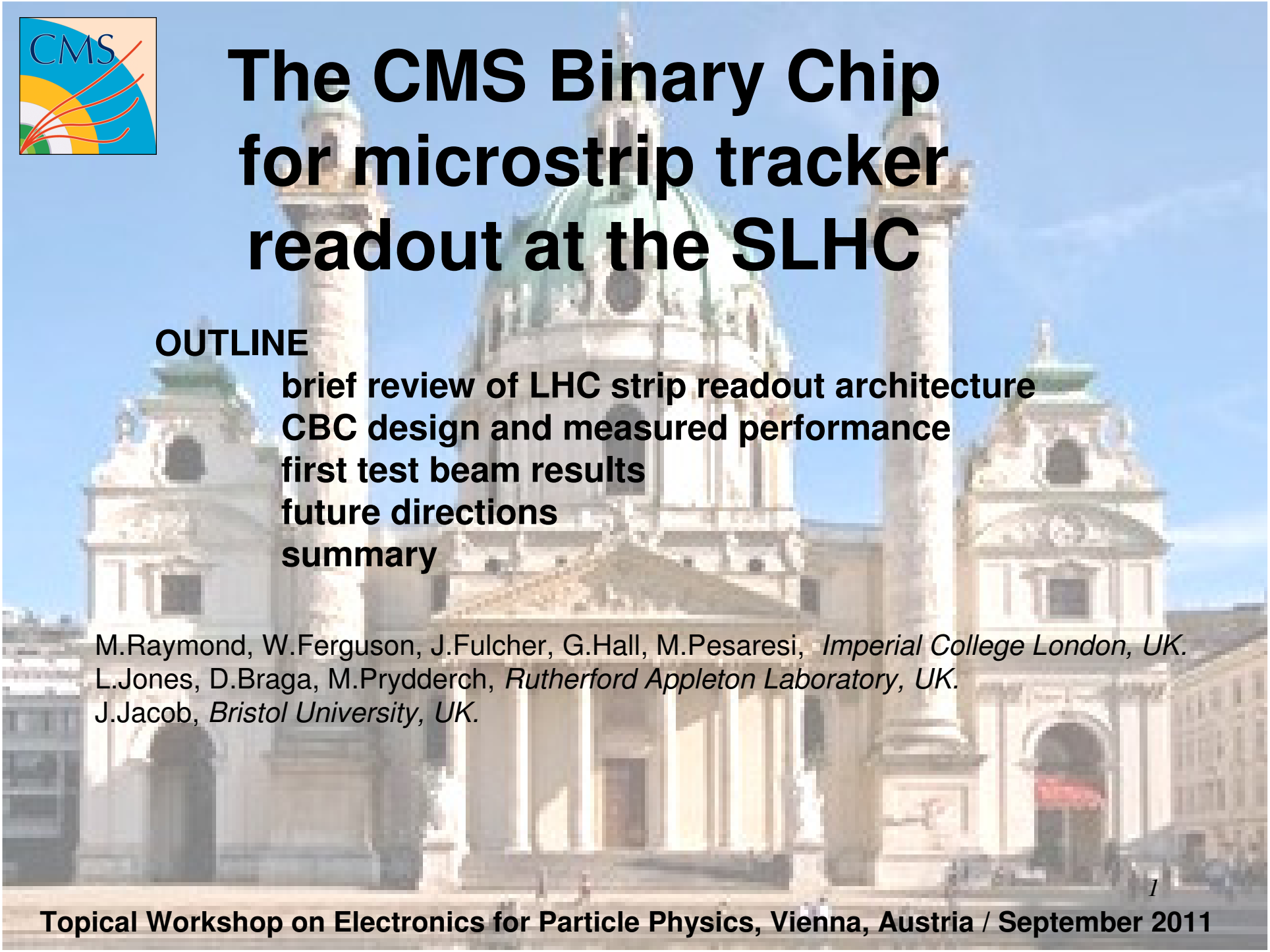


# The CMS Binary Chip for microstrip tracker readout at the SLHC

**OUTLINE**

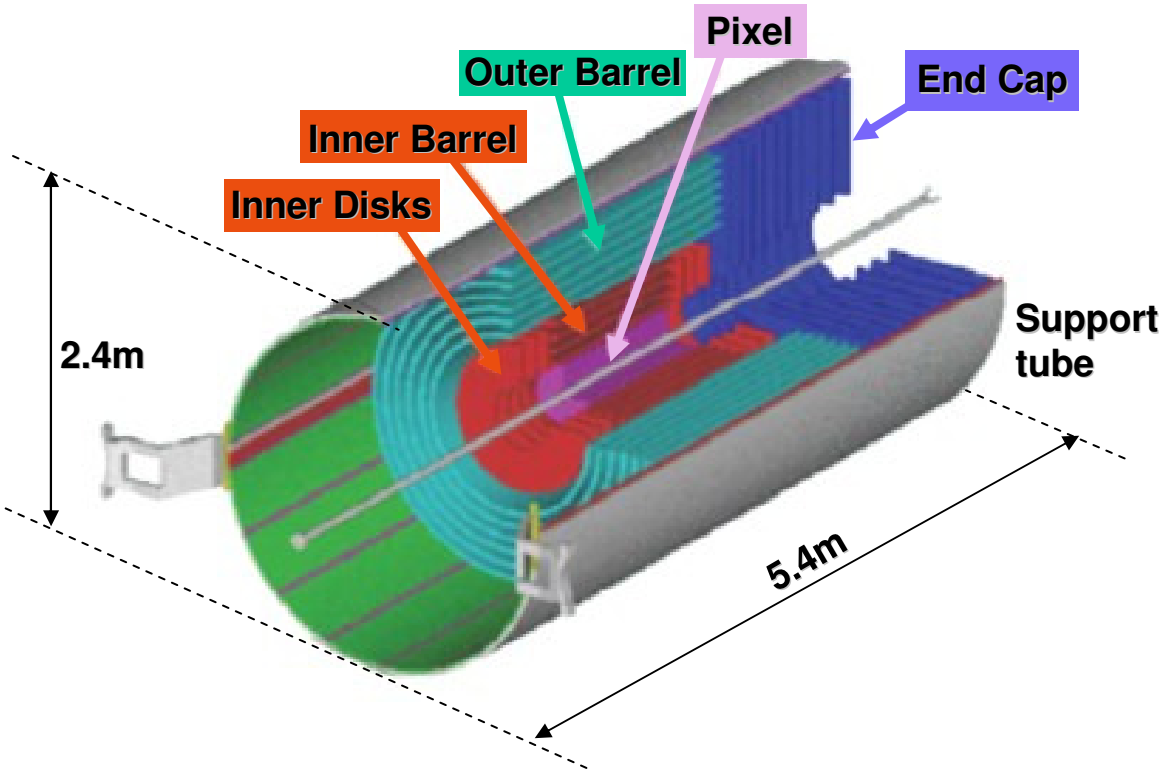
- **brief review of LHC strip readout architecture**
- **CBC design and measured performance**
- **first test beam results**
- **future directions**
- **summary**

M.Raymond, W.Ferguson, J.Fulcher, G.Hall, M.Pesaresi, *Imperial College London, UK.*
L.Jones, D.Braga, M.Prydderch, *Rutherford Appleton Laboratory, UK.*
J.Jacob, *Bristol University, UK.*



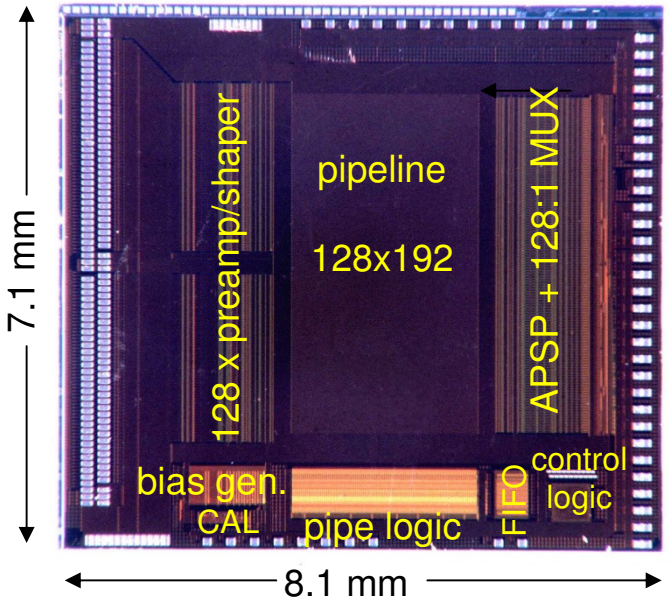
**Topical Workshop on Electronics for Particle Physics, Vienna, Austria / September 2011**

# CMS LHC tracker



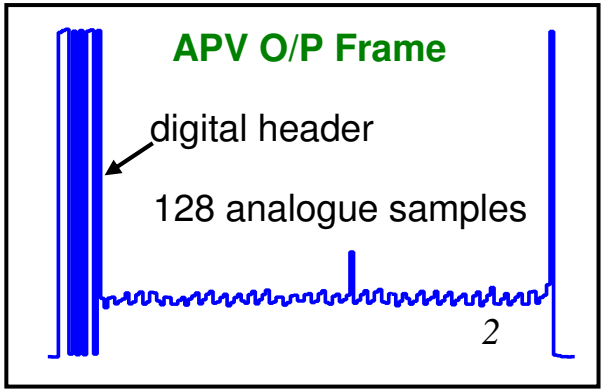

~ 200 m$^2$ sensor area
~ 15,000 detector modules altogether
22 different types
~ 10$^7$ strips, ~75,000 FE chips (APV25)

APV25




inner & outer barrels, endcaps instrumented by Si microstrips
up to ~ 18 cm (~25 pF), AC coupled

read out by APV25 chips
0.25 µm CMOS
power ~ 2.7 mW / channel
analogue, unsparsified readout
analogue optical link off-detector



# SLHC challenges

**power consumption**

luminosity increases -> higher track density -> higher granularity tracker required
=> shorter strips and more channels

**power delivery**

need to bring in power at higher voltages to limit current in cables
=> serial powering or DC-DC conversion inside tracker

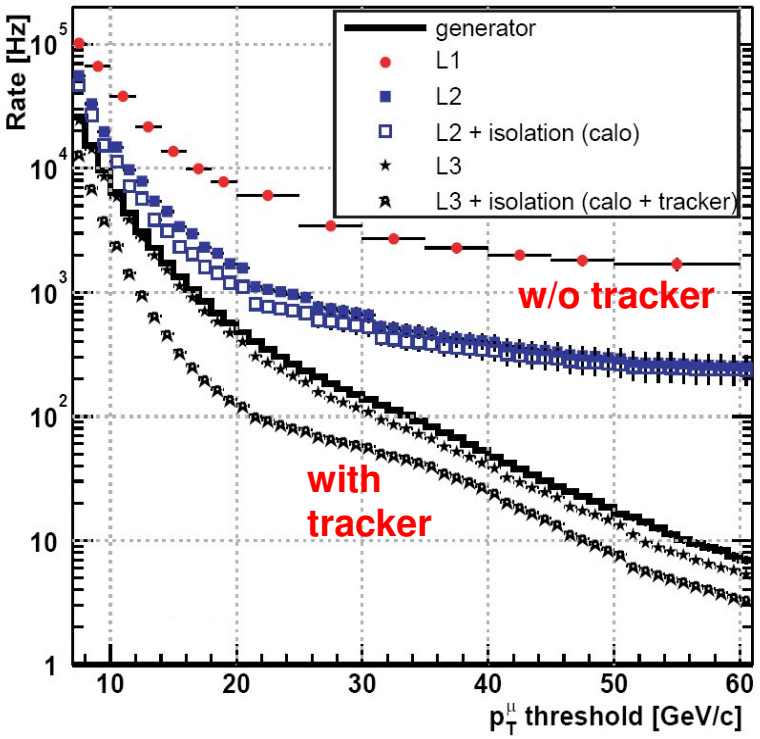
CMS tracker has adopted DC-DC as baseline

**triggering**

current tracker doesn't contribute to L1 trigger

can't keep SLHC L1 rate at 100 kHz without tracker info
=> new architectures needed

**L=$10^{34}$ muon trigger rate**



# CMS Binary Chip (CBC)

**what we like about our present system**

analog pulse height info
(made possible by custom analog link)

system simplicity - no on-detector sparsification
-> occupancy independent data volume

**what must change for SLHC**

off-detector links -> high speed digital
follows commercial trends

=> large data volumes if keep pulse height info

**CBC short strip readout chip prototype for SLHC**

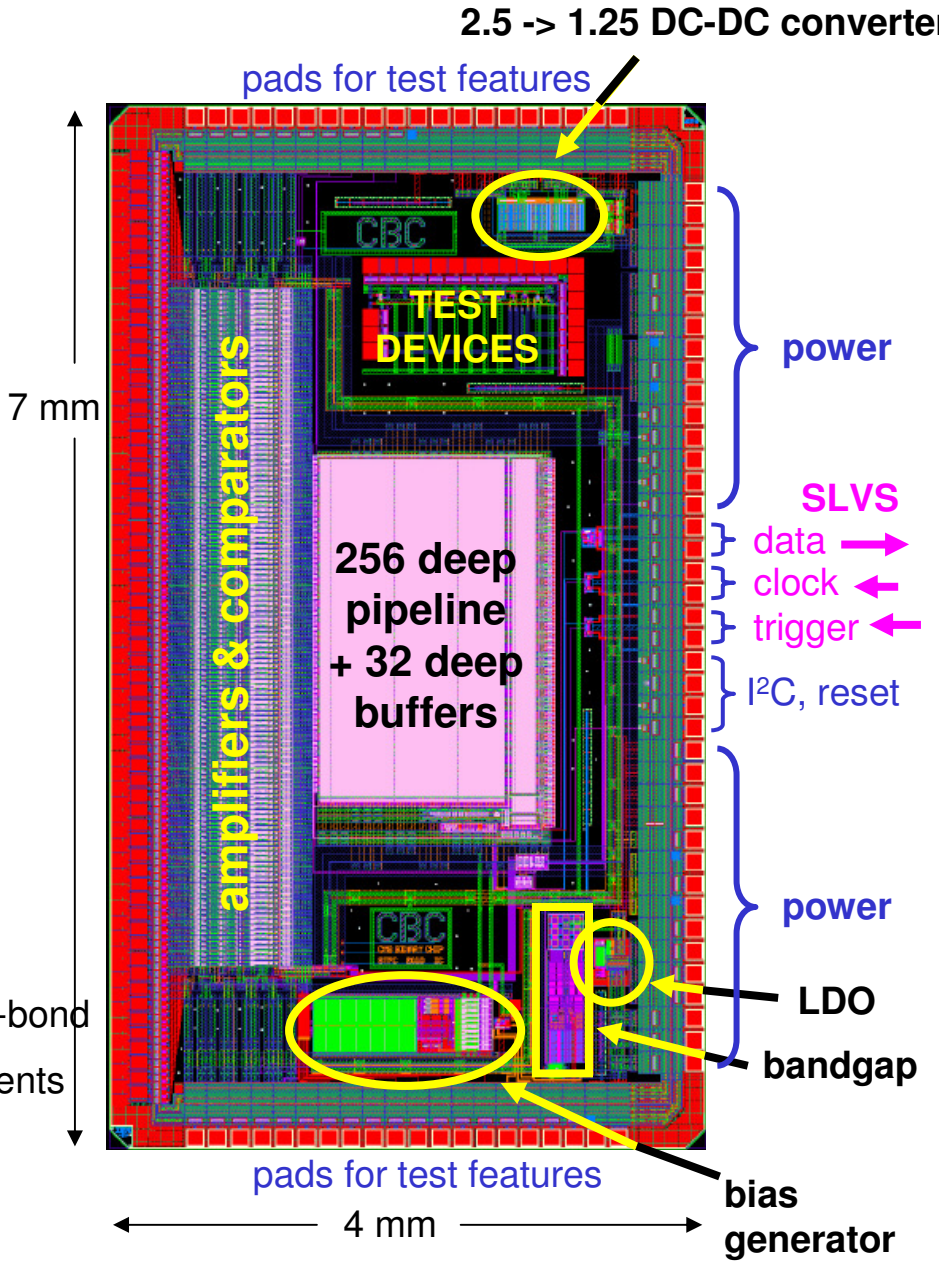
binary, unsparsified architecture
retains chip and system simplicity
but no pulse height

designed for short strips, ~2.5 - 5cm, < ~ 10 pF

full size prototype - 128 channels, 50 μm pitch wire-bond

256 deep pipeline + 32 deep buffer for triggered events

powering test features:
2.5 -> 1.2 DC-DC converter
LDO regulator (1.2 -> 1.1) feeds analog FE

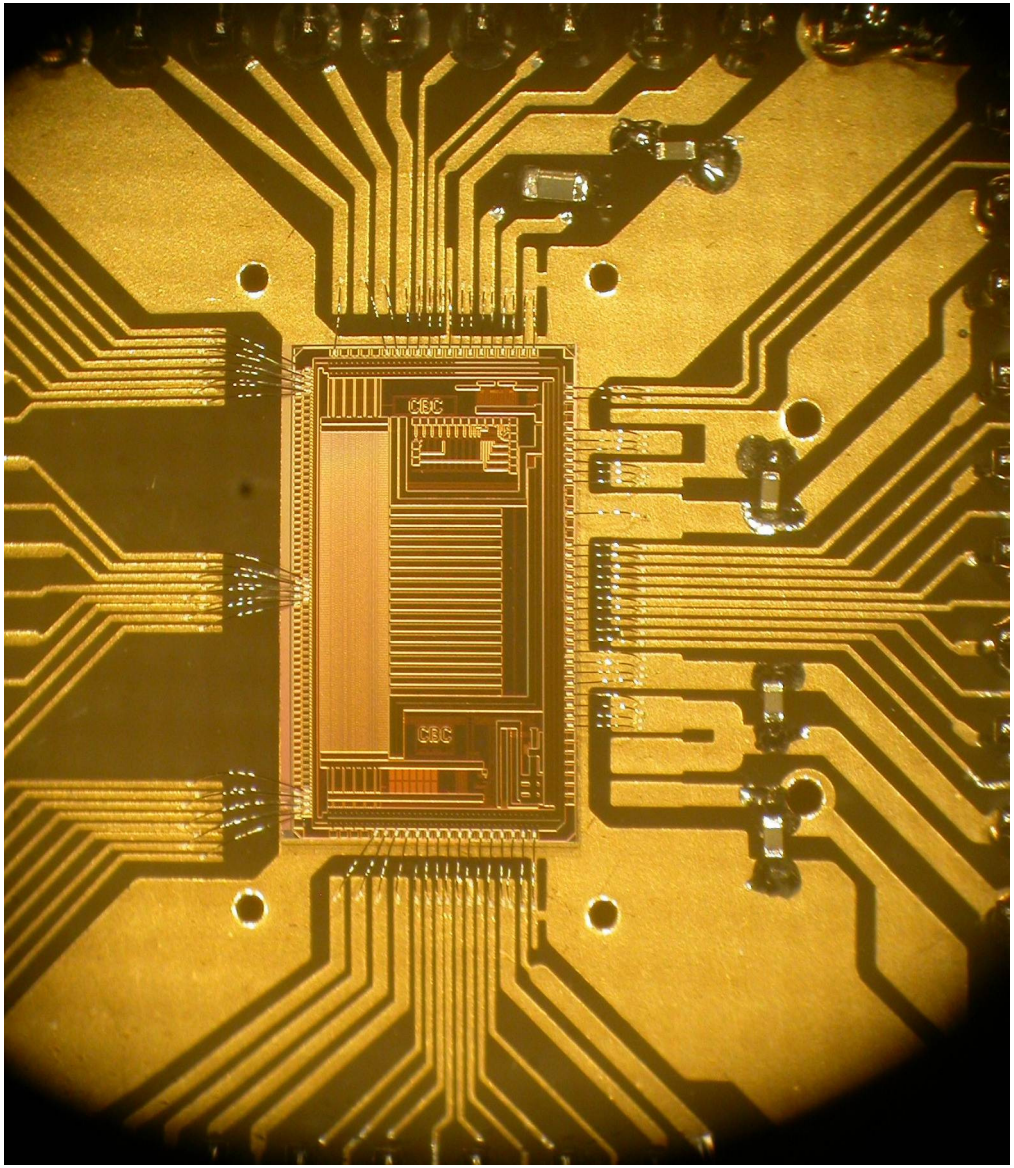


# CBC under test

produced in IBM 130 nm CMOS process

2010 CERN MPW run

chips on test bench since Feb. 2011




**CBC on test board**

# basic functionality

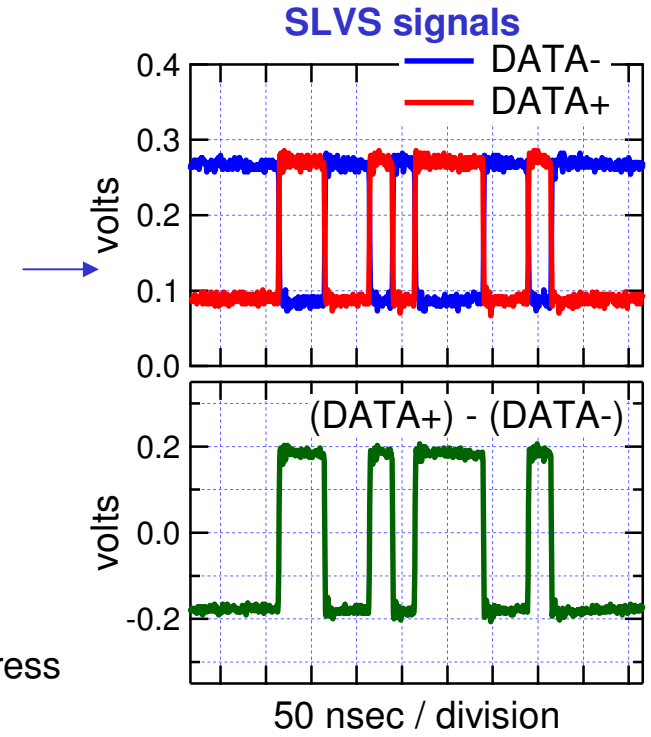
**communication interfaces**

**fast**: SLVS (Scalable Low Voltage Signalling) - CERN
thanks to Sandro Bonacini and Kostas Kloukinas
used for 40 MHz clock I/P, L1 trig and data out

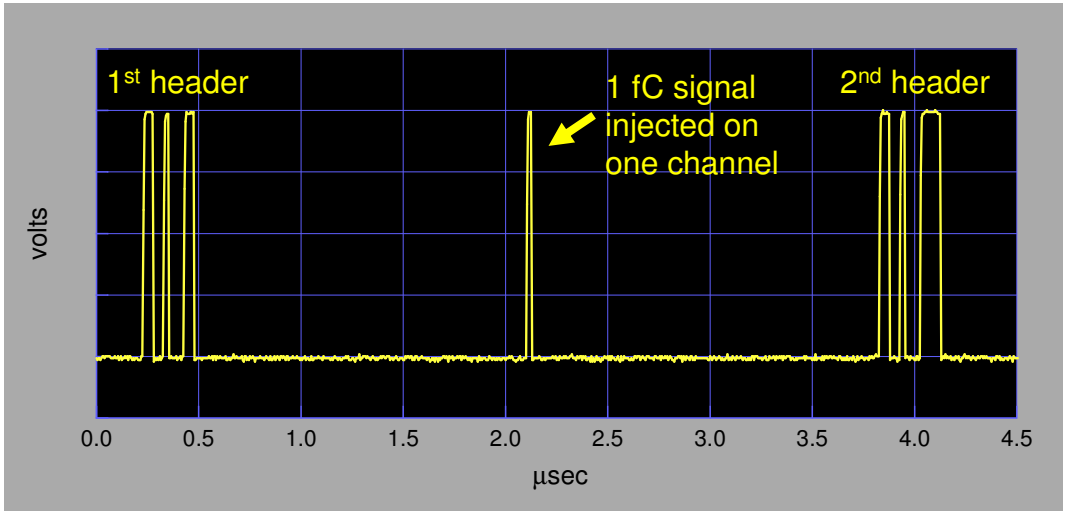
**slow:** I2C - used to programme
bias generator
operational modes, latency,..
128 comparator threshold trim values

**output data frame**

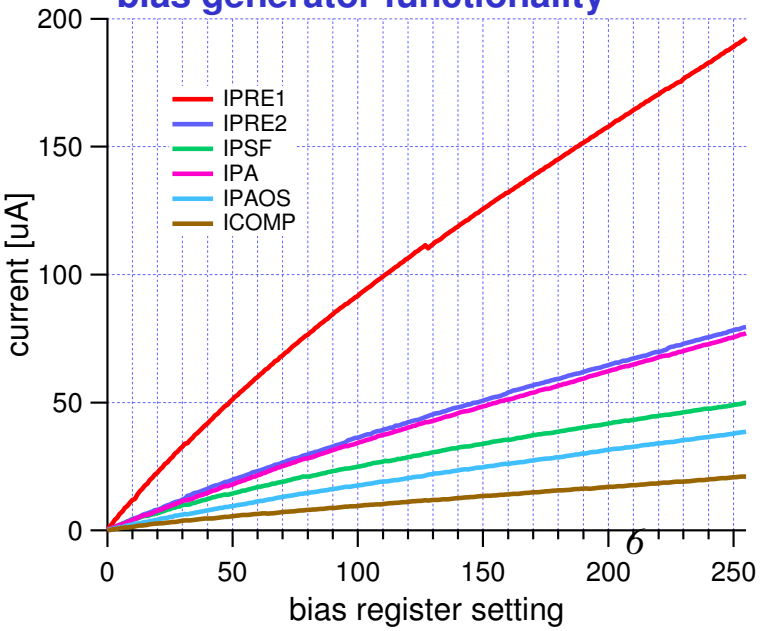
following trigger get 12-bit header
2 start bits, 2 error bits (latency, fifo overflow), 8 bit pipe address
followed by 128 channel bits



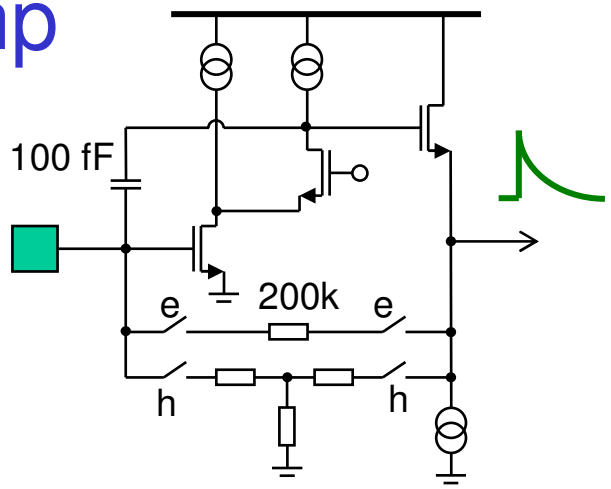

**e.g. 2 consecutive data frames (2 triggers)**




**bias generator functionality**



# preamp




designed to allow DC coupling

200k resistor feedback absorbs $I_{LEAK}$

noise contribution ~ 200 e

200mV DC shift at O/P for $I_{LEAK}$=1 µA

$R_f.C_f$ implements short 20ns diff. time constant

=> no pile-up issues

works with both sensor polarities

**electrons mode (n-in-p)**

single 200k resistor, leakage shifts output +ve

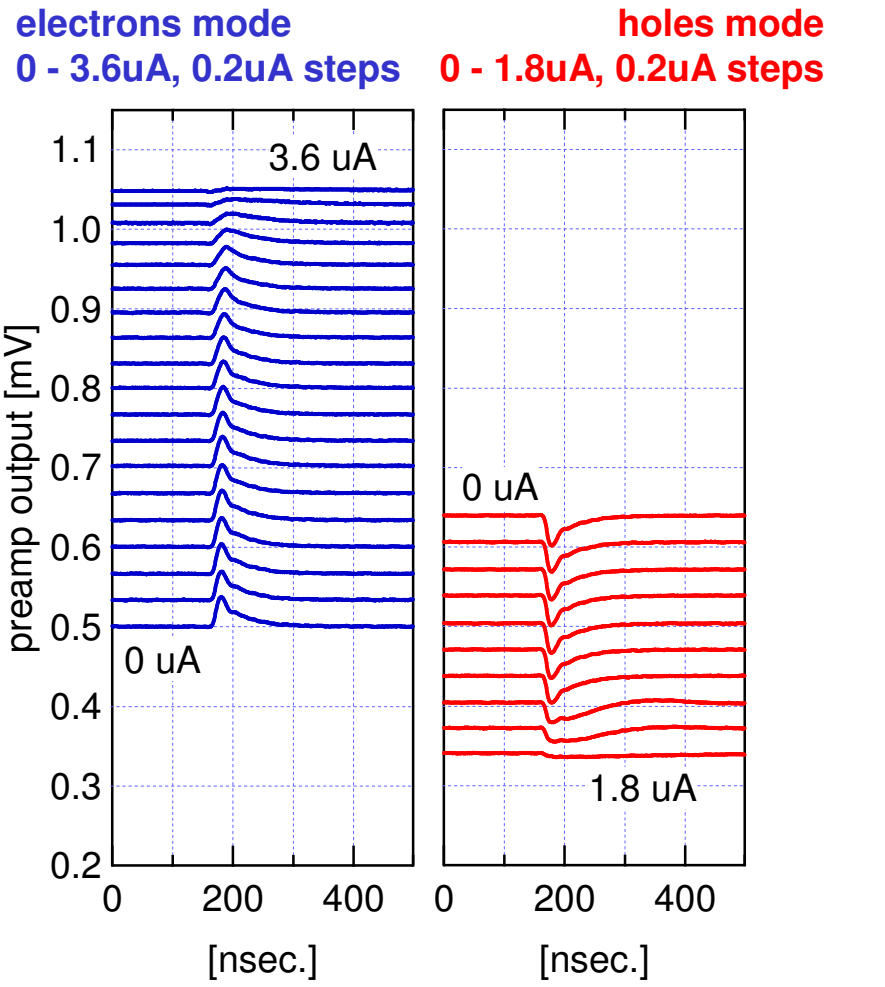
plenty of headroom

**holes mode (p-in-n)**

T network (≡ 200k) produces +ve offset

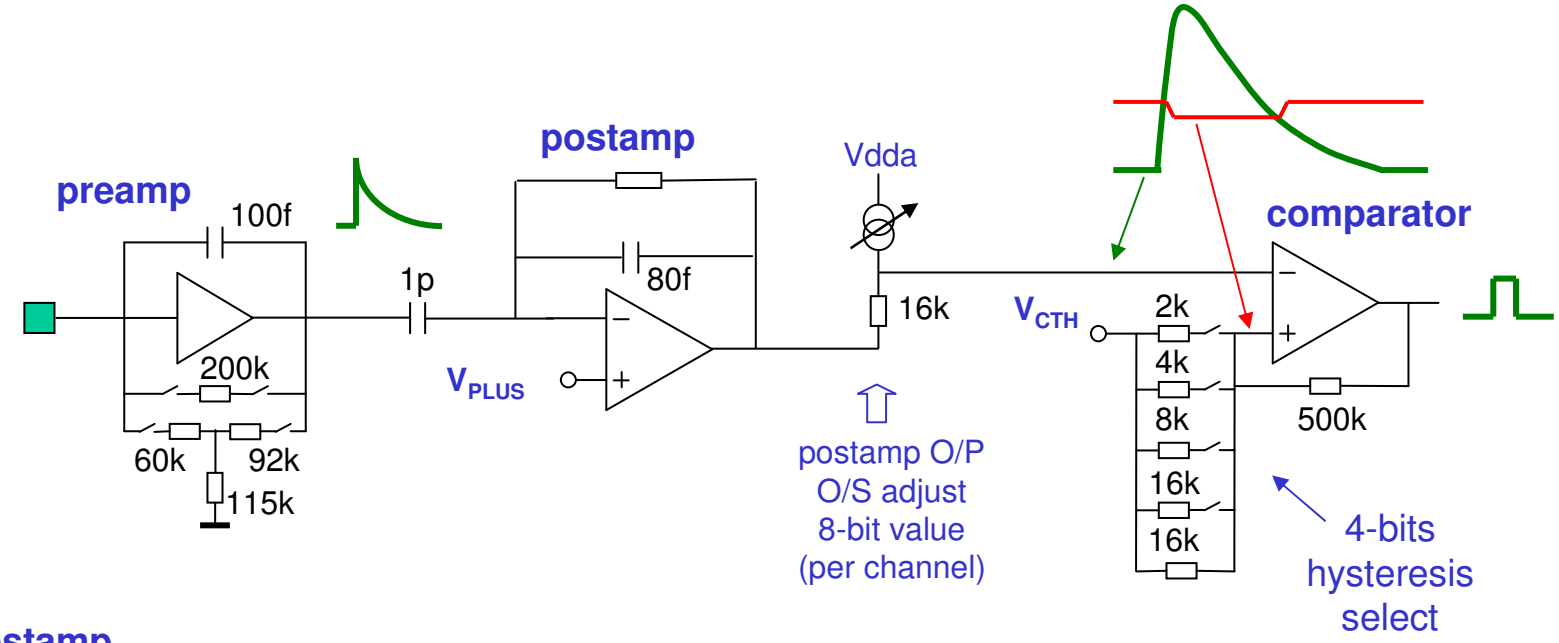
leakage shifts output -ve, sufficient headroom for 1 uA

**effect of leakage current on preamp O/P waveforms measured on test channel**




(note: waveforms include ~ 300 mV offset due to source follower on test channel O/P)

# preamp, postamp & comparator




**postamp**

provides gain and low pass noise filtering

overall pulse peaking time 20 nsec

gain ~ 50 mV / fC

AC coupling to preamp removes any DC shift from leakage current

individually programmable O/P DC level implements channel threshold tuning

**comparator**

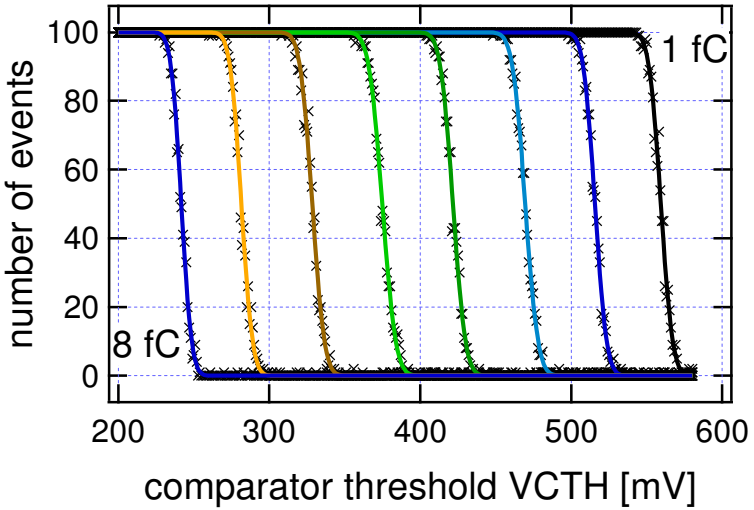
global threshold $V_{CTH}$

programmable hysteresis

# S-curves & gain

inject charge and sweep comparator threshold -> s-curve

**s –curves (electrons mode)**



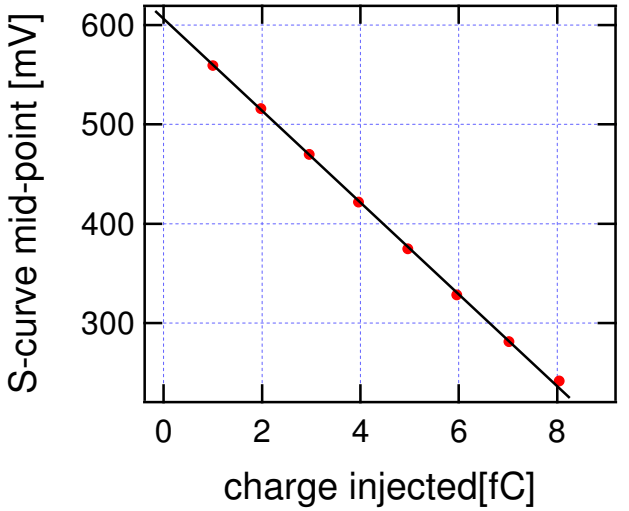

← s- curves for signals in range 1 - 8 fC : 1 fC steps

s-curve mid-point vs. charge injected →

gain ~ 50mV / fC

linearity only important in region where comparator threshold will be set (~ 1fC)

**gain**



# noise and analogue power

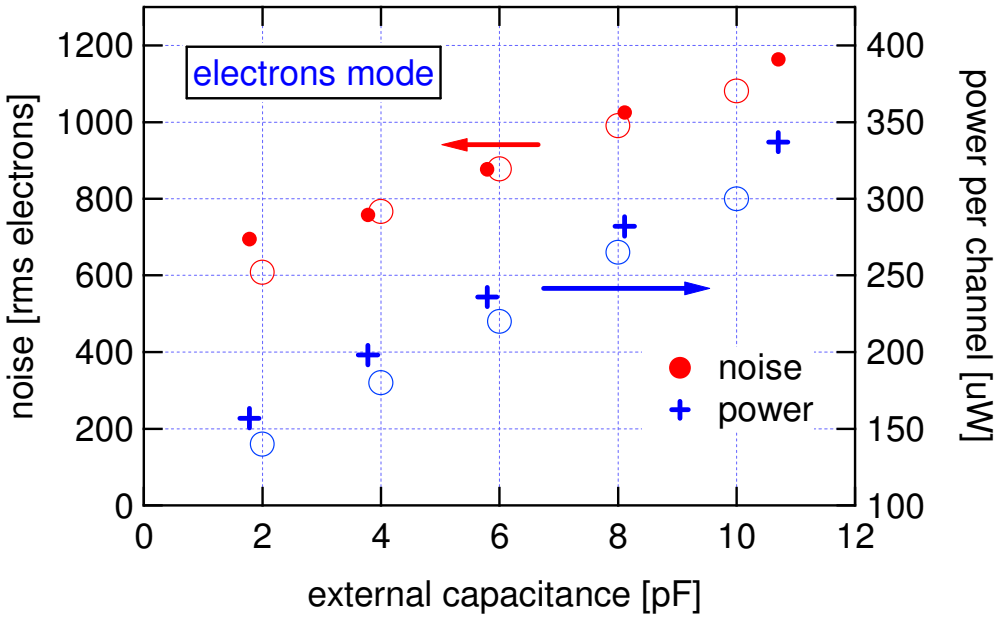
**measurement technique**

preamp O/P risetime varies with I/P capacitance

risetime $\propto C/g_m$
$\propto C/I_{DS}$ (W.I.)

=> need to vary current in input transistor to keep pulse shape independent of C

=> analogue power consumption will depend on C




**noise determined from s-curves**

close agreement between measurements (solid symbols) & simulations (open circles)

target spec.: < 1000e for 5 pF sensor
measurement: ~ 800e for analog power < 250 µW/chan

very little difference between electrons and holes modes

# comparator - threshold uniformity & tuning

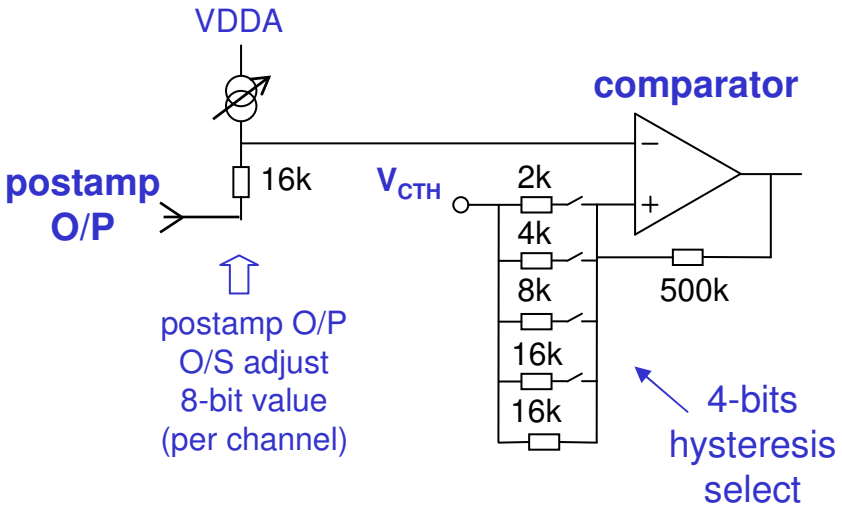
all channels have same global threshold

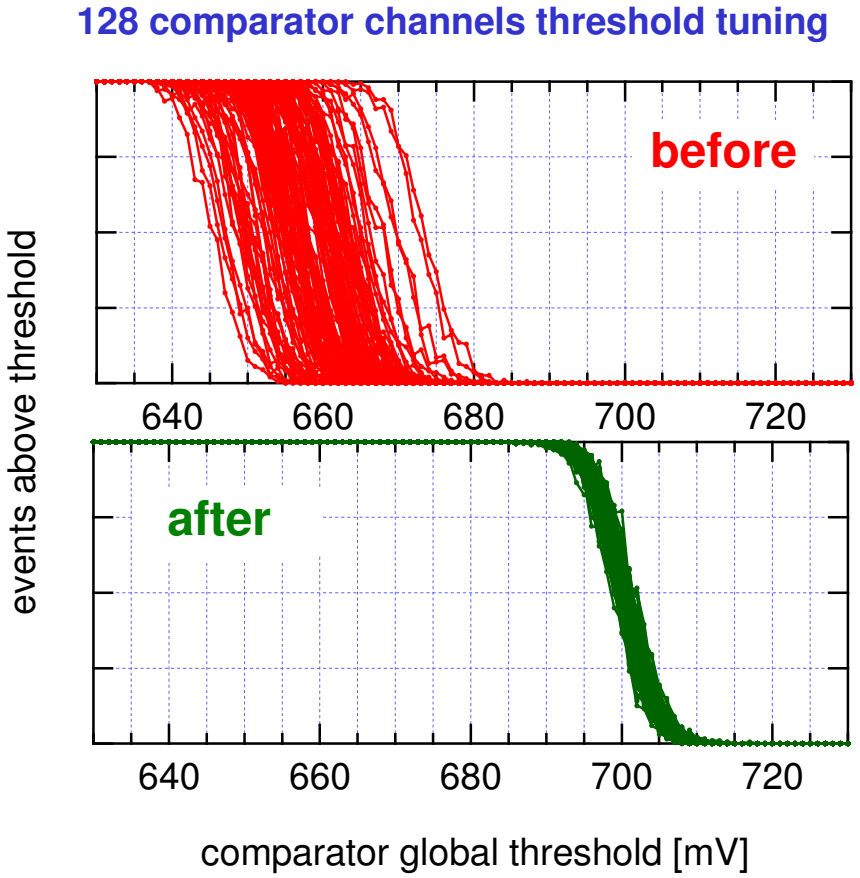
individual channel tuning achieved by introducing programmable offset at postamp O/P

128 registers, 8-bit precision

before tuning pk-pk threshold spread ~30 mV (~ 0.6 fC)

tuning reduces spread to ~ mV level



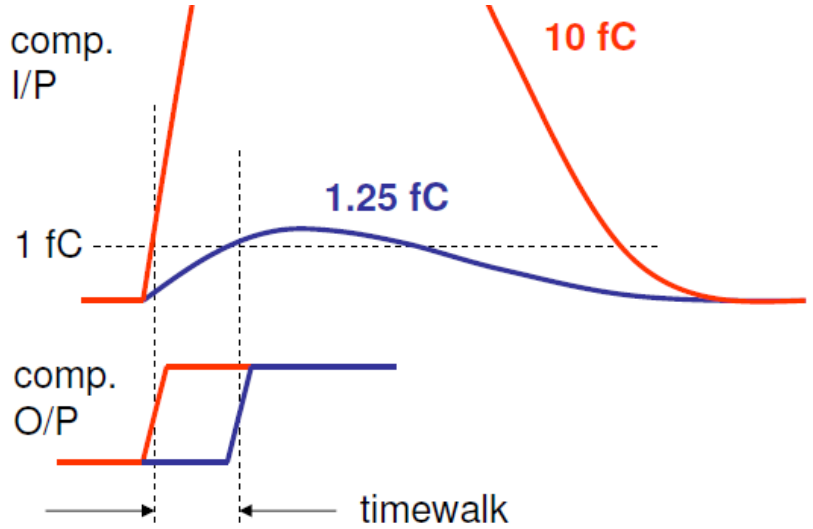



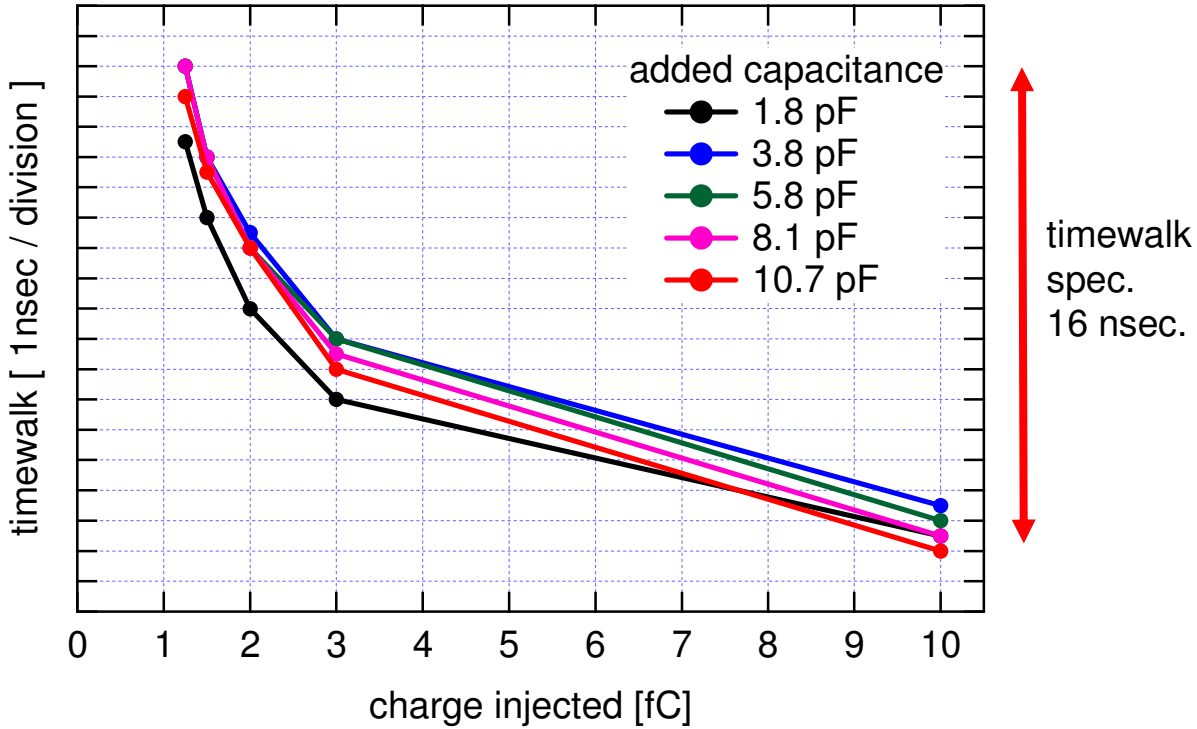
# comparator - timewalk

measure by sweeping time of charge injection
always triggering same pipeline location

timewalk spec. < 16 ns between 1.25 and 10 fC
signals, with comp. threshold set to 1 fC

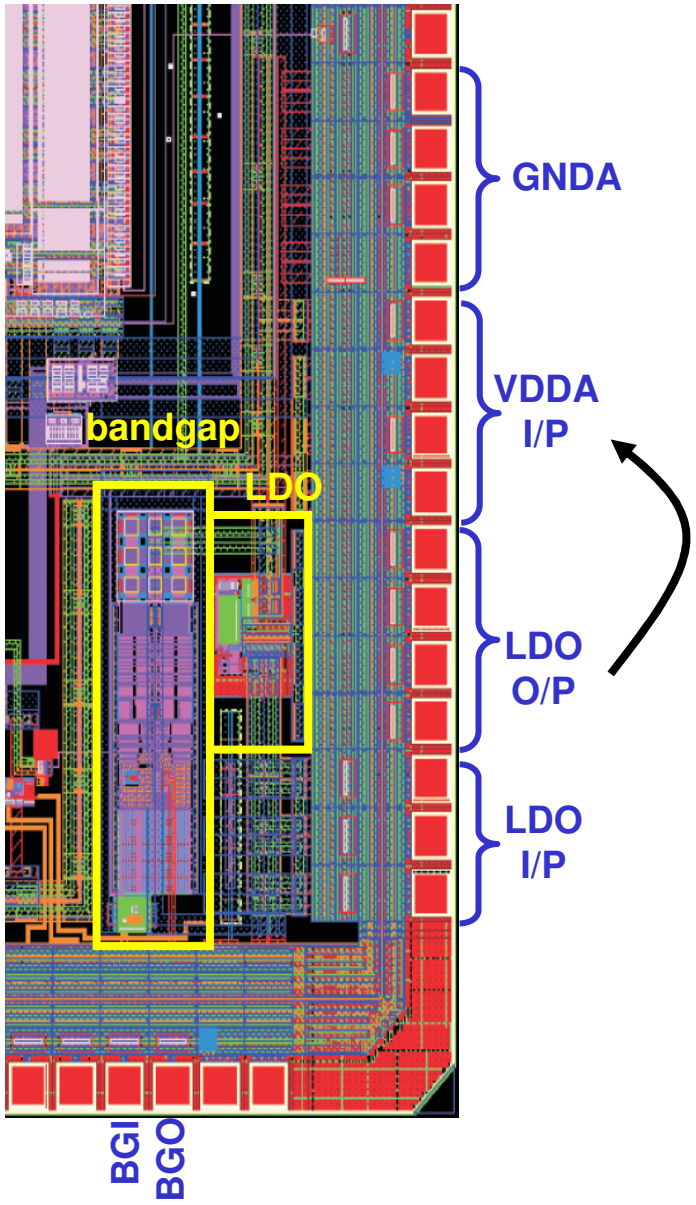
measurements just within spec.




timewalk
spec.
16 nsec.

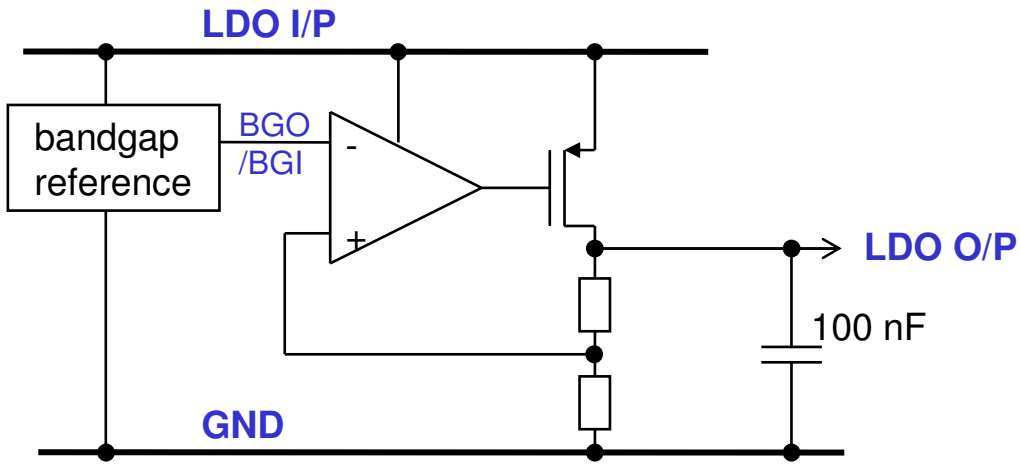
# powering - LDO




CMS SLHC tracker plans to use DC-DC powering scheme
=> possible noise on power rails

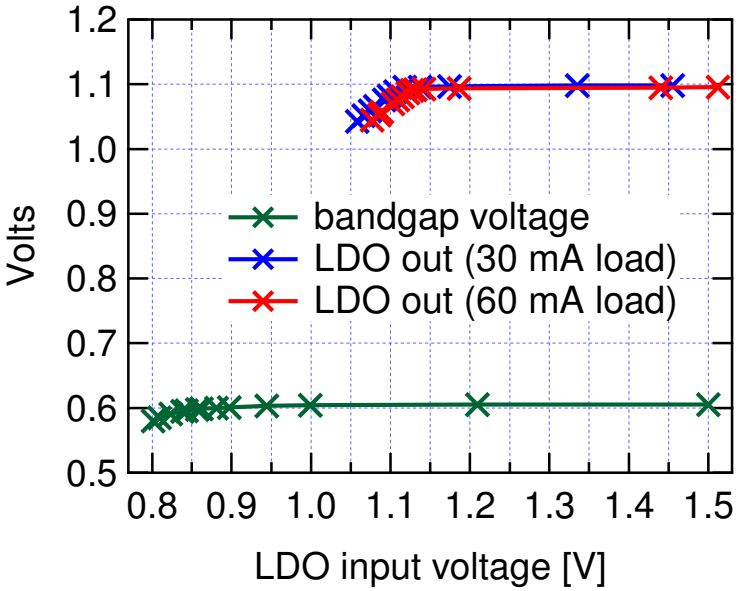
on-chip LDO included to provide clean, regulated rail to analog FE
~ 1.2 Vin, 1.1 Vout

uses CERN bandgap as reference (0.6 V)
thanks to Xavi Cudie & Paulo Moreira



# LDO performance

## Vout vs. Vin

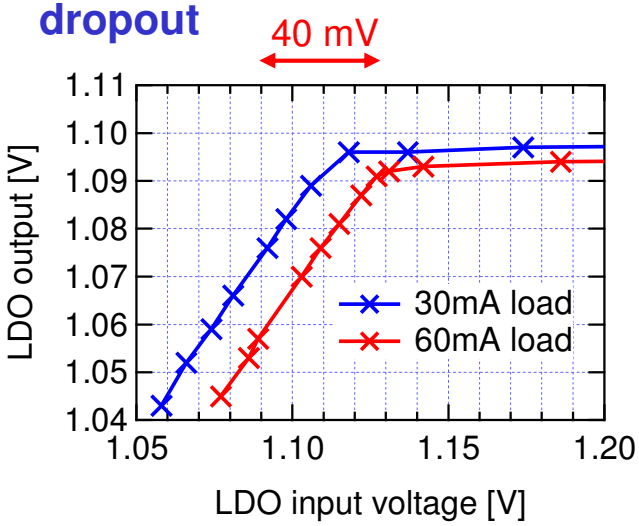



## DC measurements

bandgap flat down to 0.9 V

dropout ~ 40 mV for 60 mA load

## dropout




## AC measurements

need to decouple bandgap output

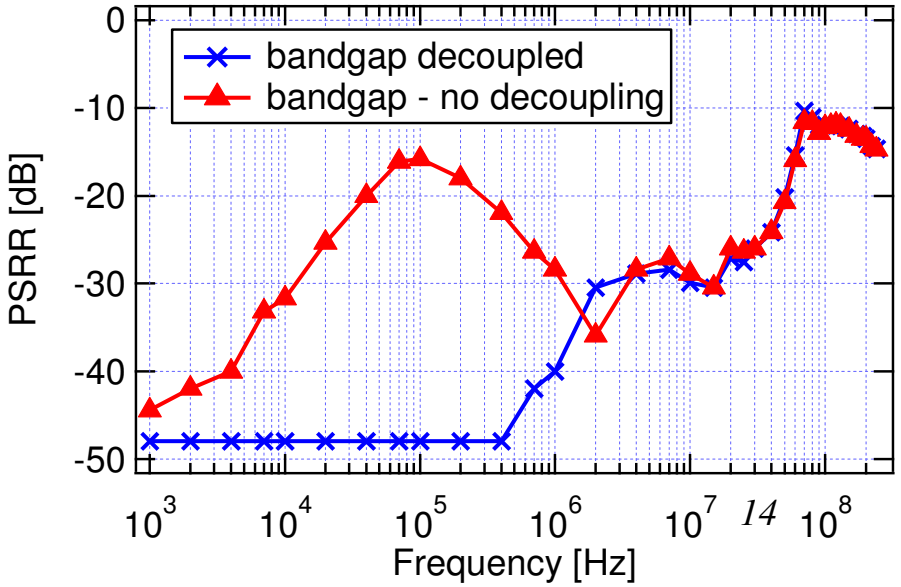
bandgap fed by unregulated LDO input supply
=> on-chip filter for next iteration

with bandgap decoupled get very good rejection at low frequencies (at limit of measurability)

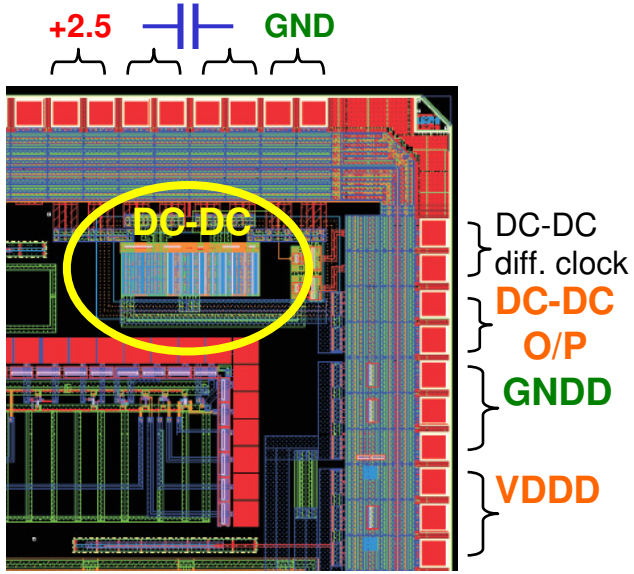
quite good rejection up to ~ 10 MHz

( PSRR = $20\log(v_{OUT} / v_{IN})$ )

## Power Supply Rejection



# powering - DC-DC



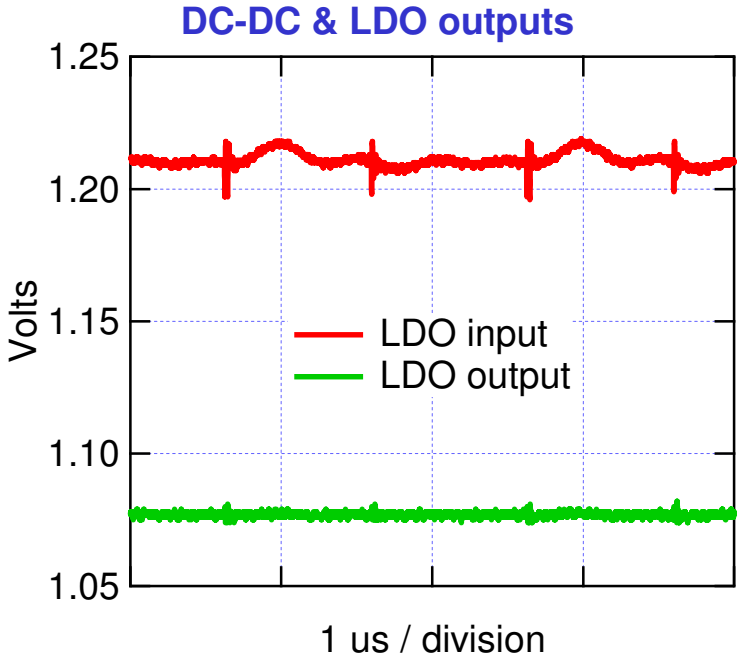

DC-DC switched capacitor circuit provided by CERN
thanks to Michal Bochenek, Federico Faccio

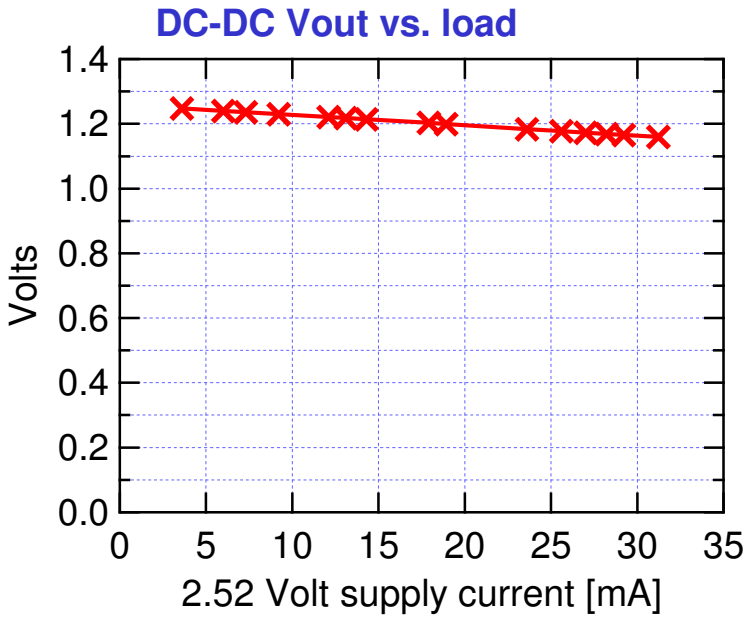
converts 2.5V -> ~ 1.2V using 1 MHz clock
could be used with 12V -> 2.5V external buck converter
(difficult to convert 12 -> 1.2 in 1 step)

could be used to supply **VDDD** (digital) & analog via LDO

efficiency measured for ~ nominal CBC load
2.52 V / 14.2 mA -> 1.2 V / 26.4 mA
=> ~ 90%

effects on CBC channel noise under study



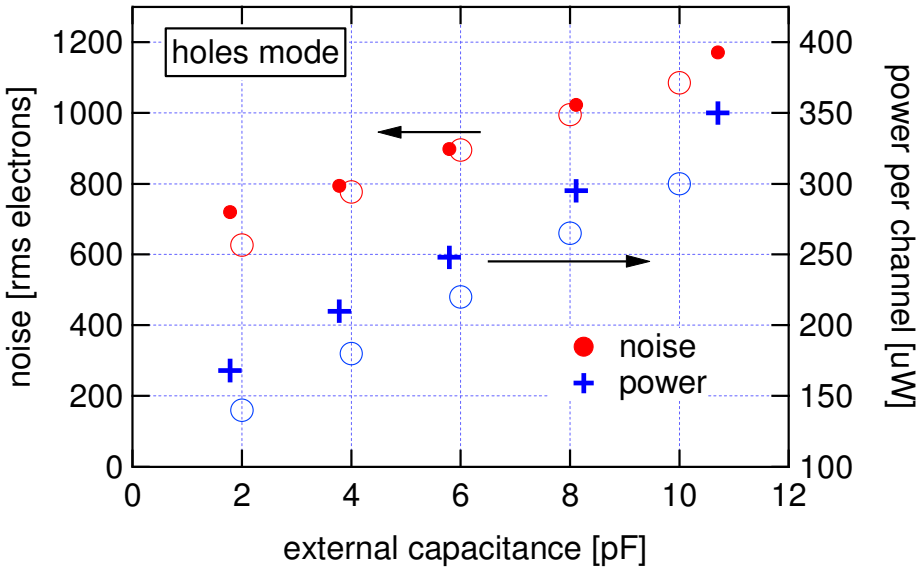



# power consumption

**analogue**

tuned for specific sensor capacitance →

**130 + (21 x $C_{SENSOR}$[pF]) μW / channel**




**digital**

$I_{VDDD}$ = 2.8 – 4.5 mA for whole chip

(depends on SLVS bias setting)

**< 50 μW / channel**

no measurable dependence on L1 trigger rate (0 – 100 kHz)
digital circuitry functions correctly down to $V_{DDD}$ = 0.9V

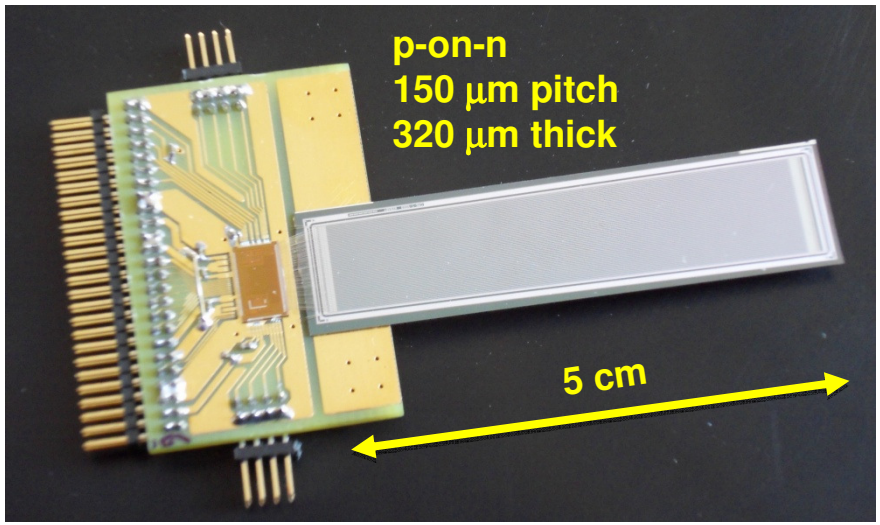
**total**

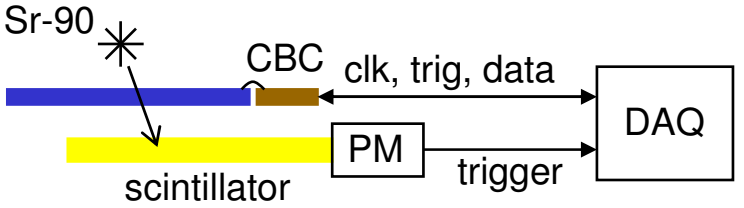
**180 + (21 x $C_{SENSOR}$[pF]) μW / channel**

**e.g. < 300 uW /channel for 5 pF sensor capacitance**

(c.f. APV25 ~2.7 mW / chan. (but long strips))

# results with sensor - beta source




count hits in CBC for fixed number of scintillator triggers

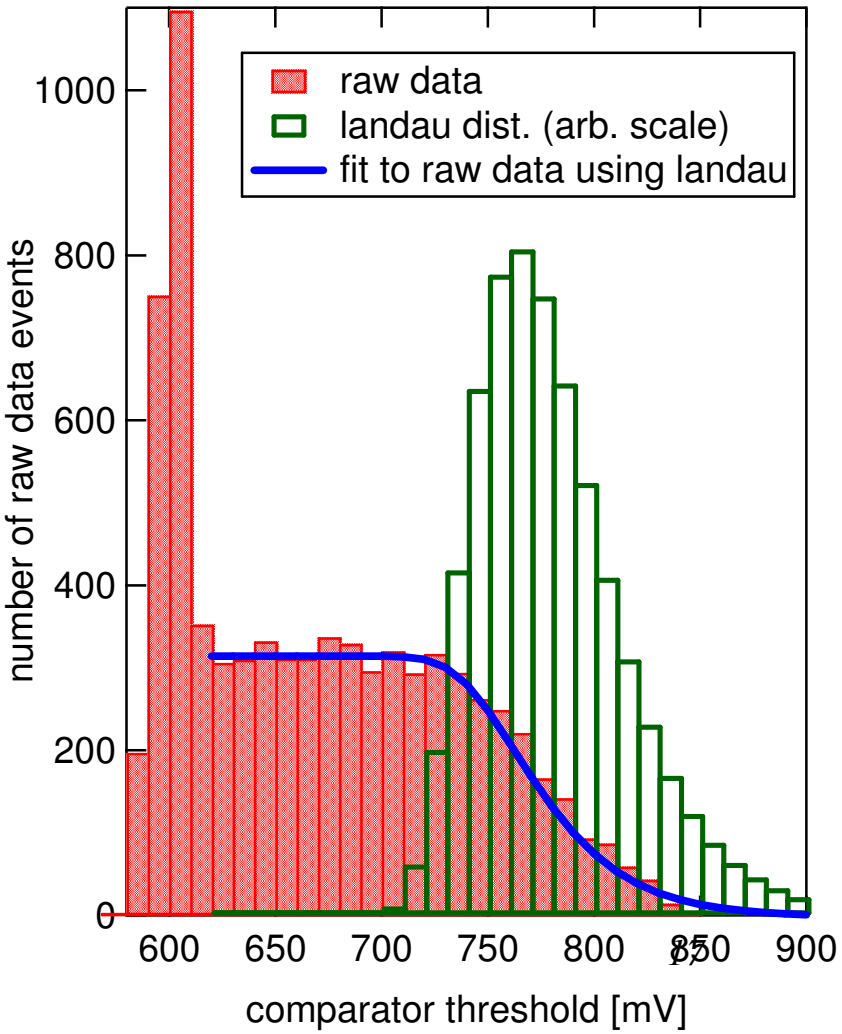
sweep comparator threshold in 10mV steps -> raw data →

fit with curve generated from Landau

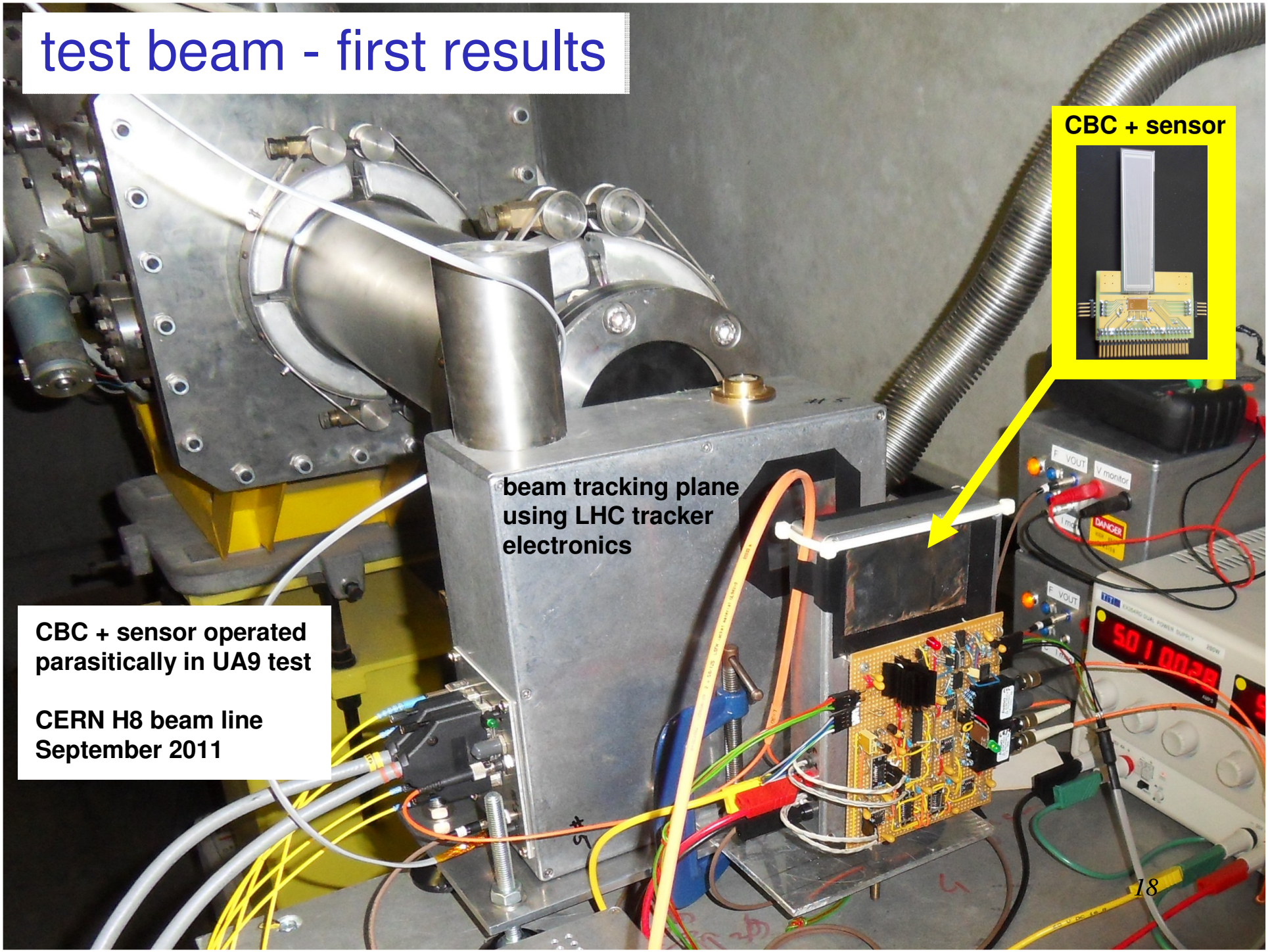
cross-check signal size with electronic calibration

-> most probable signal value ~ 3.5 fC (22,000 e)

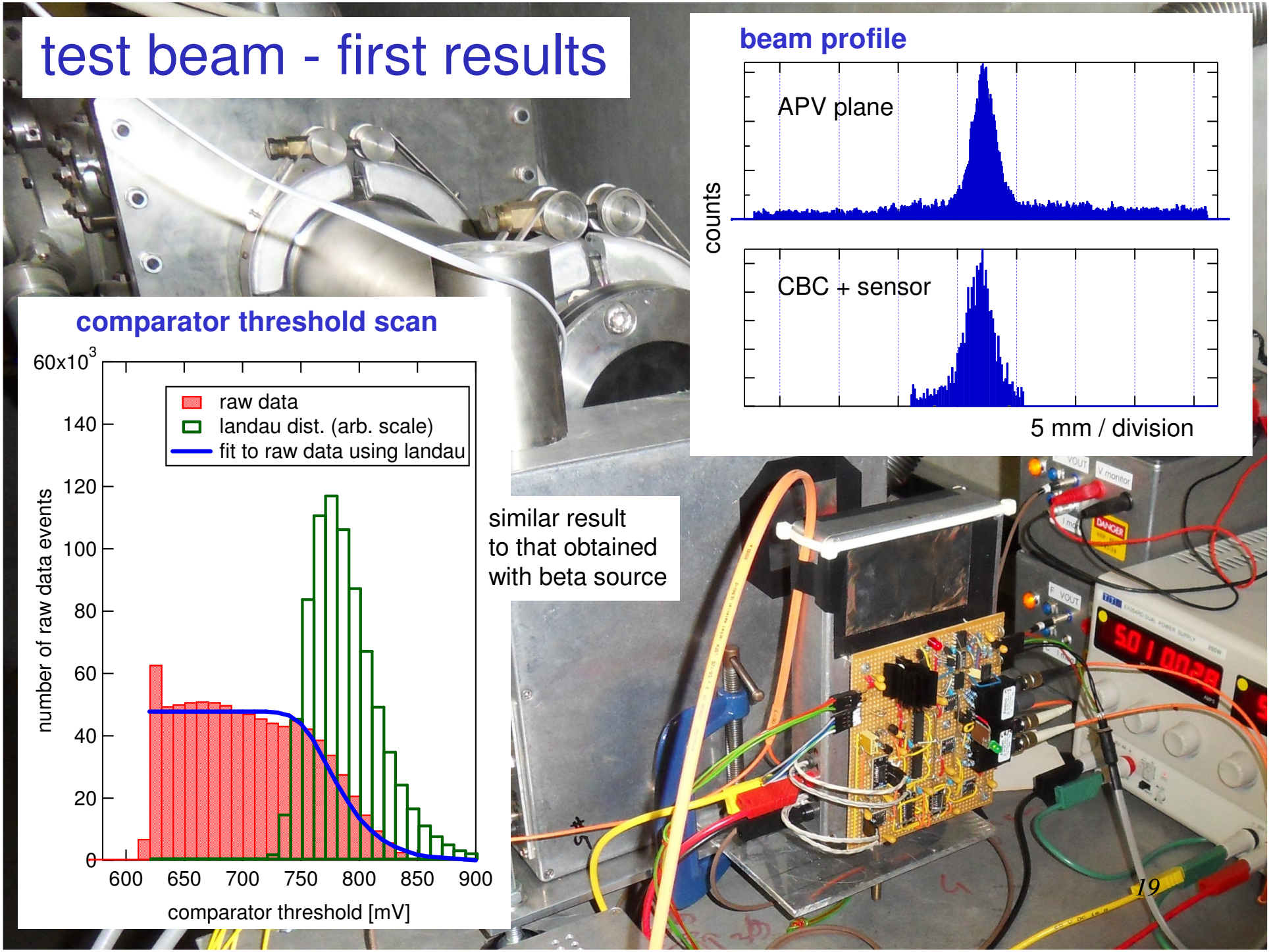
840 electrons noise



# test beam - first results



# test beam - first results



**beam profile**




**comparator threshold scan**




similar result
to that obtained
with beta source

# future directions

256 channels,  bump-bondable

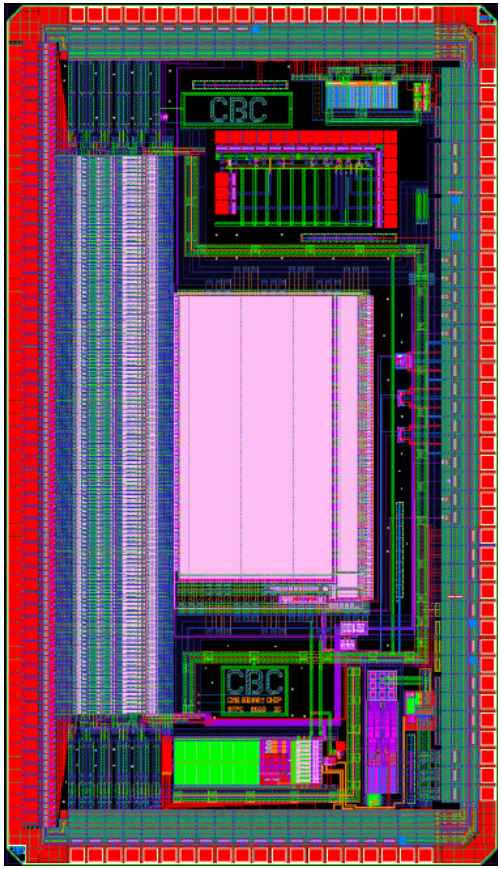
250 μm pitch C4 pads

some issues:

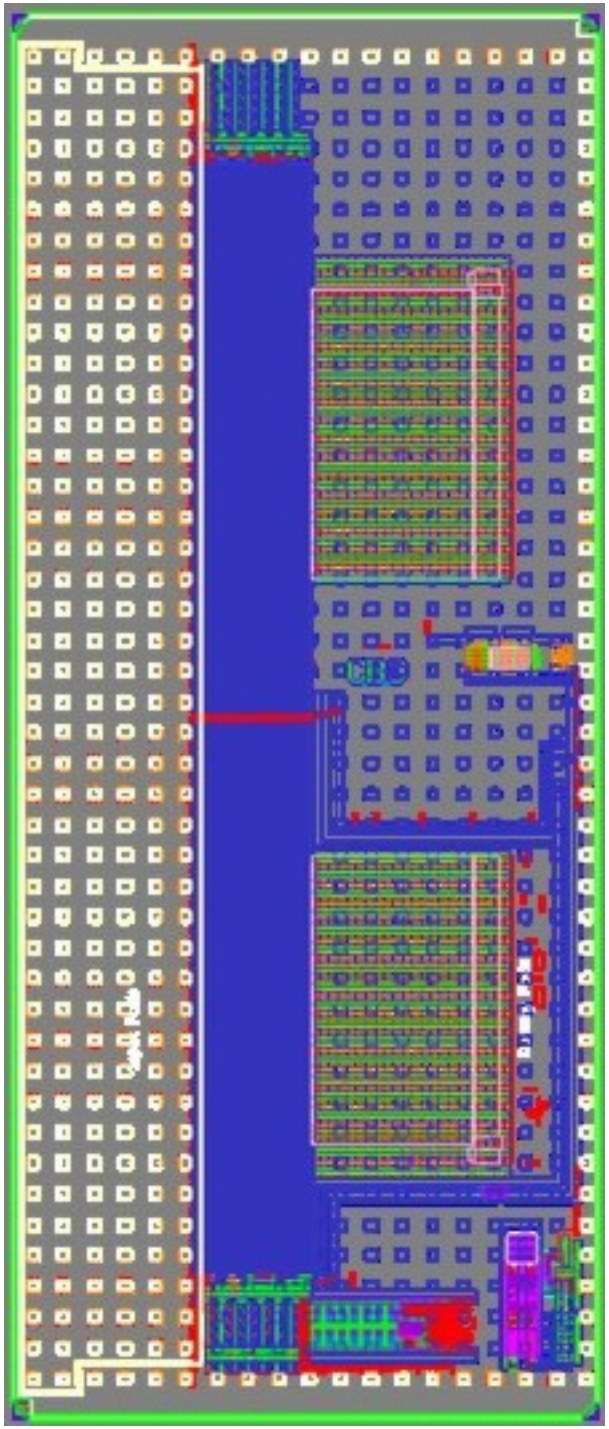
chip and hybrid design has to proceed in parallel - routing capabilities of substrate has impact on pad locations

how to test - prototype and production

plan to submit prototype early 2012




128 channels
wirebond: 50 um pitch
7mm x 4mm



256 channels
bump-bond: 250 um pitch
11.4mm x 4.75mm

# future directions - triggering

not possible to maintain 100kHz L1 trigger rate
without information from tracker

impossible to transfer all data off-detector

=> on-detector data reduction using stacked tracking approach

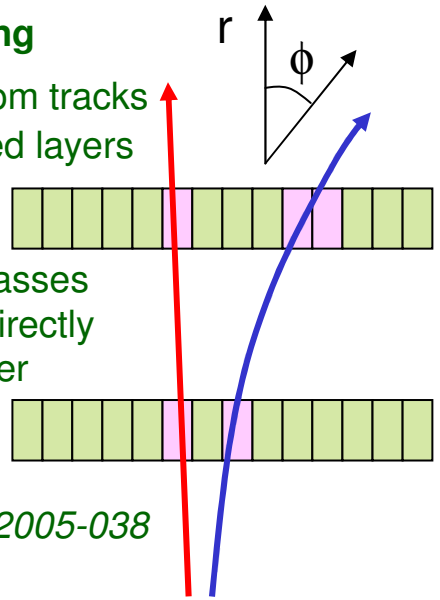
"hi-tech" 2-in-1 module concept

bring signals from 2 sensor layers together in one chip

logic to perform correlation will be prototyped in next CBC version

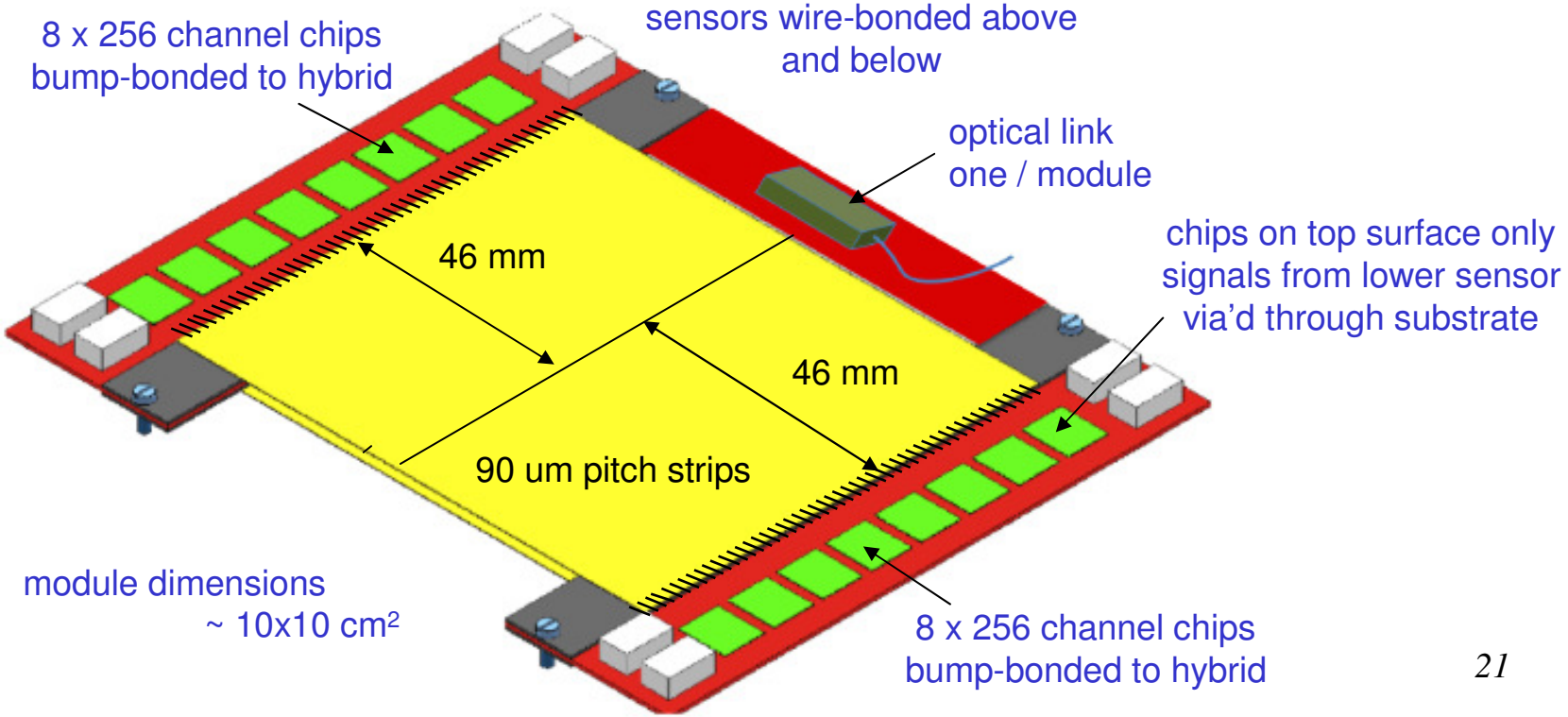
**stacked tracking**

correlate hits from tracks
in closely spaced layers




high PT track passes
through strips directly
above each other

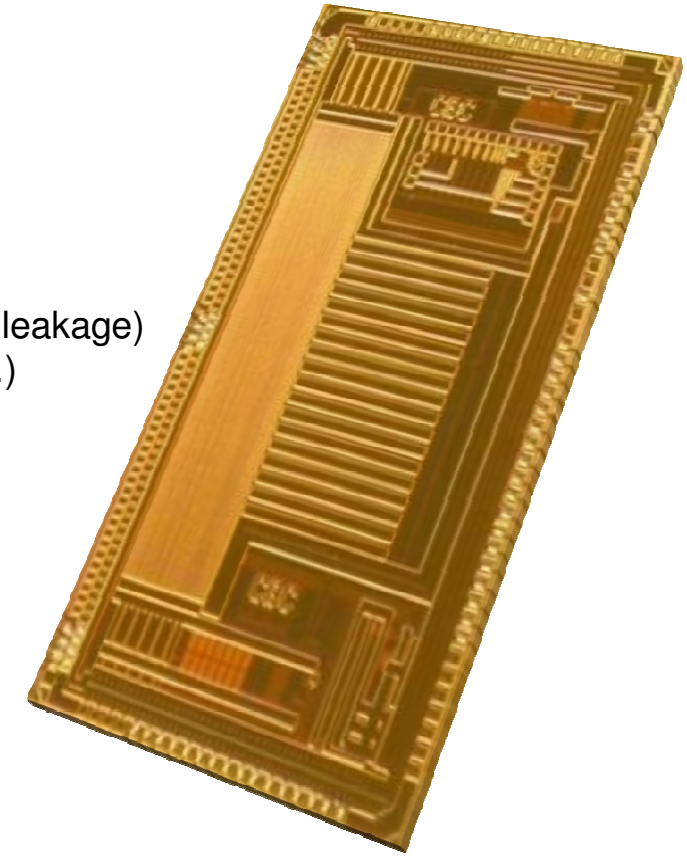
*J.Jones et al*
*CERN-LHCC-2005-038*



# summary

**CBC**

130 nm CMOS chip for short strips readout at SLHC
128 channels of front end amplifier, comparator, pipeline
unsparsified binary output data format



**measured performance**

works for both sensor polarities, can be DC coupled (1 μA leakage)
front end performance close to expectation (noise, gain, …)

e.g. 800 electrons noise @ < 300 μW/channel
for 5 pF sensor capacitance

lab measurements confirmed in test beam

**further testing**

more detailed study of powering options
temperature effects
radiation: ionizing and SEU

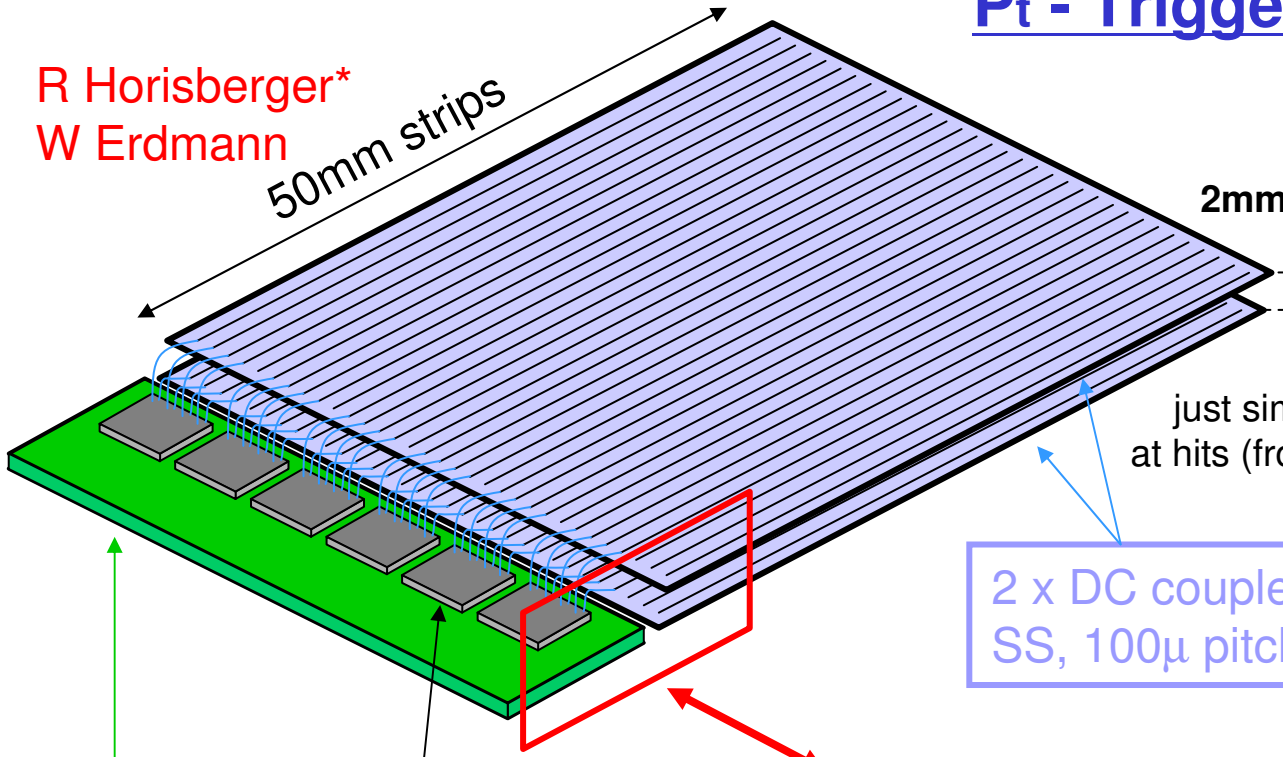
**next chip iteration**

plan to submit 256 channel bump-bondable version, with triggering features, early 2012

# extra slides

# $P_t$ - Trigger for TOB layers

R Horisberger*
W Erdmann




## Two-In-One Design

bond stacked upper and lower sensor channels to adjacent channels on same ASIC
no interlayer communication
no extra correlation chip
just simple logic on readout chip, looking at hits (from 2 layers) on adjacent channels

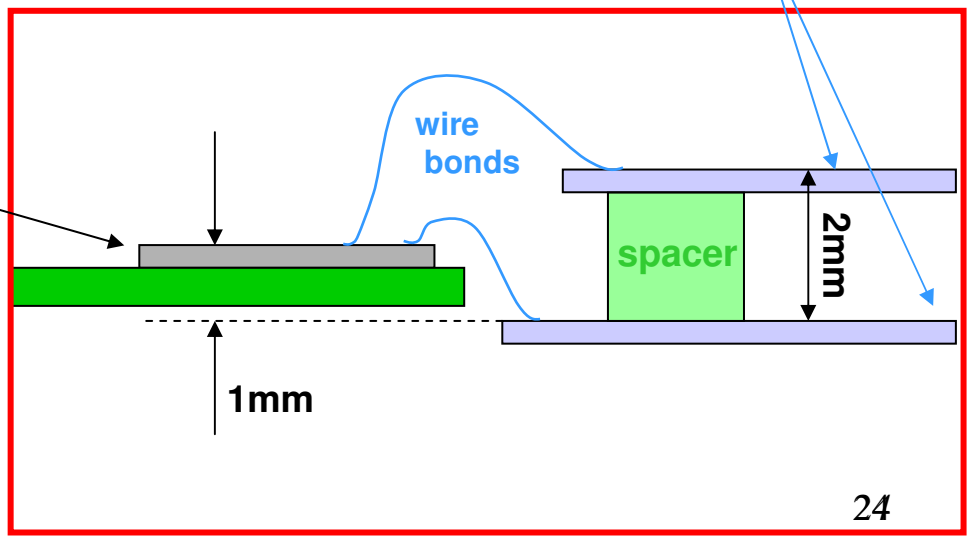
2 x DC coupled Strip detectors
SS, 100µ pitch ~8CHF/cm²

Strip Read Out Chip
2 x 100µ pitch with on-chip correlator

Hybrid

track angular resolution ~20mrad

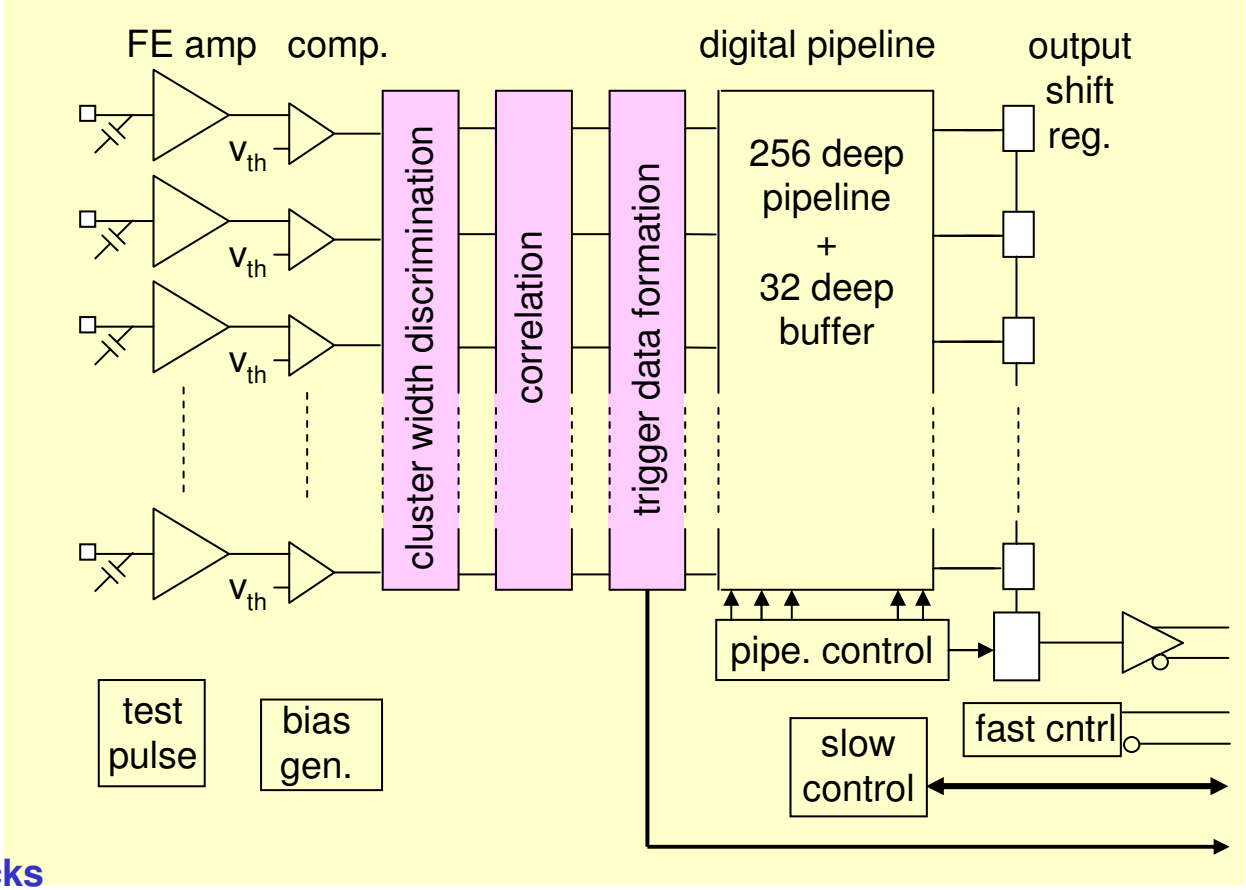
→ good $P_t$ resolution






* *http://indico.cern.ch/getFile.py/access?contribId=3&sessionId=0&resId=0&materialId=0&confId=36580*

# CBC modifications for 2-in-1 concept




**3 new blocks**

**cluster width discrimination**

wide clusters within a sensor layer not consistent with high PT track - electronically simple

**correlation**

do the stacked tracking operation - electronically relatively simple

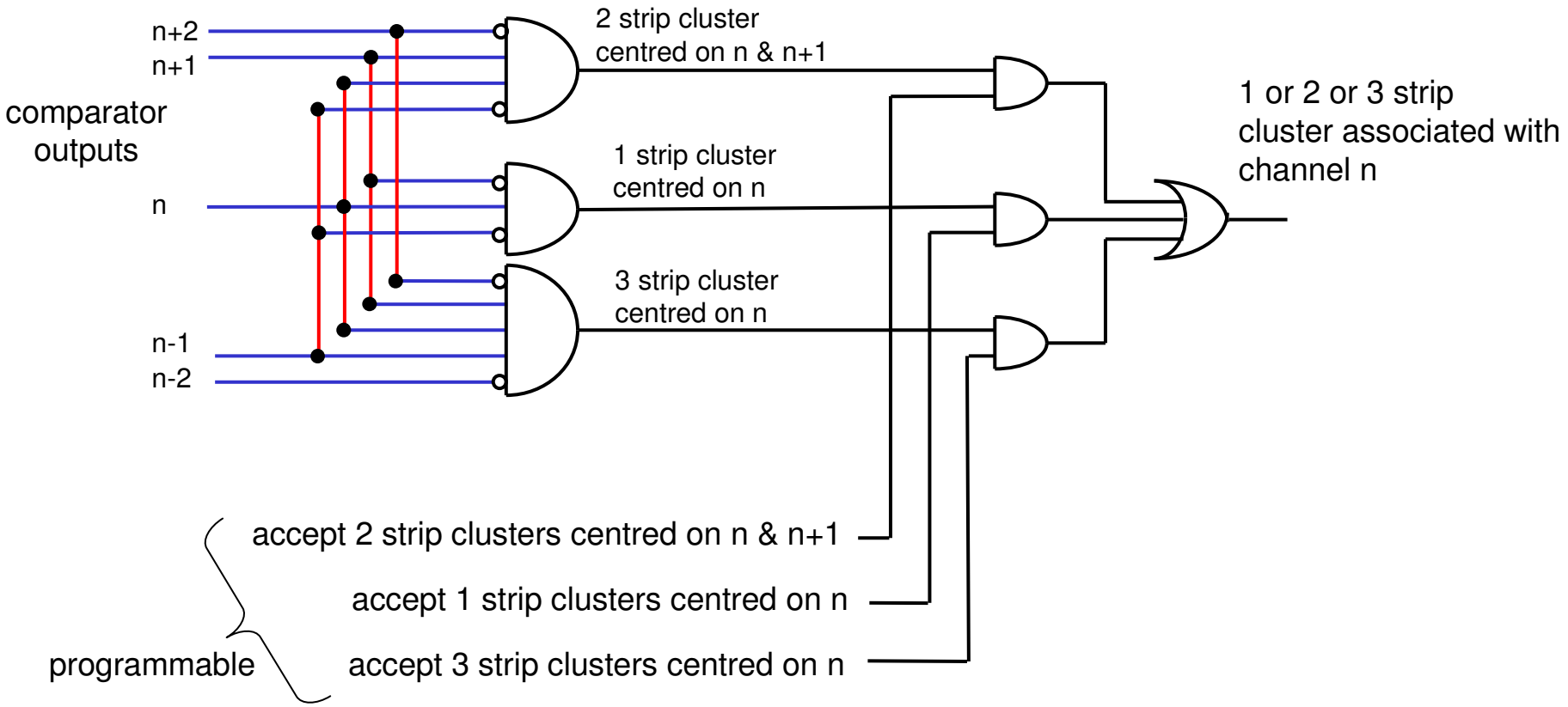
**trigger data formation and off-chip transmission**

options under discussion

either synchronous => limited no. of stubs per BX

or asynchronous => no hard limit, but buffering & timestamping required.

# cluster width discrimination



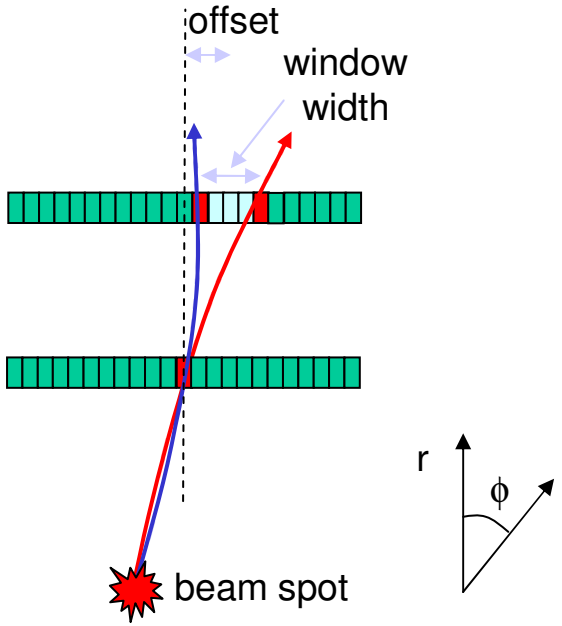

**n-1, n, n+1, … are neighbouring channels on one sensor layer (inner or outer)**
**(but every other channel on chip)**
**could increase to accept wider clusters if necessary**

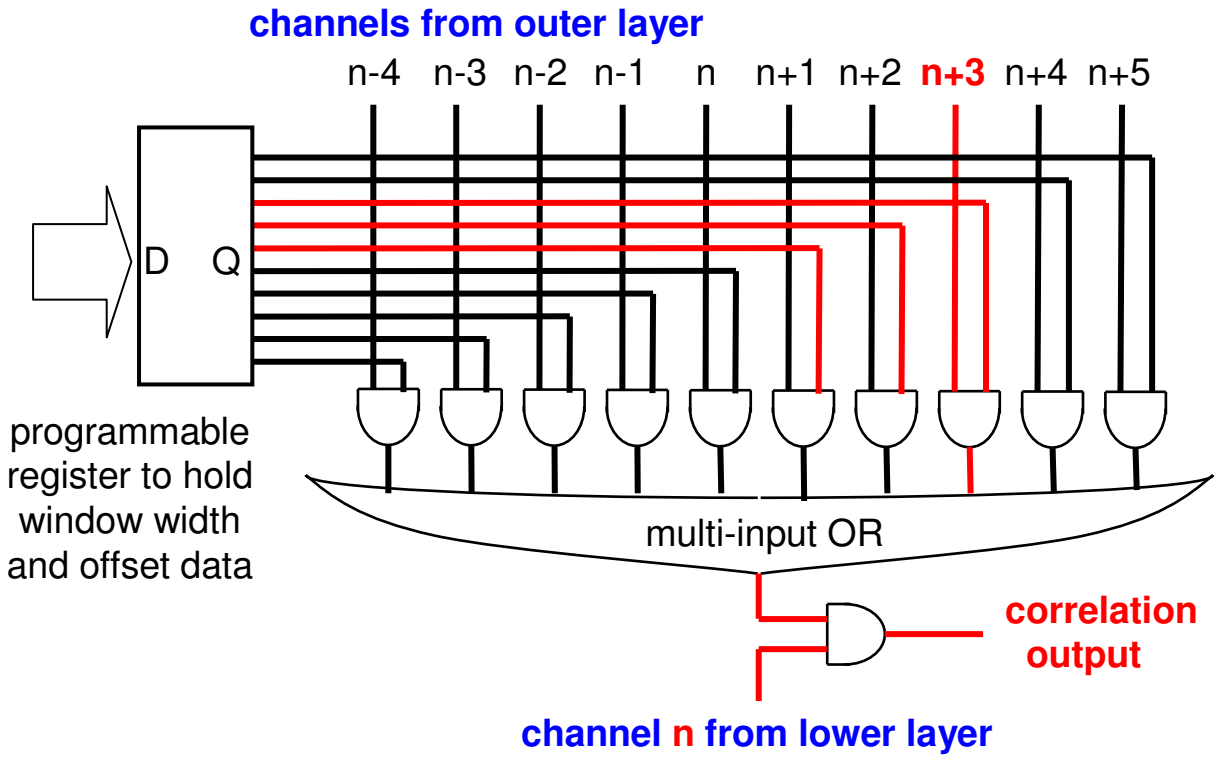
# correlation and offset correction

want to correlate cluster in lower layer with cluster occurring within window in upper layer

need programmability of cluster window width
width depends on $P_T$ threshold cut
(narrower window => higher $P_T$ threshold)

lateral offset of window centre will vary across module




need one of these circuits on every channel
programmable register inputs to AND gates to allow for cluster window and offsets between layers
offset varies depending on location across sensor
in above example 2 channel offset applied to 3 channel window in outer layer
cluster on channel n+3 in outer layer correlates with cluster on
channel n in inner layer