CBC front end design review

RAL – 20/10/2009

CMS Binary Chip

have converged on **binary un-sparsified** architecture for outer tracker short strip readout at SLHC

some advantages:

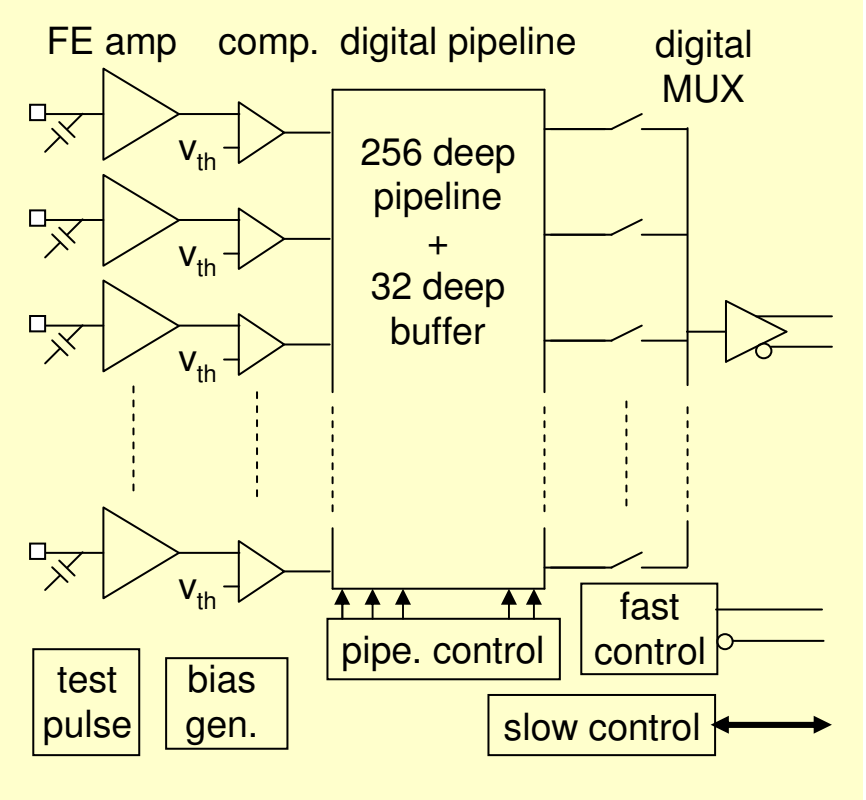
- no ADC power
- simpler on-chip logic
- should offer lowest possible FE power

retaining no zero suppression

- simper overall system
- occupancy independent data volume

main functional blocks

fast front end amplifier – 20 nsec peaking
comparator with threshold trim
pipeline (256 deep)
buffer for triggered events (32 deep)
output mux and driver
fast and slow control interfaces
programmable bias
test pulse



design considerations

SLHC environment

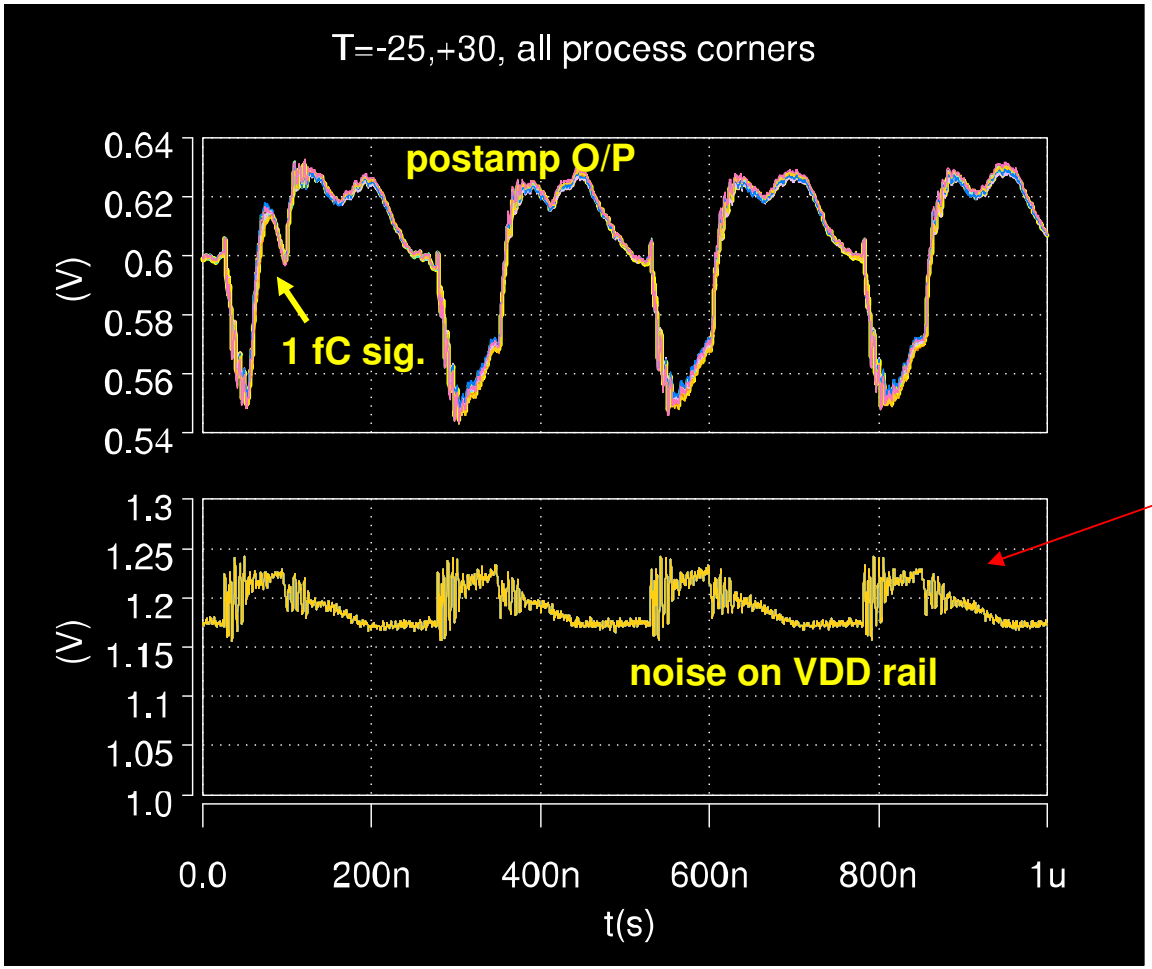
higher luminosity => higher granularity (than LHC) => shorter strips
occupancy will rise to ~ few %
CMS tracker at SLHC will operate at v. low temperatures
    maybe as low as -30 -> -40 degrees
    (but will still want to test and run chips and modules at room temperatures)

simulation strategy

specs should be met at -20 -> -40 deg. for all process corners
can accept some relaxation at room temperature – e.g. don't require full range of leakage current compensation at higher temperatures

analogue front end and comparator should run at VDD=1.1 V to allow filtering or LDO in supply rail to improve PSR

front end PSR without LDO supply



time domain picture

measured noise waveform added to VDD rail supplying FE circuit

sampled scope data for Enpirion "quiet" converter provided by Aachen

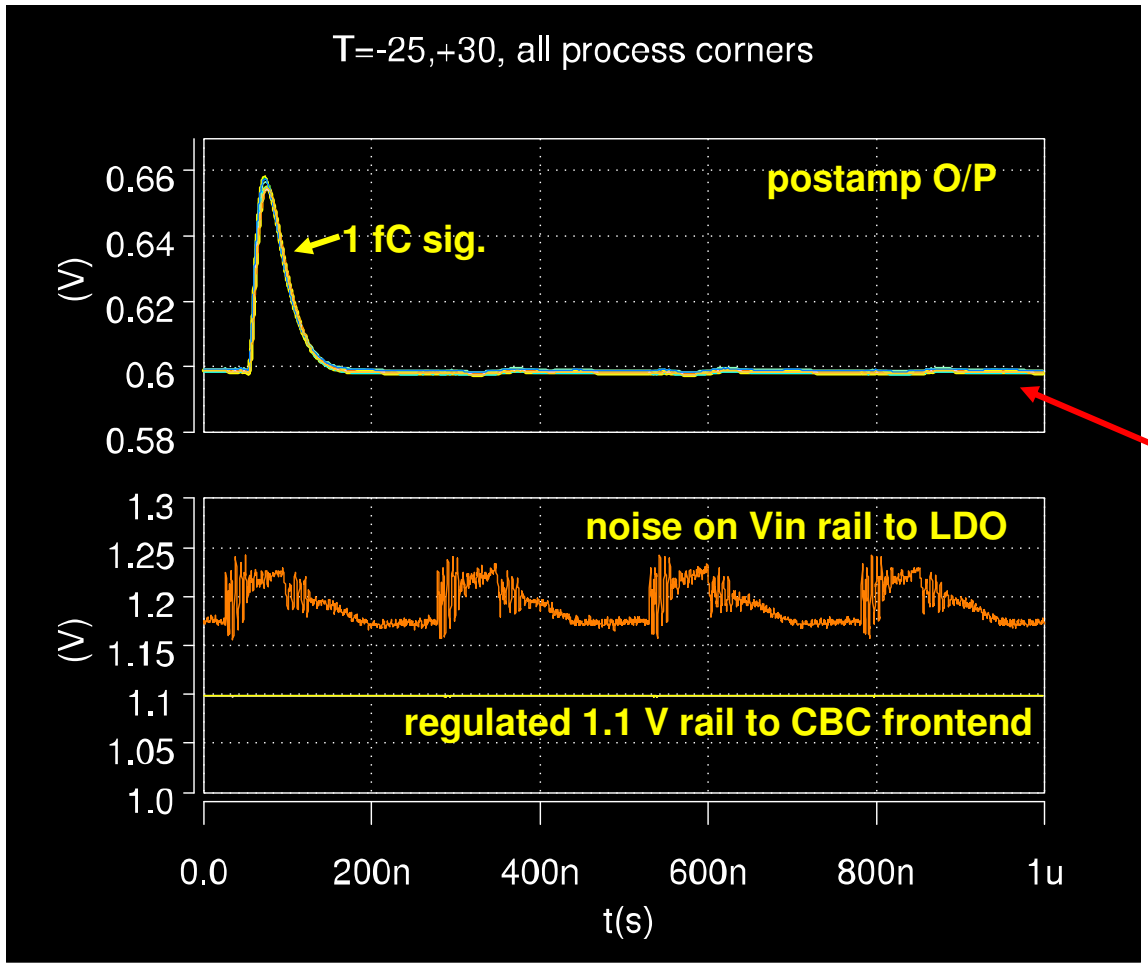
but x10 to (artificially) make it noisier

~ 80 mV pk-pk

1 fC normal signal completely swamped by noise

Ref: *http://indico.cern.ch/getFile.py/access?contribId=24&sessionId=0&resId=0&materialId=slides&confId=47293*

front end PSR **with** LDO supply



measured **x10** (80 mV pk-pk) noise waveform now added to LDO Vin

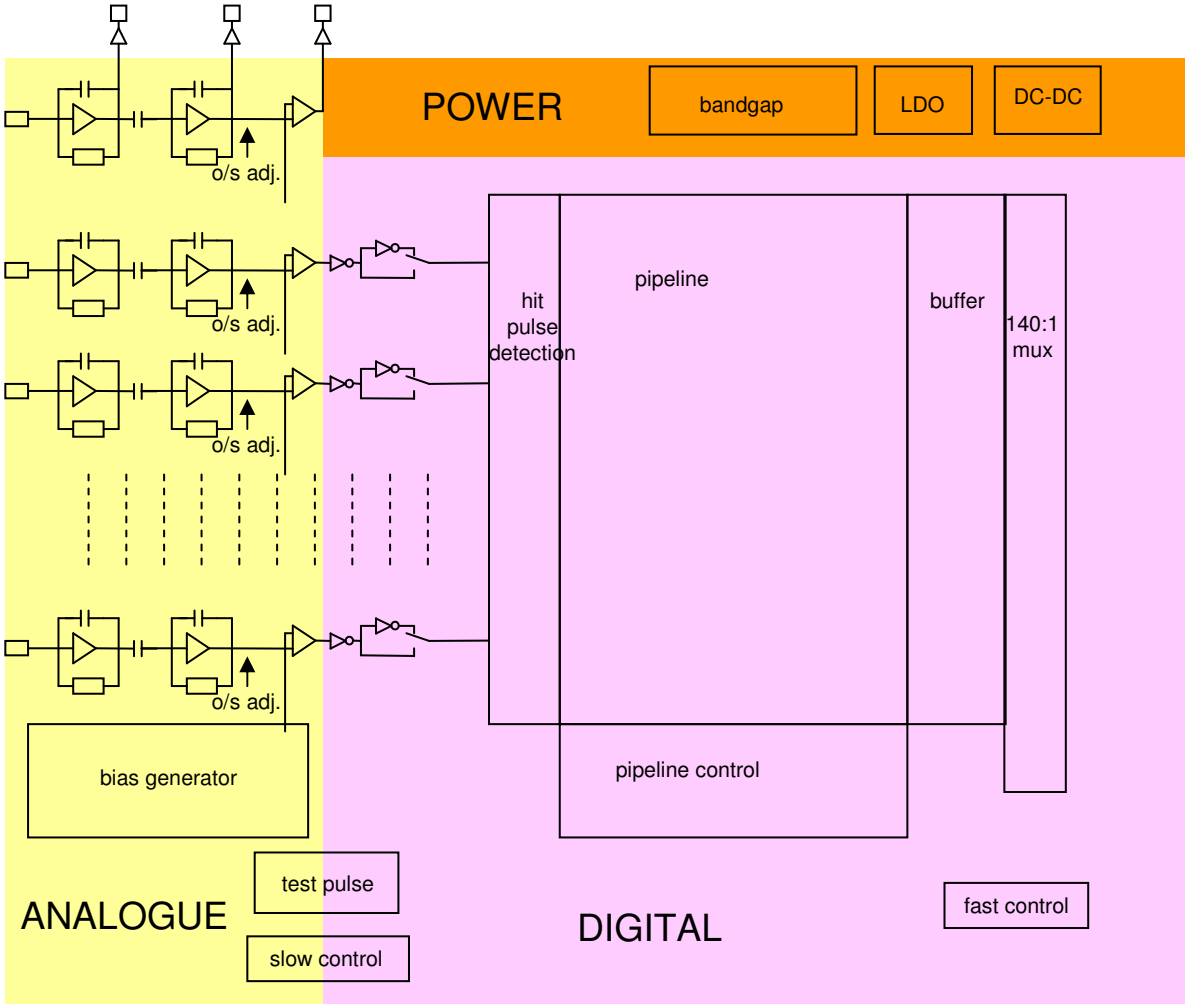
LDO loaded by single CBC frontend + 25 mA extra dummy load

1 fC signal at postamp O/P now appears

postamp O/P noise just visible

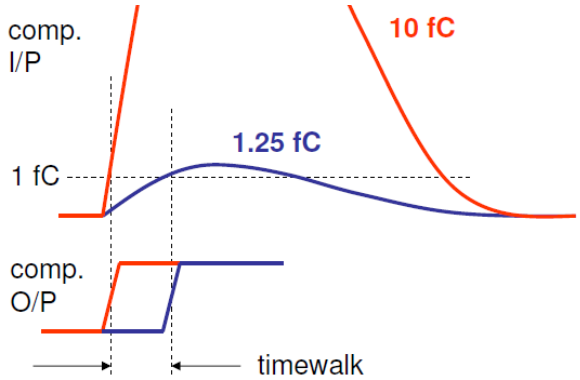
~ 125e pk-pk

analogue / digital domains



front end specifications

signal polarity:	both (electrons and holes)
strip length and C:	2.5 - 5 cm => C in the range 3 – 6 pF
coupling:	AC or DC
DC leakage:	up to 1 uA
overload recovery:	normal response within ~ 2.5 us after 4 pC signal
charge collection time:	<10 ns (need timewalk spec to be met for this value)
noise:	less than 1000e for sensor capacitance up to 5 pF
leakage current noise:	500e for 1uA leakage (implications for pulse shape)
power:	~ 200 uW (for 5 pF)
operating temp.:	< 0 in experiment (probably -20 -> -40) (will want to test at room temp.)
power supply:	1.1 V (assumes front end supplied through LDO to get supply noise rejection)
gain:	want > 50 mV / fC at comparator input (arbitrary choice but seems reasonable)
timewalk:	< 16 ns for 1.25 fC and 10 fC signals with comp. thresh. set at 1 fC
linear range:	previously unspecified, ~ 4 fC seems reasonable (only really need linearity in comp. thresh. range)

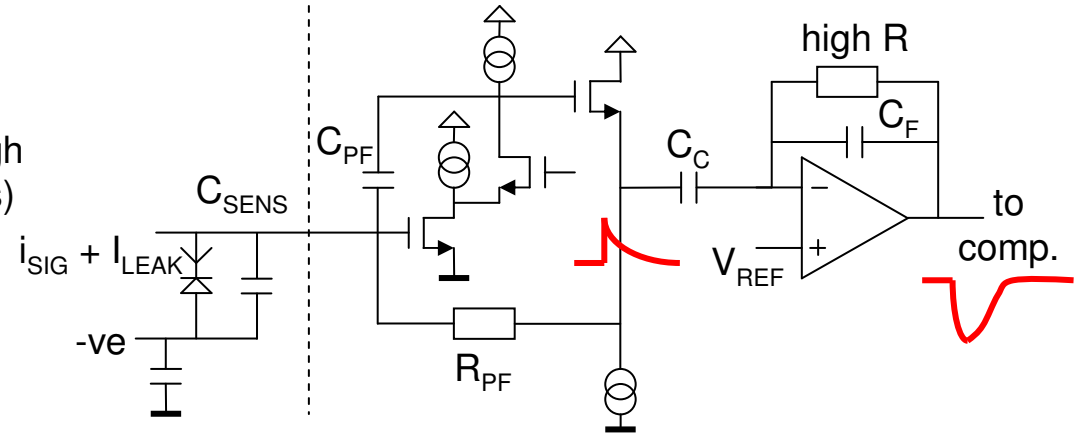


basic architectural choices

Preamp

NMOS I/P device

no noise penalty - 1/f corner low enough
(simulation & published measurements)
better connection to sensor for PSR
(sensor bias decoupling and
I/P FET source both at GND)



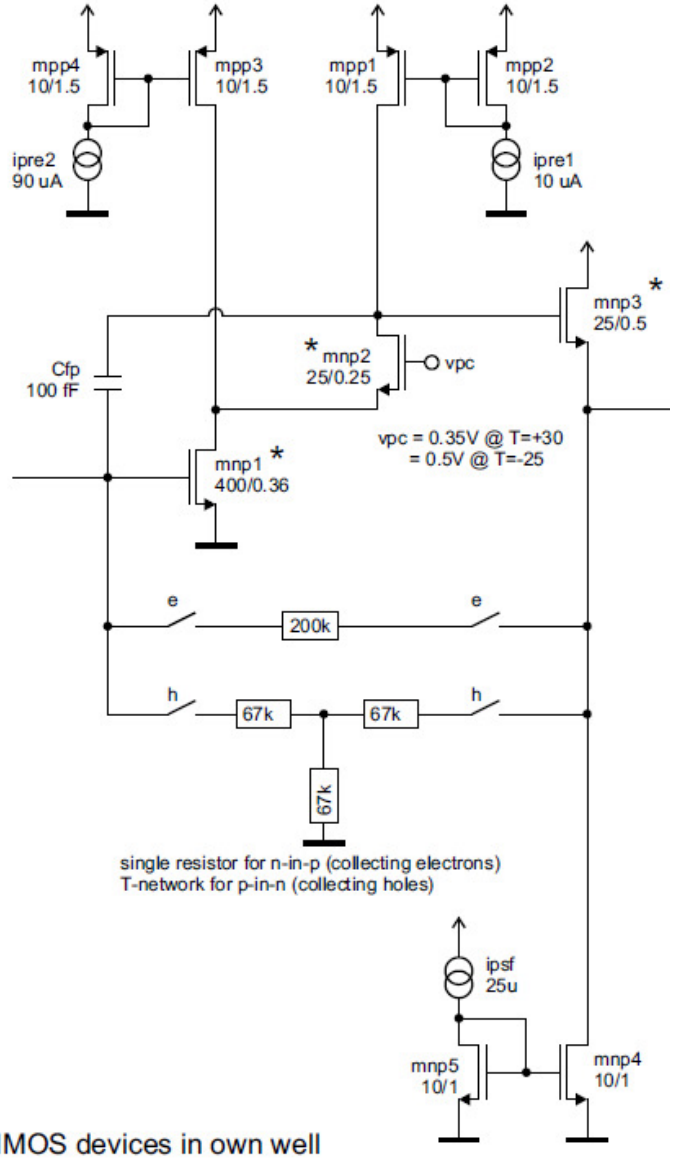
DC coupling to sensors possible

low Rpf (200k) absorbs DC leakage
(1 µA -> 200 mV)
200k noise contribution only ~ 220e
Rpf//Cpf = 200k//100fF = 20 ns decay time constant of preamp
=> no pile-up and helps with overload recovery

Postamp

provides gain & risetime provides integrating time constant
AC coupled to preamp
blocks DC shift due to leakage (DC coupled sensors)

preamp schematic



*NMOS devices in own well

simple linear cascode with separate power feed

allows to optimize cascode and I/P device currents independently

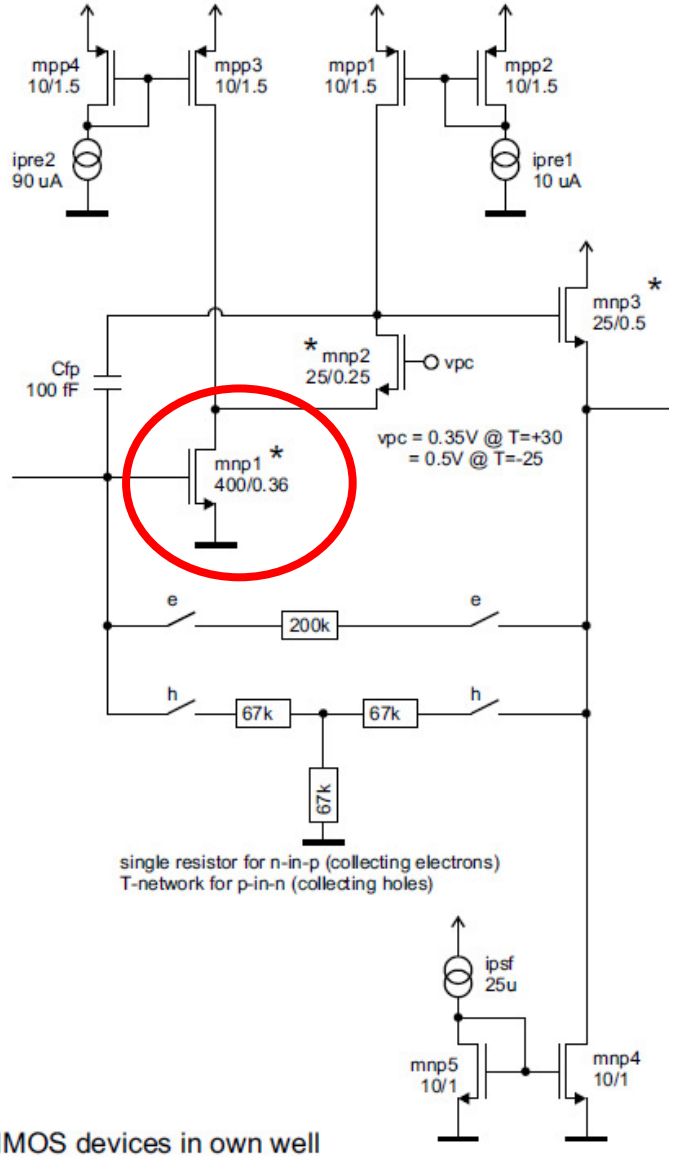
switchable resistor network depending on I/P signal polarity

effective resistance 200k in both cases

Cf.Rf time constant implements diff. component of overall pulse shaping – 20 nsec.

rel. low value => fast recovery to overload

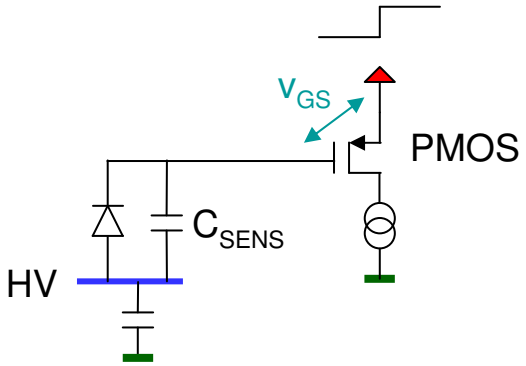
input device choice



*NMOS devices in own well

input device choice (1)

why NMOS preferred?



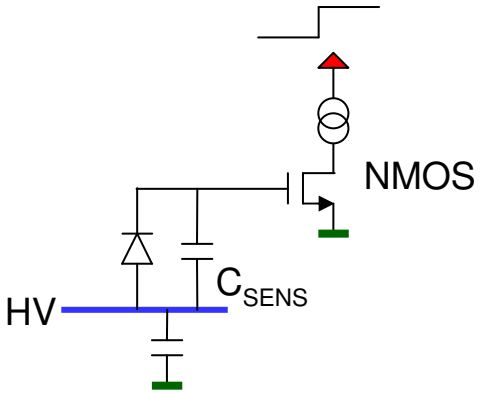
single-ended circuit most sensitive at input stage

for PMOS case, any noise on 1.2 V rail changes V_{GS} for input device

e.g. a voltage step of just 1 mV on 1.2 V rail results in spurious charge injection signal of

1 mV x C_{SENS} => 1 fC per pF

could circumvent by taking PMOS source to ground and having negative supply – unconventional powering scheme



for NMOS case, source and C_{SENS} coupled to GND so get some supply immunity without unconventional power supply

so NMOS preferred but conventional choice PMOS because 1/f corner historically high for NMOS

NMOS noise

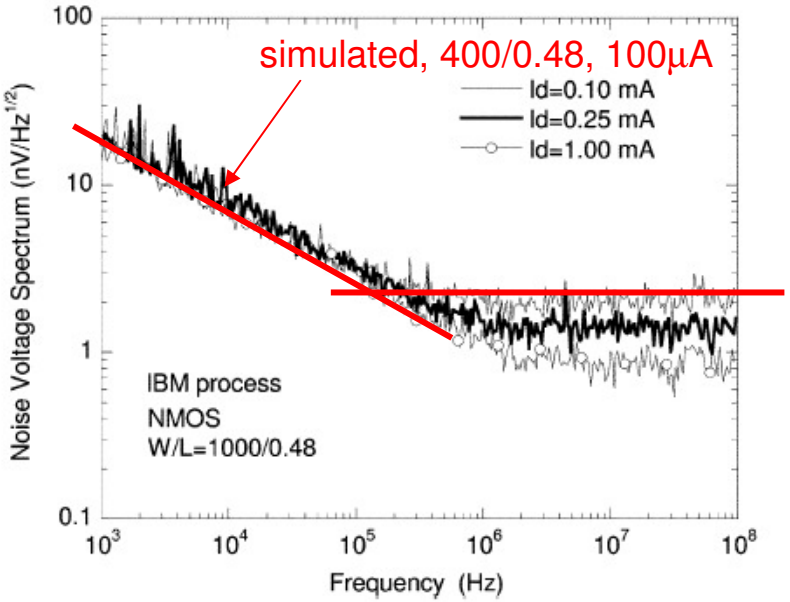
Ok if don't choose minimum device length

doesn't give much advantage in thermal region

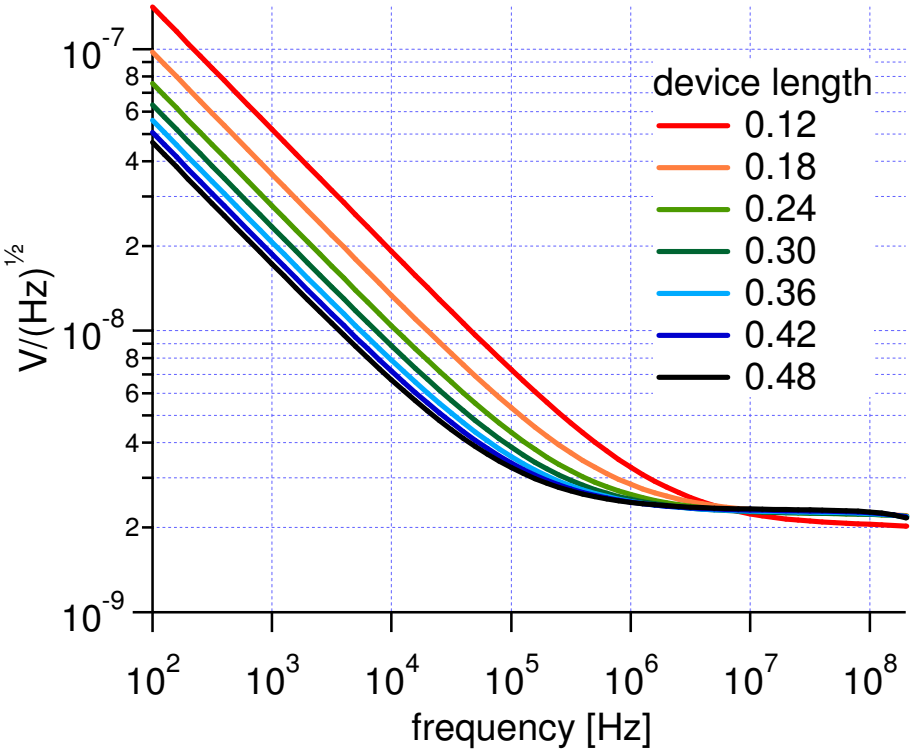
keep well clear of 1/f corner

0.36 seems about right

do we trust simulated noise?



simulated device noise for I_{DS} = 100 µA, W=400 µm



from Manghisoni et al, Noise performance of 0.13µm Technologies for detector front-end applications IEEE Trans.Nucl.Sci. Vol.53, no.4,Aug.2006 (2456-2462)

Fig. 11. Noise voltage spectra of an NMOS with $W/L = 1000/0.48$ at different values of the drain current I_D ($V_{DS} = 0.6$ V). The samples belong to the IBM 0.13 μm process.

input device choice (2)

how to choose device dimensions?

input transistor power/speed/noise v. C_{SENSOR} trade-off →

$$\text{noise} \propto [C_{SENSOR}+C_{FET}]/\sqrt{g_m}$$

$$\text{risetime} \propto C_{SENSOR}+C_{FET}]/g_m$$

$$g_m \propto \sqrt{C_{OX}(W/L)I_{DS}} \quad \text{S.I.}$$

$$\propto I_{DS} \quad \text{W.I.}$$

want to achieve good noise performance for short strips
C_{SENSOR} in range ~ 2 – 10 pF

also want low power

Recap 0.25 μm APV25

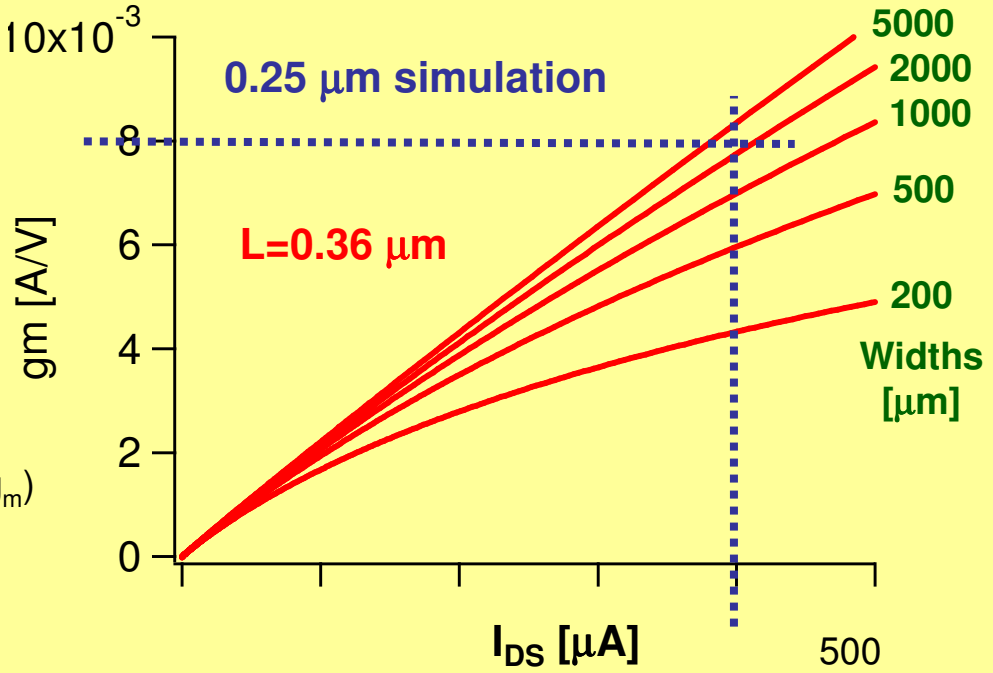
APV25 was for C_{SENSOR} up to ~ 24 pF

needed high I/P g_m (~8 mA/V)
for noise and speed

can see effect of SI – WI as W increases
(lines become straighter)

=> clearly no benefit going much beyond
2000 mm (just get more C_{GS} for no more g_m)

-> led to large W/L (2000/0.36)
with I_{DS} = 400 μA



input device choice (3)

already have L = 0.36 (noise)

repeat g_m v I_{DS} simuations for different widths →

for short strips

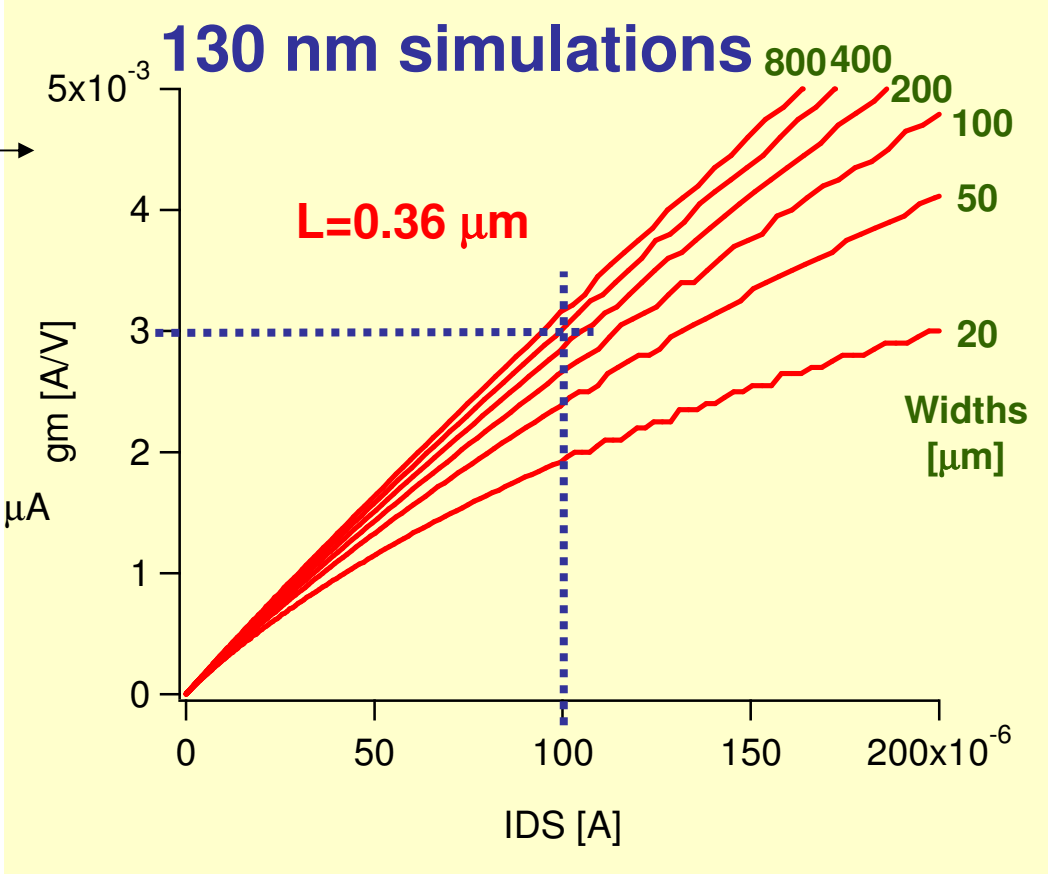
strip length => C_{SENS} reduces

=> can allow gm to reduce too

can get ~3 mA/V with W ~ 200 - 400 μm for 100 μA

choose W = 400 μm to allow for running higher currents if required

=> C_{FET} ~ 2 pF



note: this choice a "power vs noise" compromise for C_{SENS} > ~ few pF
not well optimised for very low capacitance

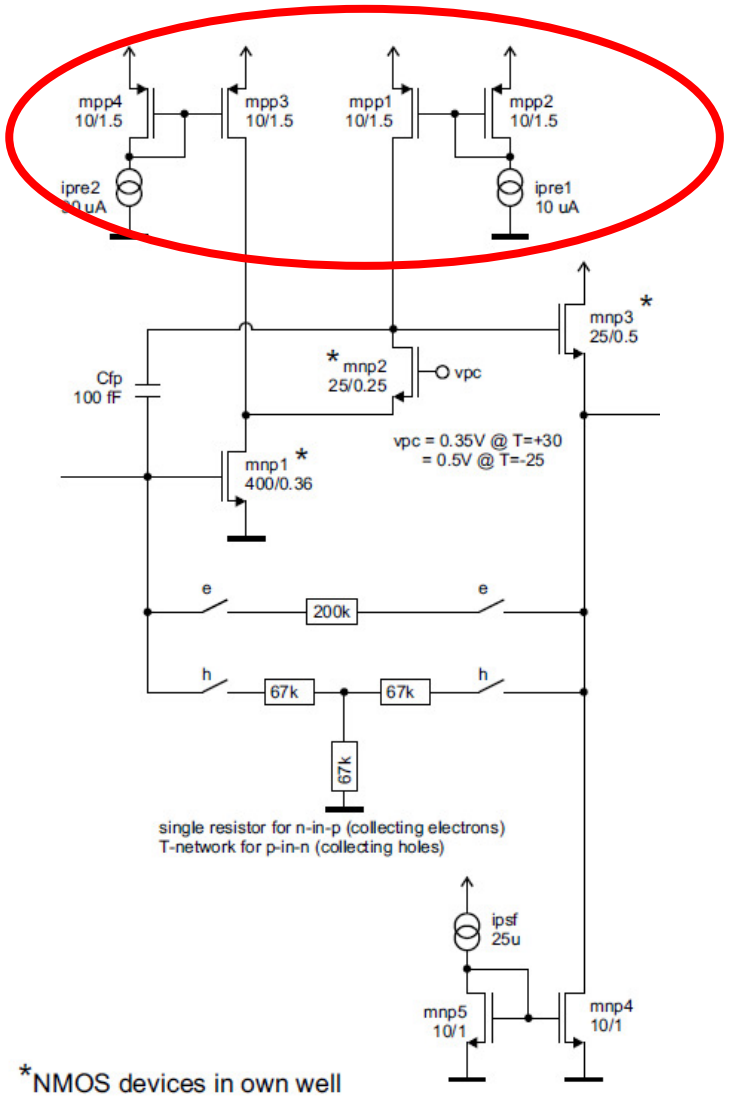
$$\text{noise} \propto [C_{SENSOR}+C_{FET}]/\sqrt{g_m}$$

$$\text{risetime} \propto [C_{SENSOR}+C_{FET}]/g_m$$

$$g_m \propto \sqrt{C_{OX}(W/L)I_{DS}} \quad \text{S.I.}$$

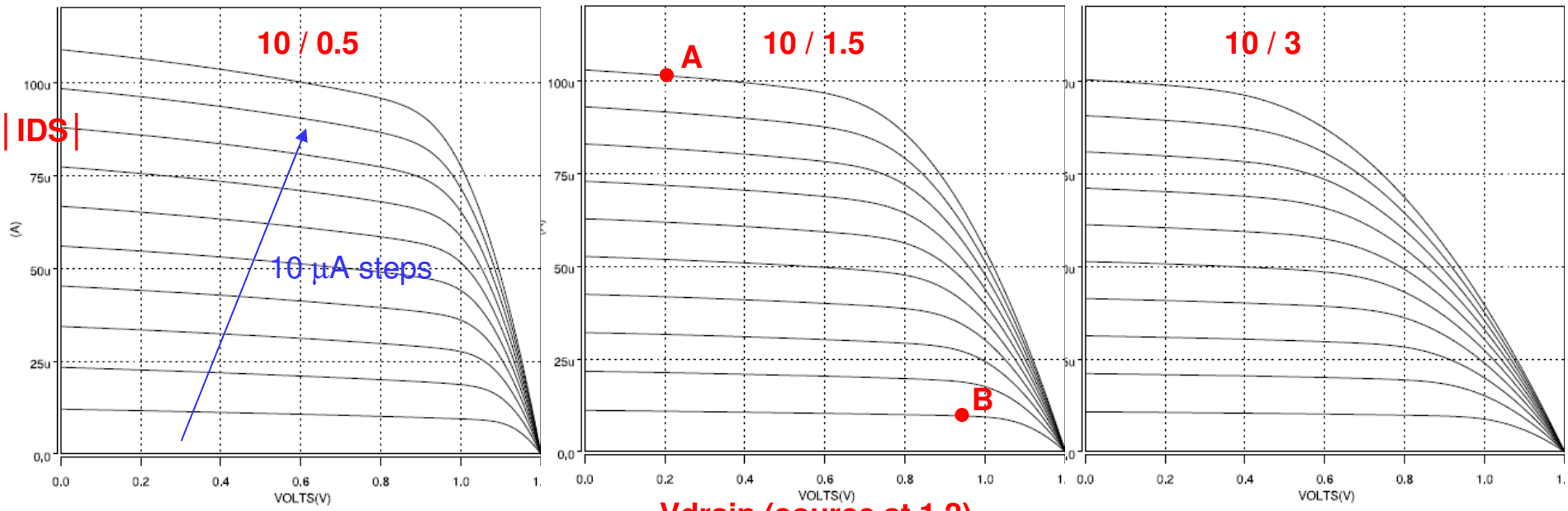
$$\propto I_{DS} \quad \text{W.I.}$$

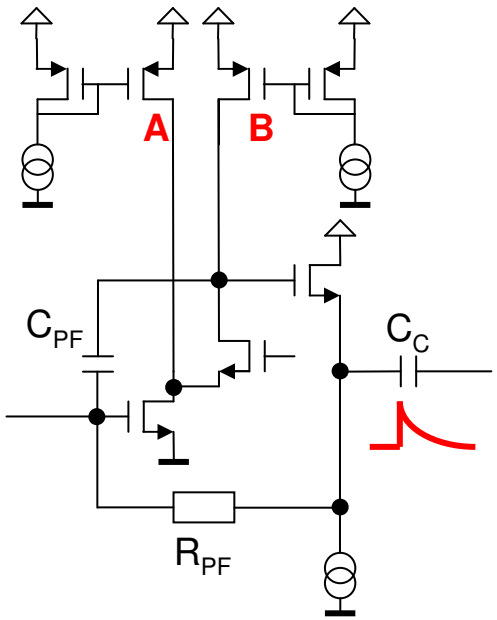
schematic



PMOS current mirrors

PMOS current mirrors

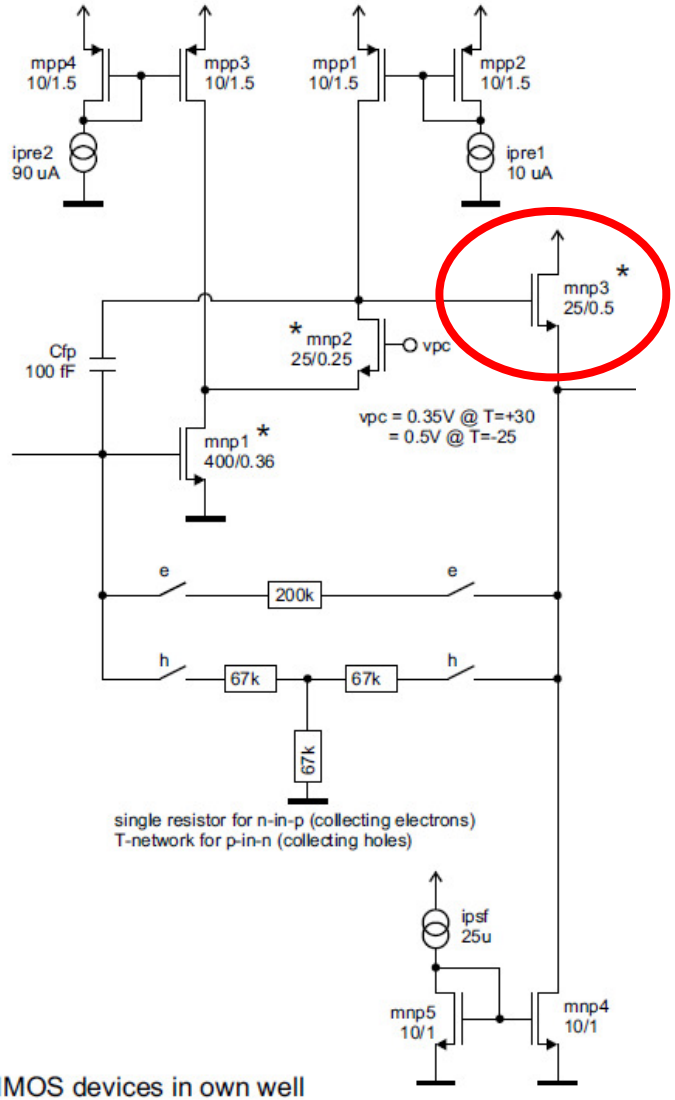




want big L for small gds – particularly device B
want low W/L for low gm – keep noise contribution small
VDSAT ~ $(L.I_{DS} / W)^{0.5}$ so can't choose L/W too big
can run low current in B – which has lower |VDS|
higher current in A – higher |VDS|
and still keep both devices in saturation

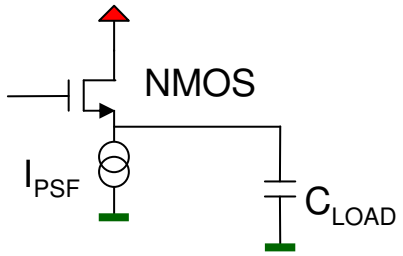
10 / 1.5 seems about right – no sig. advantage in different dimensions for the two mirrors

schematic



choice of source follower

source follower



sits in own (triple) well, so get gain close to 1

not a critical device – just has to drive ~ 1pF

I_{PSF} determined by slew-rate

normal signal size ~ 4 fC produces pulse ~ 30 mV at preamp O/P

require slew-rate ~ 10 x faster than overall pulse peaking time => 2 nsec

=> 15 V / µsec

for C_{LOAD} ~ 1pF => I_{PSF} ~ 15 µA

NMOS device (IDS=25µA)

W	L	gm
25	0.13	0.59
25	0.26	0.66
25	0.5	0.65
25	1.0	0.58
50	0.5	0.71
15	0.5	0.6

for ~ 2 ns time constant need s.f. gm ~ 0.5 mA/V

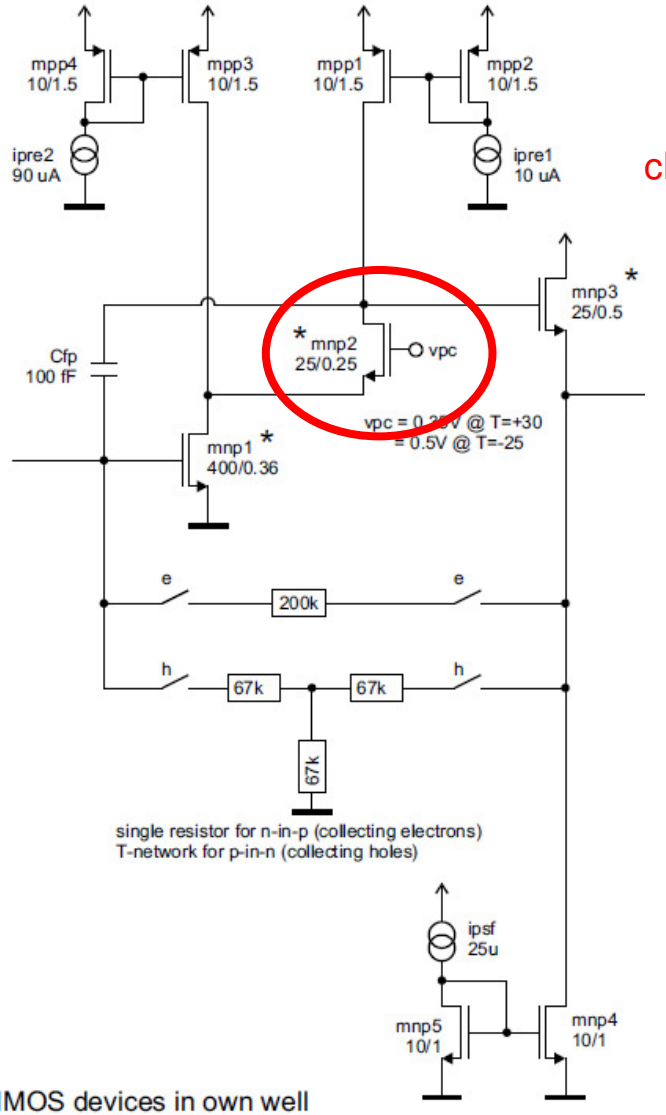
simulations show need ~ **25 µA** to get this (or thereabouts)

device dimensions not critical (W.I.)

25/0.5 seems about right

(circuit has been extensively simulated around this point)

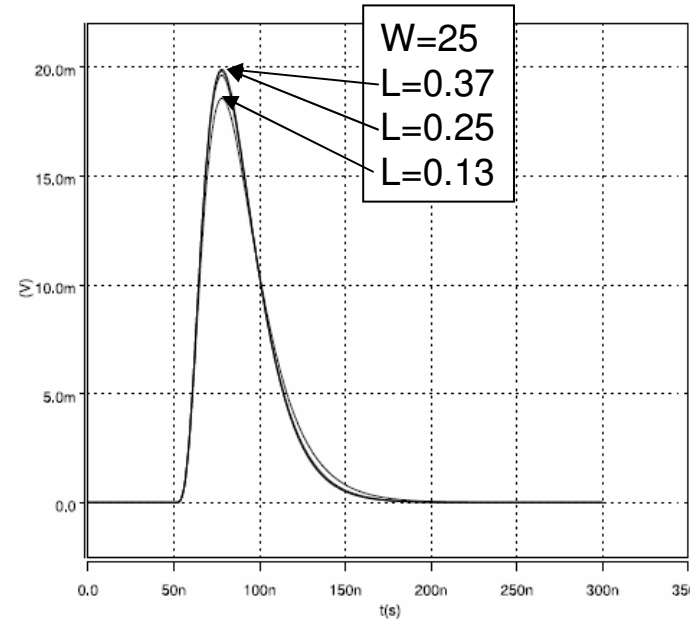
schematic

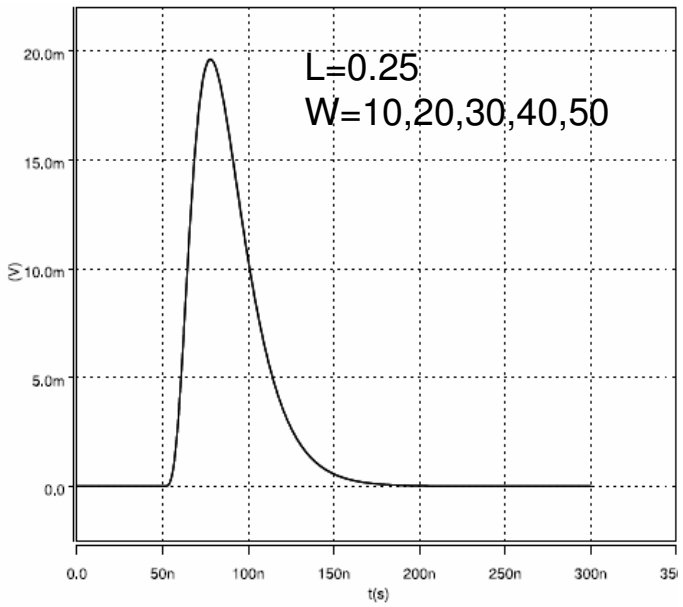


choice of cascode

*NMOS devices in own well

choice of cascode dimensions

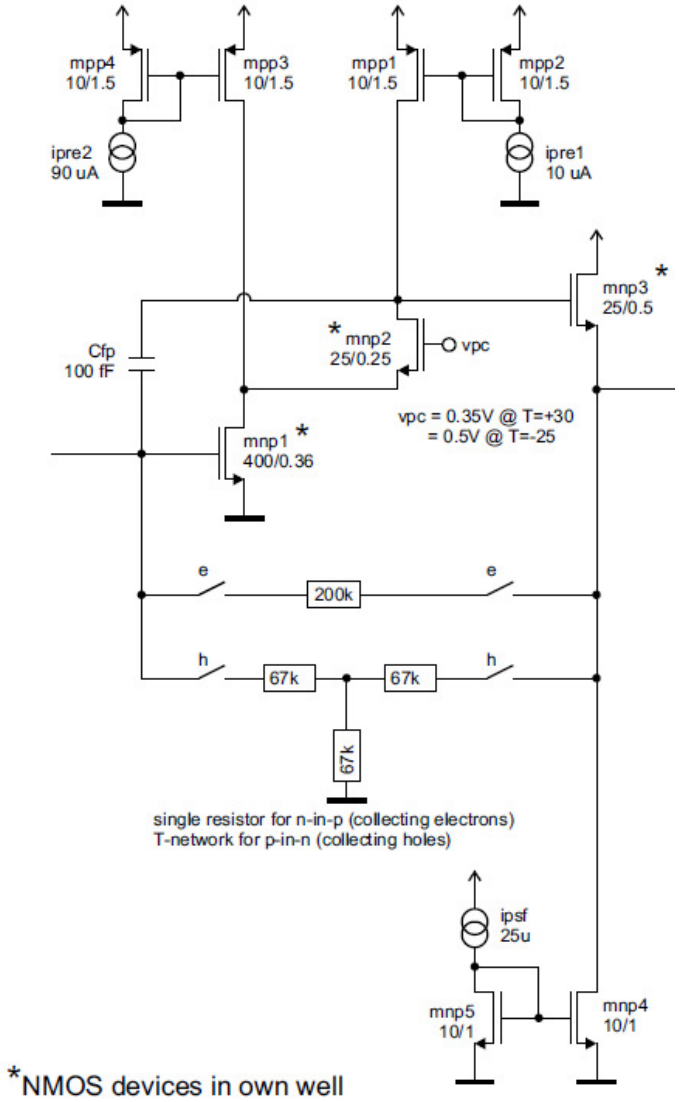




some loss of signal amplitude if use minimum length device
~ no dependence on device width (WI)

go for W=25u L=0.25u

preamp final dimensions



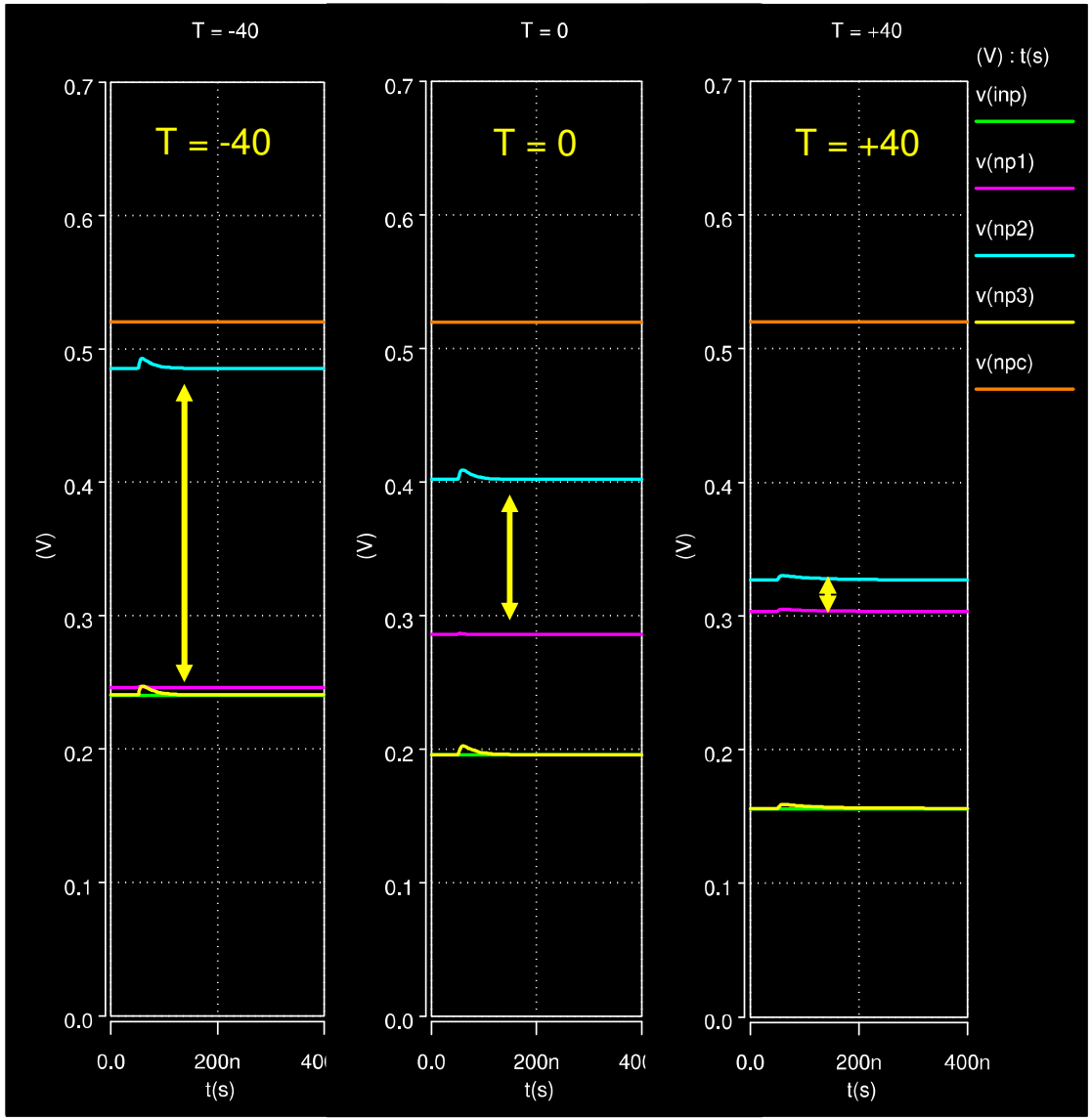
have justified dimensions for ~ all preamp transistors

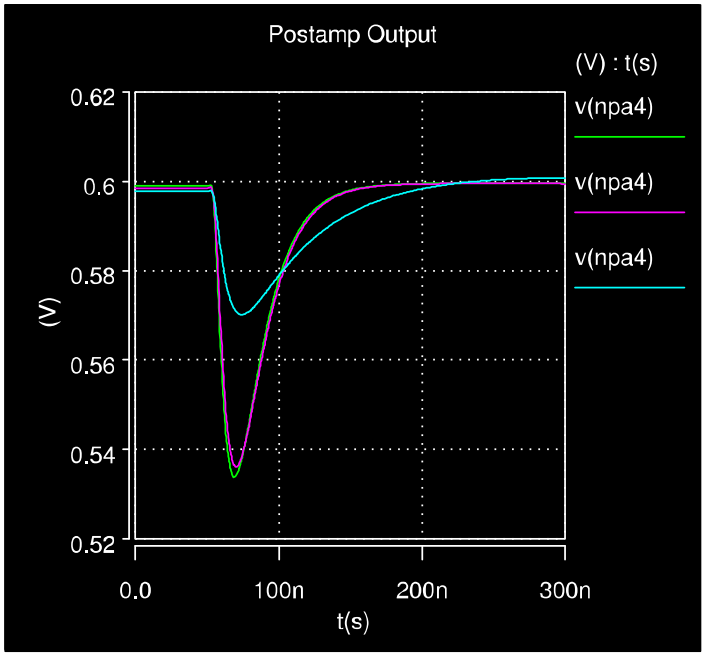
will now proceed to simulated performance

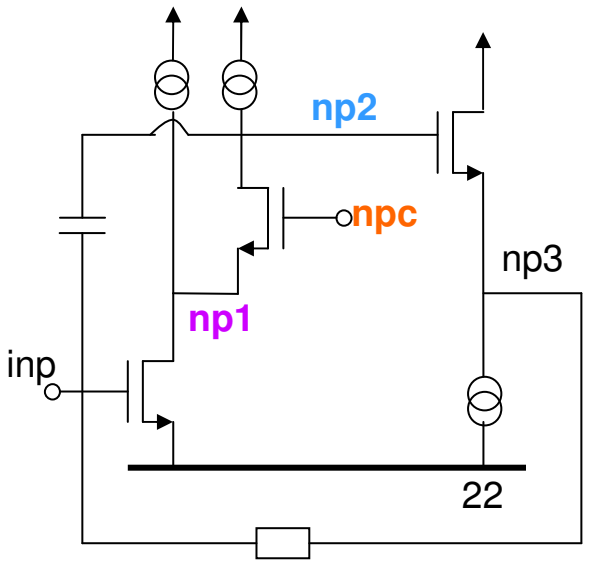
treat electron and hole signal cases separately

but discuss adjustments required for temperature variation first

cascode bias vs temperature

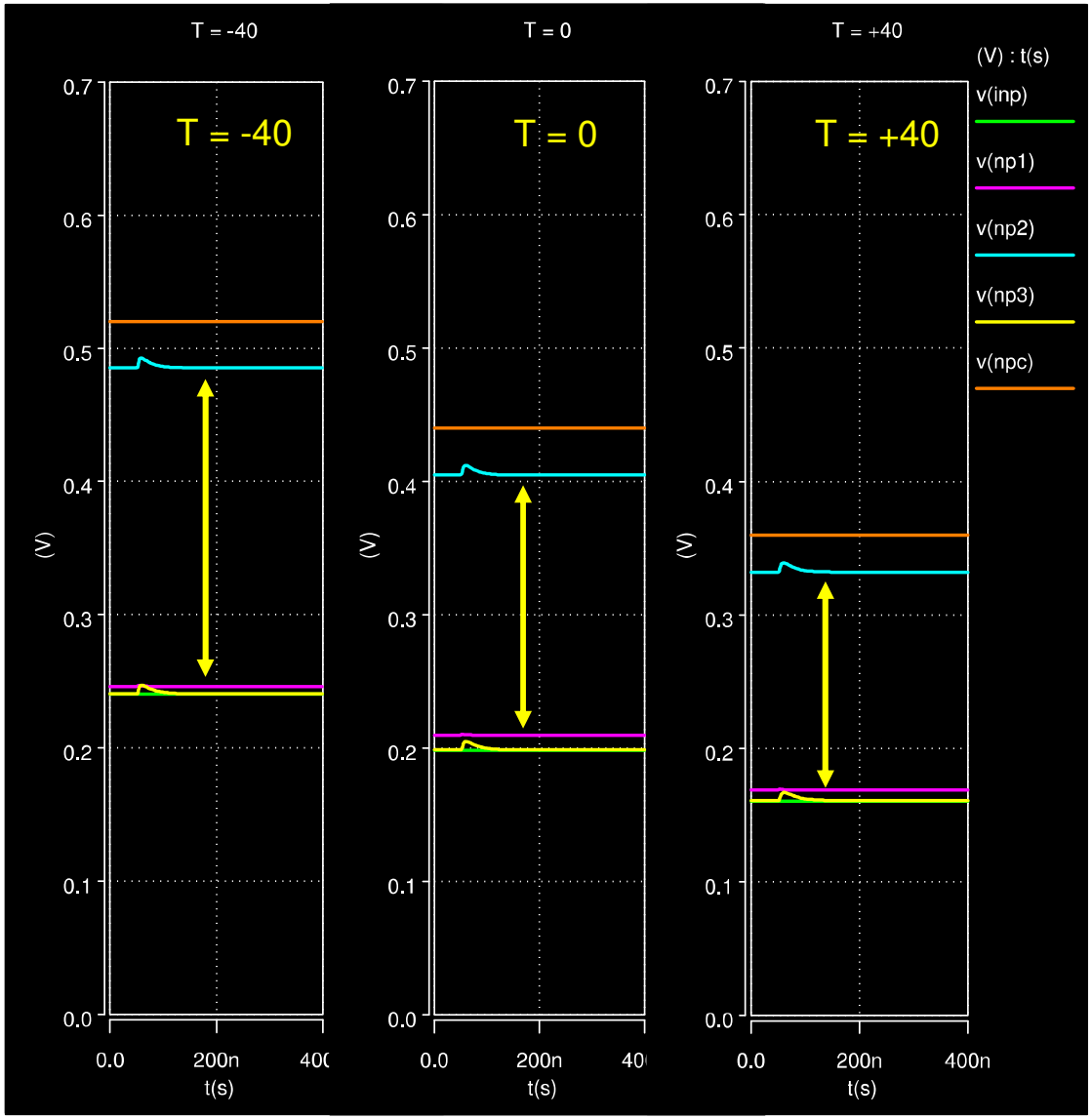


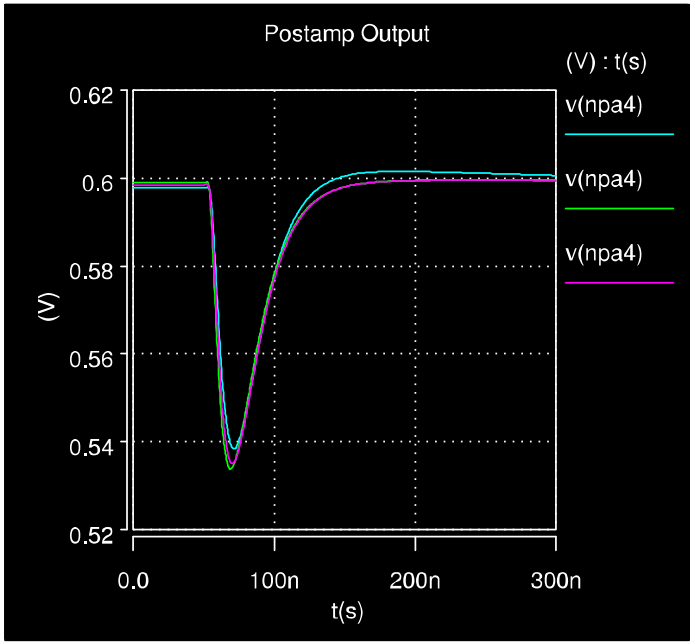




NMOS VT reduces as T increases => V across cascode gets too small if cascode gate voltage left unchanged with temperature

cascode bias vs temperature



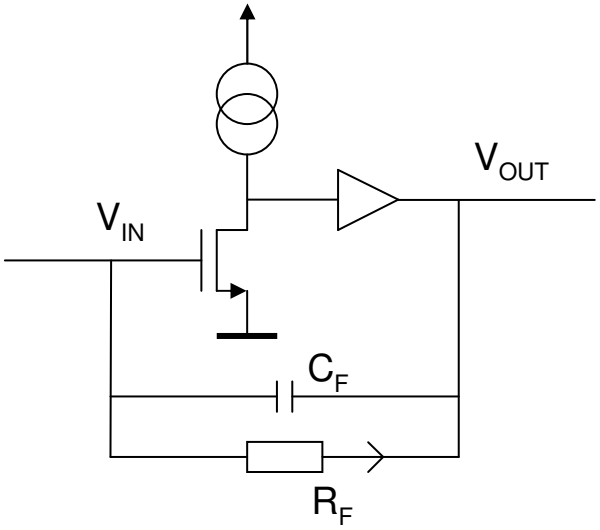


reducing cascode gate voltage (**npc**) with increasing temperature solves problem

this adjustment implicit in all following simulations vs temperature

this is only adjustment required for whole front end circuit to allow for temperature variation

preamp feedback for electrons (n-in-p)



in quiescent state, no leakage, resistive negative feedback path maintains $V_{IN} = V_{OUT}$

= ~ 0.25V for NMOS I/P

for n-in-p (collecting electrons) I_{LEAK} flows out of amplifier
neg. feedback adjusts V_{OUT} to maintain V_{IN} the same

ΔV (+ve) = $I_{LEAK}.R_F$ (e.g. 1 µA x 200k = 200 mV)

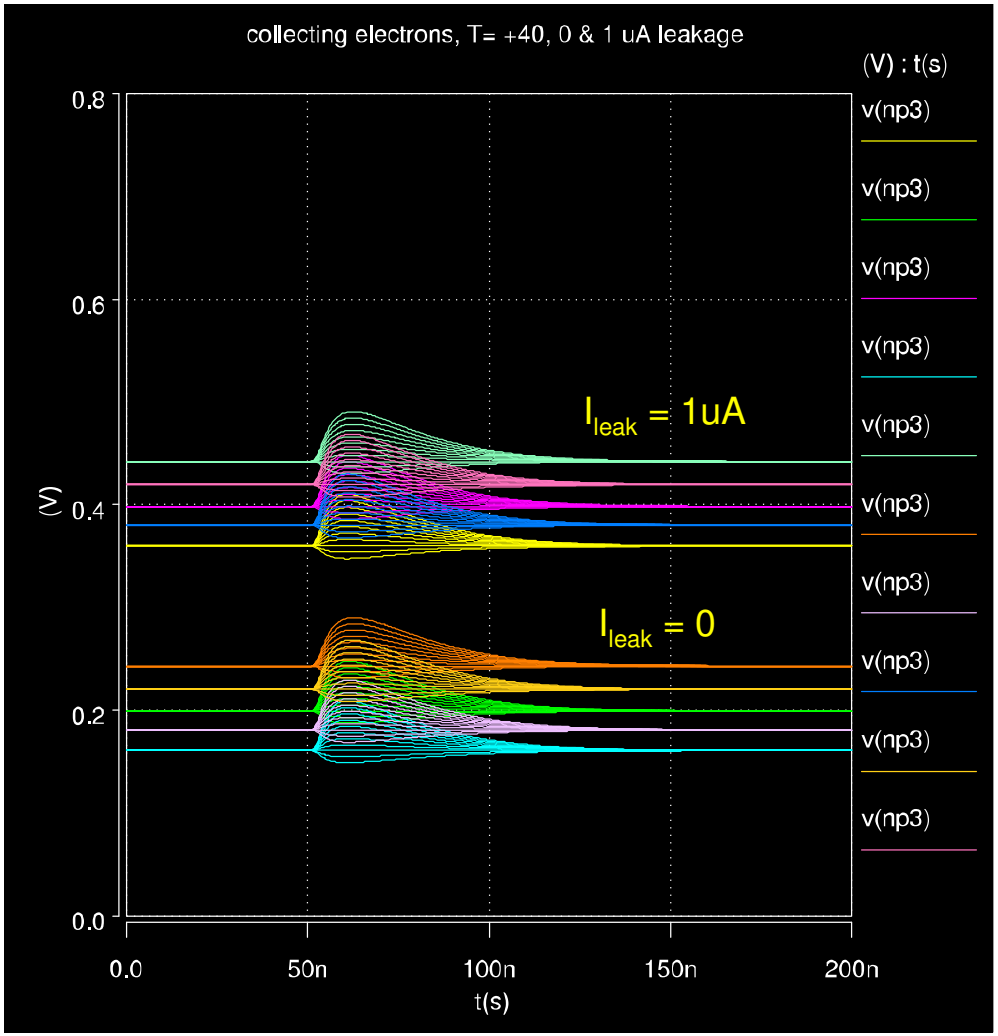
positive movement of V_{OUT} easily accommodated in amp headroom

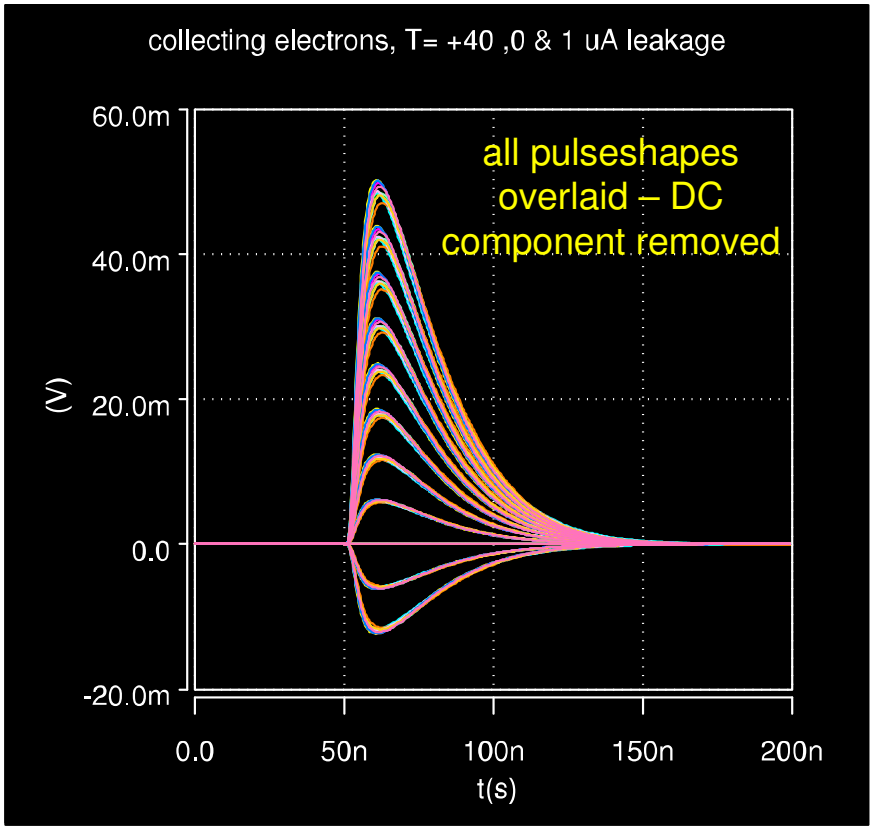
for p-in-n (collecting holes) I_{LEAK} flows into amplifier => V_{OUT} goes negative and quickly hits GND

=> need alternative scheme to create headroom to accommodate leakage current for p-in-n

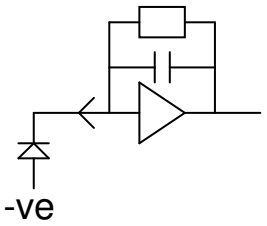
(previously proposed raising source of input device but now prefer to replace R_F by T network)

preamp performance for n-in-p (collecting electrons)

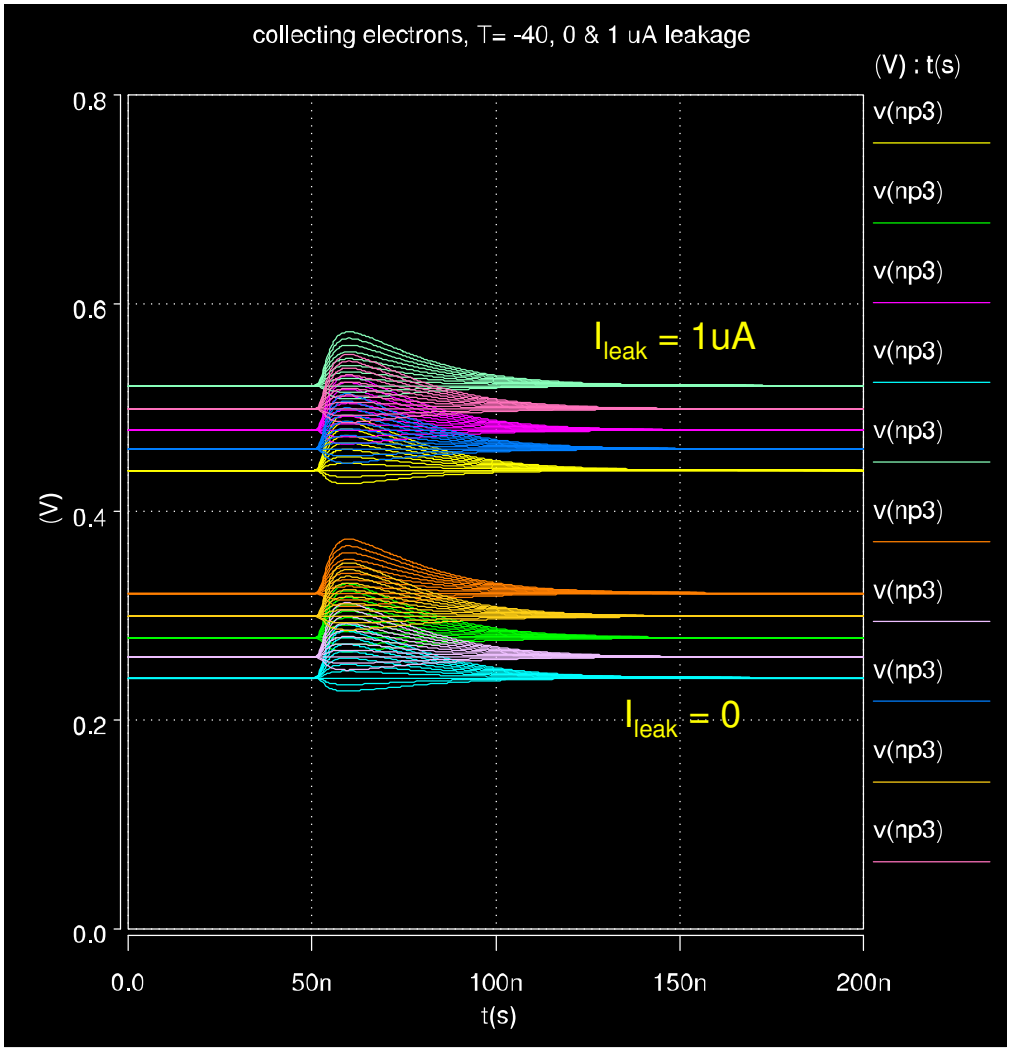


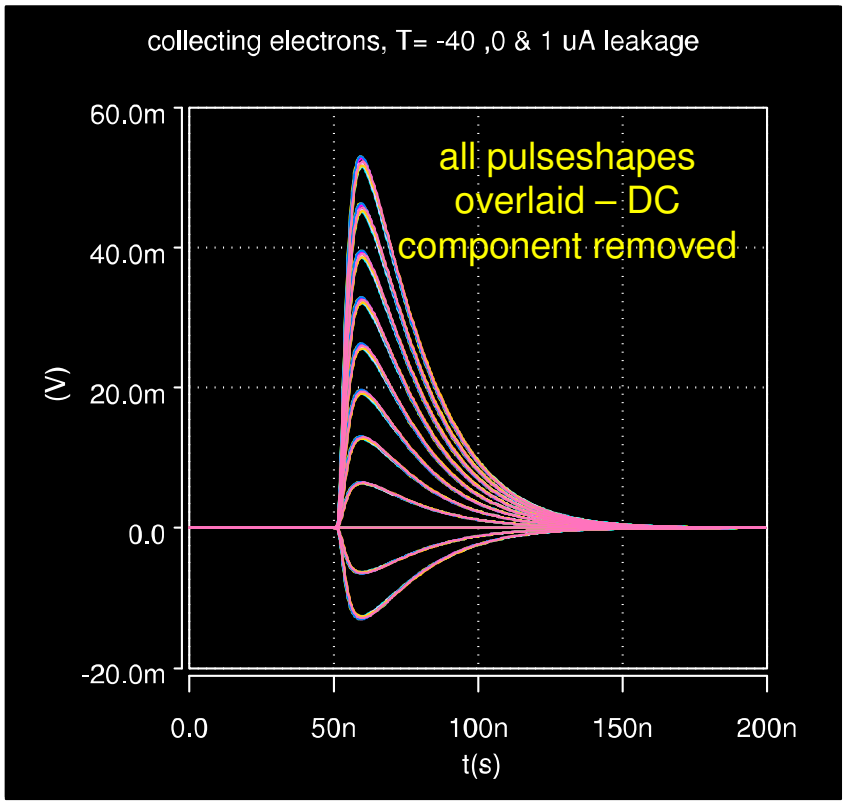


signal (at preamp O/P) from -2fC to 8fC in 1 fC steps
all process corners
T = +40 degrees



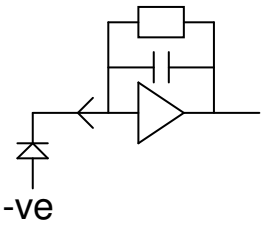
preamp performance for n-in-p (collecting electrons)



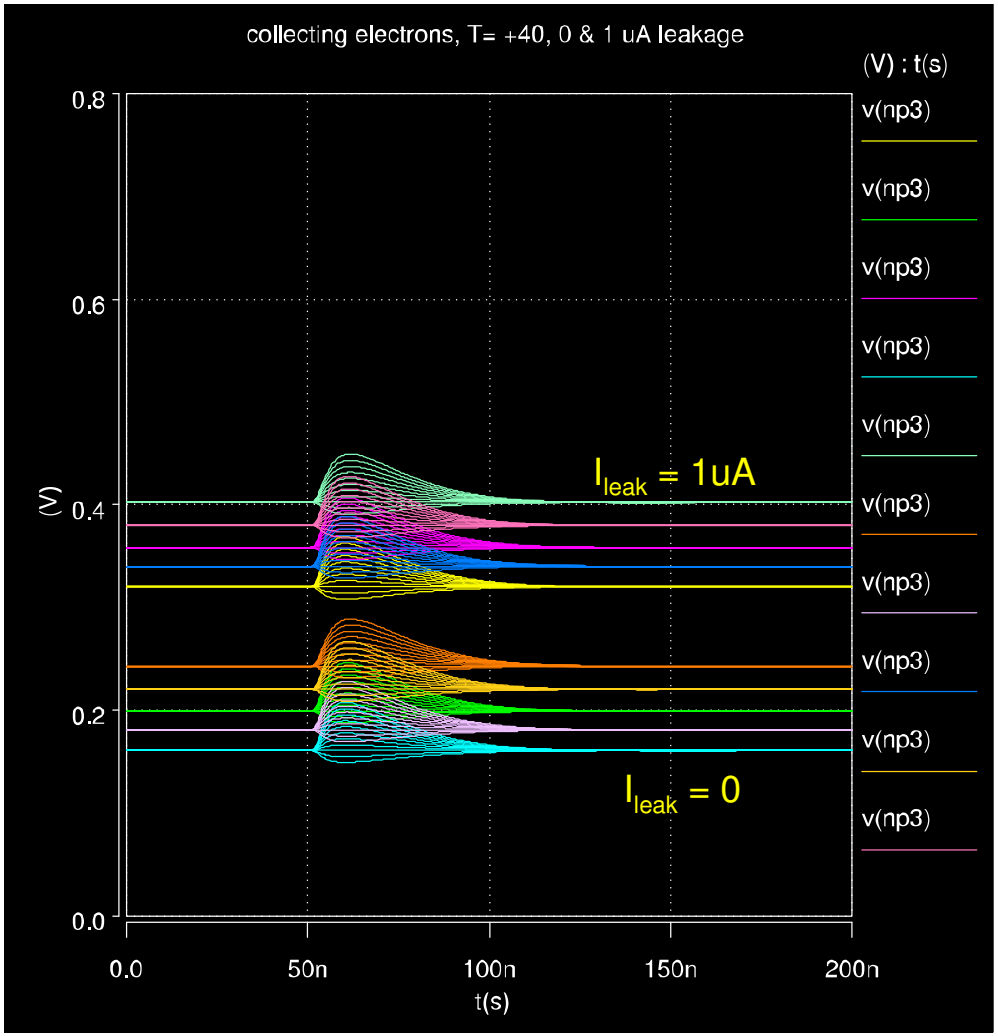


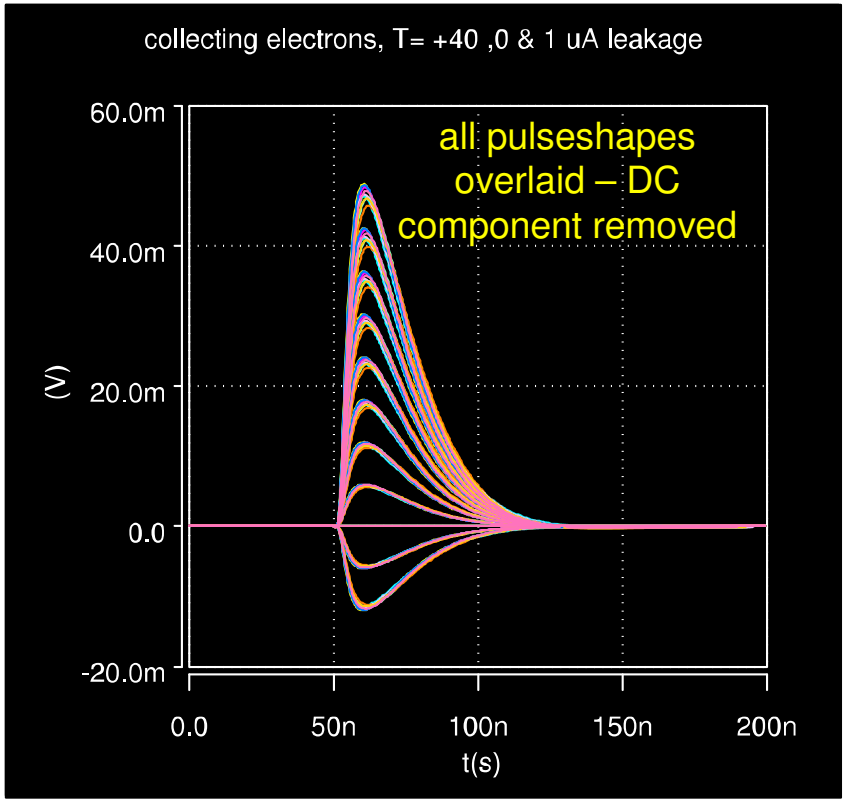
signal (at preamp O/P) from -2fC to 8fC in 1 fC steps
all process corners

T = - 40 degrees

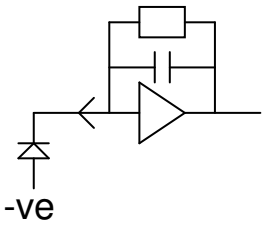


preamp performance for n-in-p (collecting electrons)



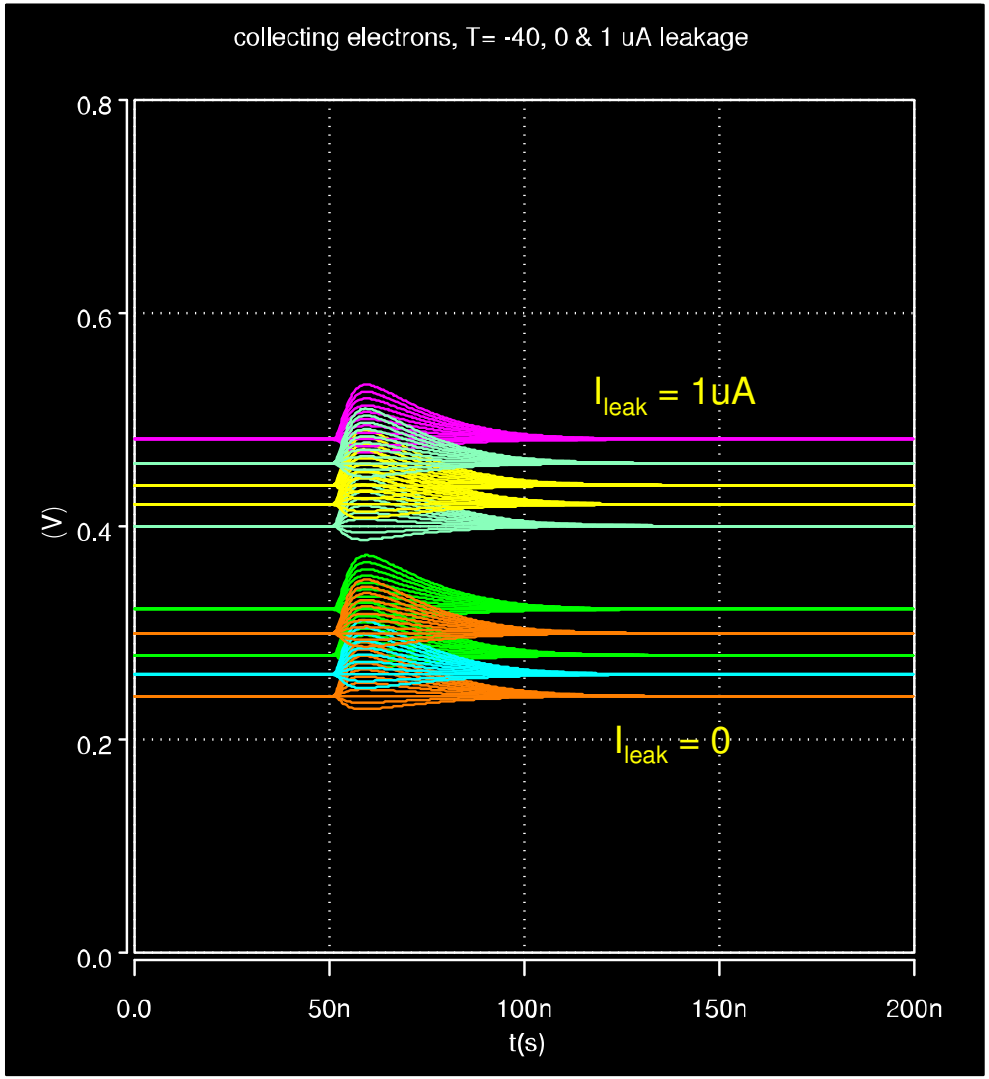


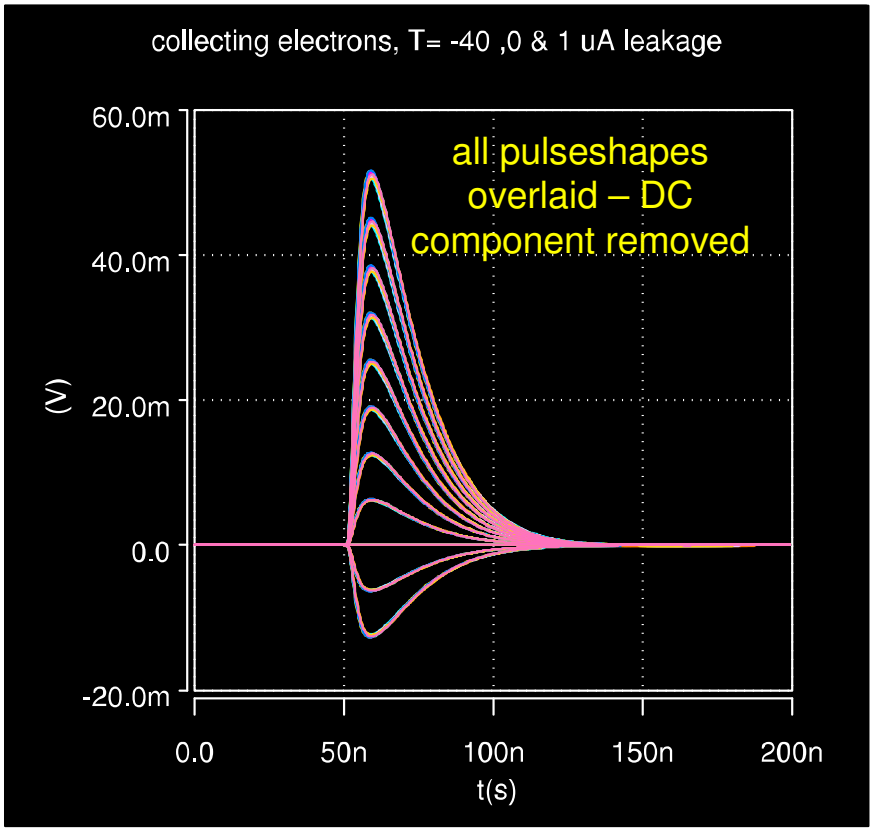
signal (at preamp O/P) from -2fC to 8fC in 1 fC steps
all process corners
T = + 40 degrees



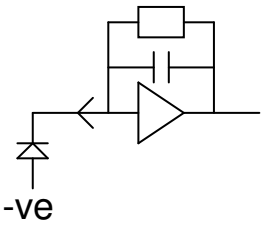
Effect of 20% Rf reduction to 160k

preamp performance for n-in-p (collecting electrons)



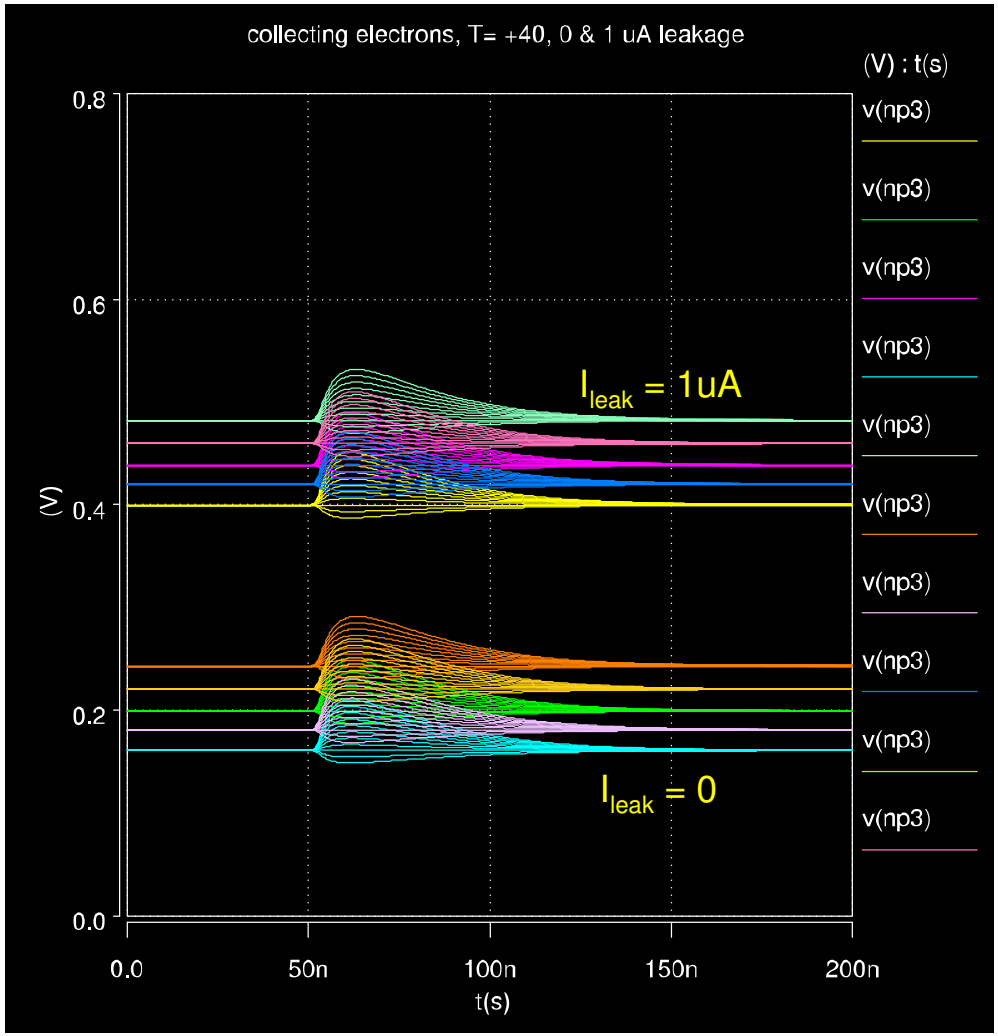


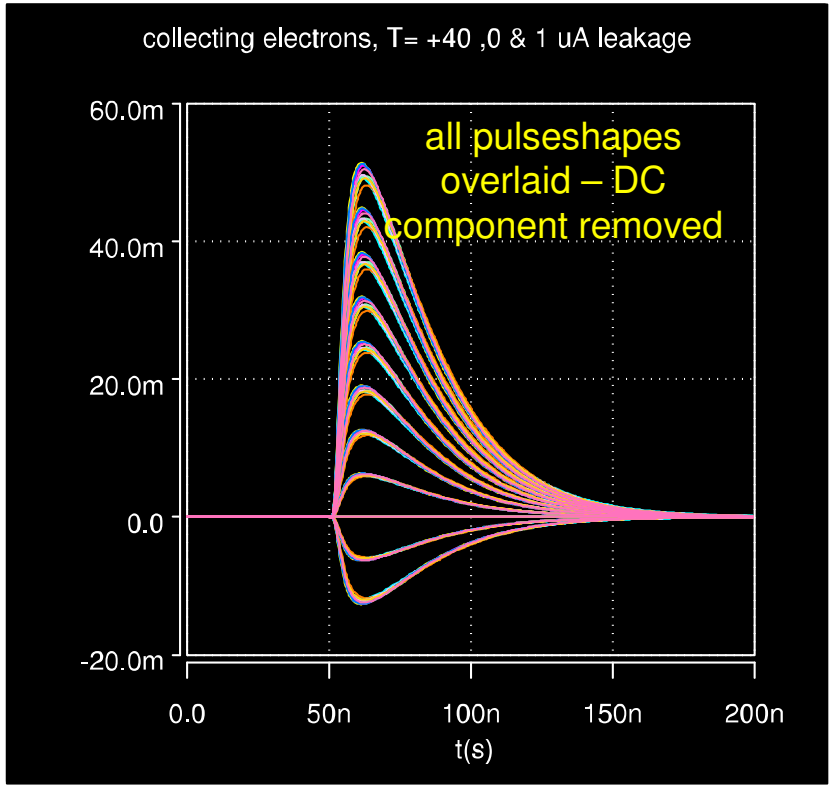
signal (at preamp O/P) from -2fC to 8fC in 1 fC steps
all process corners
T = - 40 degrees



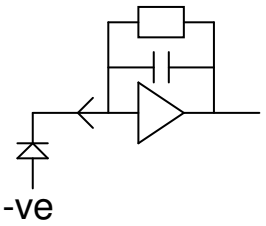
Effect of 20% Rf reduction to 160k

preamp performance for n-in-p (collecting electrons)



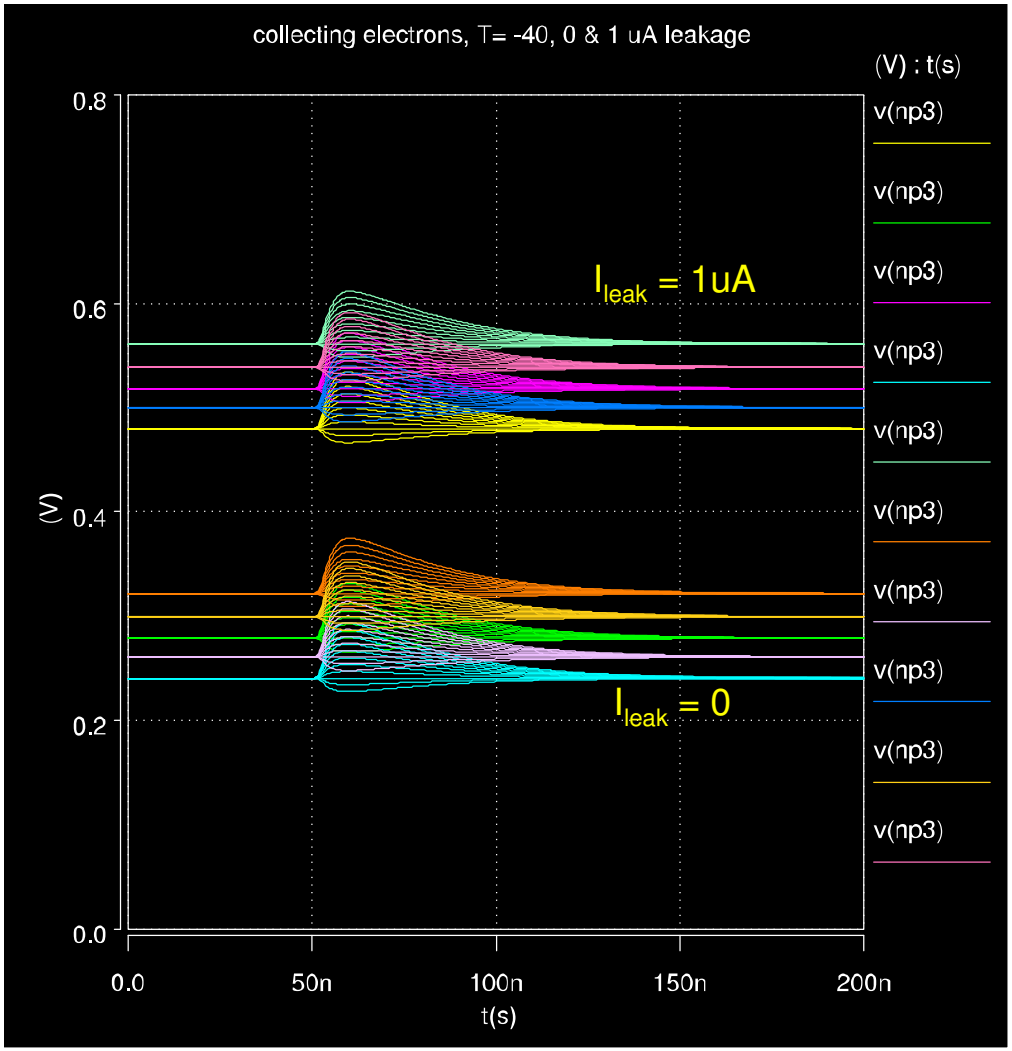


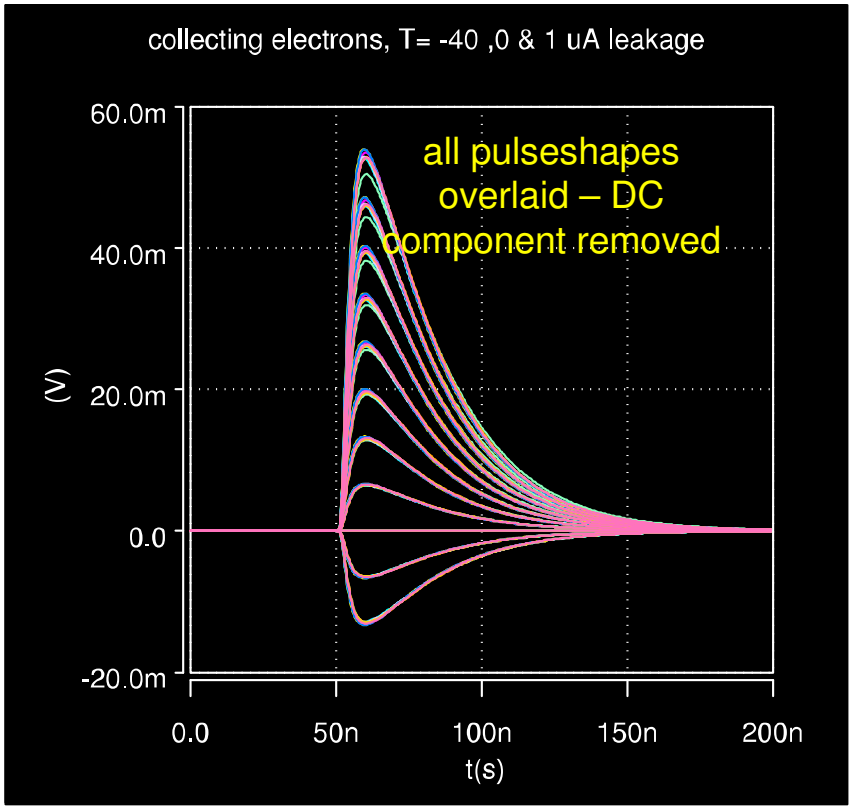
signal (at preamp O/P) from -2fC to 8fC in 1 fC steps
all process corners
T = + 40 degrees



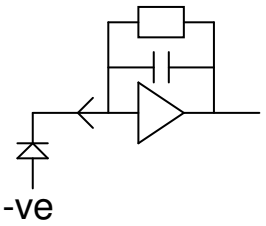
Effect of 20% Rf increase to 240k

preamp performance for n-in-p (collecting electrons)

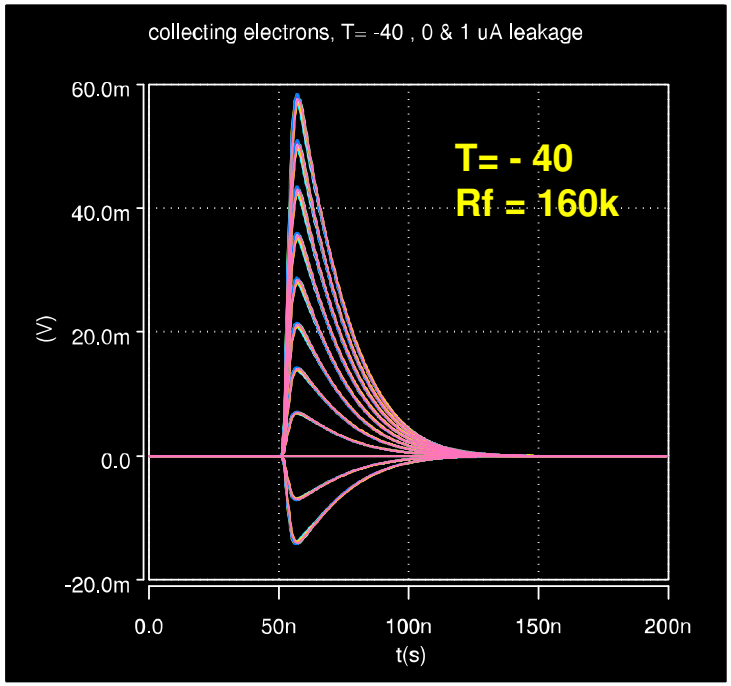




signal (at preamp O/P) from -2fC to 8fC in 1 fC steps
all process corners
T = - 40 degrees



Effect of 20% Rf increase to 240k

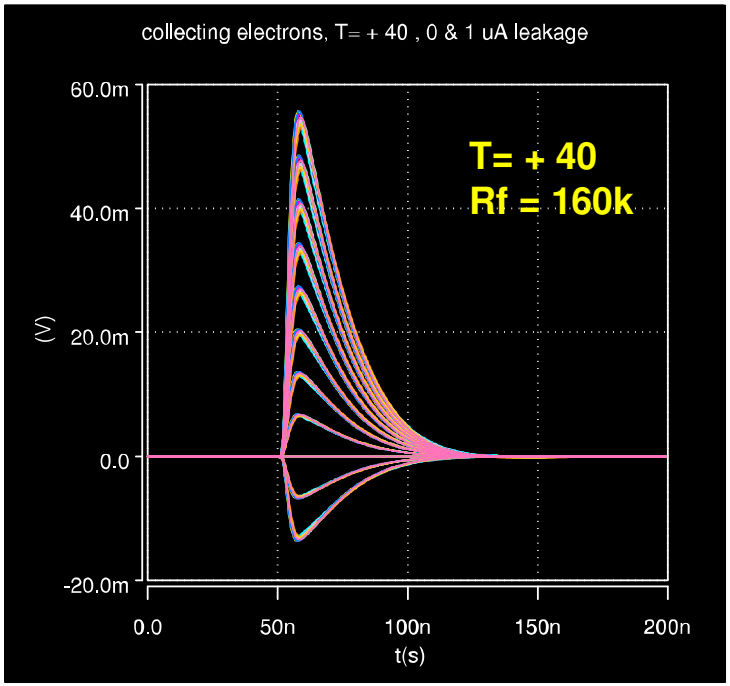


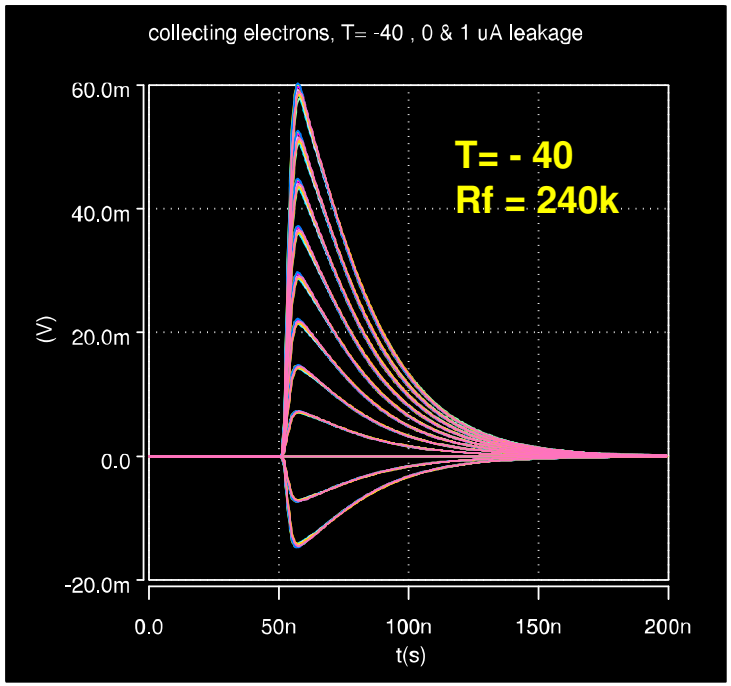
preamp for n-in-p (collecting electrons)

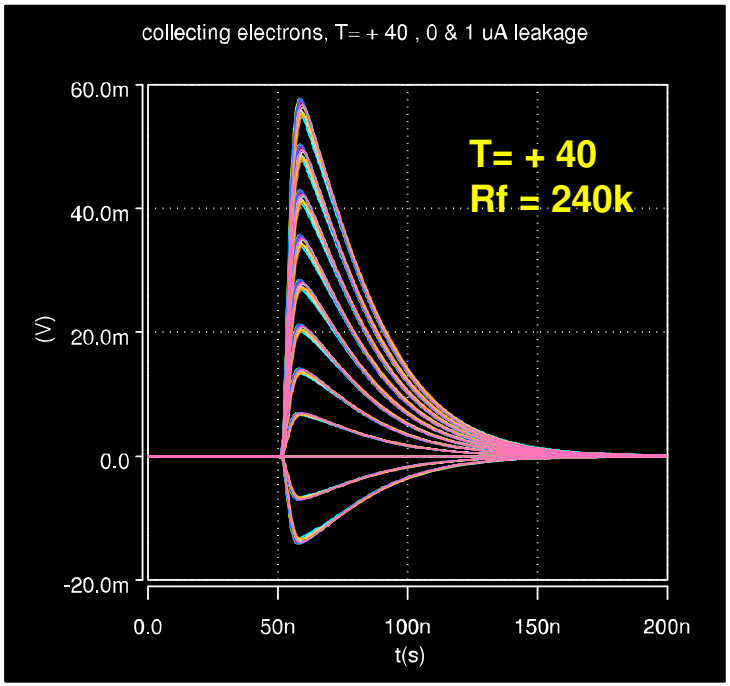
check performance for different factors affecting DC operating point (Csensor/IDS, Rf process variations)

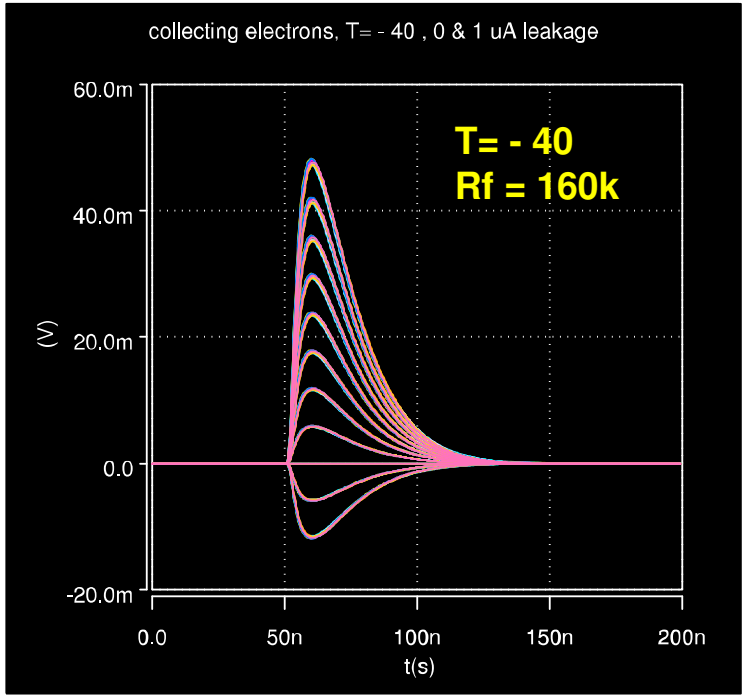
all sims for all process corners and Ileak = 0 & 1 uA

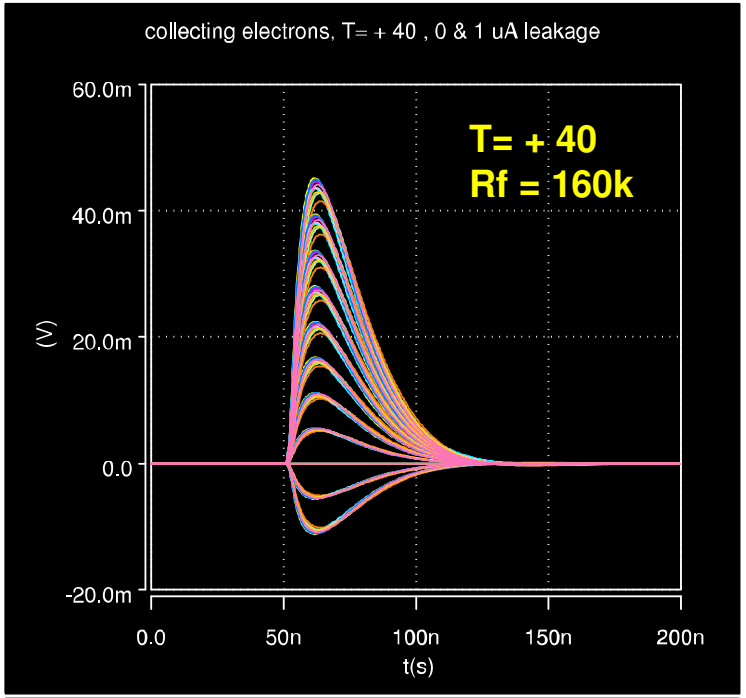
Csensor = 2pF
IDS = 65 µA





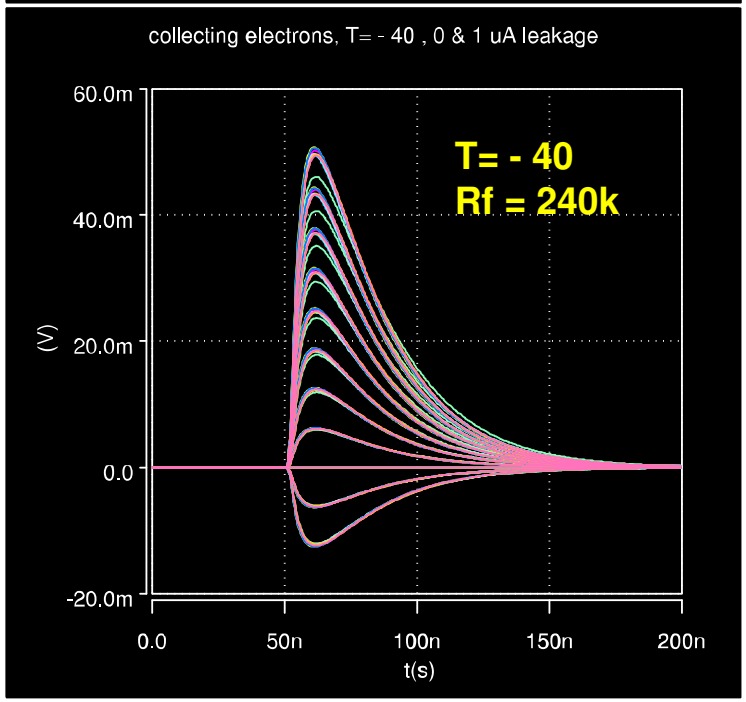


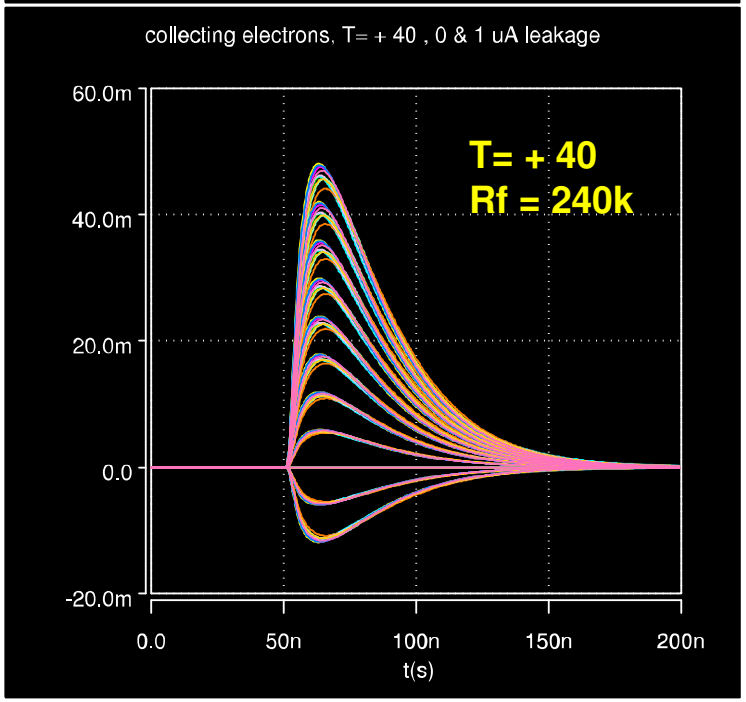




preamp for n-in-p (collecting electrons)

Csensor = 10 pF
IDS = 195 µA





preamp performance for n-in-p (collecting electrons)

conclusions

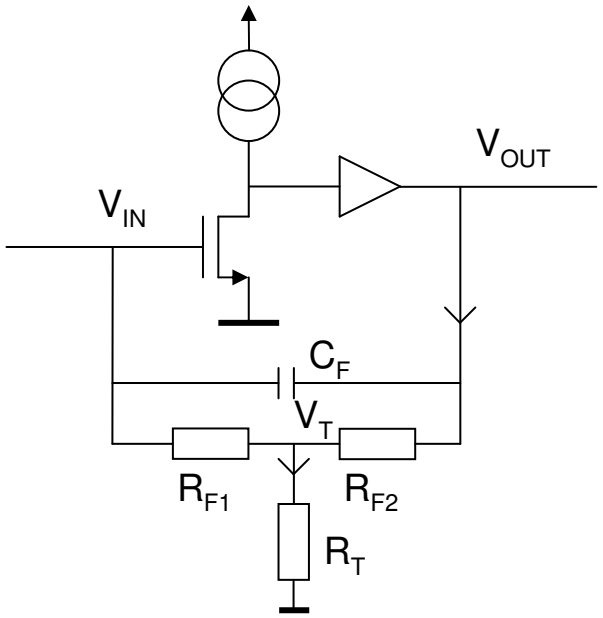
preamp design for n-in-p looks pretty robust to extremes of:

leakage current: 0 & 1 μA
temperature: -40 to +40
feedback resistor variation: +/- 20%
all functional process corners:

but sensor choice for outer sLHC tracker now looks likely to be p-in-n

collecting holes rather than electrons

preamp feedback for p-in-n



T network of resistors in preamp feedback

in quiescent state, no leakage, resistive negative feedback path maintains $V_T = V_{OUT}$

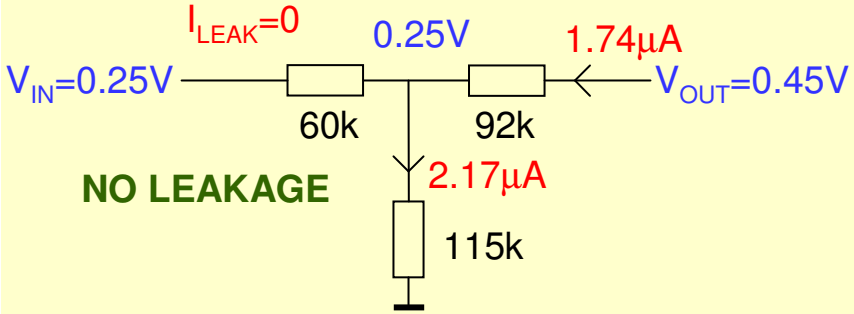
= ~ 0.25V for NMOS I/P

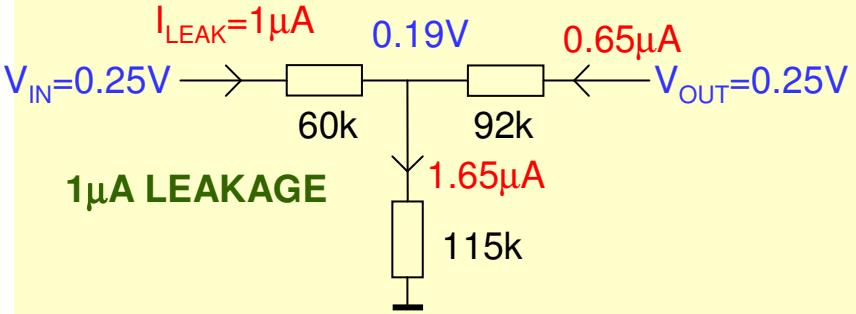
=> V_{OUT} has to shift +ve to keep $V_T = V_{IN}$

=> by appropriate choice of resistor values can compensate for -ve shift produced by leakage

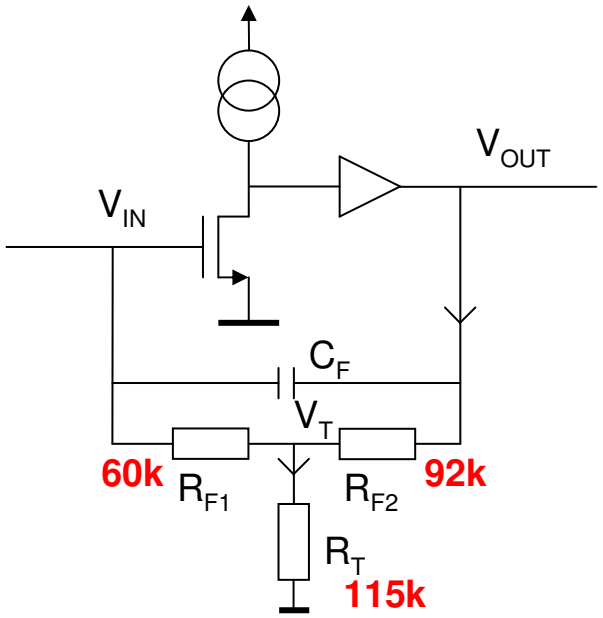
e.g. if R_{F2} = 92k, R_{F1} = 60k, R_T = 115k, then $V_T = V_{OUT}/2$ = 0.25V, and V_{OUT}(quiescent) = 0.45V

If I_{LEAK} = 1 µA then V_{OUT} shifts to 0.25V to accommodate





preamp feedback for p-in-n



note that V_{OUT}(DC) depends on V_{IN}(DC) with a gain factor 1.8

$$(R_{F2}+R_T) / R_T$$

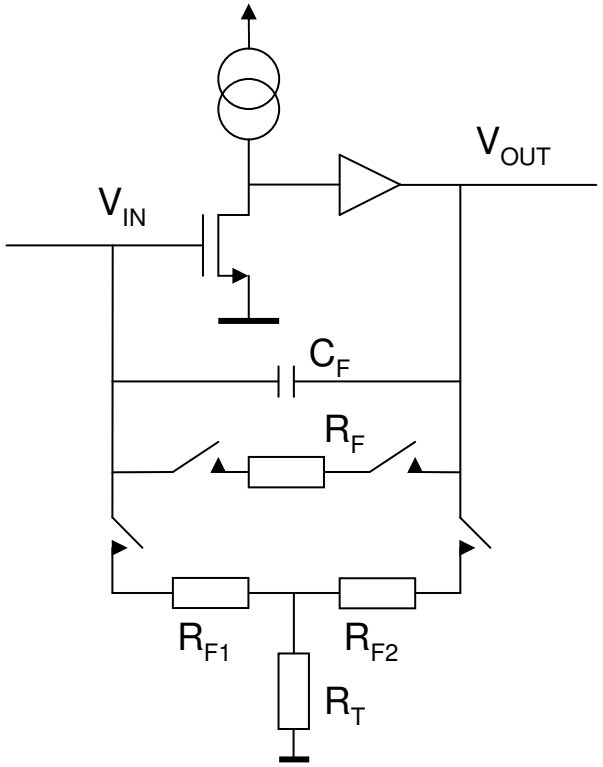
(also in single resistor n-in-p case, but there the gain factor = only 1)

So need to take care of simulating all conditions that affect DC value of V_{IN} including:

Temperature and process corners
DC current in input device
resistor process variations

the choice of actual resistor values was made (under simulation) by trying to maintain the effective noise resistance as high as possible, while ensuring satisfactory tolerance to process, temperature and operating point variations

to accommodate both polarities



need switches to select network for appropriate polarity

choice of resistor values

need $C_F.R_F = C_F.R_{TNETWORK}$

$$R_{TNETWORK} = R_{F1} + R_{F2} + R_{F1}.R_{F2}/R_T$$

so for R_F = 200k want $R_{NETWORK}$ = 200k

e.g. R_{F1} = 60k, R_{F2}= 92k R_T = 115k

noise

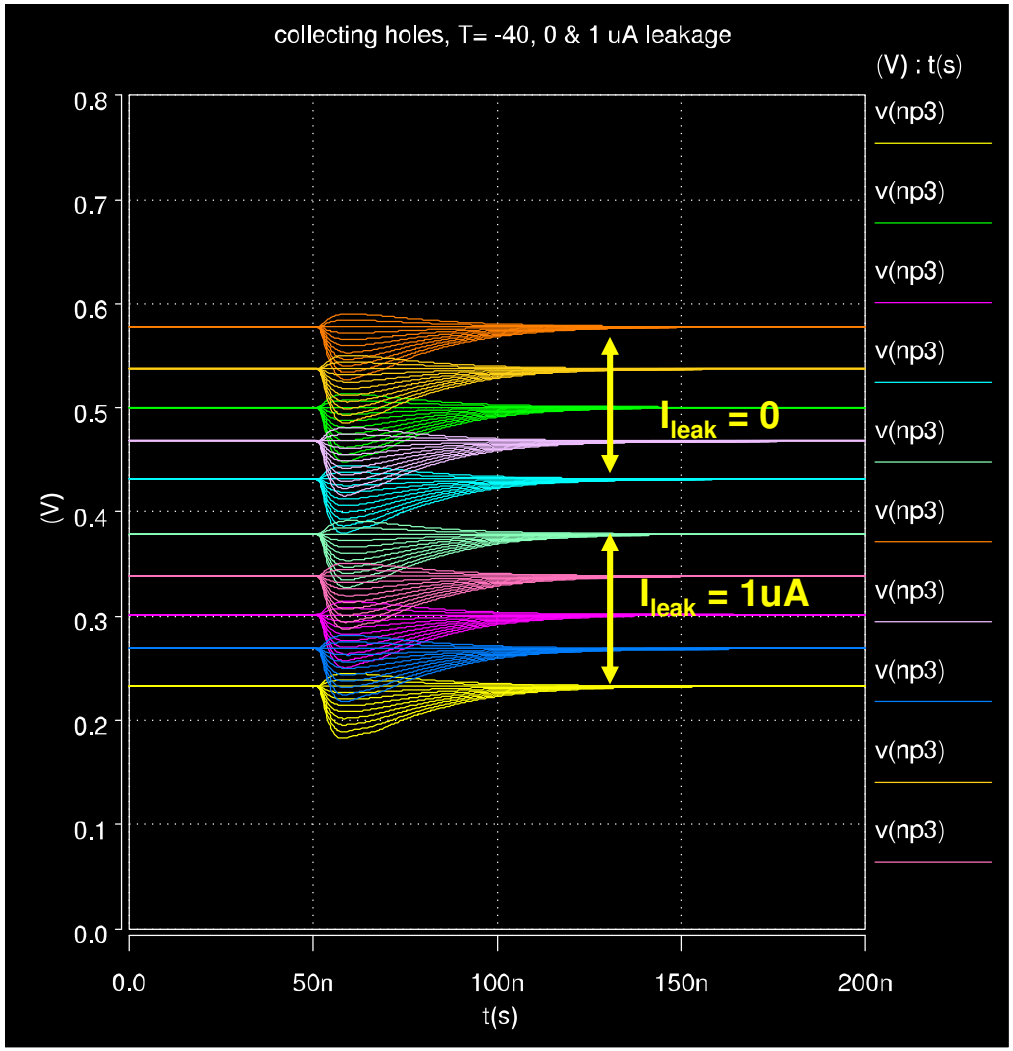
T network gives increased noise

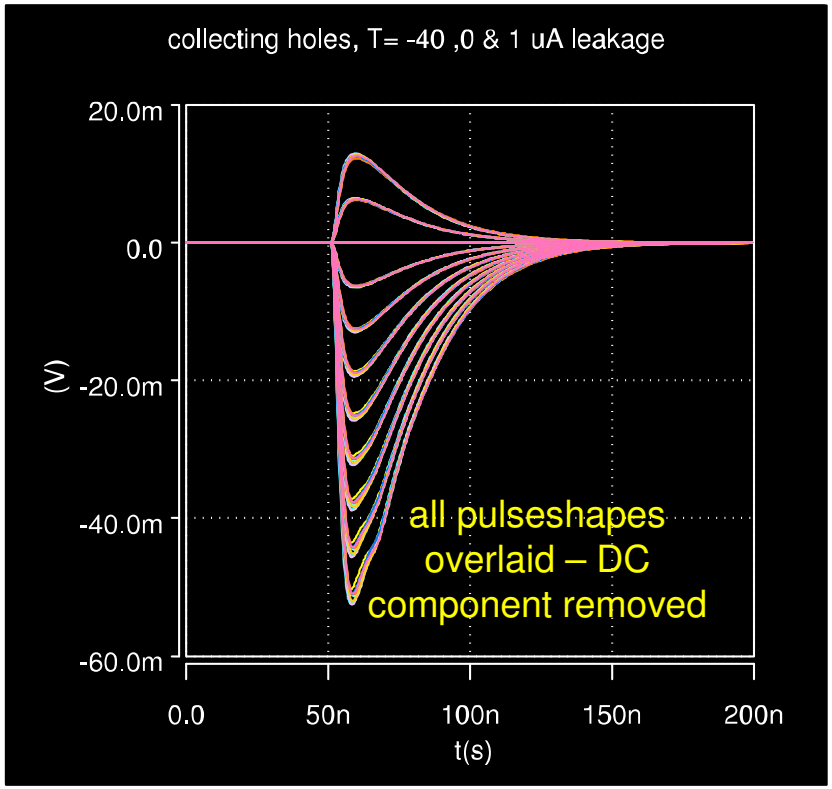
for resistor values above the effective noise resistance is 111k [60k + (92k//115k)]

=> 1.34 x noise contribution of 200k

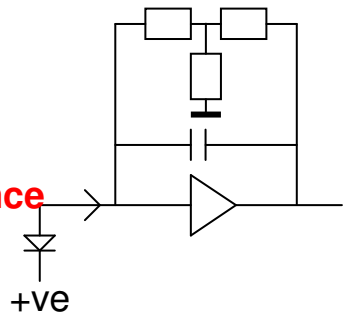
(but still small compared with amplifier noise)

preamp performance for p-in-n (collecting holes)



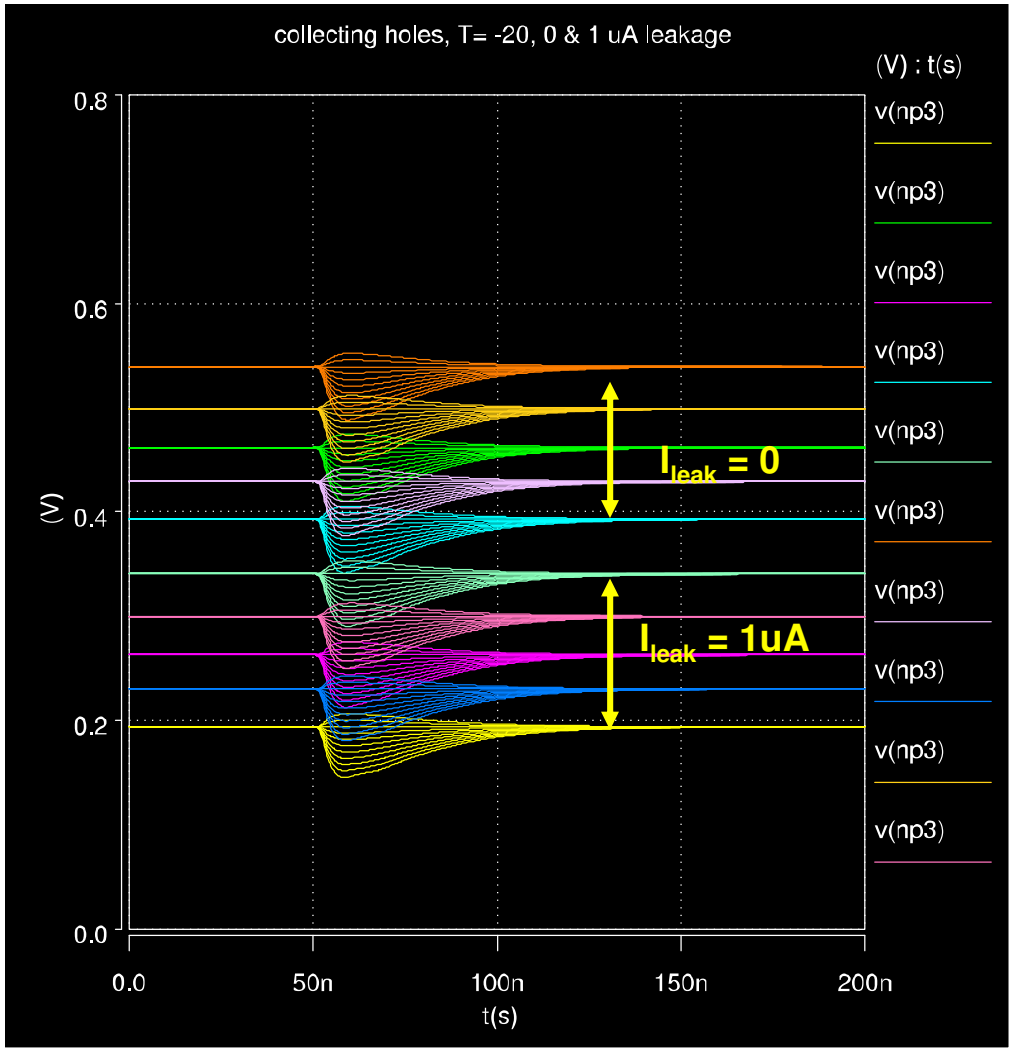


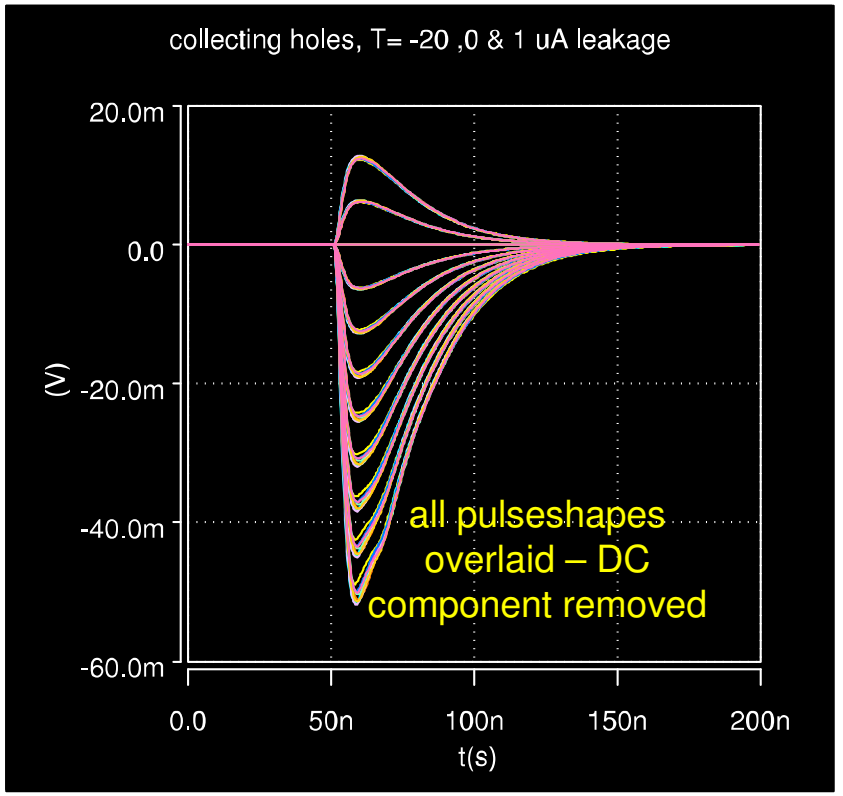
signal (preamp O/P) from 2fC to -8fC in 1 fC steps
all process corners
T = - 40 degrees



note: this (and following) simulations for 6 pF mid-range sensor capacitance and IDS = 130 µA

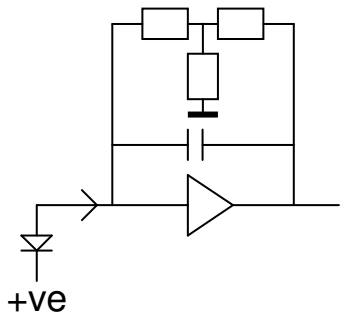
preamp performance for p-in-n (collecting holes)



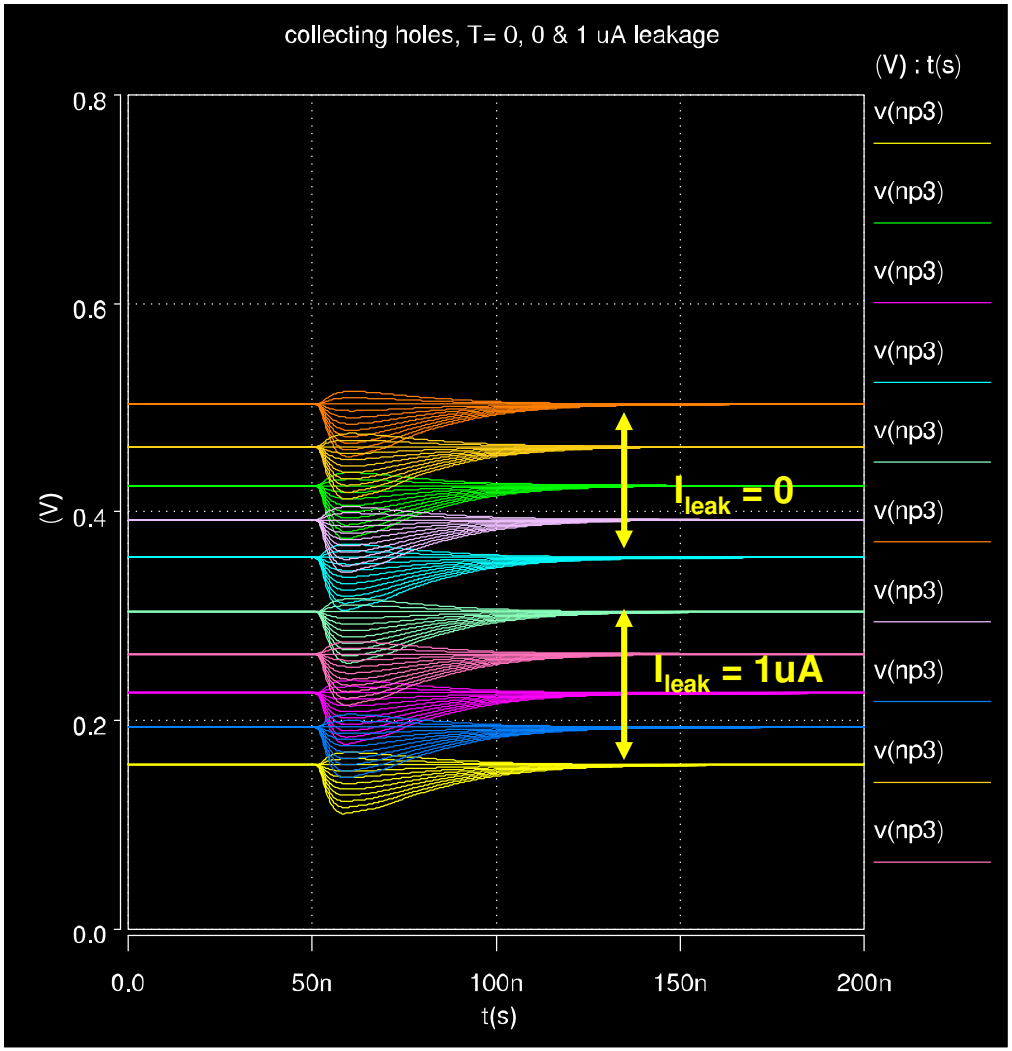


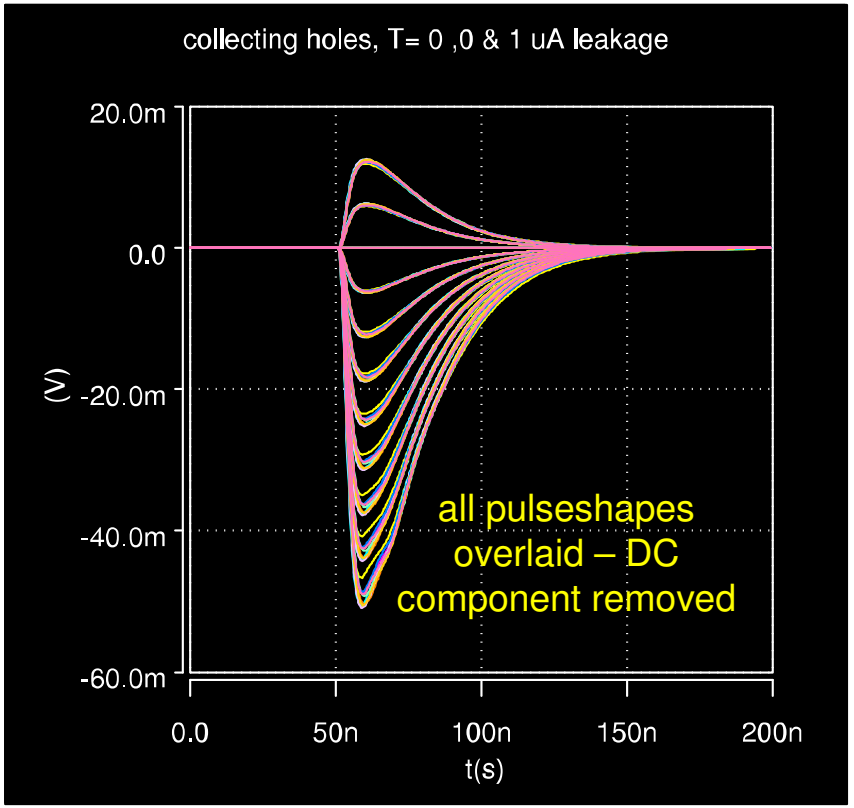
signal (preamp O/P) from 2fC to -8fC in 1 fC steps
all process corners

T = - 20 degrees



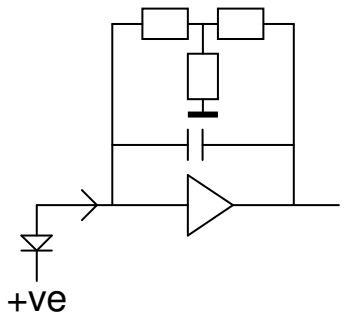
preamp performance for p-in-n (collecting holes)



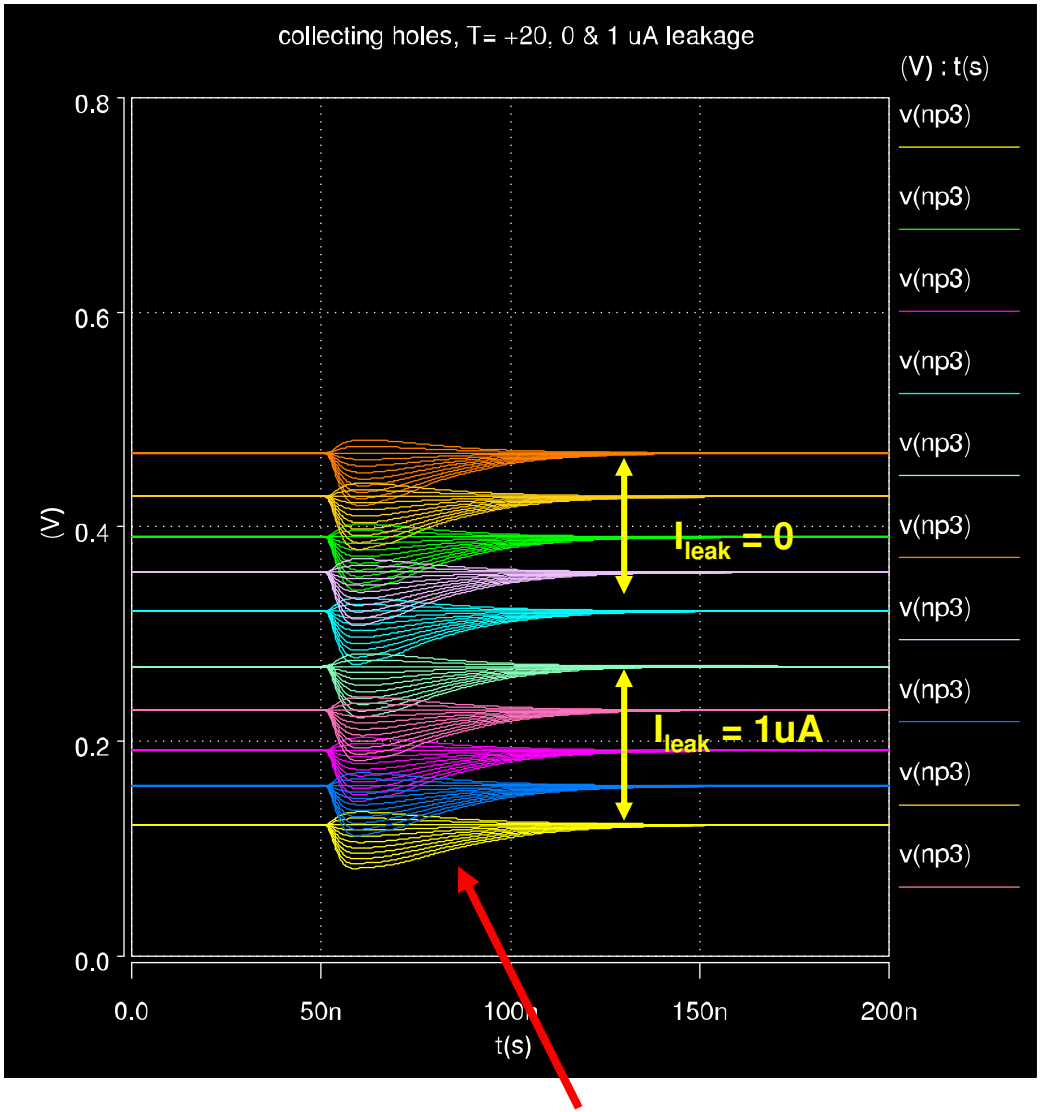


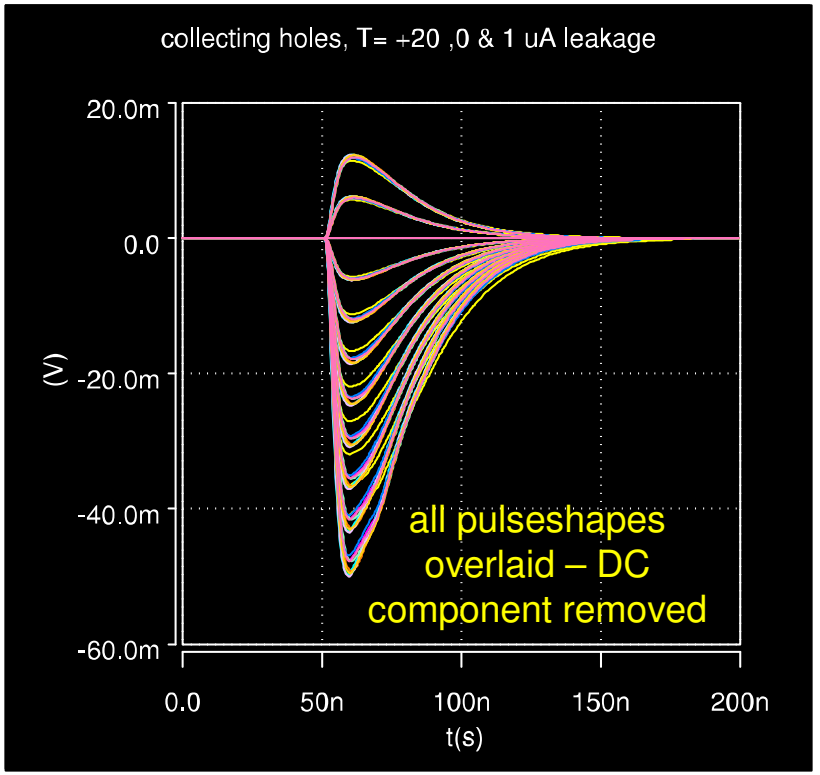
signal (preamp O/P) from 2fC to -8fC in 1 fC steps
all process corners

T = 0 degrees

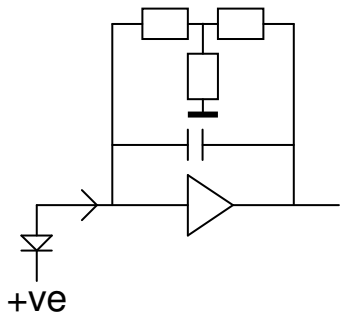


preamp performance for p-in-n (collecting holes)



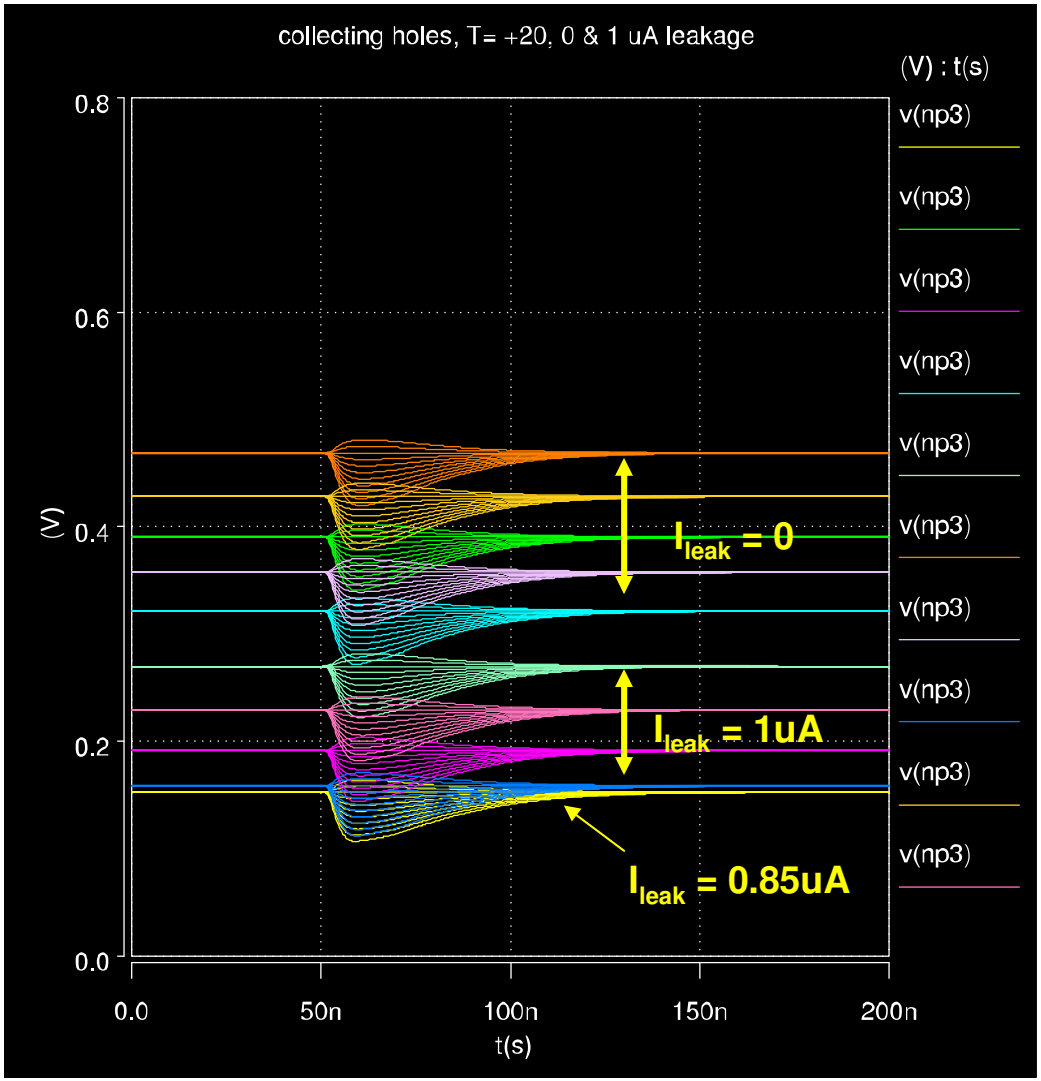


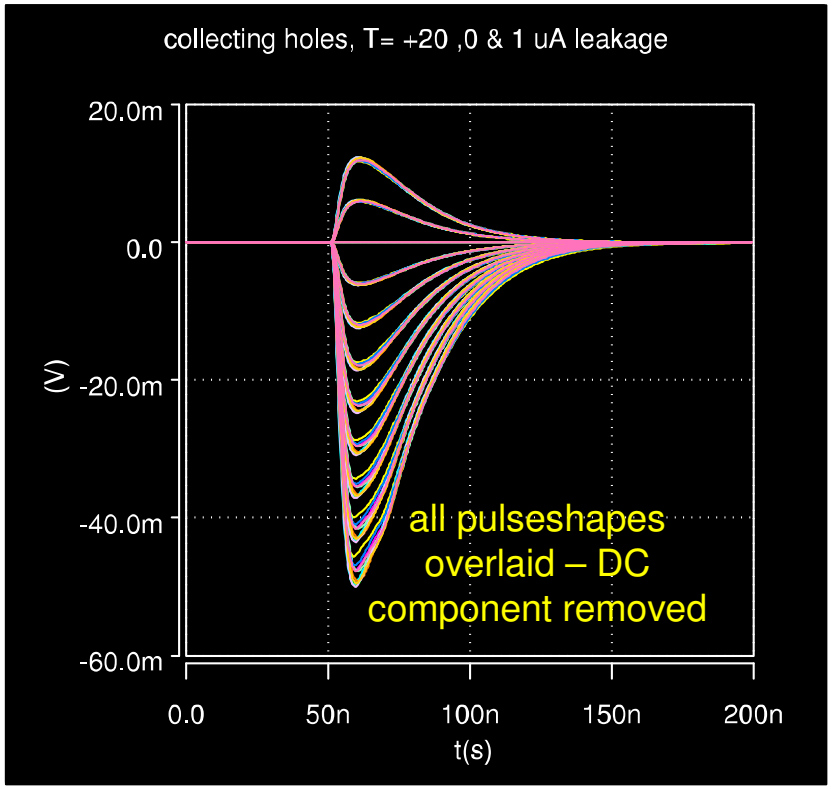
signal (preamp O/P) from 2fC to -8fC in 1 fC steps
all process corners
T = +20 degrees



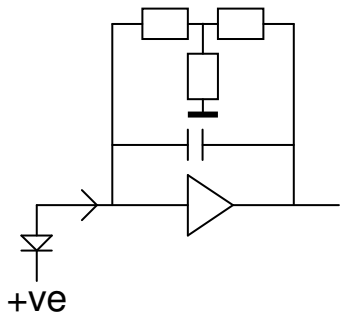
I_{LEAK} = 1uA at FF corner takes Preamp O/P too close to VSS

preamp performance for p-in-n (collecting holes)



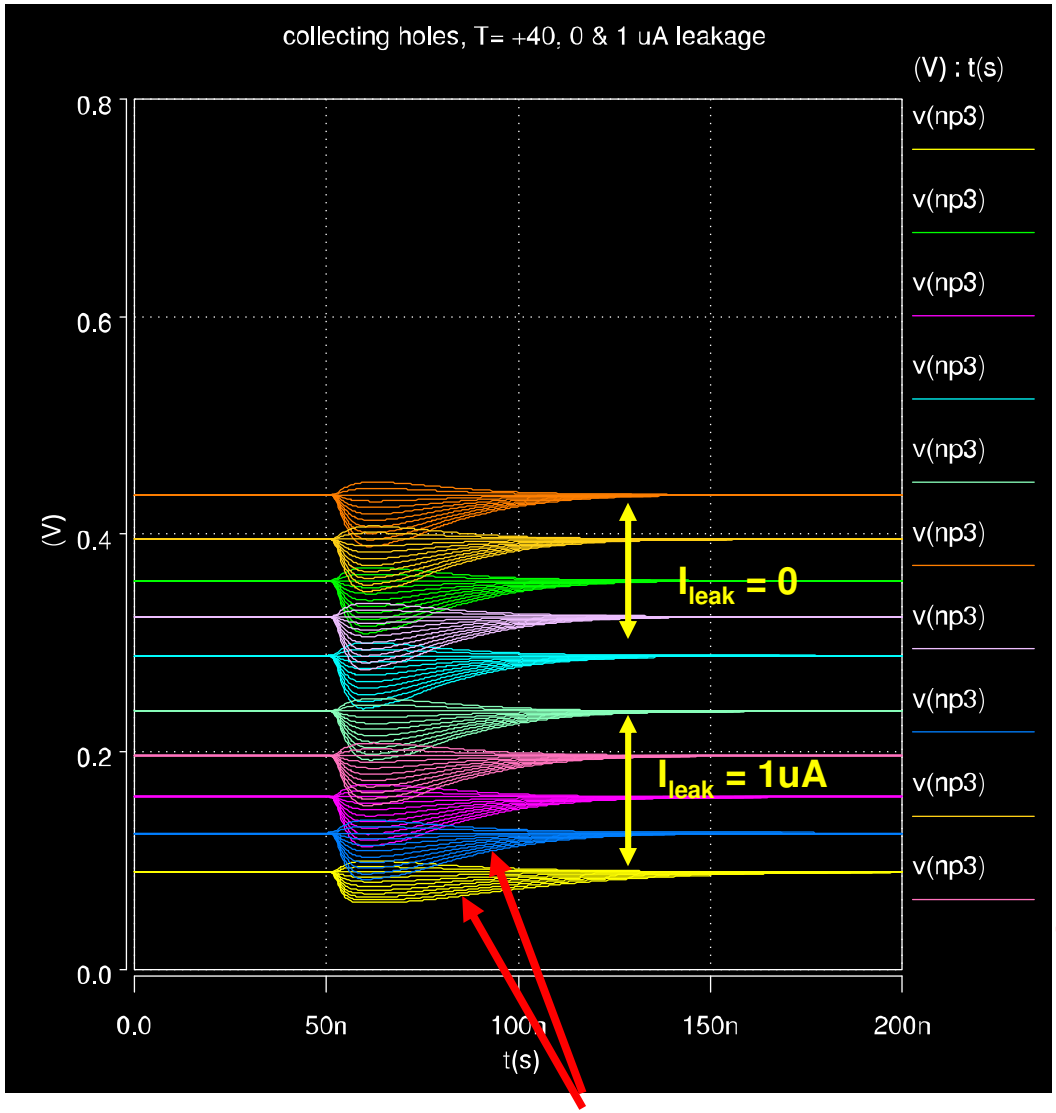


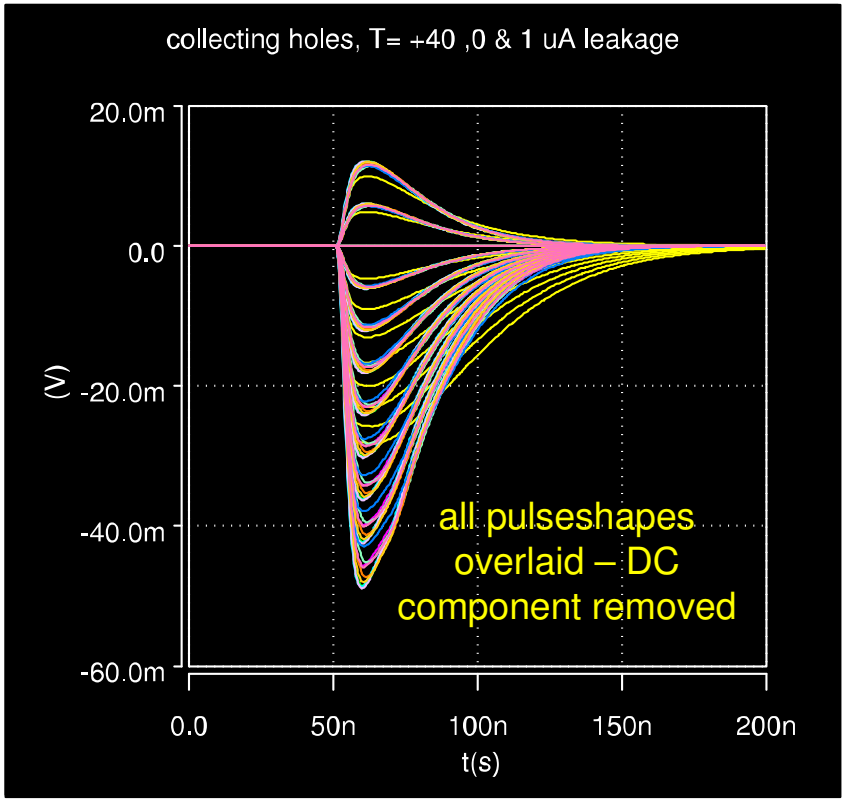
signal (preamp O/P) from 2fC to -8fC in 1 fC steps
all process corners
T = +20 degrees



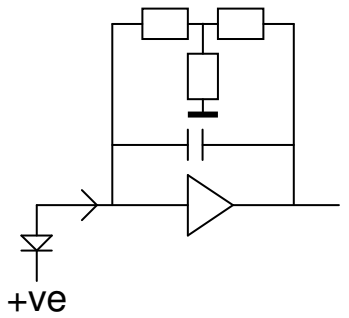
tolerable I_{LEAK} for FF corner reduced to 850nA for T=+20

preamp performance for p-in-n (collecting holes)





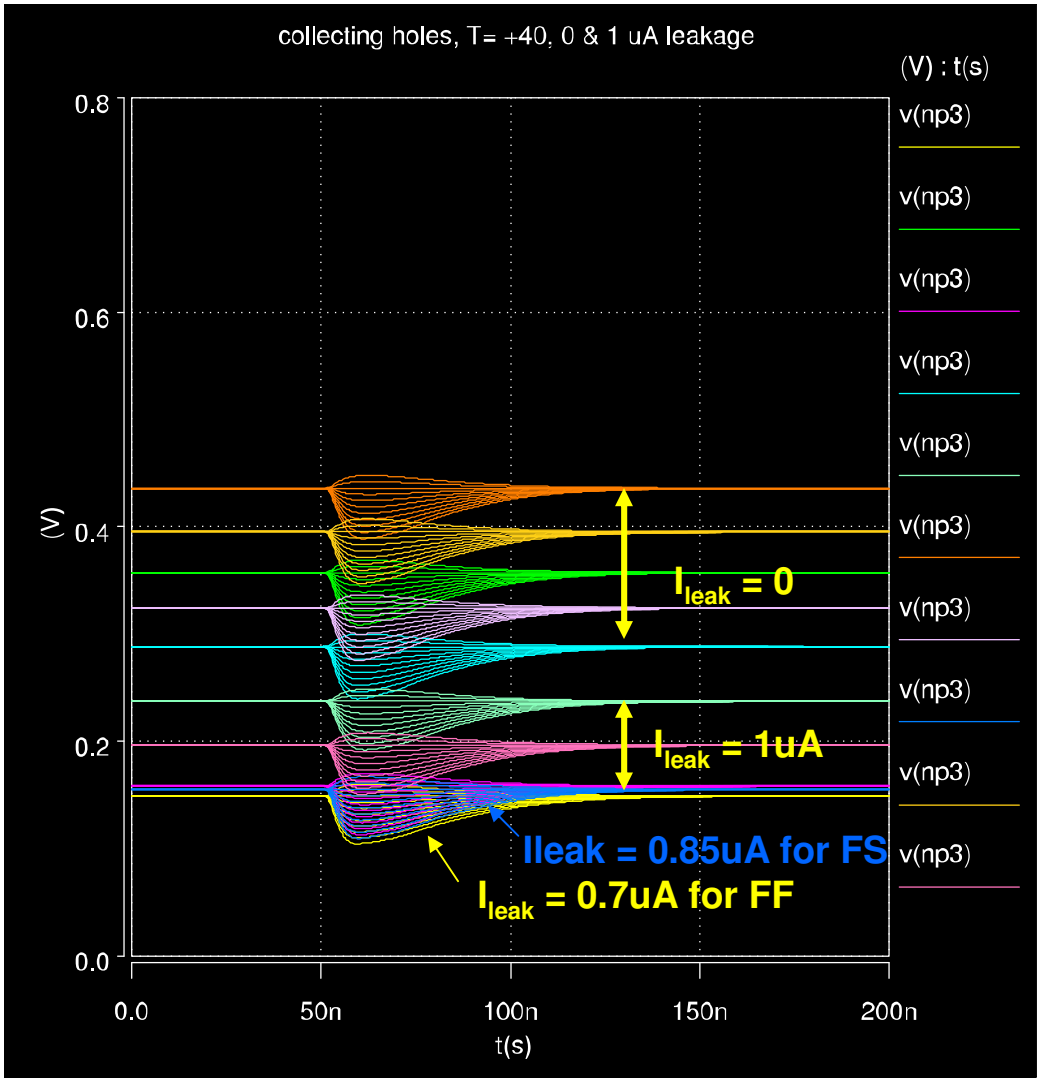
signal (preamp O/P) from 2fC to -8fC in 1 fC steps
all process corners
T = +40 degrees

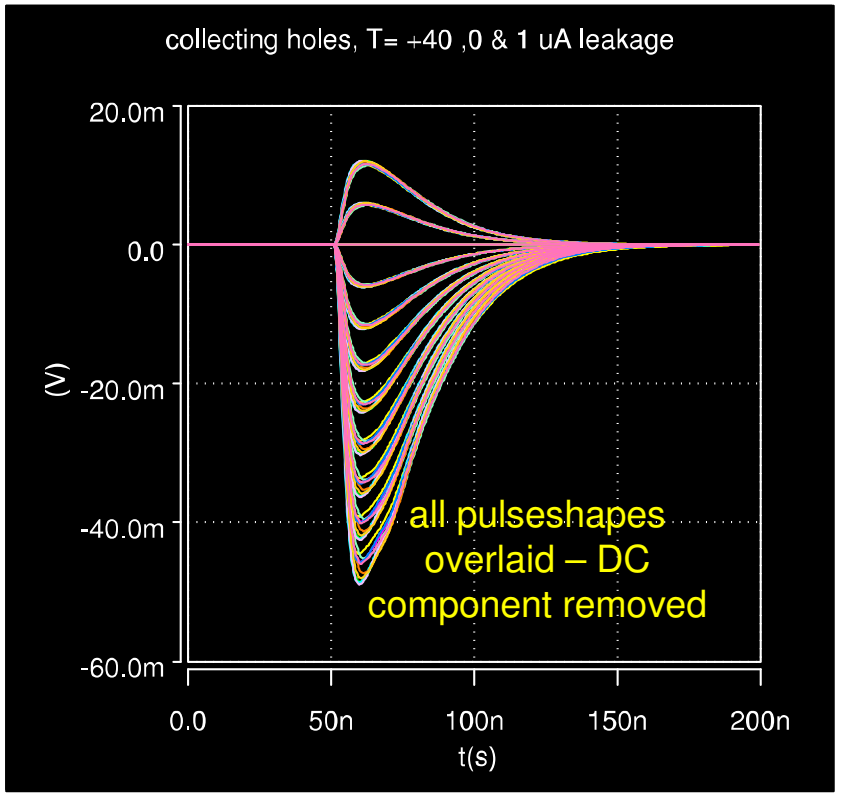


I_{LEAK} = 1uA at FF & FS corner takes Preamp O/P too close to VSS

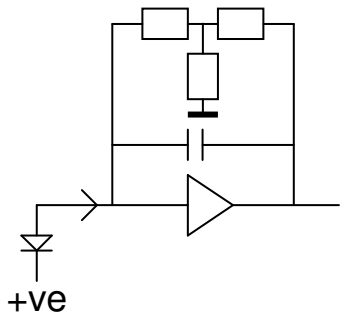
FF = Fast N, Slow P

preamp performance for p-in-n (collecting holes)





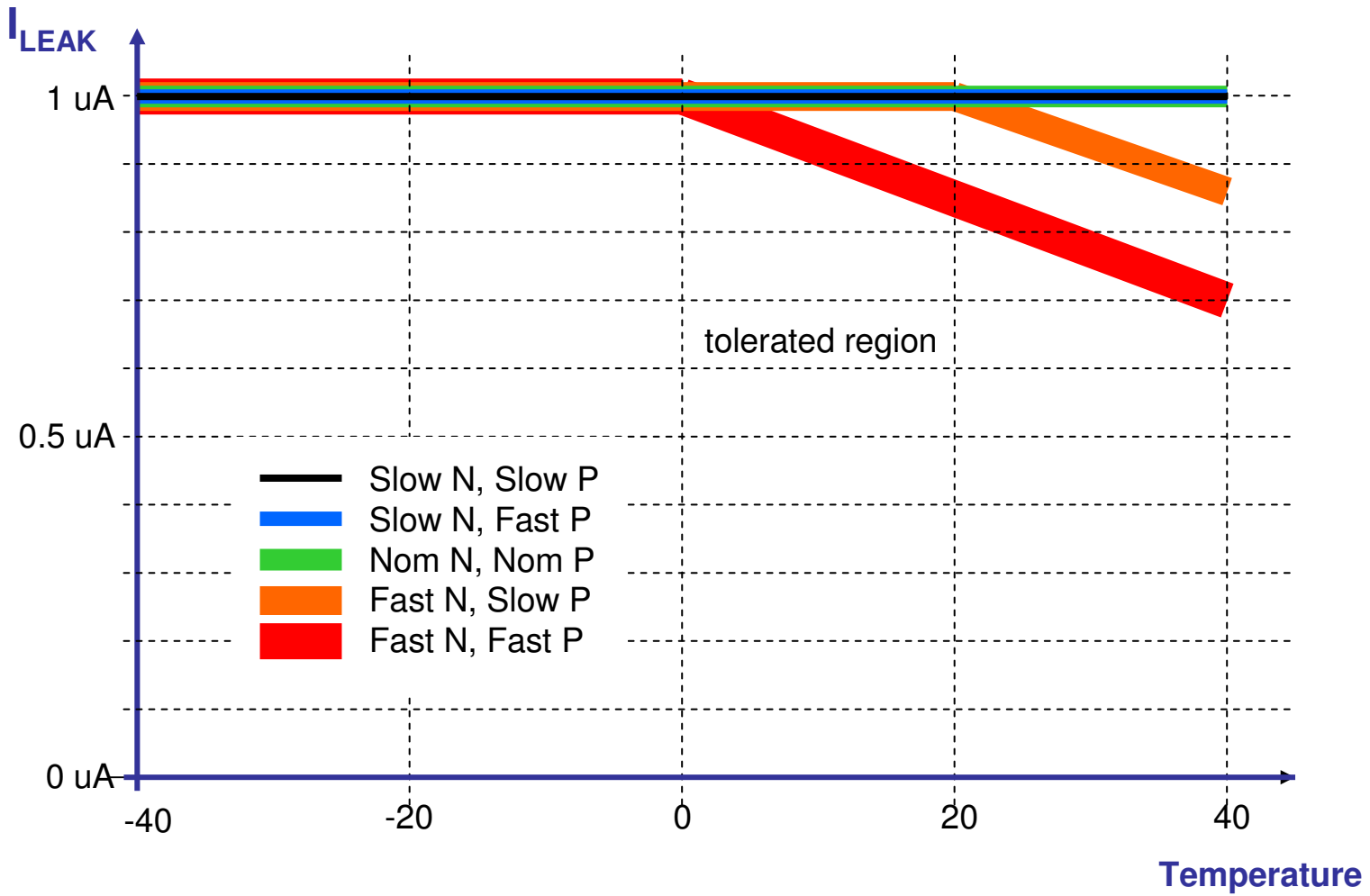
signal (preamp O/P) from 2fC to -8fC in 1 fC steps
all process corners
T = +40 degrees



tolerable I_{LEAK} for FF corner reduced to 700nA for T=+20 & 850nA for FS corner

preamp performance for p-in-n (collecting holes)

for IDS = 130 µA the tolerable DC leakage current is reduced for 2 of the process corners
but no reductions are necessary for temperatures below zero



preamp performance for p-in-n (collecting holes)

repeat all variety of simulations previously shown for n-in-p

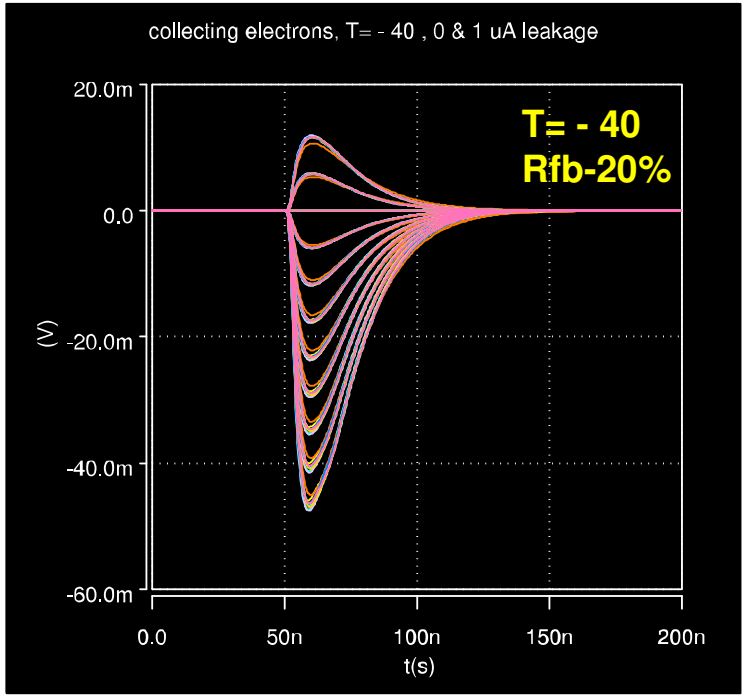
use values appropriate for 2 pF (IDS=65 μA) and 10 pF (IDS=195 μA)
(relative to nominal 130 μA @ 6 pF)

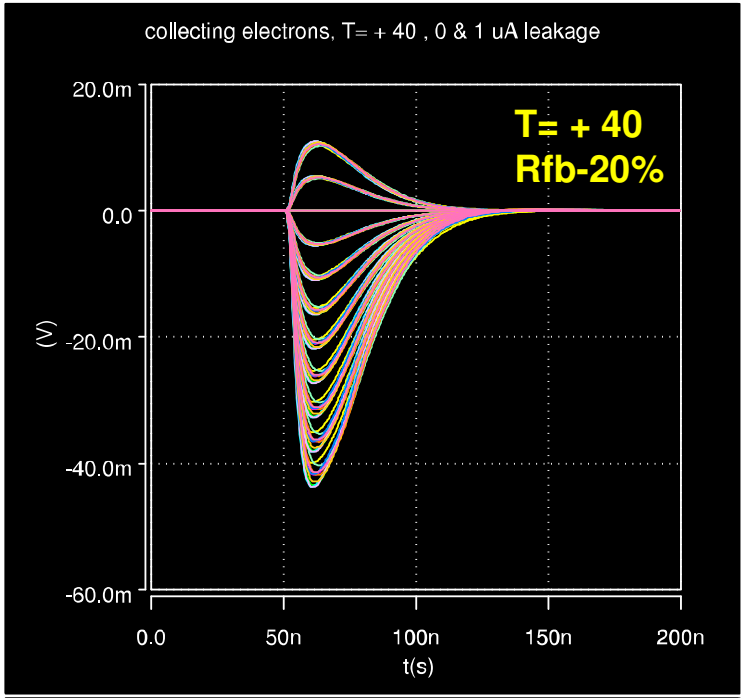
and extremes of temperature (-40, +40) and Rf (-20%, +20%)

all 3 resistors in T network reduced or increased by 20% at same time

always 0 and 1 uA and all process corners

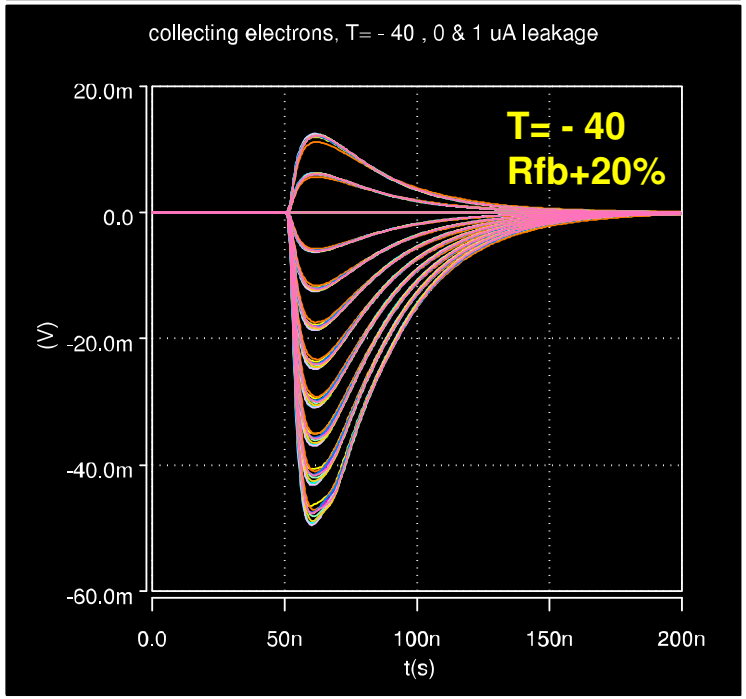
leave out the DC picture for brevity





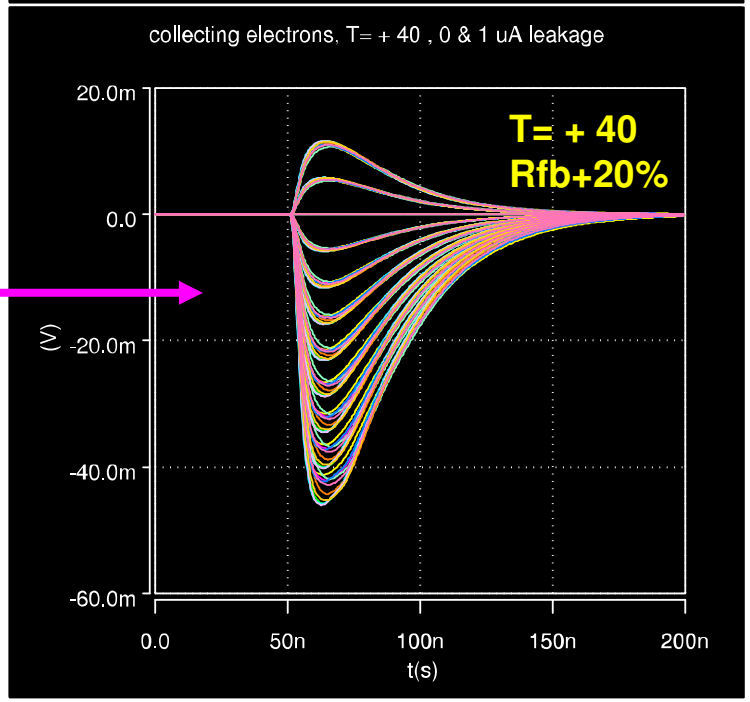
preamp
for p-in-n
(collecting
holes)

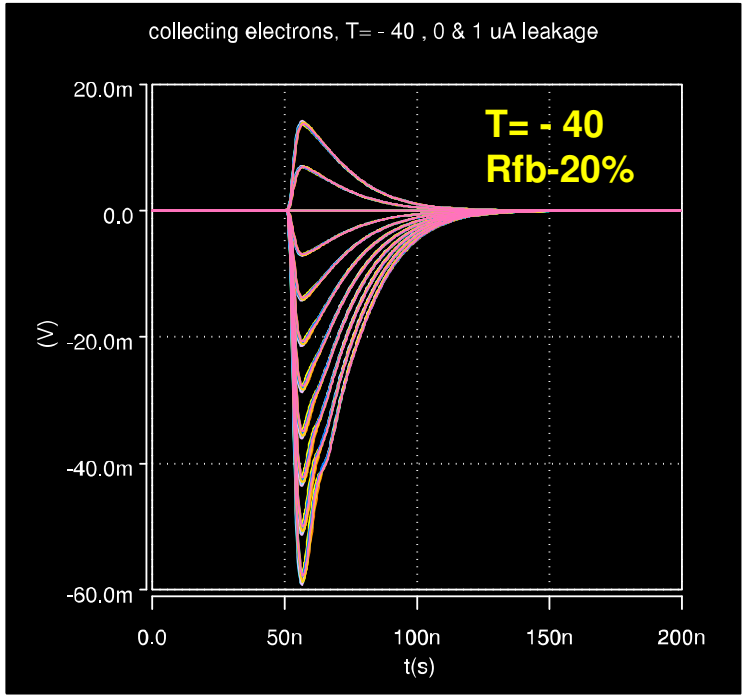
Csensor = 10 pF
IDS = 195 μA



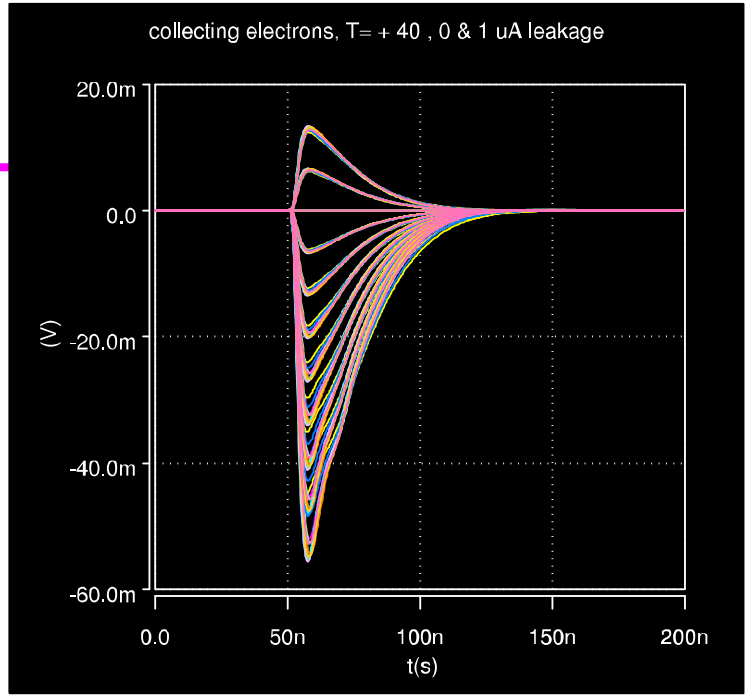
FF and FS
Ileak values
reduced as
for C = 6 pF

note:not found
necessary
for Rfb-20%



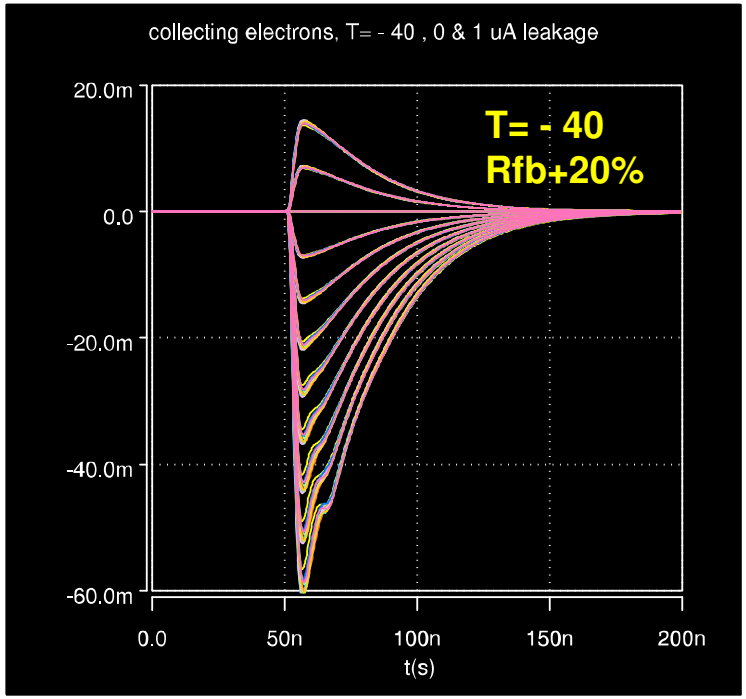


for FF only Ileak value reduced to 0.8 uA



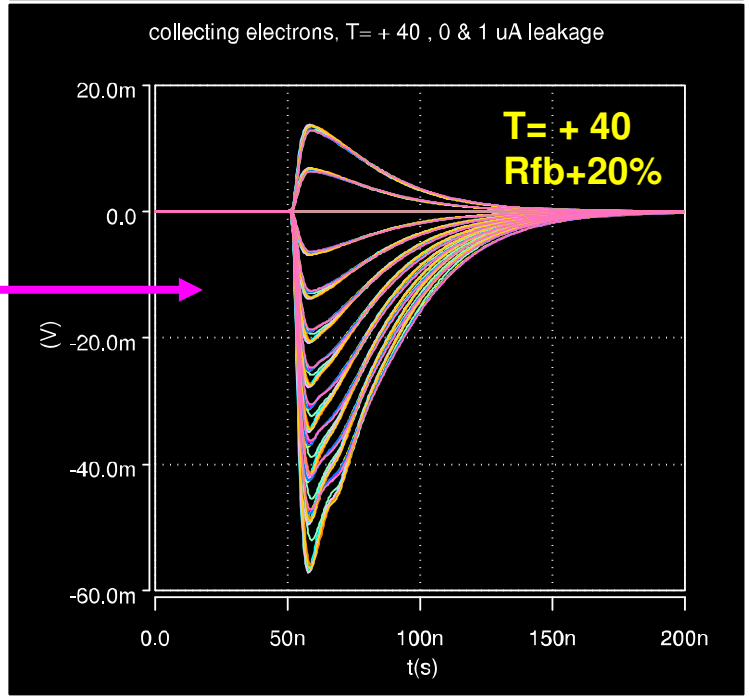
preamp for p-in-n (collecting holes)

Csensor = 2 pF
IDS = 65 μA



FF and FS and TT Ileak values reduced

this case least tolerant to Ileak

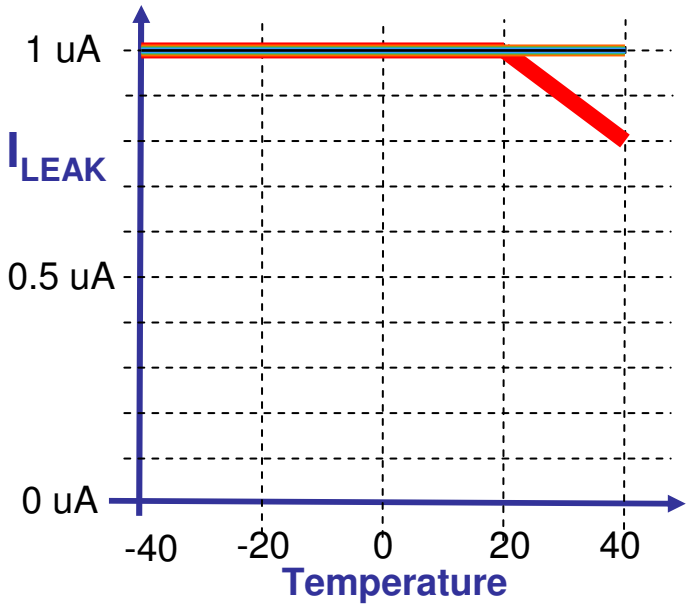


Csensor = 10 pF
IDS = 195 µA

Csensor = 2 pF
IDS = 65 µA

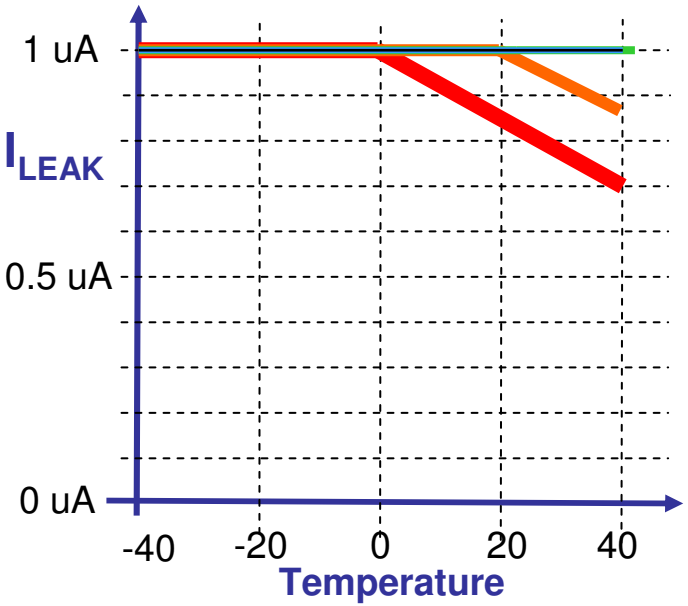
NO RESTRICTIONS

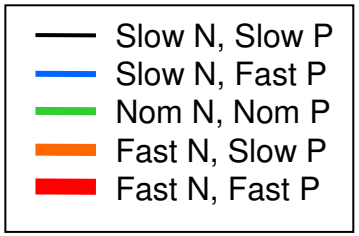
← Rfb -20% →

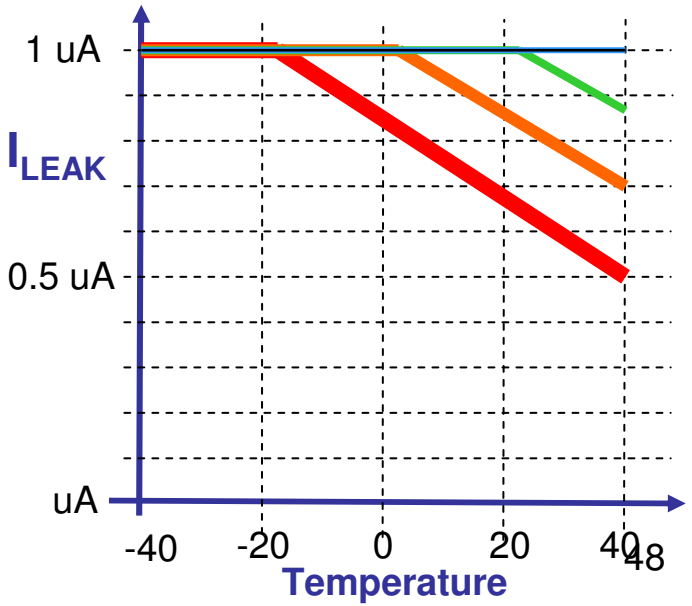


plots show that in some cases, for higher temperatures, the tolerable DC leakage current is less than 1 µA.
***But** 1 µA can be tolerated in all cases for temperatures below ~ -15 degrees. Note that the coincidence of worst case resistor tolerance, worst case process corner and worst case operating point choice is unlikely.*

← Rfb +20% →







preamp performance for p-in-n (collecting holes)

conclusions

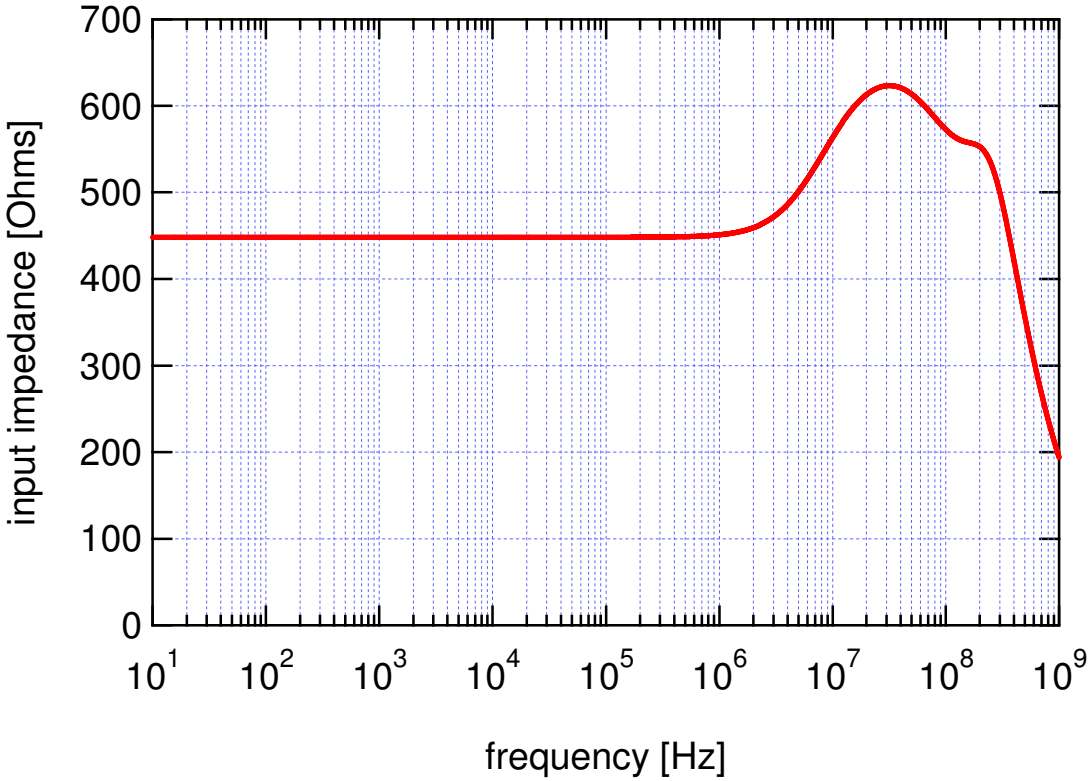
preamp design for p-in-n not quite as robust as n-in-p:

maximum spec. leakage current value cannot be tolerated under all conditions
but can be at low operating temperature

T resistor network simple to implement (and preferable to previous off-chip resistor solution)

small extra noise contribution negligible (will show later)

typical preamp input impedance

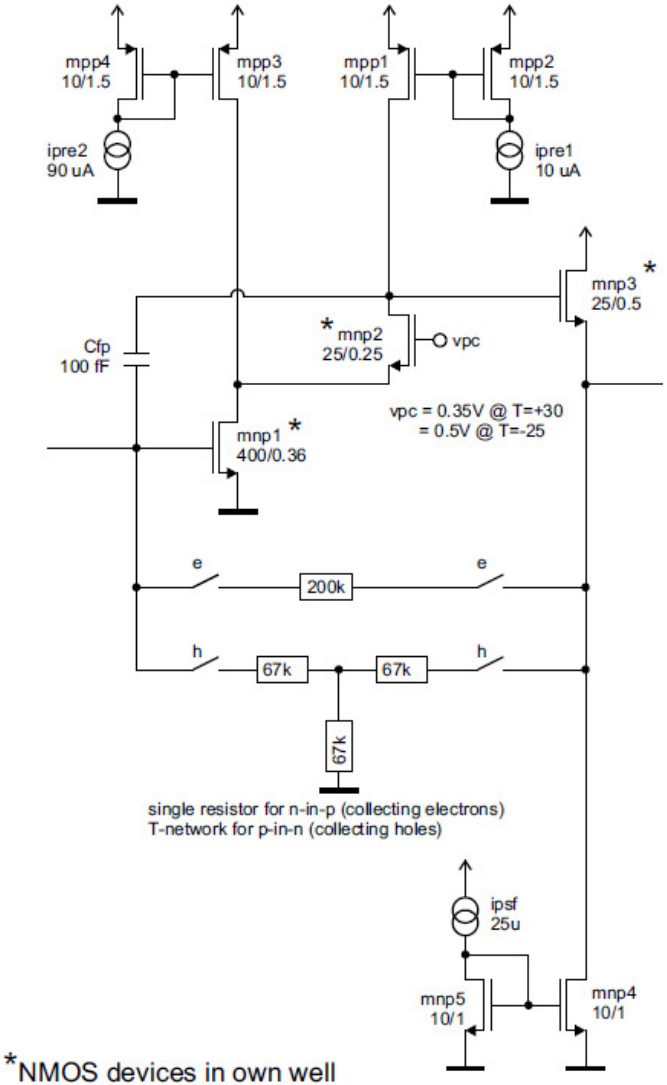


~ 450 Ω up to ~ 10^6 Hz

200k / OL preamp gain (~440)

higher frequency behaviour due to interplay of OL gain roll-off and effect of Cf

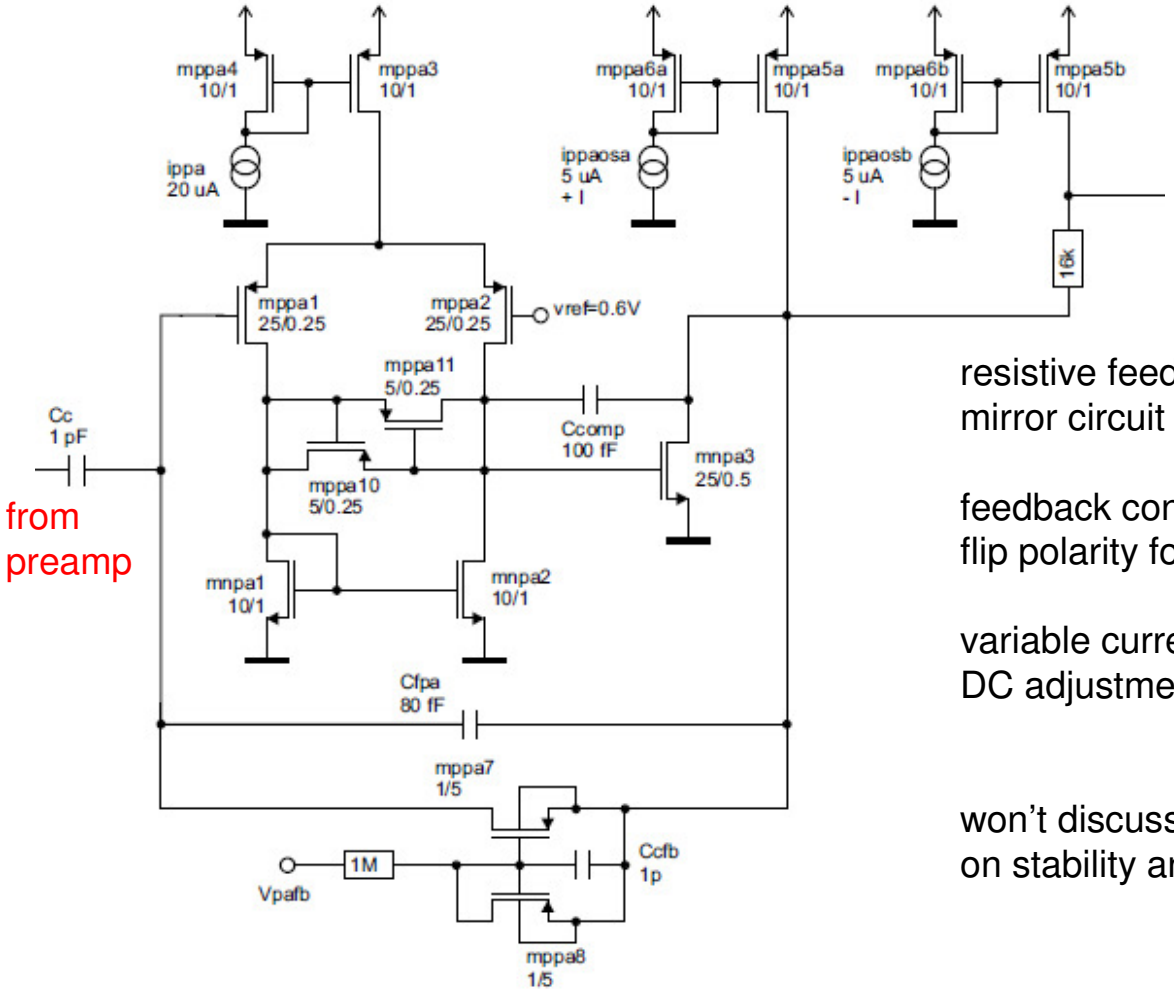
preamp conclusions



performance extensively simulated for wide range of operating conditions

appears robust and meets specs at target operating conditions (with a few minor provisions for higher temps)

postamp



AC coupled to preamp

dominant pole compensated opamp

inverting configuration
voltage gain Cc / Cfpa

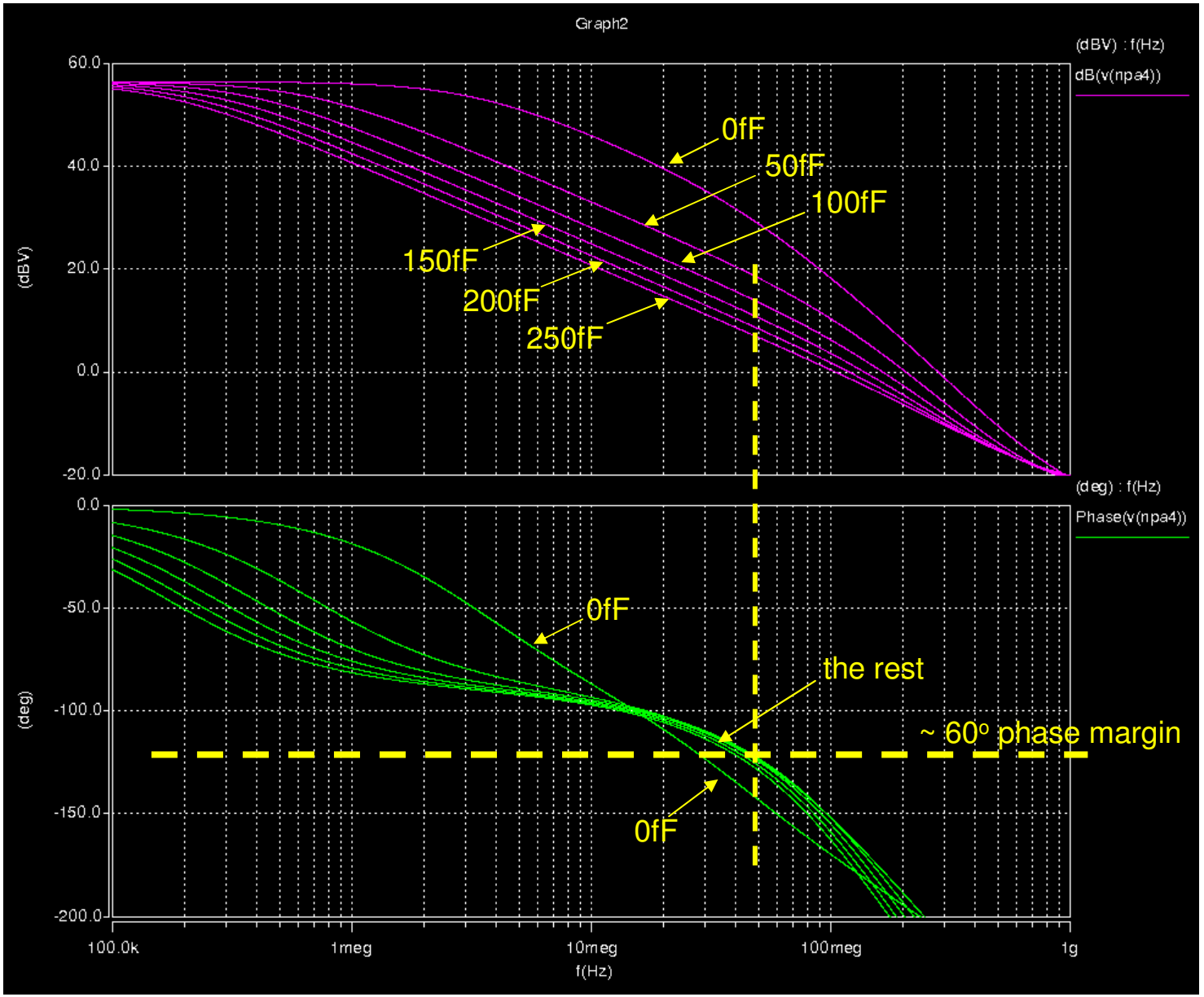
resistive feedback (v. high value) provided by current mirror circuit (more details to follow)

feedback config for p-in-n (holes) shown – have to flip polarity for n-in-p (some complications here)

variable current through 16k output resistor allows DC adjustment of level to comparator (fine tuning)

won't discuss opamp design in detail, but concentrate on stability and resistive feedback

postamp compensation



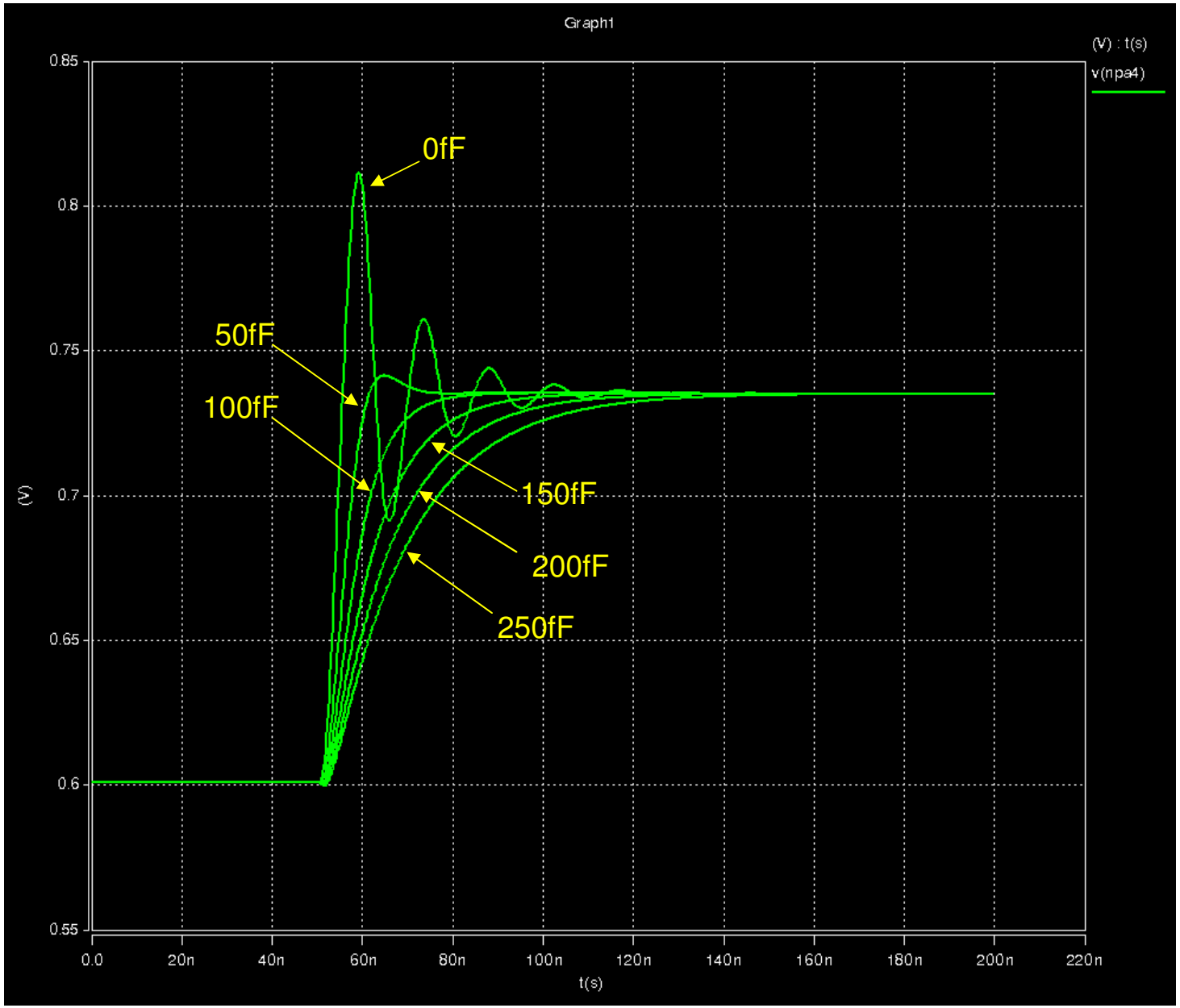
OL gain and phase vs. Ccomp

want gain of ~12 from postamp so need > 60° phase margin at ~ 20 dB for stability

plots show stable for gain > 20 dB with Ccomp > 50fF

choose Ccomp = 100 fF for greater margin

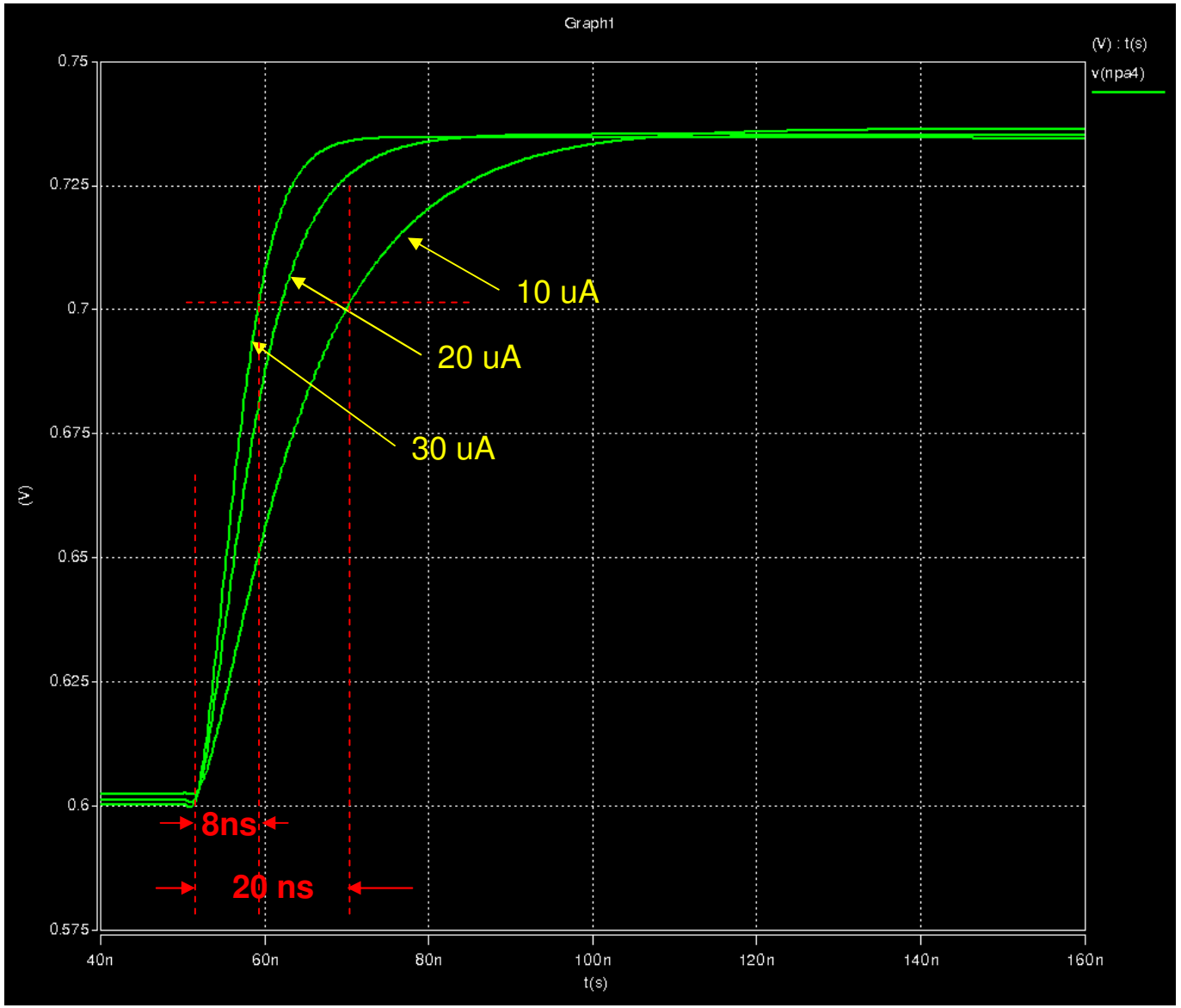
postamp compensation



transient closed loop (G = 12.5) step response vs. Ccomp shows expected behaviour

well-behaved for Ccomp = 100fF

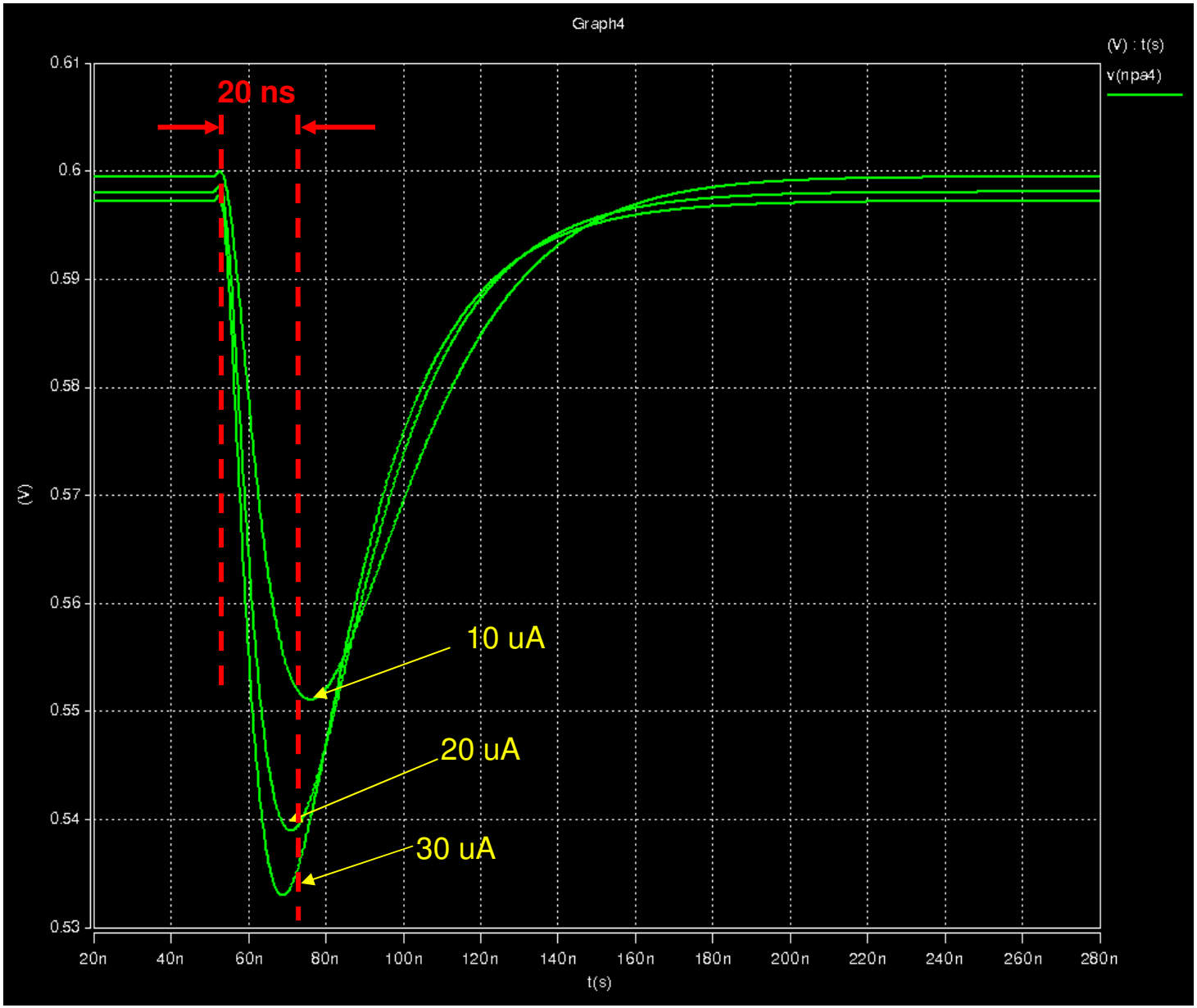
postamp tuning



can use diff. pair tail current to tune frequency response

10 - 30 uA gives rise time constant 8 – 20 us

postamp tuning

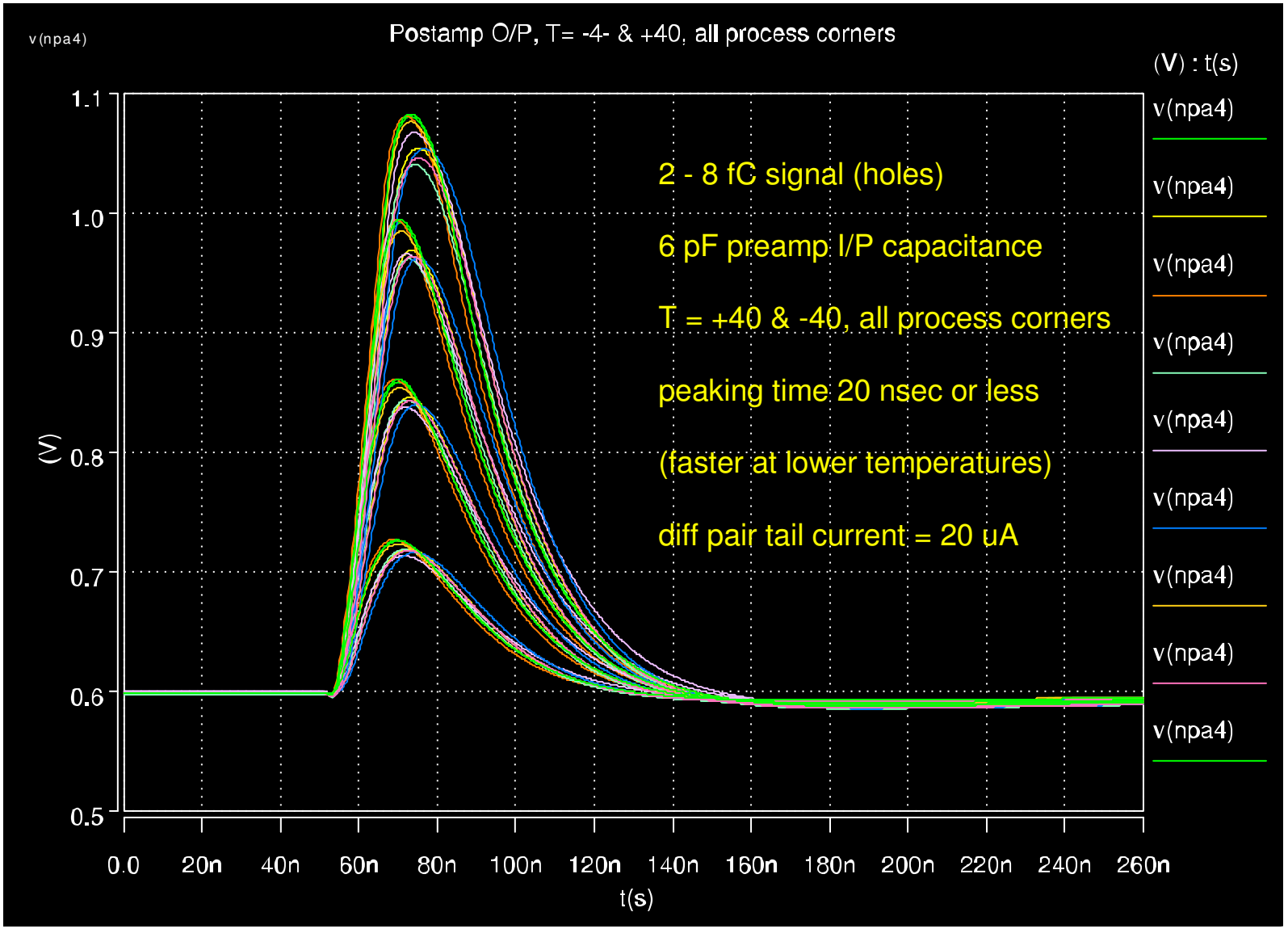


can use diff. pair tail current to achieve some pulse shape tuning

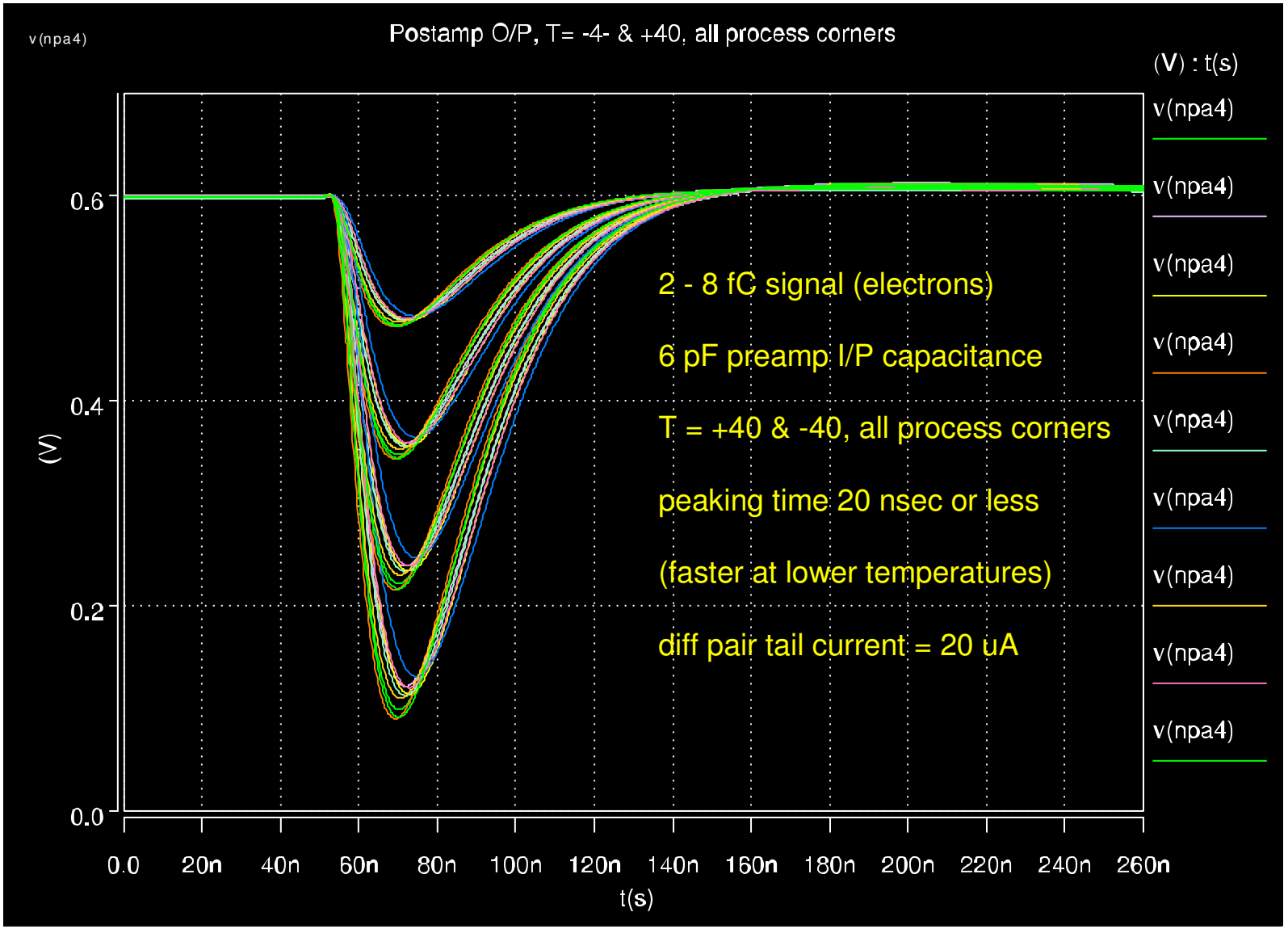
20 uA gives overall (preamp+postamp) peaking time of 20 nsec

choose this for nominal value

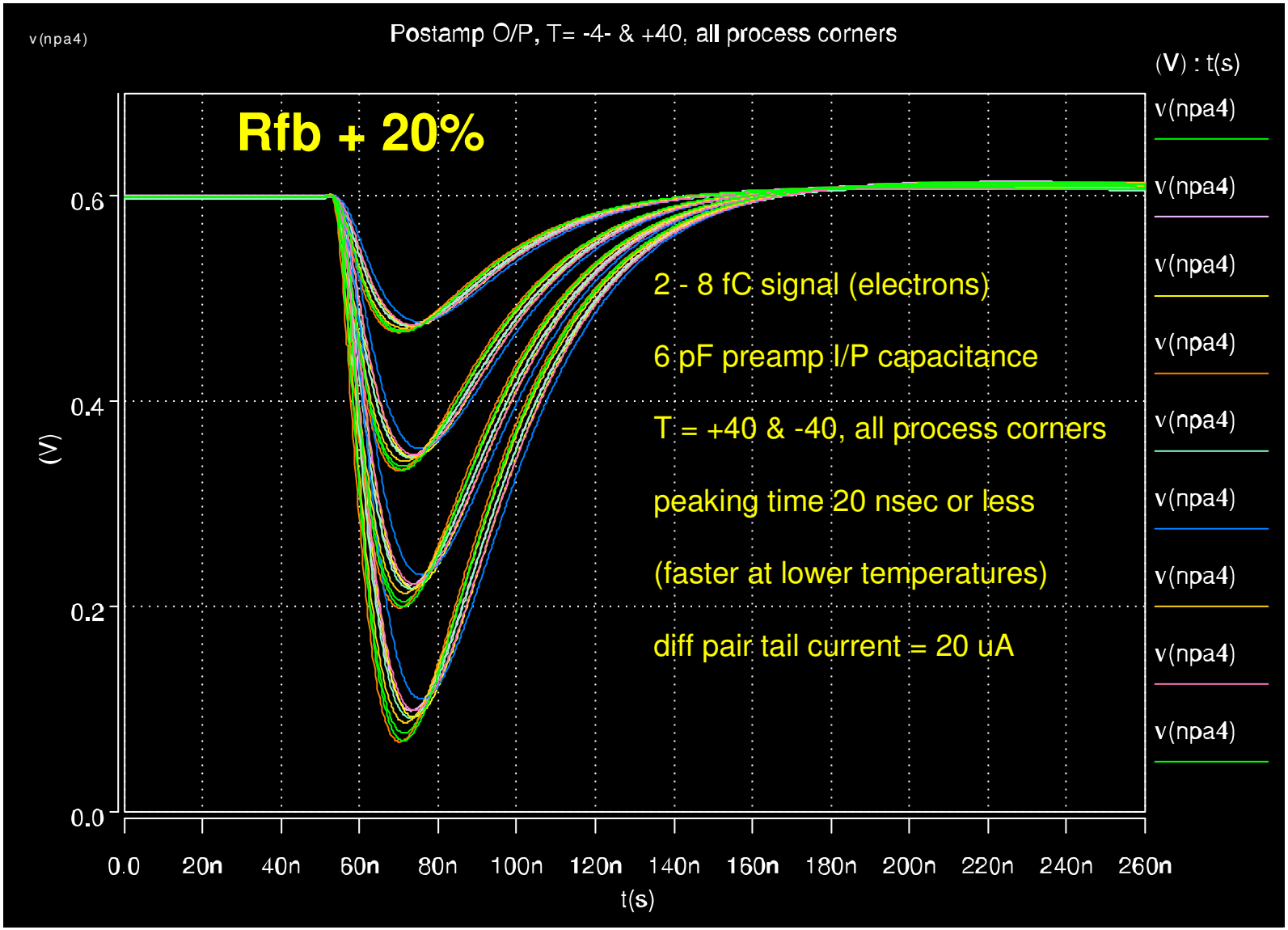
postamp pulse shape (holes)



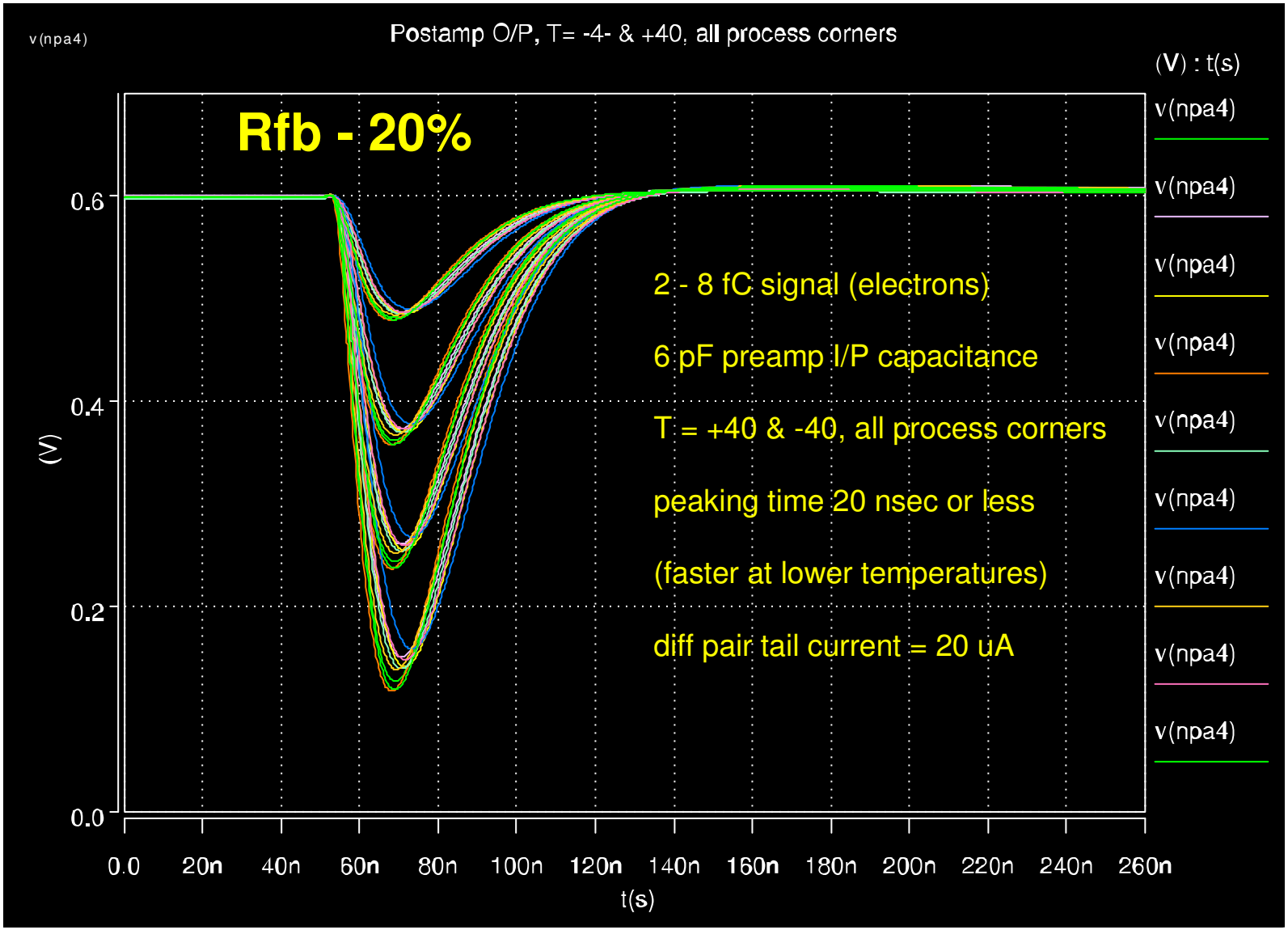
postamp pulse shape (electrons)



postamp pulse shape (electrons)

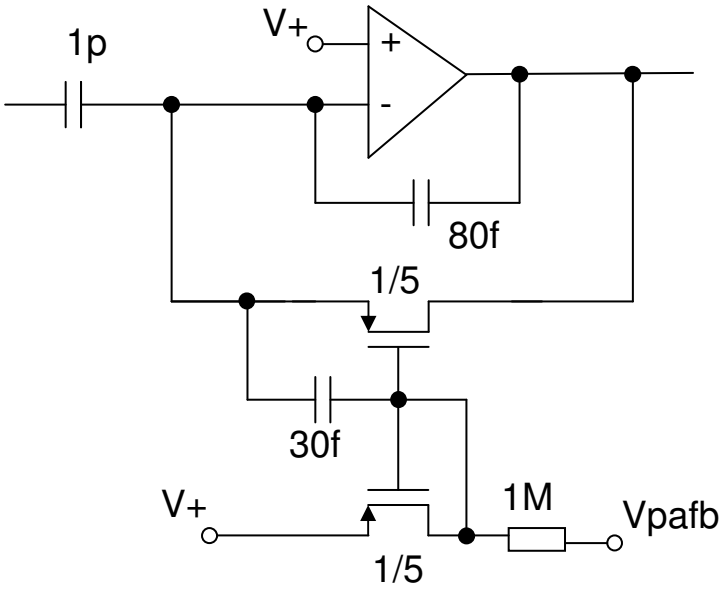


postamp pulse shape (electrons)

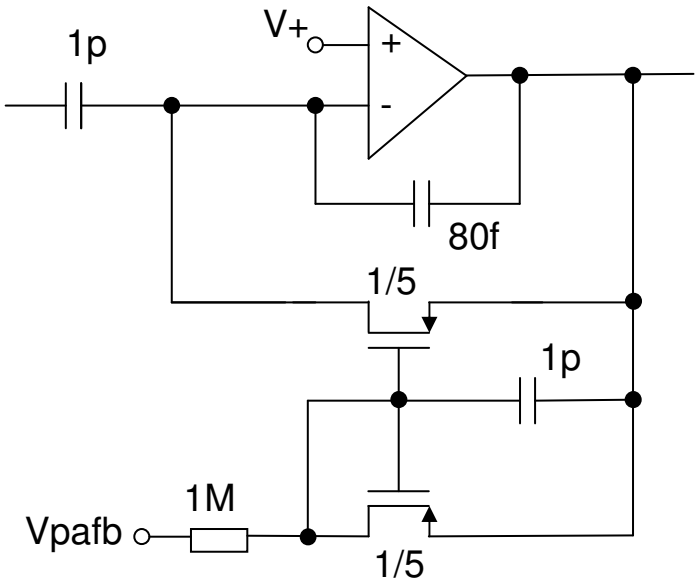


postamp feedback

electrons

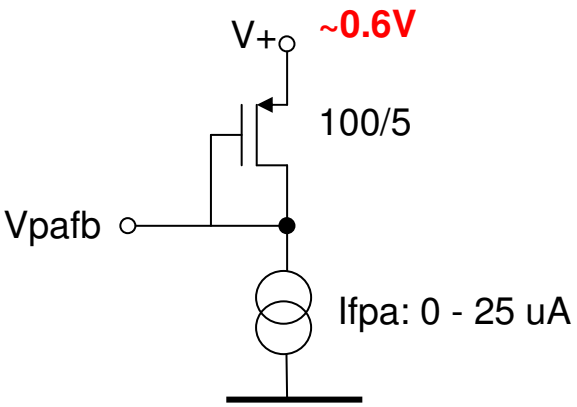


holes

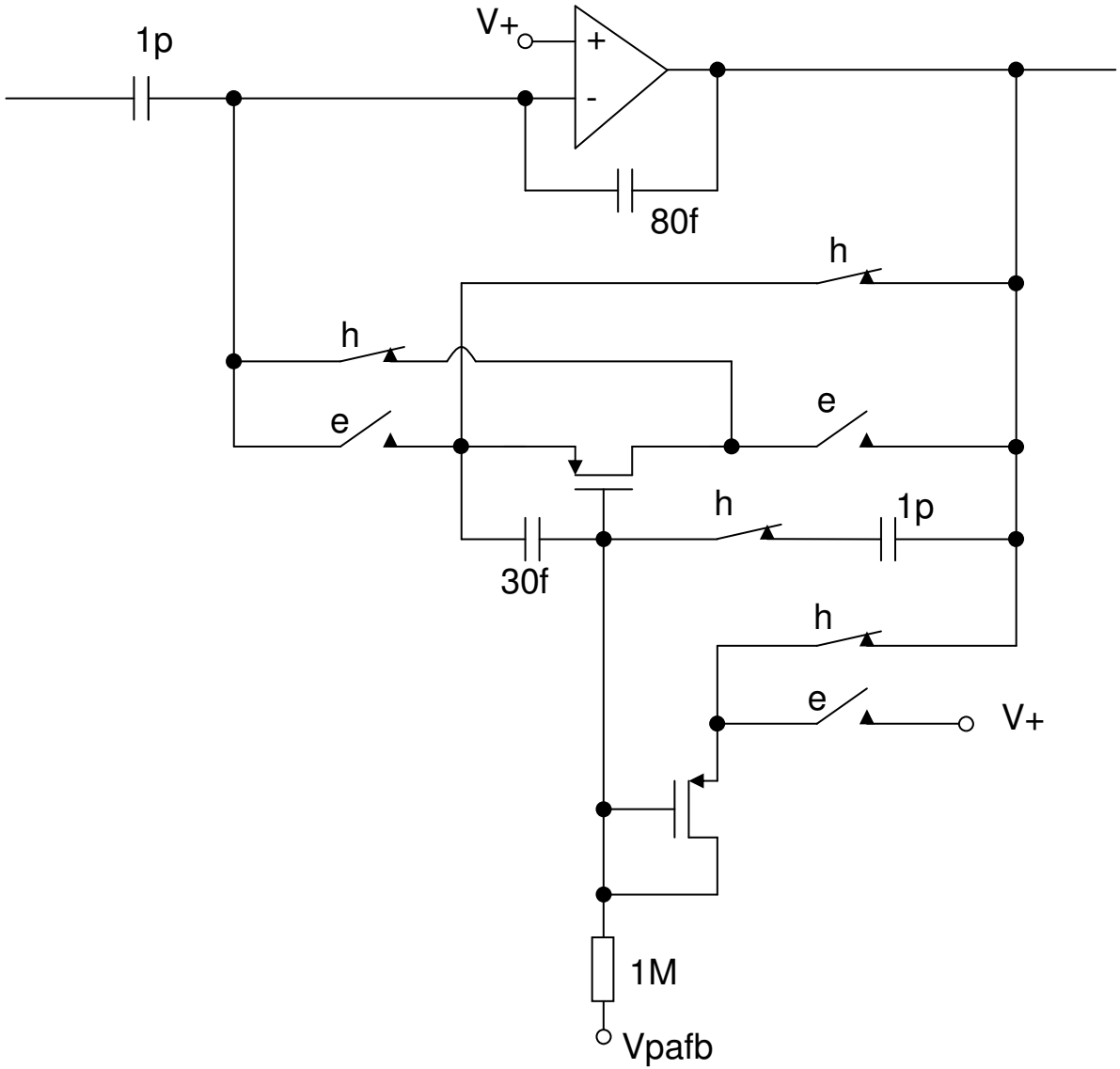


similar for both polarities, but some important differences in how the mirroring works

Vpafb derived from current into drain-source coupled device gives process independence

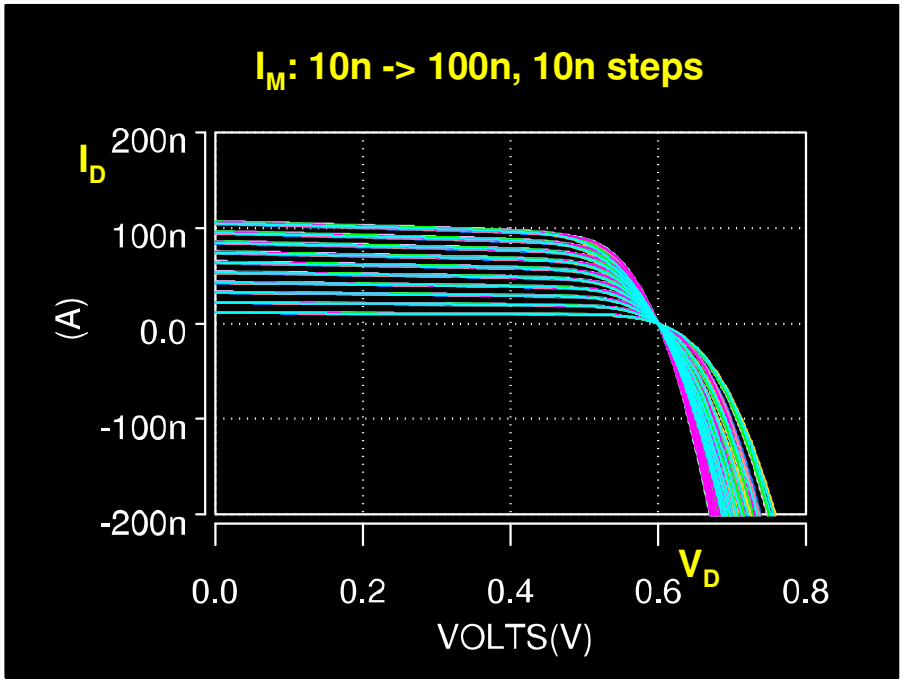


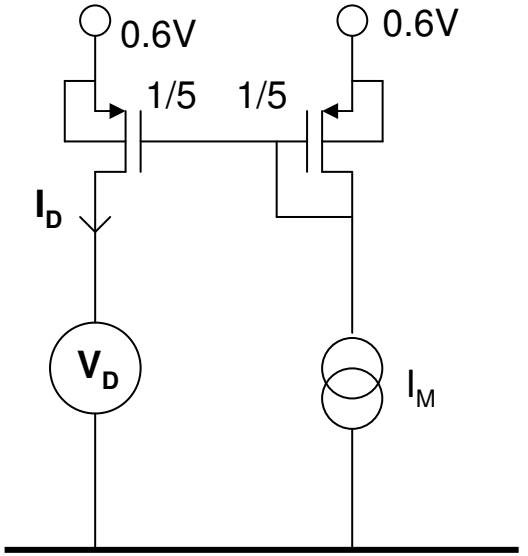
postamp feedback

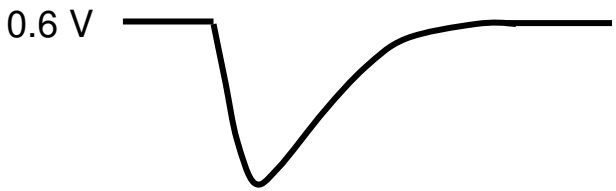


can implement with switches

postamp feedback



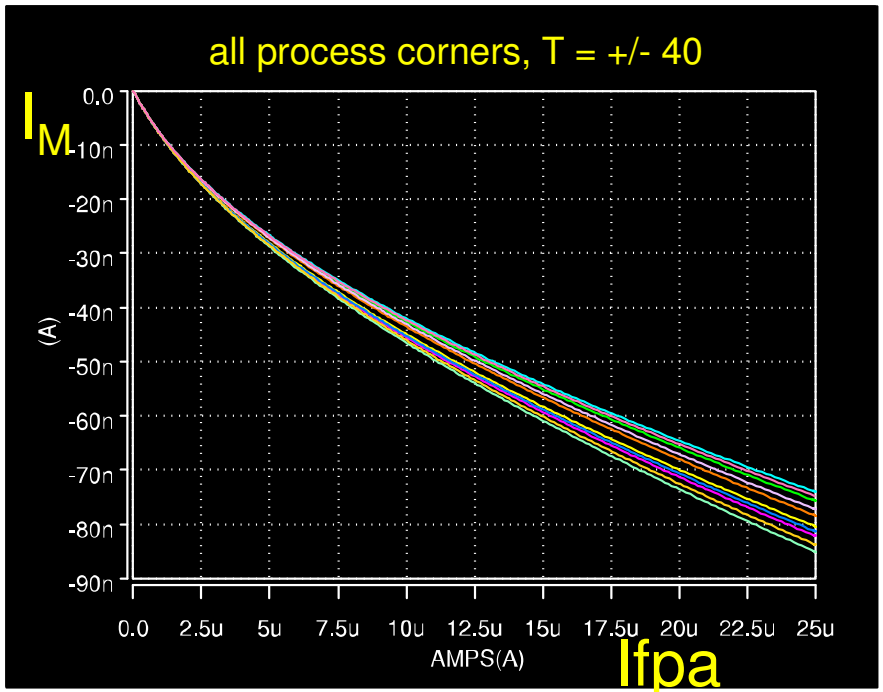


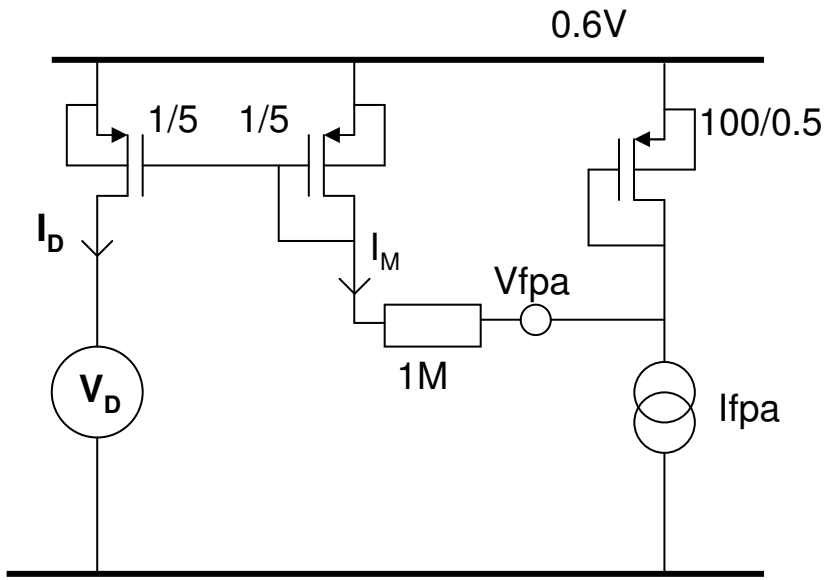


e.g. for electrons get negative going pulse at postamp output

v.high resistance for $V_D < 0.6$

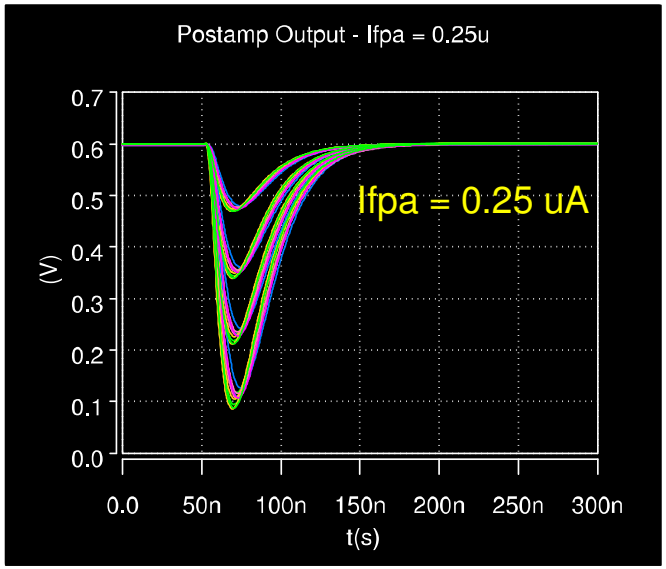
postamp feedback – how to bias

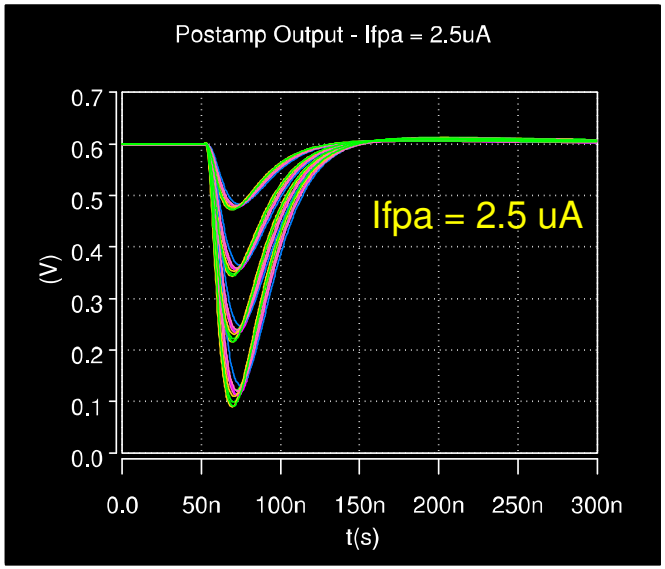


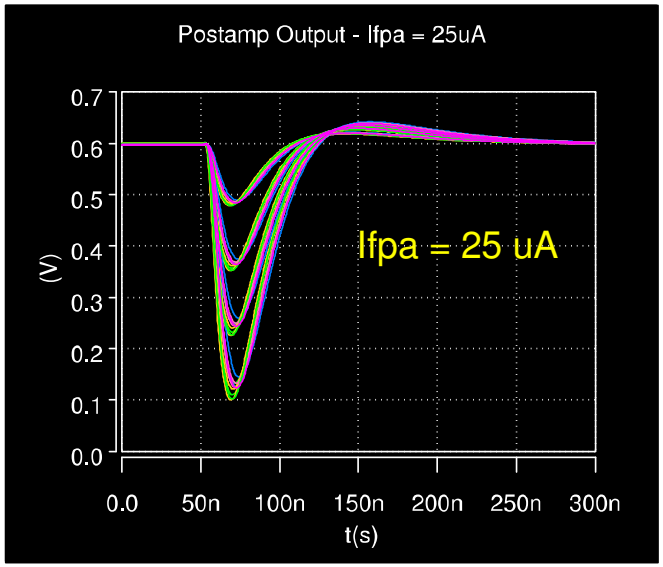


want I_M ~ 10 to few 10's nA
bias circuit shown compensates well for temperature and process
Ifpa range 0 -> 25.5 uA, 8 bit precision

postamp feedback – for electrons







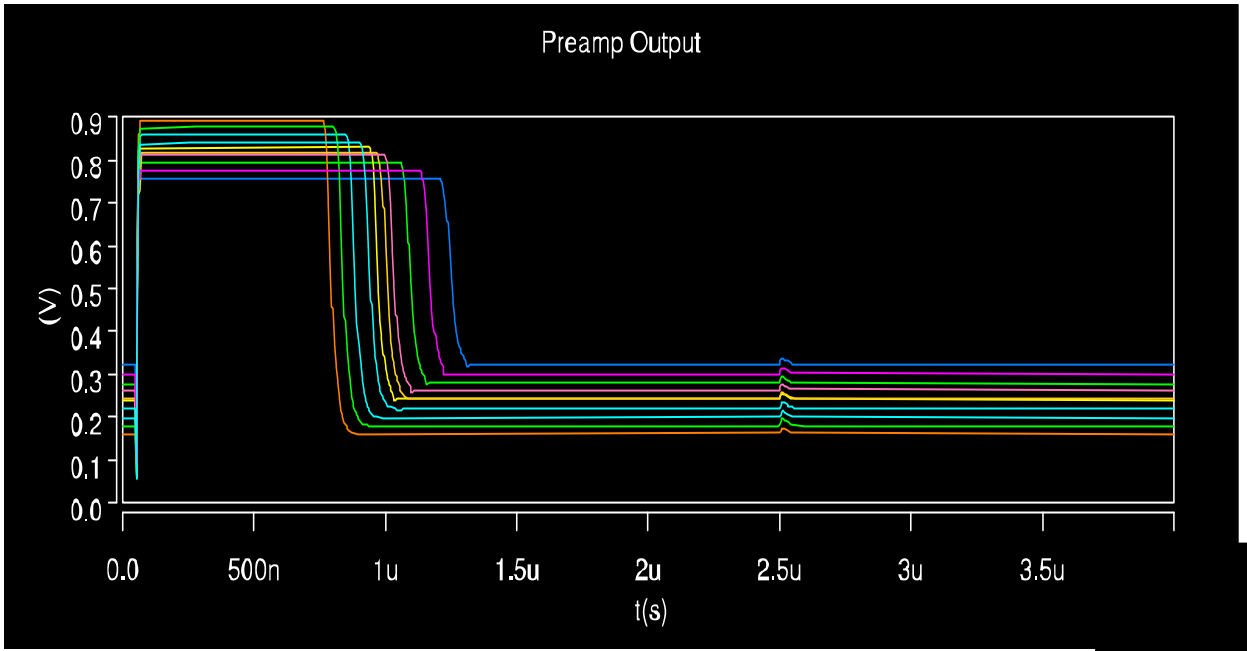
Effect of Ifpa

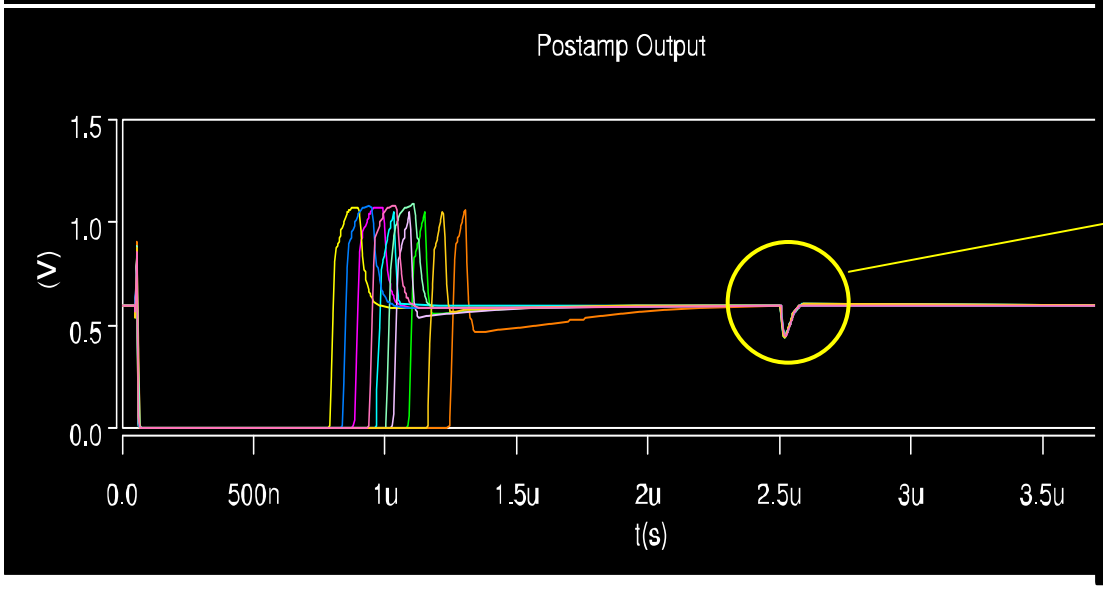
Ifpa = 0.25uA, 2.5uA and 25uA, T = - 40 & +40
preamp Cin = 6 pF, all process corners
signal injected = 2 -> 8 fC (2 fC steps)

increasing Ifpa gives noticeable overshoot

expect to operate with Ifpa small, but ability
to run with higher current (=> lower feedback R)
allows to compensate for “unexpected effects”

overload recovery – for electrons

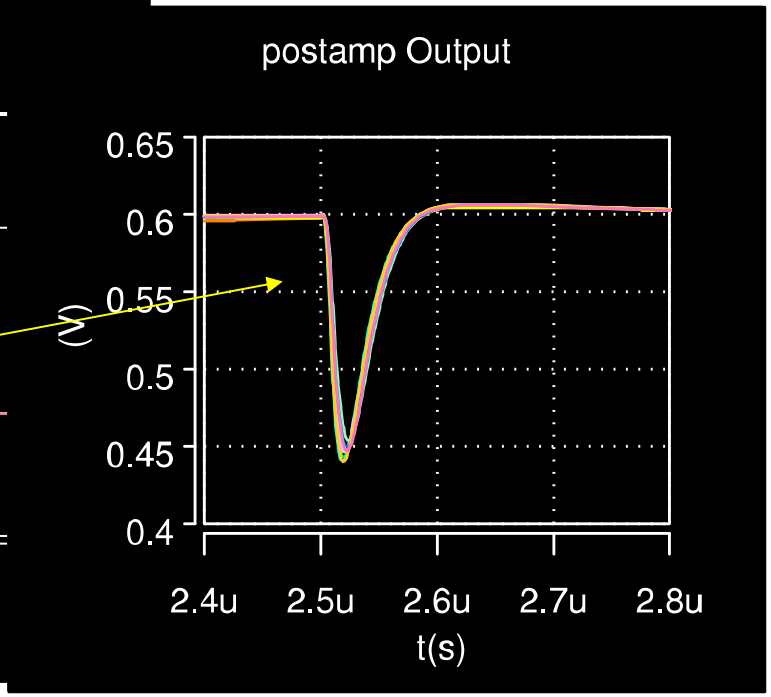




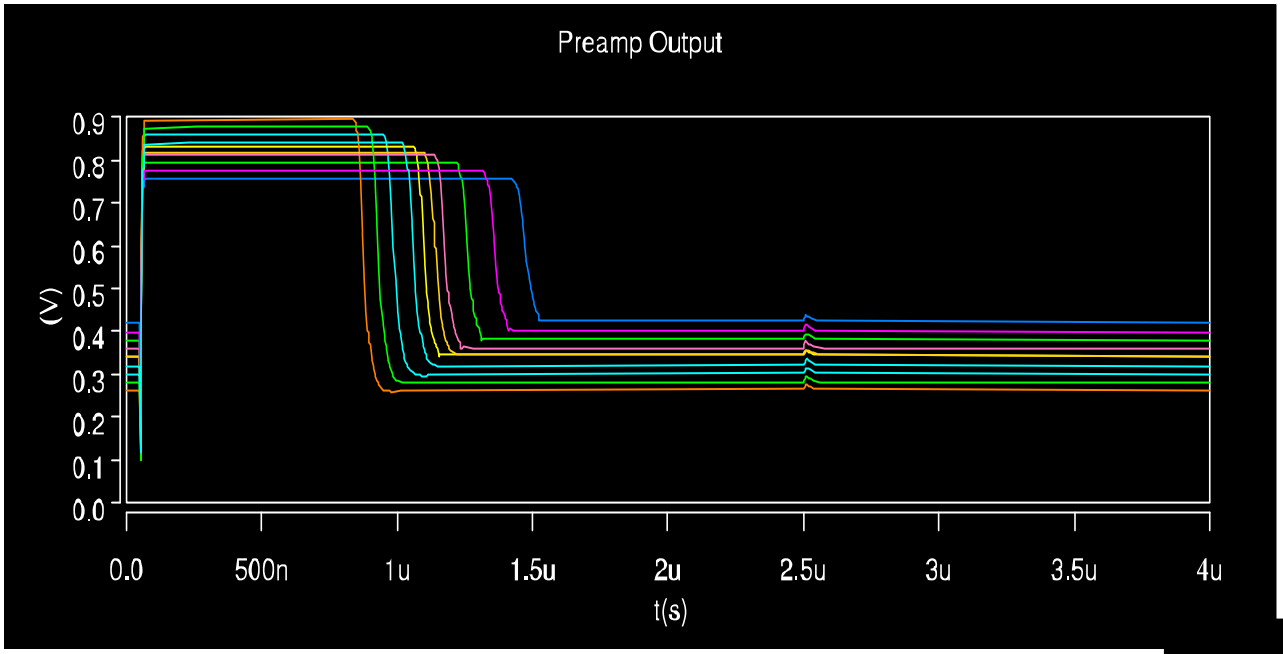
T = - 40 & +40
Ileak = 0
preamp Cin = 6 pF
all process corners
Ifpa = 2.5uA

4 pC injected at t = 50 ns
2.5 fC injected at t = 2.5 us

recovery spec. comfortably met



overload recovery – for electrons



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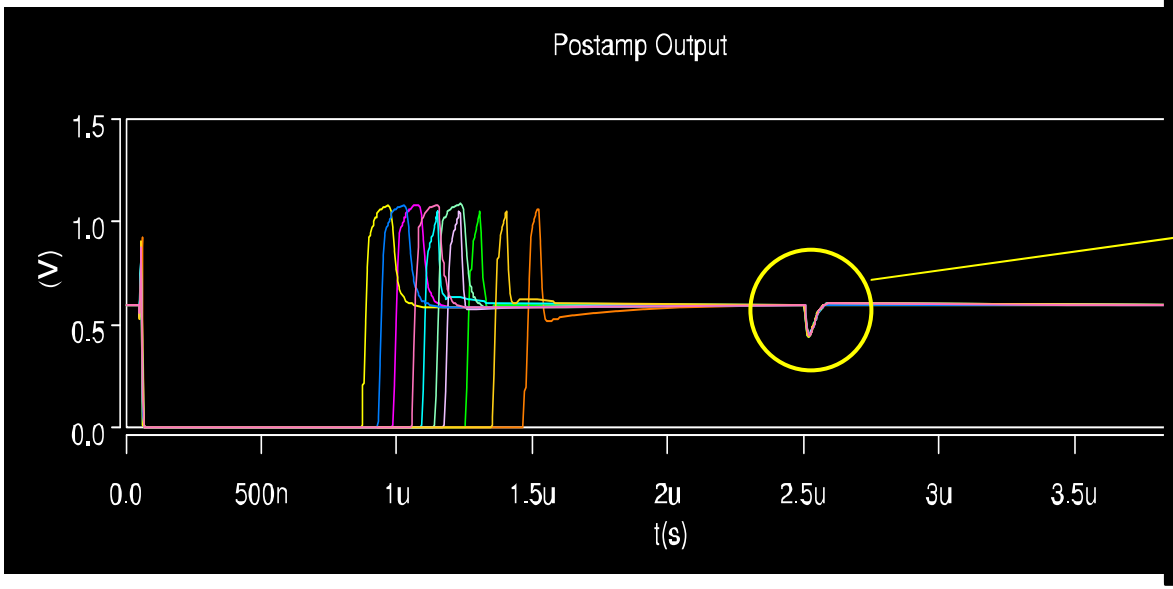
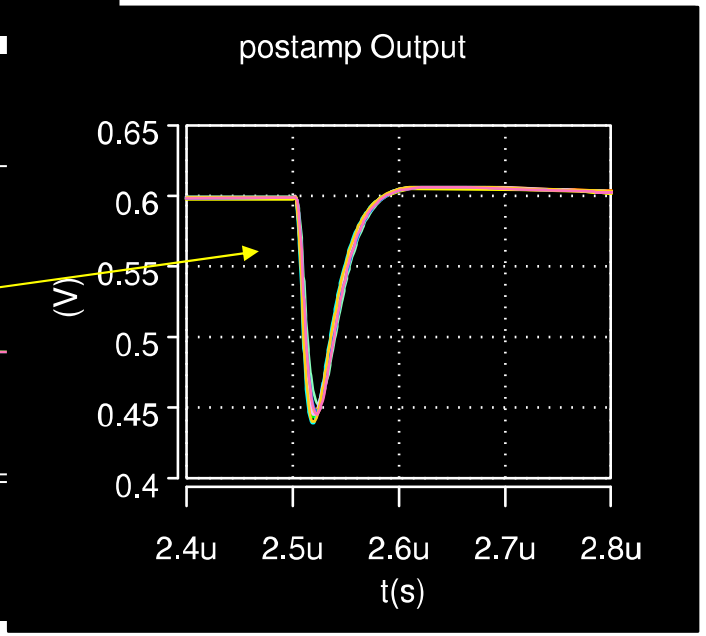
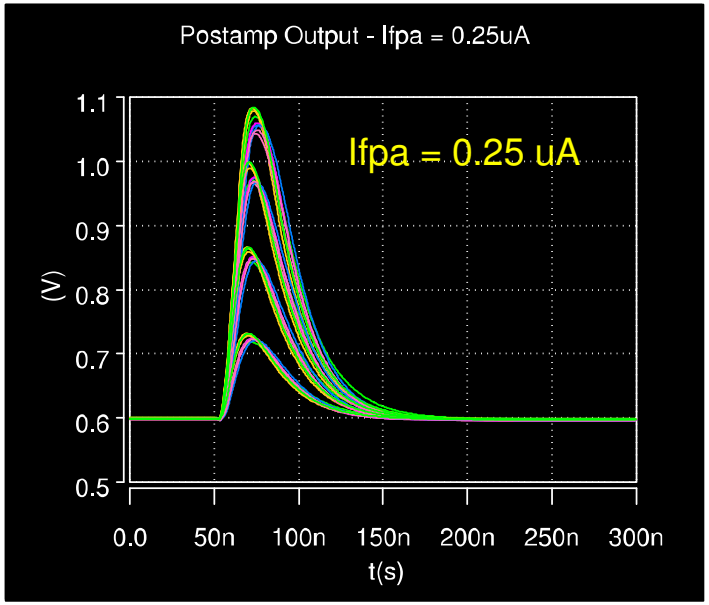
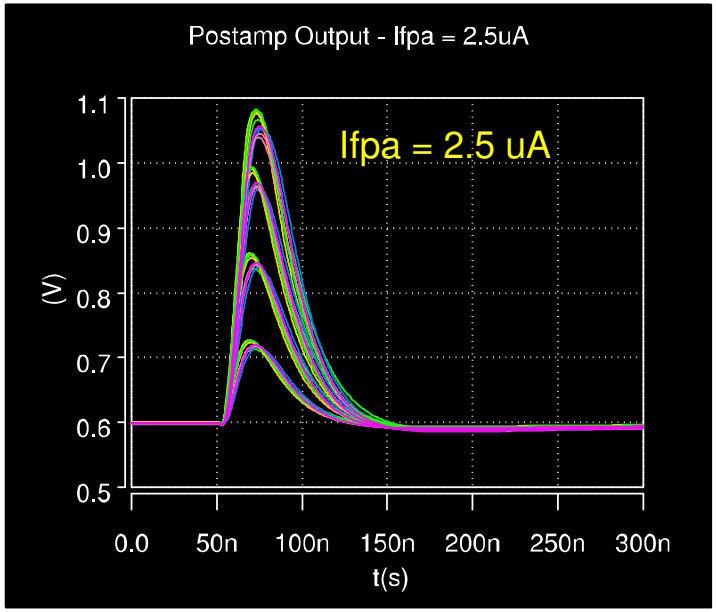
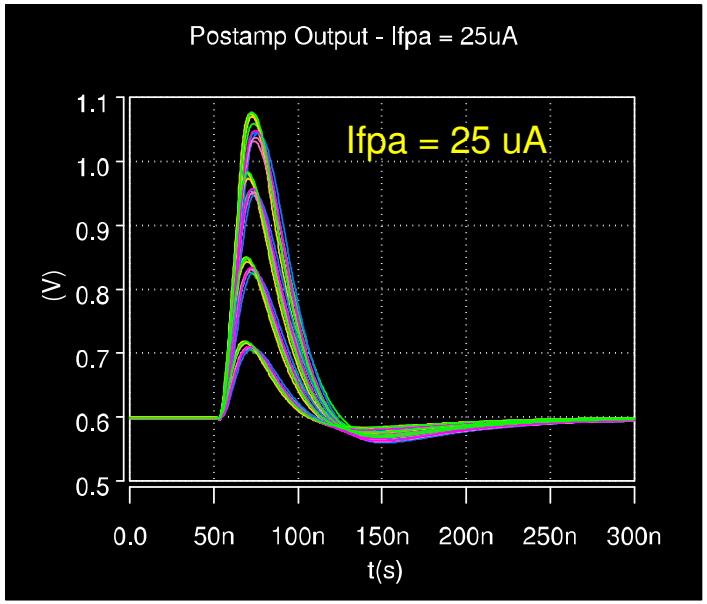




postamp feedback – for holes





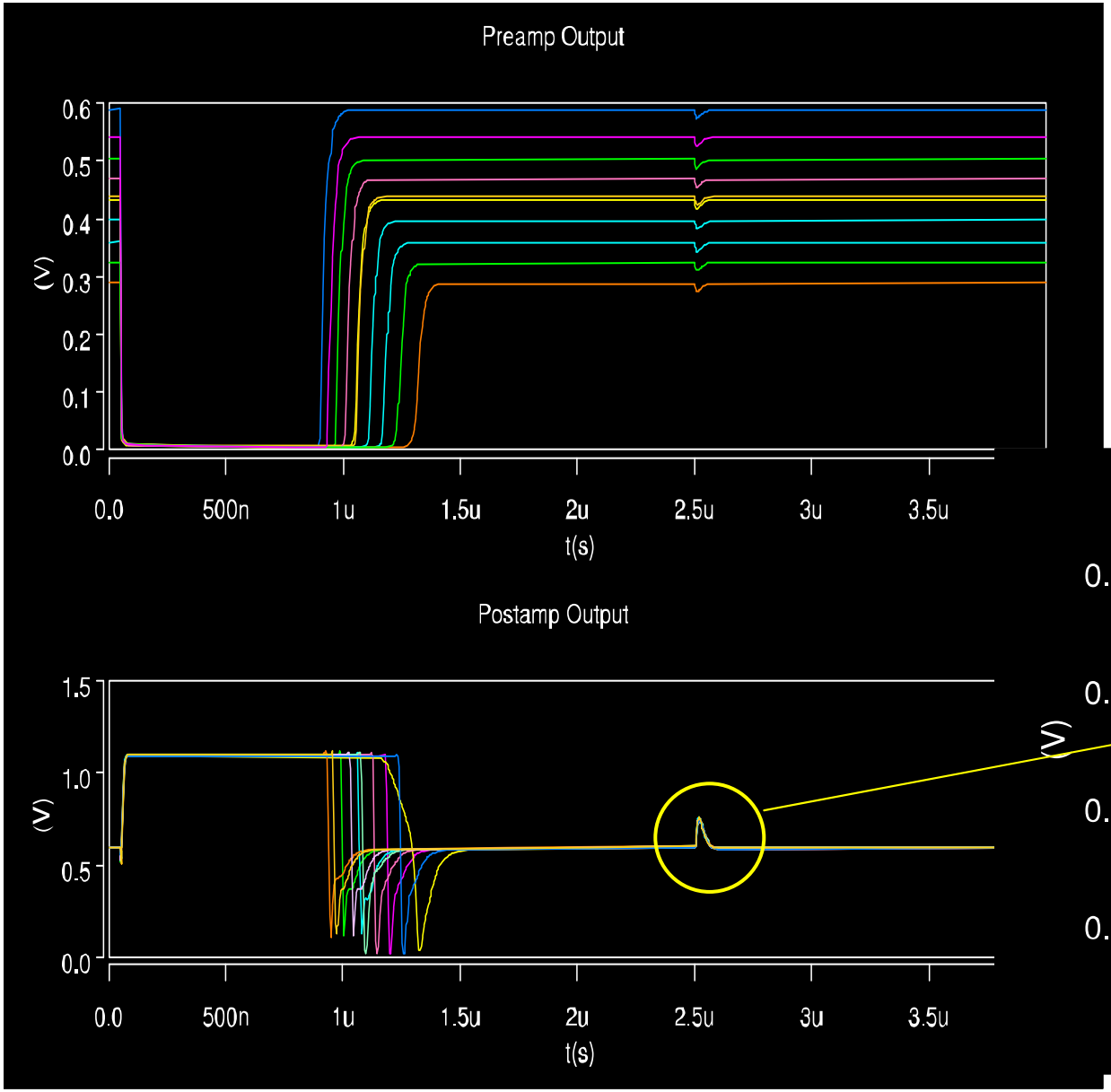


Effect of Ifpa

Ifpa = 0.25uA, 2.5uA and 25uA, T = - 40 & +40
preamp Cin = 6 pF, all process corners
signal injected = 2 -> 8 fC (2 fC steps)

similar effects to electrons case

overload recovery – for holes



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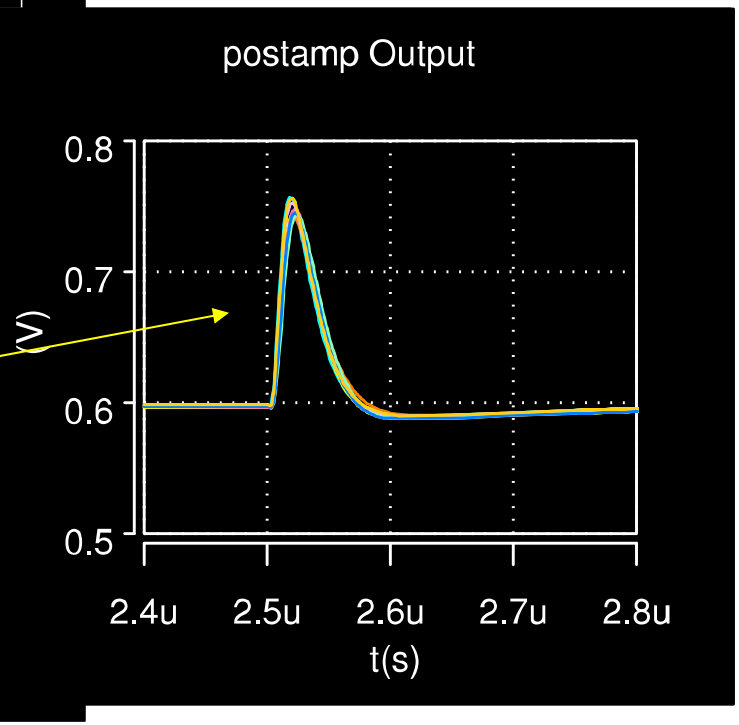
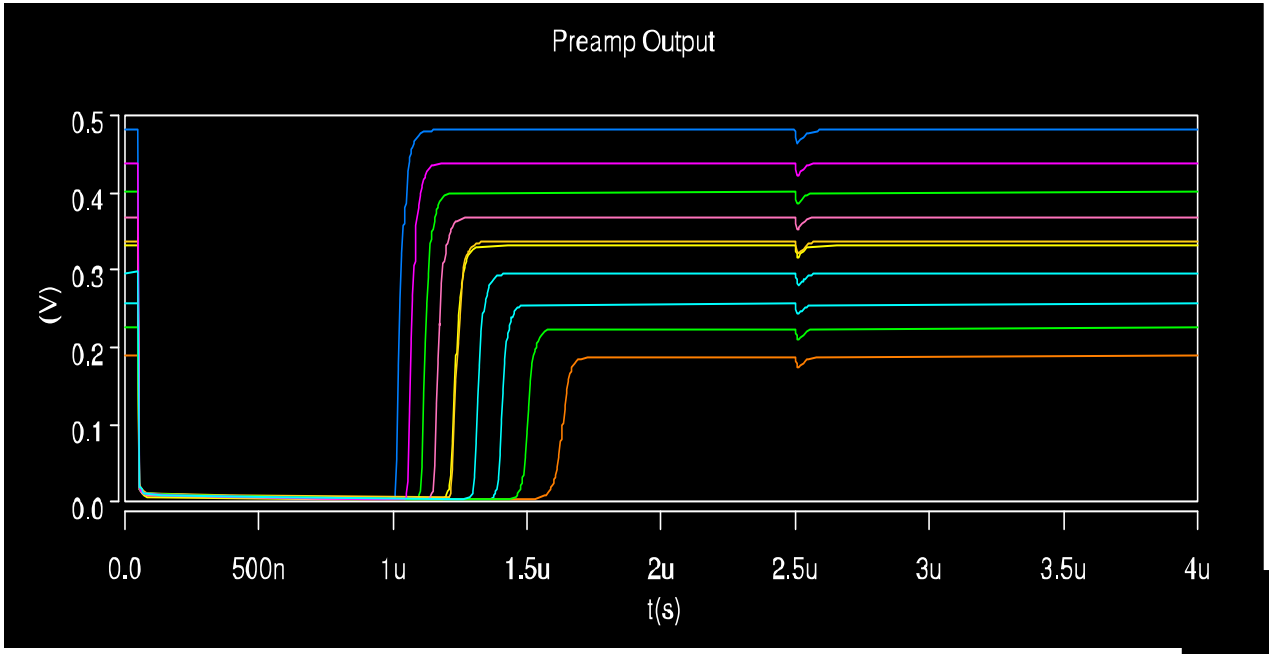
recovery spec. comfortably met



overload recovery – for holes



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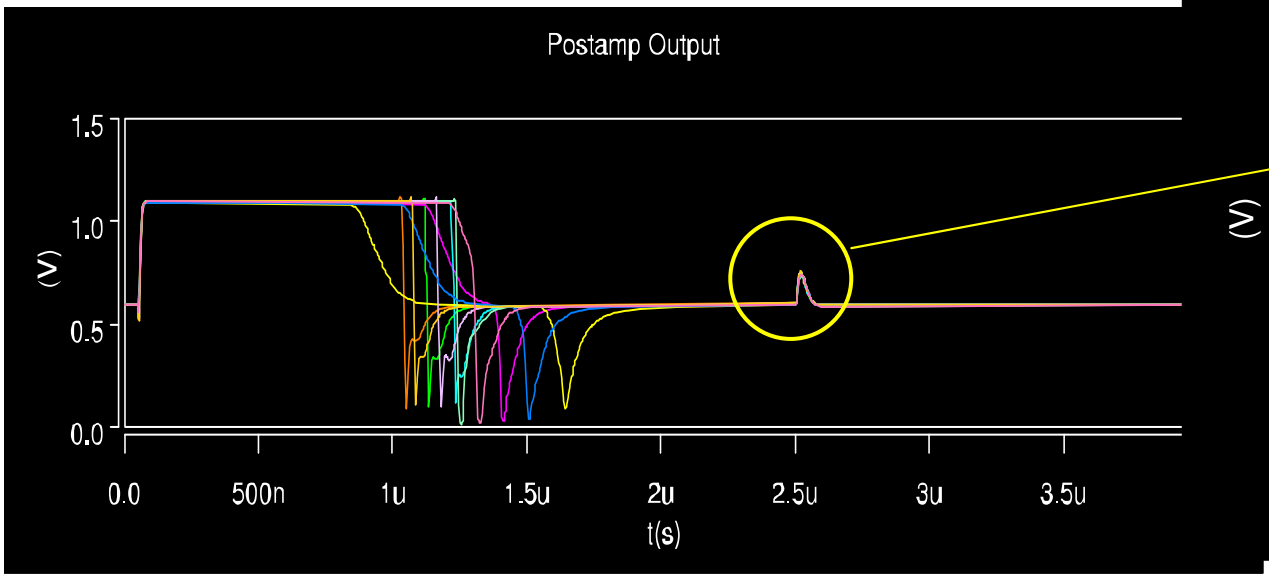
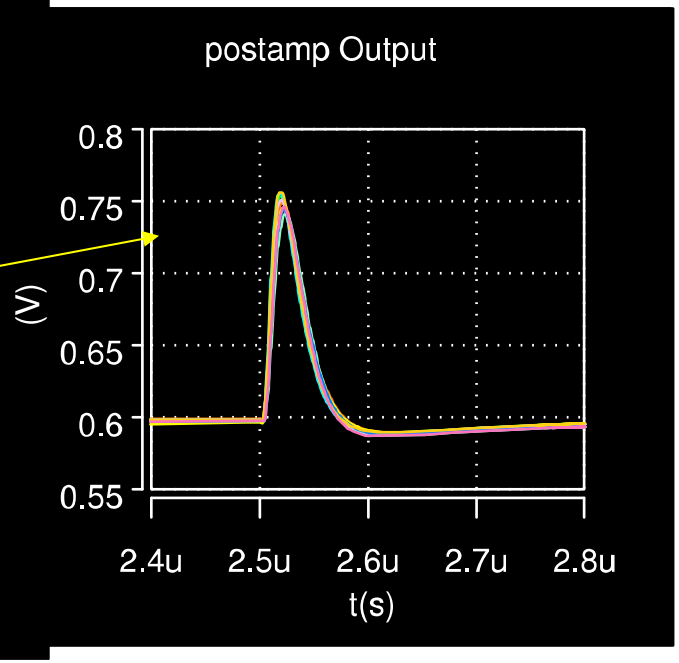
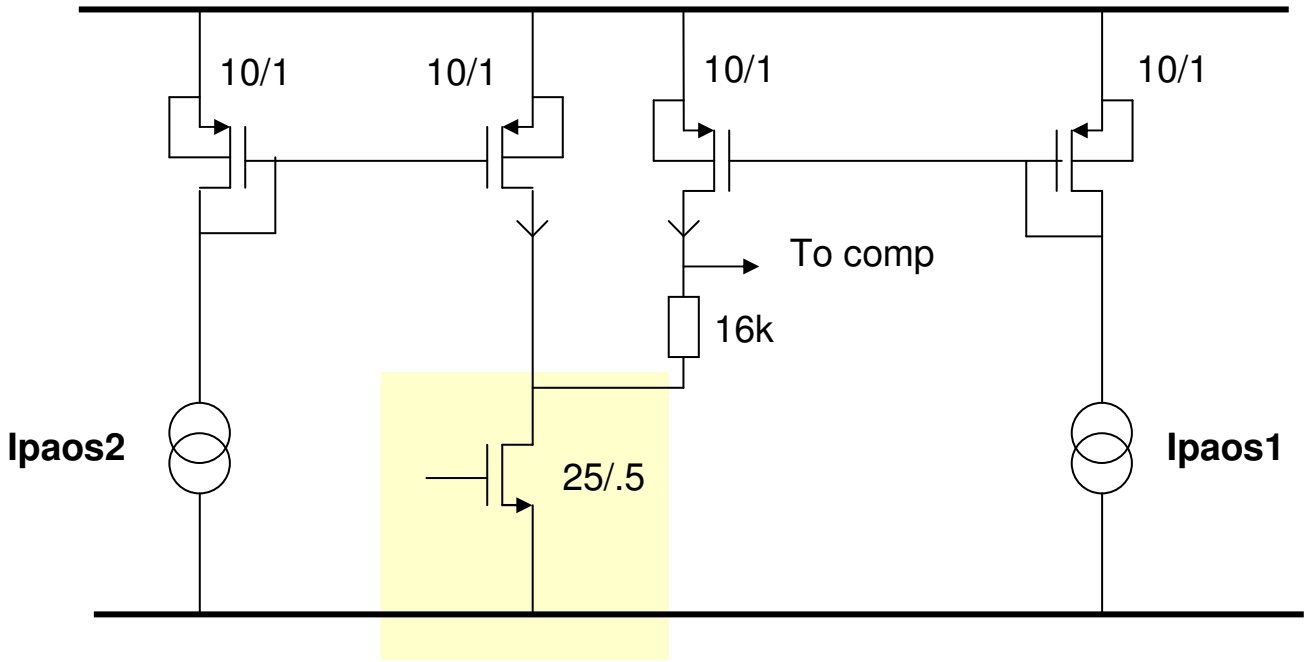




Postamp O/P level shift



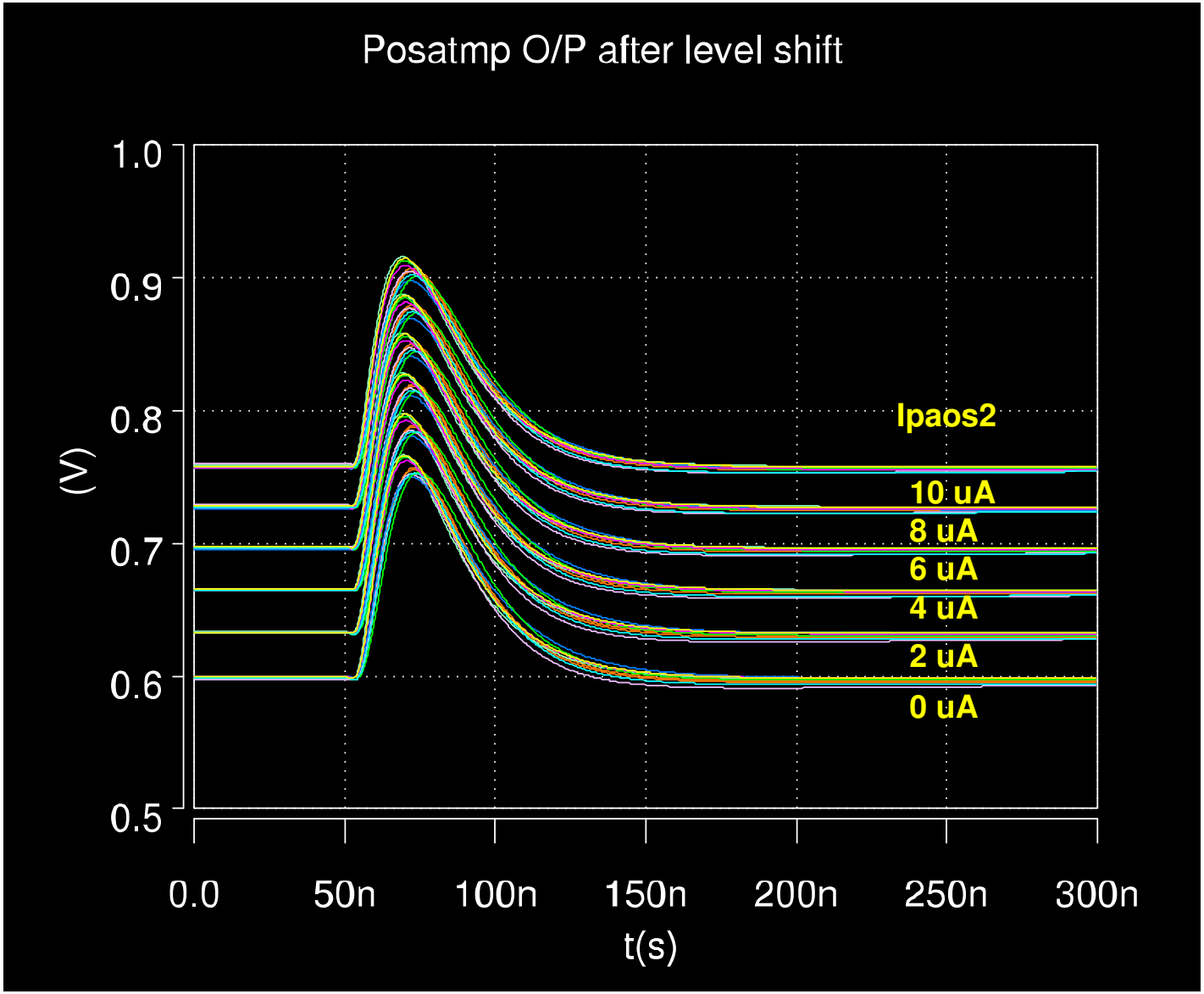
5 bit trim gives 5 mV res'n
I am thinking that now we perhaps should have more - is 6 bits possible?

Lawrence's idea for trimming comparator threshold
=> don't trim comp. threshold but trim DC level at postamp output

Ipaos1 produces DC shift across 16k (up to 10 uA -> 160 mV)

Tune Ipaos1 for desired trim value, but keep Ipaos1 + Ipaos2 constant
= total required current in Postamp O/P device = 10 uA

Postamp O/P level shift



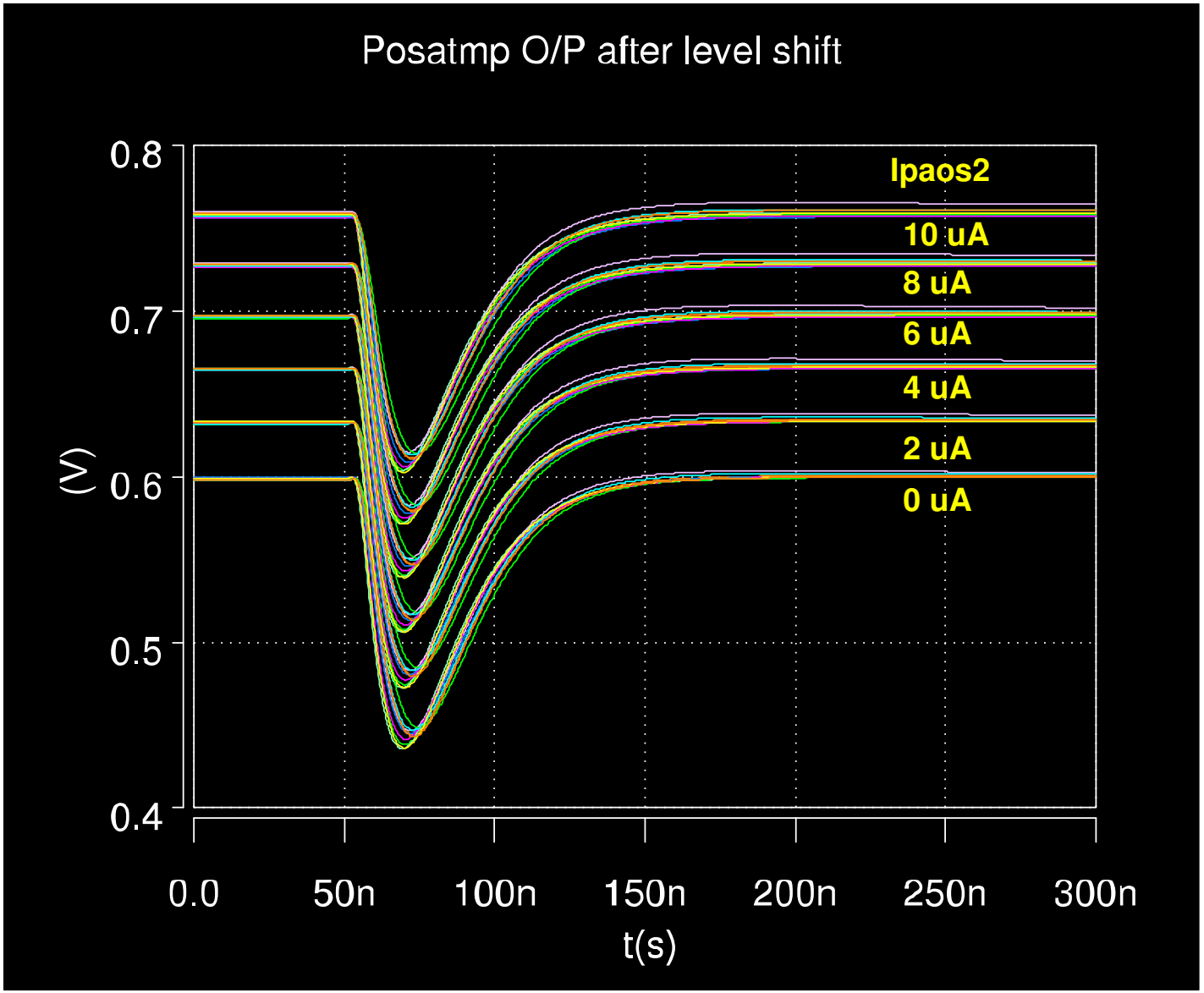
Ipaos1 + Ipaos2 = 10 uA

all process corners

T = +40 & -40

collecting **holes**

Postamp O/P level shift



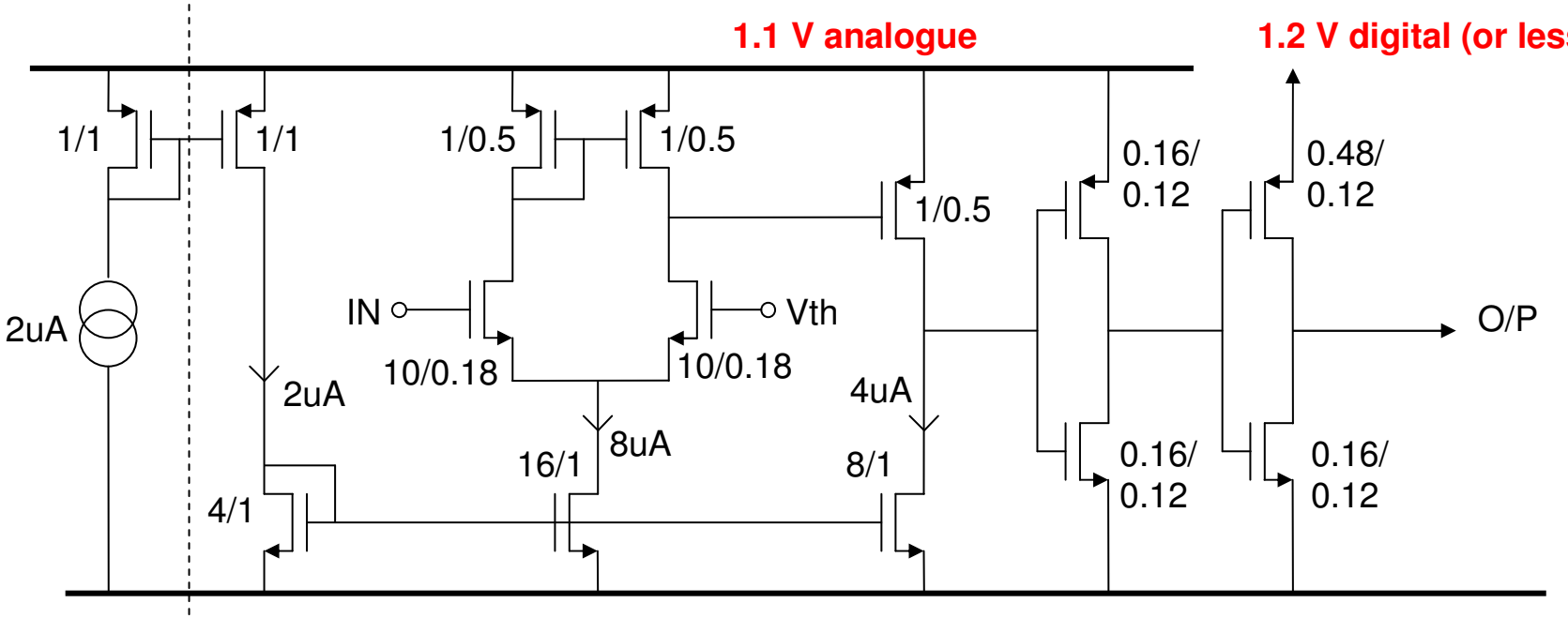
Ipaos1 + Ipaos2 = 10 uA

all process corners

T = +40 & -40

collecting **electrons**

comparator



Lawrence's design modified

all devices now normal (low VT PMOS doesn't seem necessary)
current mirror NMOS enclosed
nominal supply current 14 uA (17 uW from 1.2 V)

DC coupled to postamp output – Vth global (all channels)

postamp output DC offset implements individual channel trim

last inverter implements analogue -> digital supply rail transition

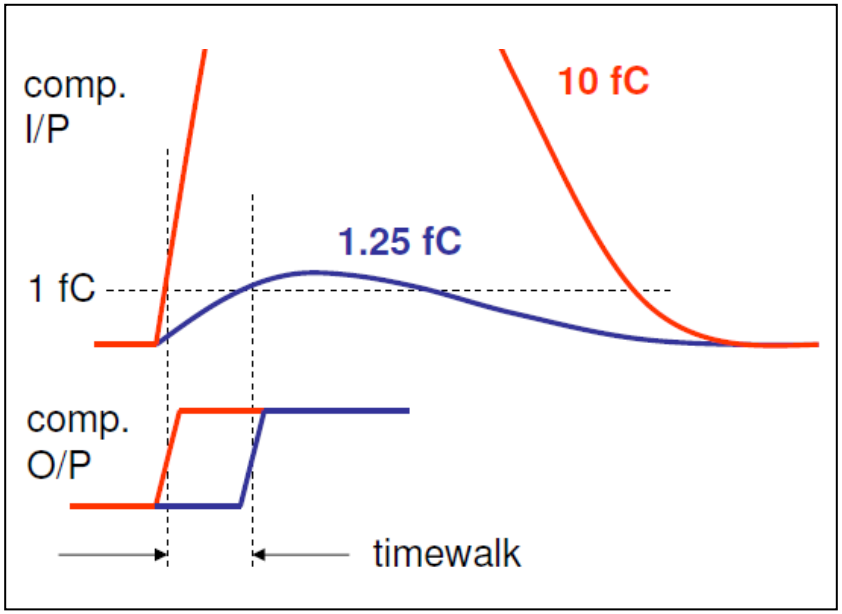
comparator timewalk specification

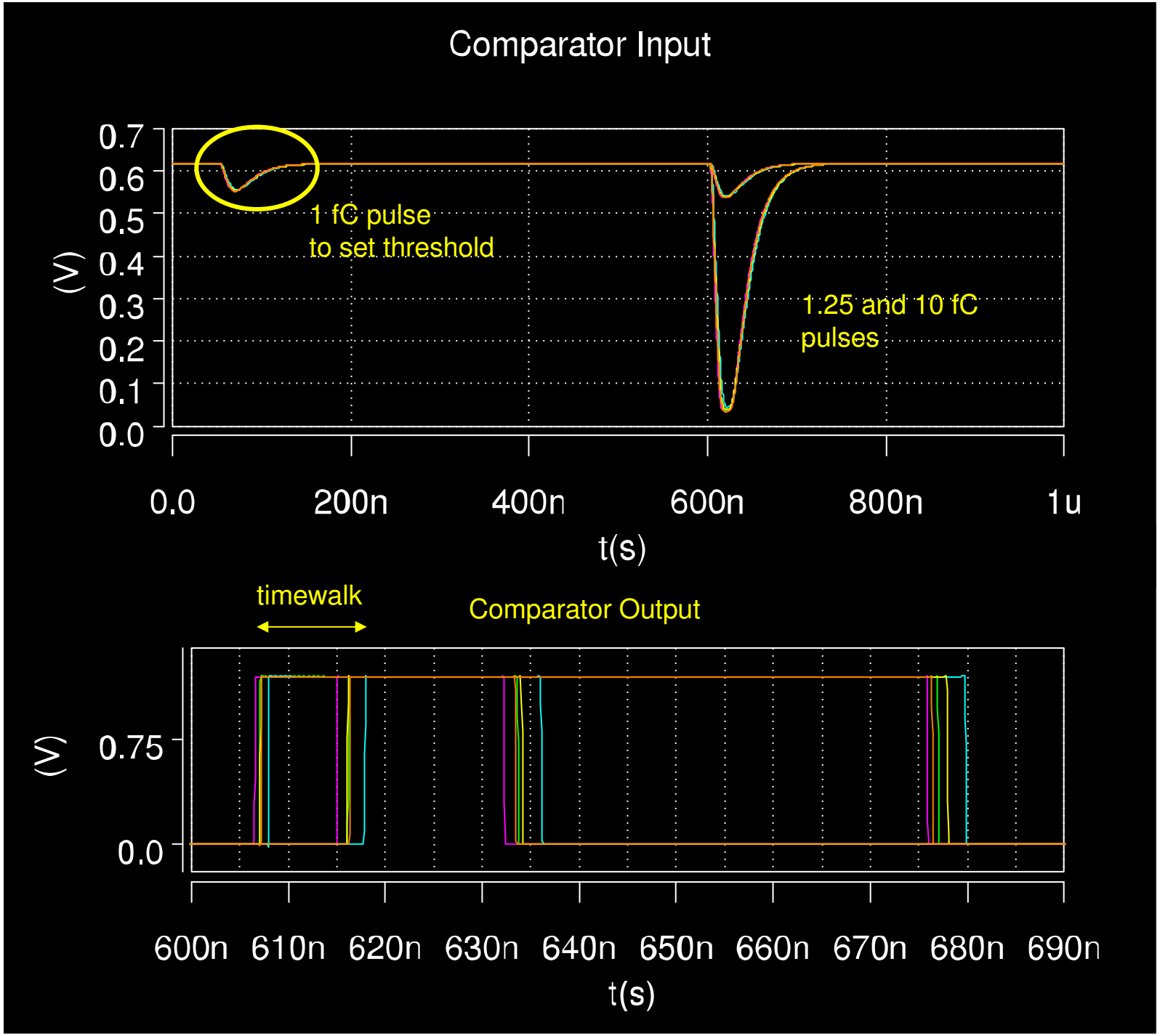
dependence of comparator fire time on signal size must be less than 1 BX
(Atlas spec.)

≤ 16 ns time difference between comparator output edges for input signals of 1.25 fC and 10 fC, for a threshold setting of 1 fC

probably a good starting point

should keep under review if other threshold settings are considered
(spec. defined for 300 μm sensors)

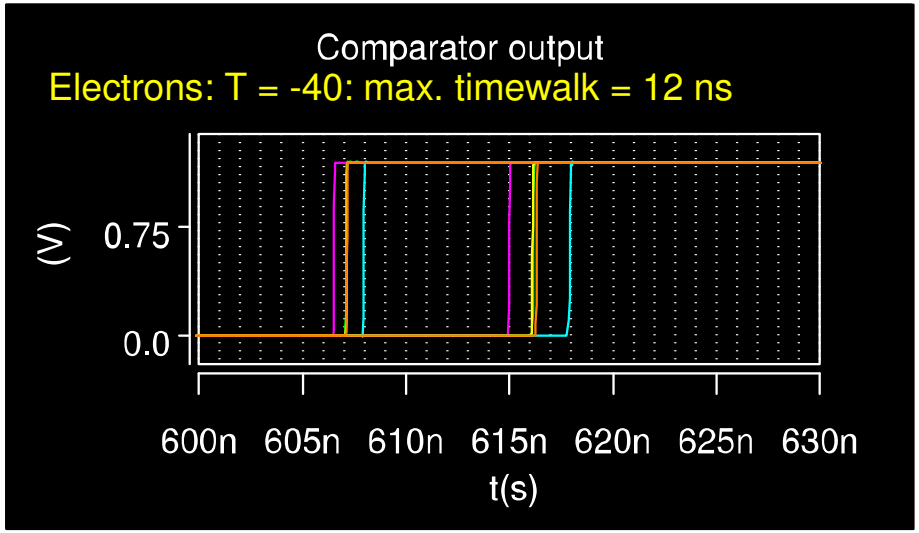


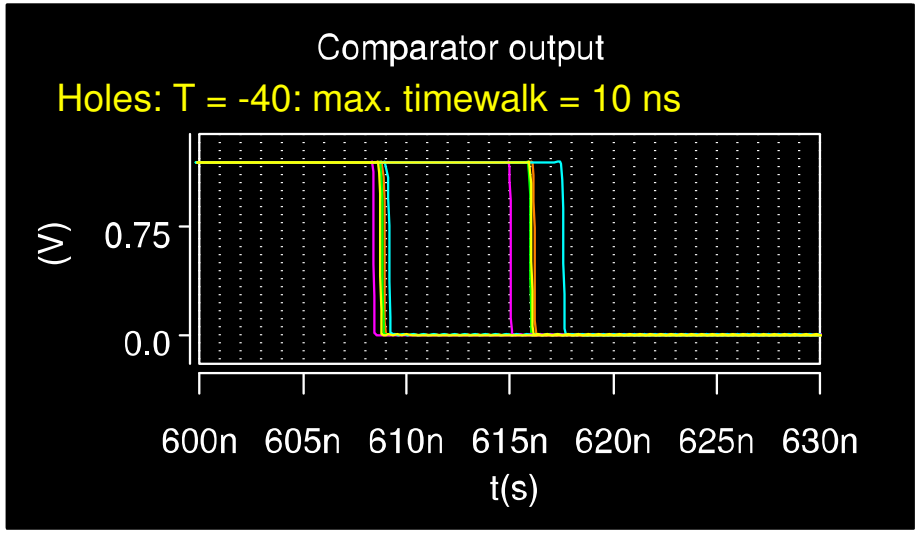


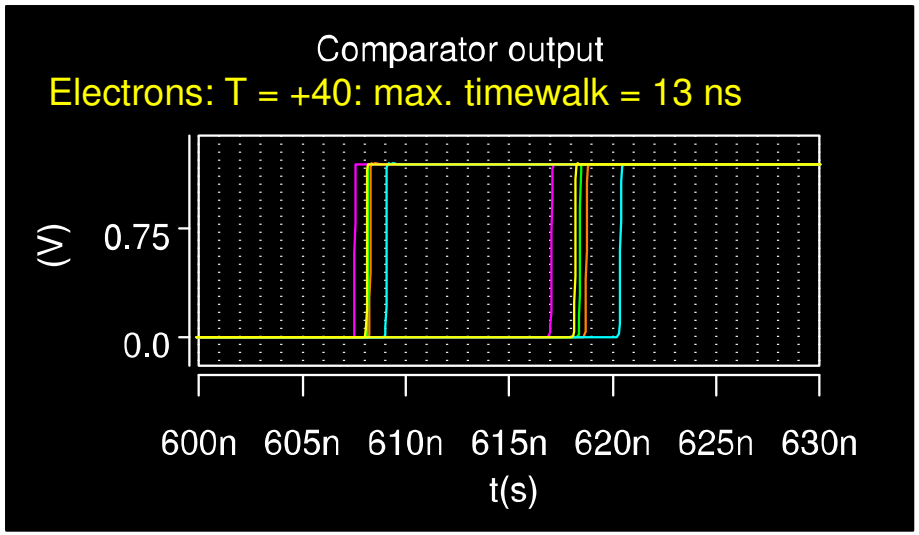
all process corners simulated

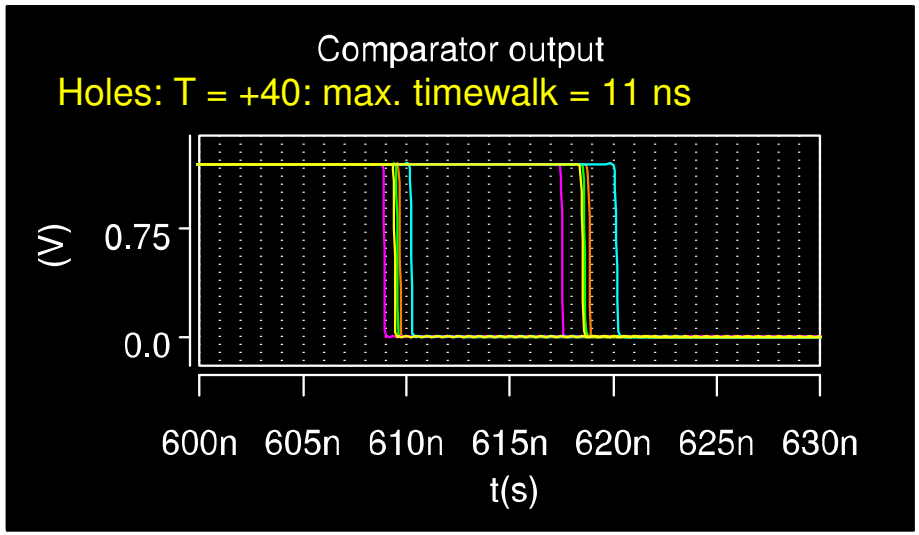
thresh. adjusted for each process corner (small differences).

comparator timewalk simulations

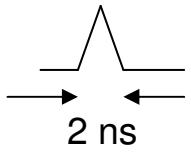




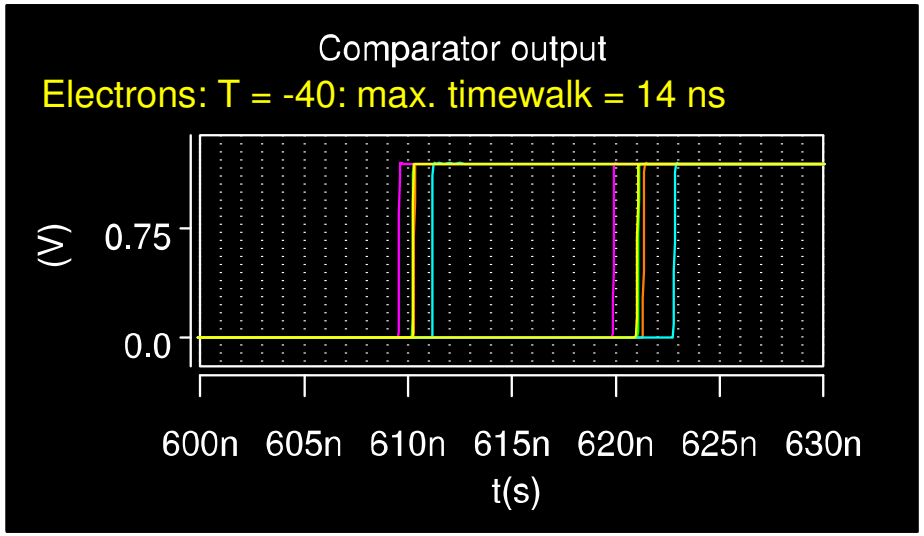


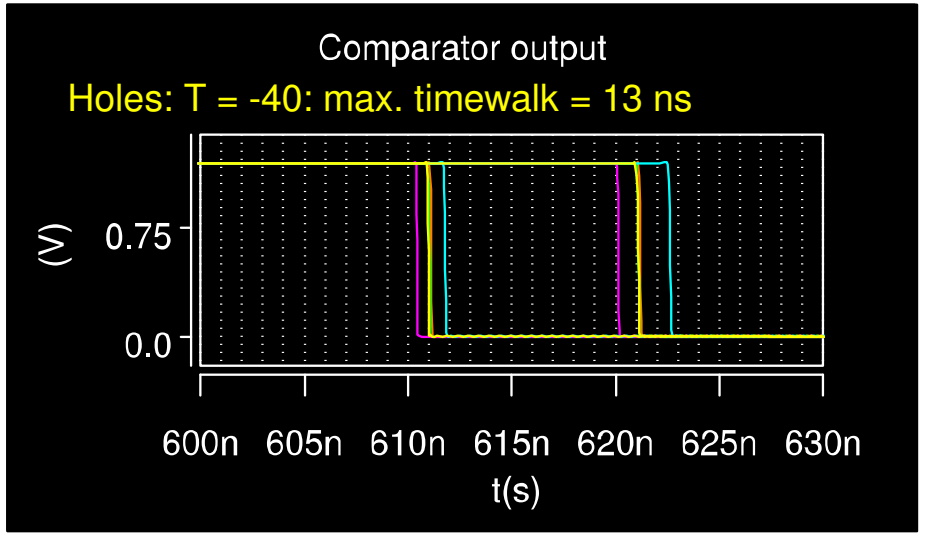


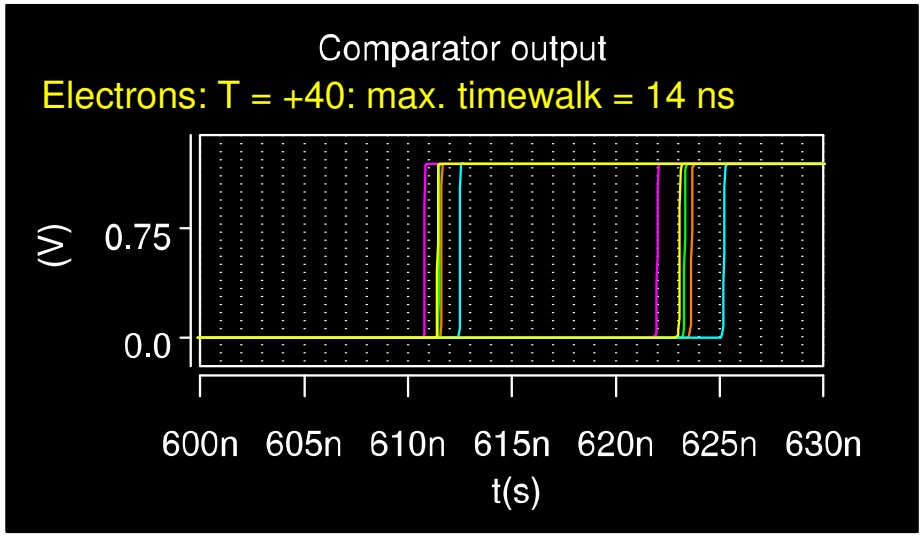
these pictures for ~1ns charge injection time => bare electronics impulse response only

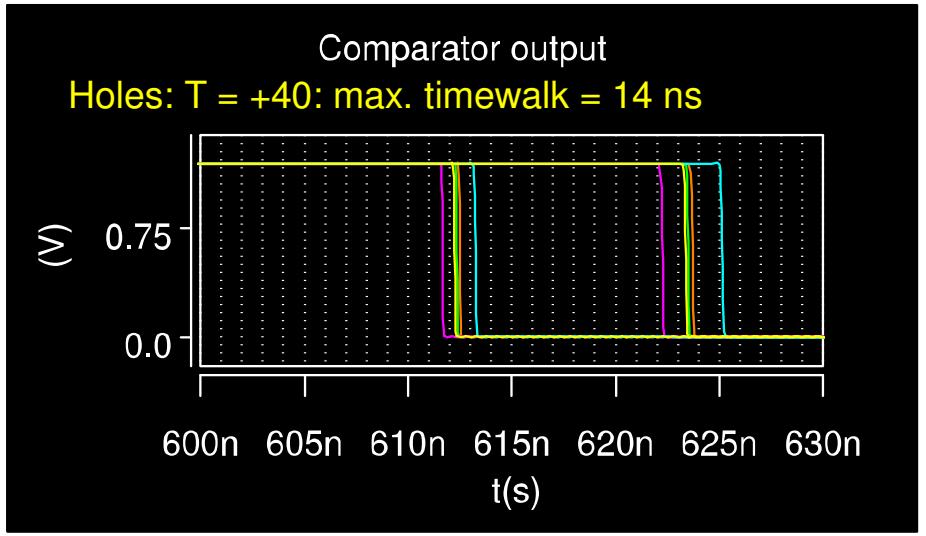


comparator timewalk simulations

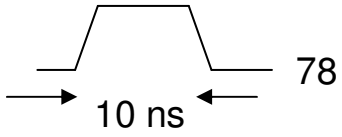




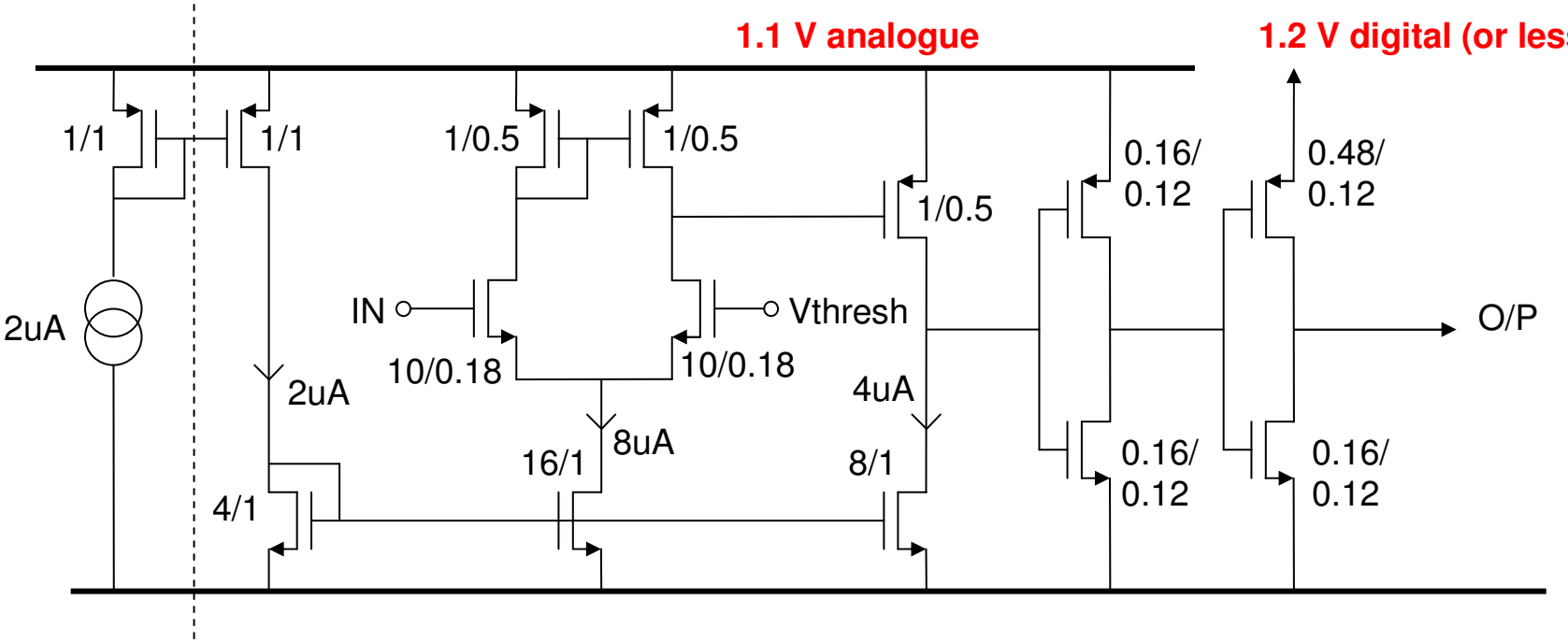




these pictures for 10ns charge injection time => spec. for sensor charge collection



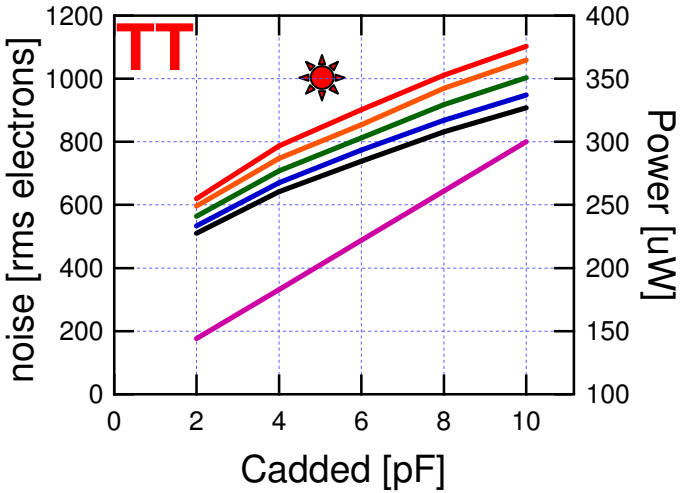
comparator conclusions

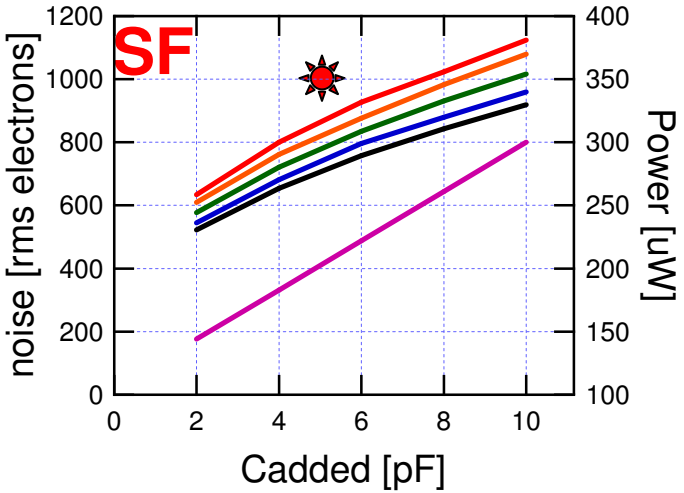


seems robust to process and temperature variations

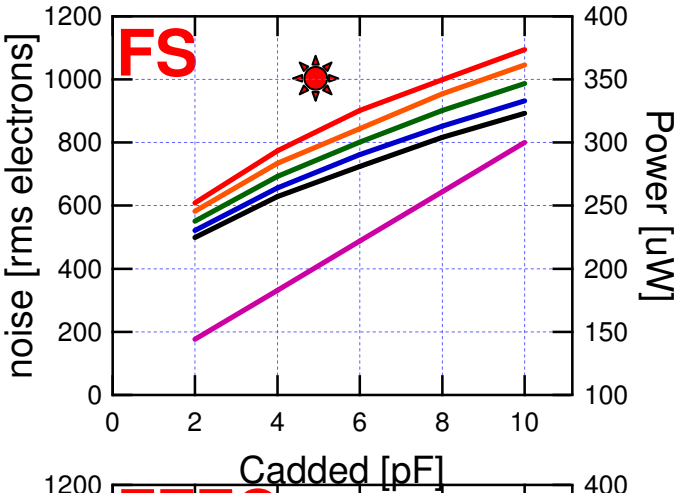
timewalk within spec.

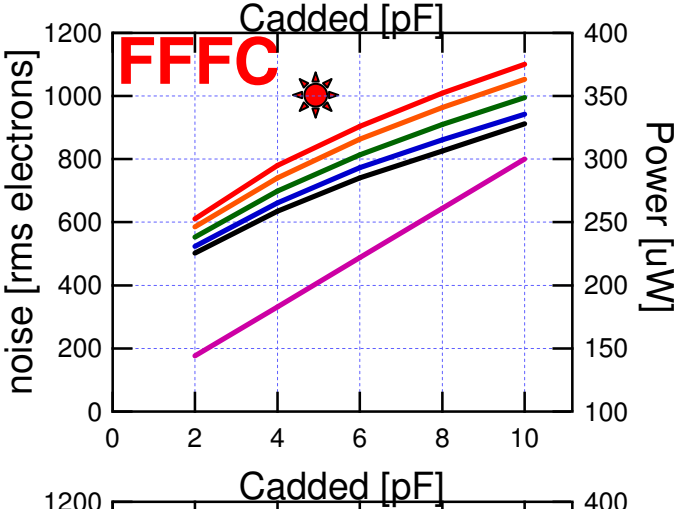
noise performance - electrons

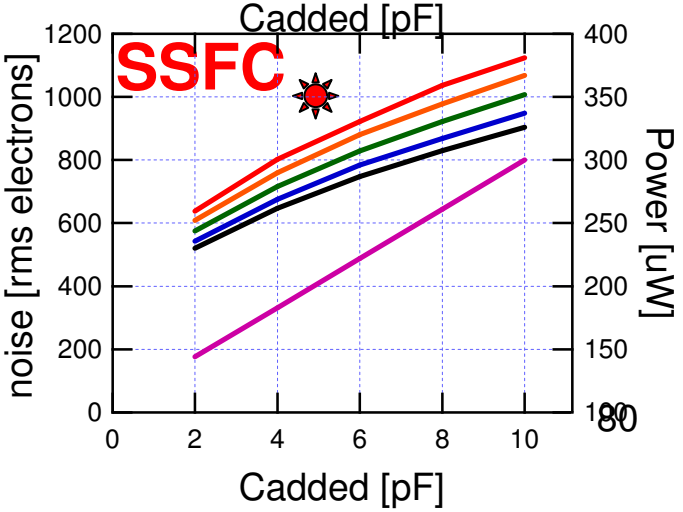




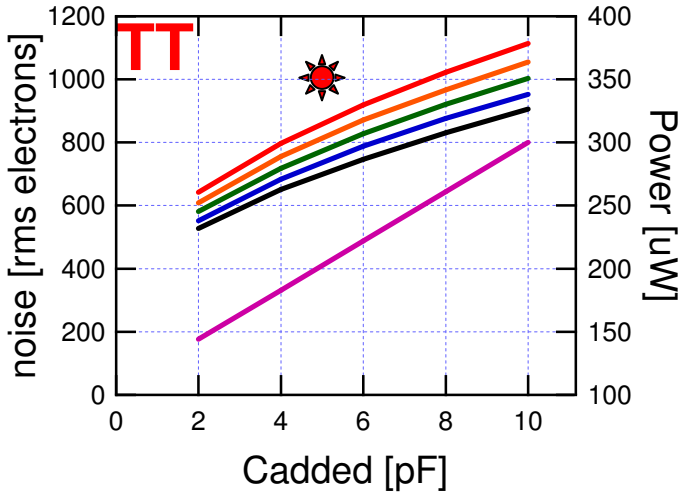
T
-40
-20
0
+20
+40

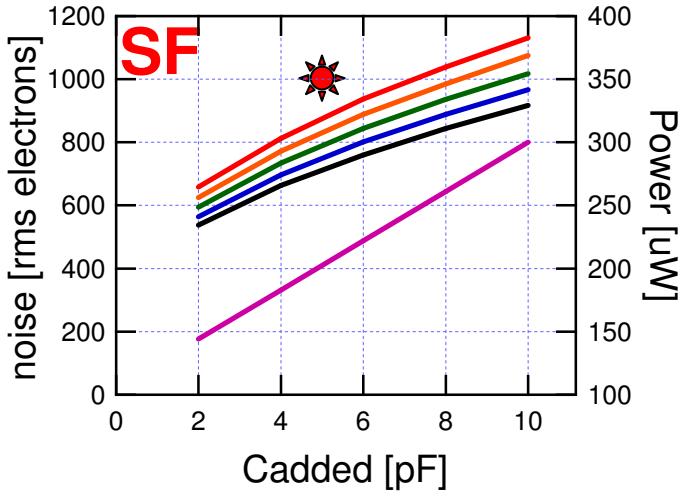




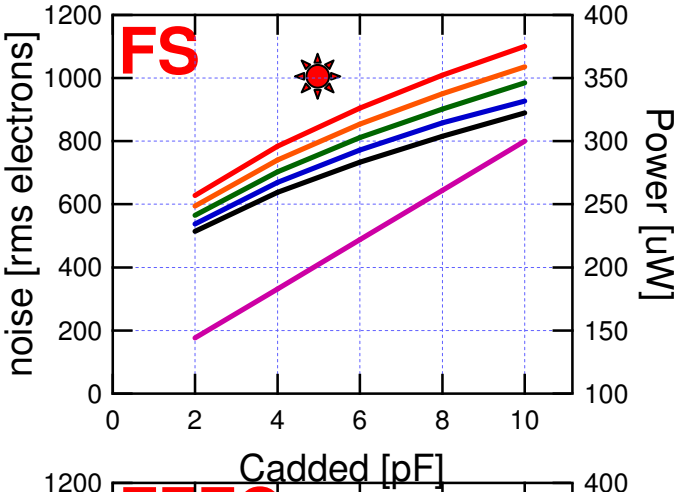


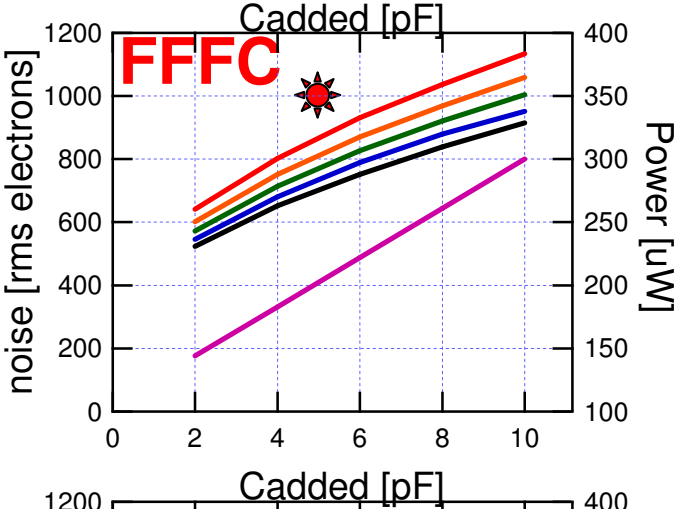
noise performance - holes

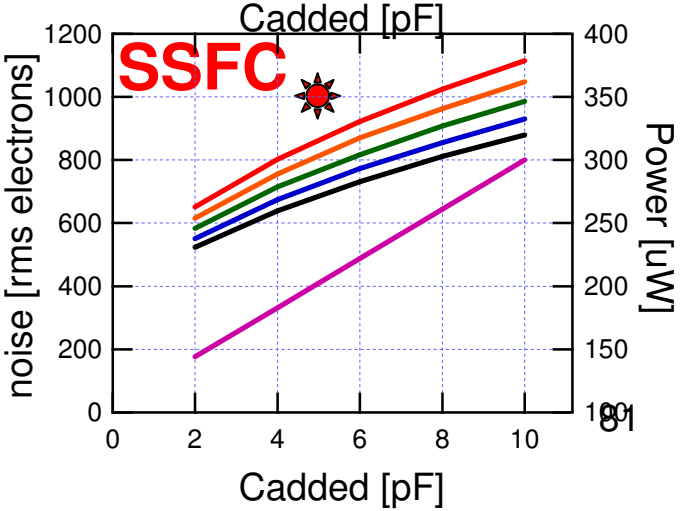




T
-40
-20
0
+20
+40





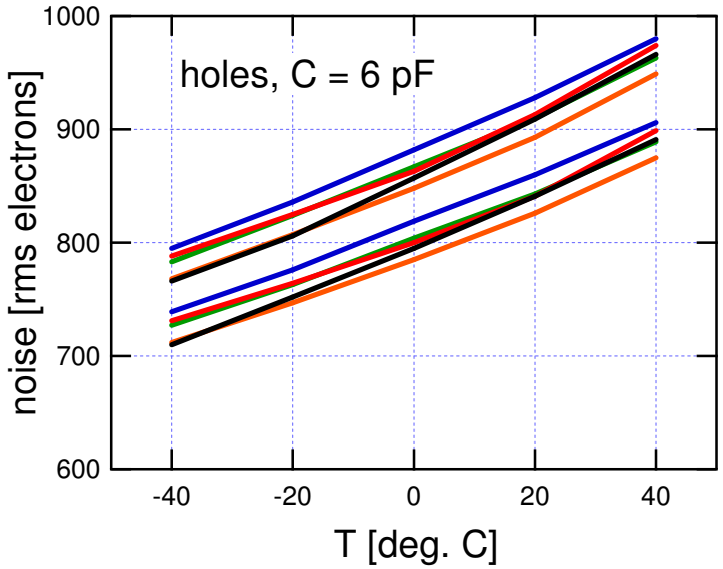


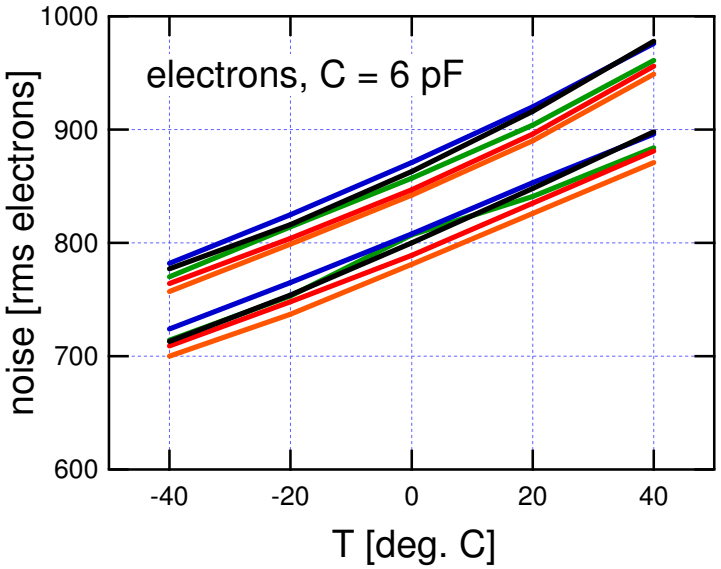
effect of +/- 20 % feedback resistor

upper family of curves for R – 20%
(all process corners)

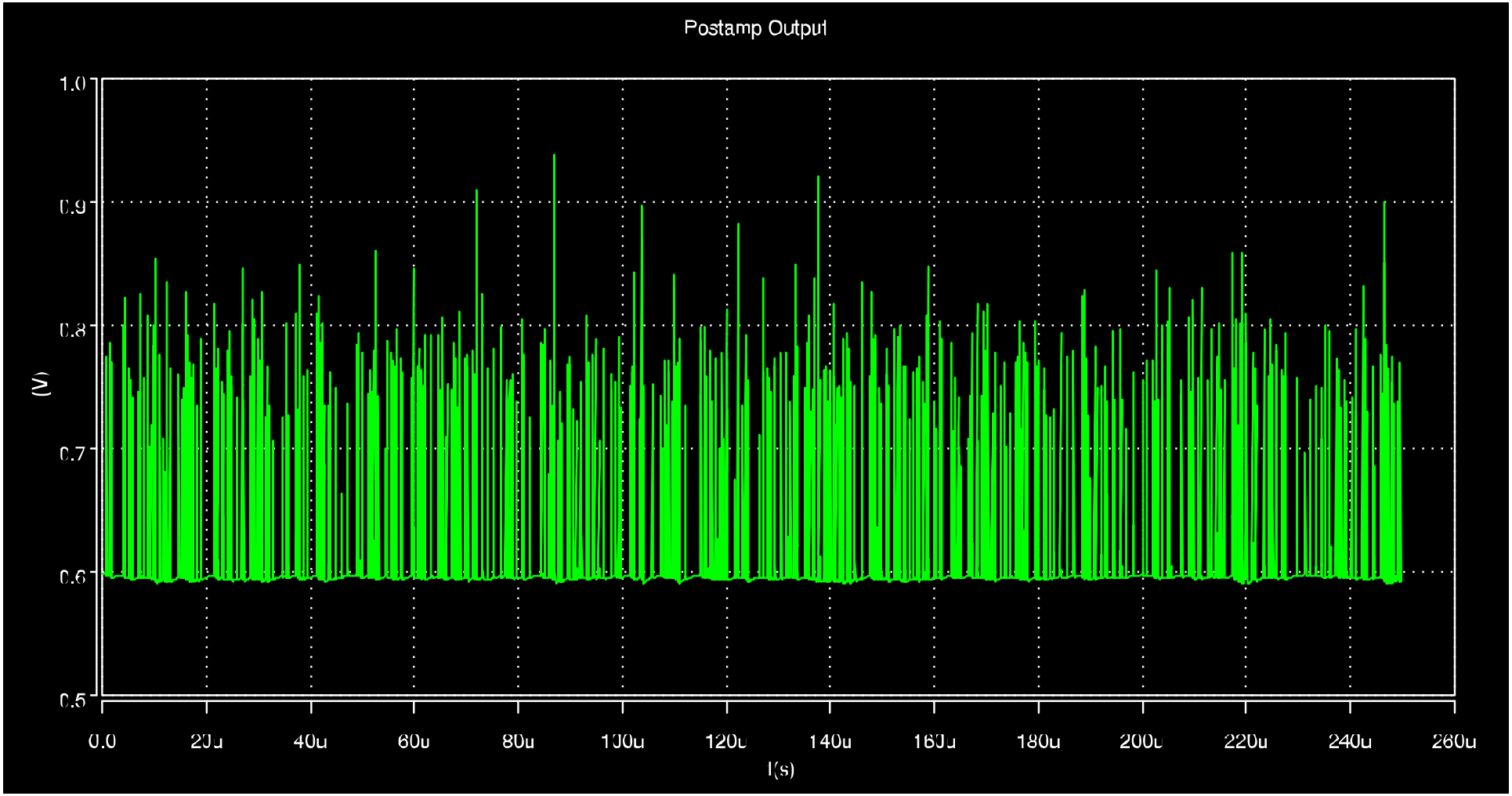
lower family for R+20%

still within noise spec.

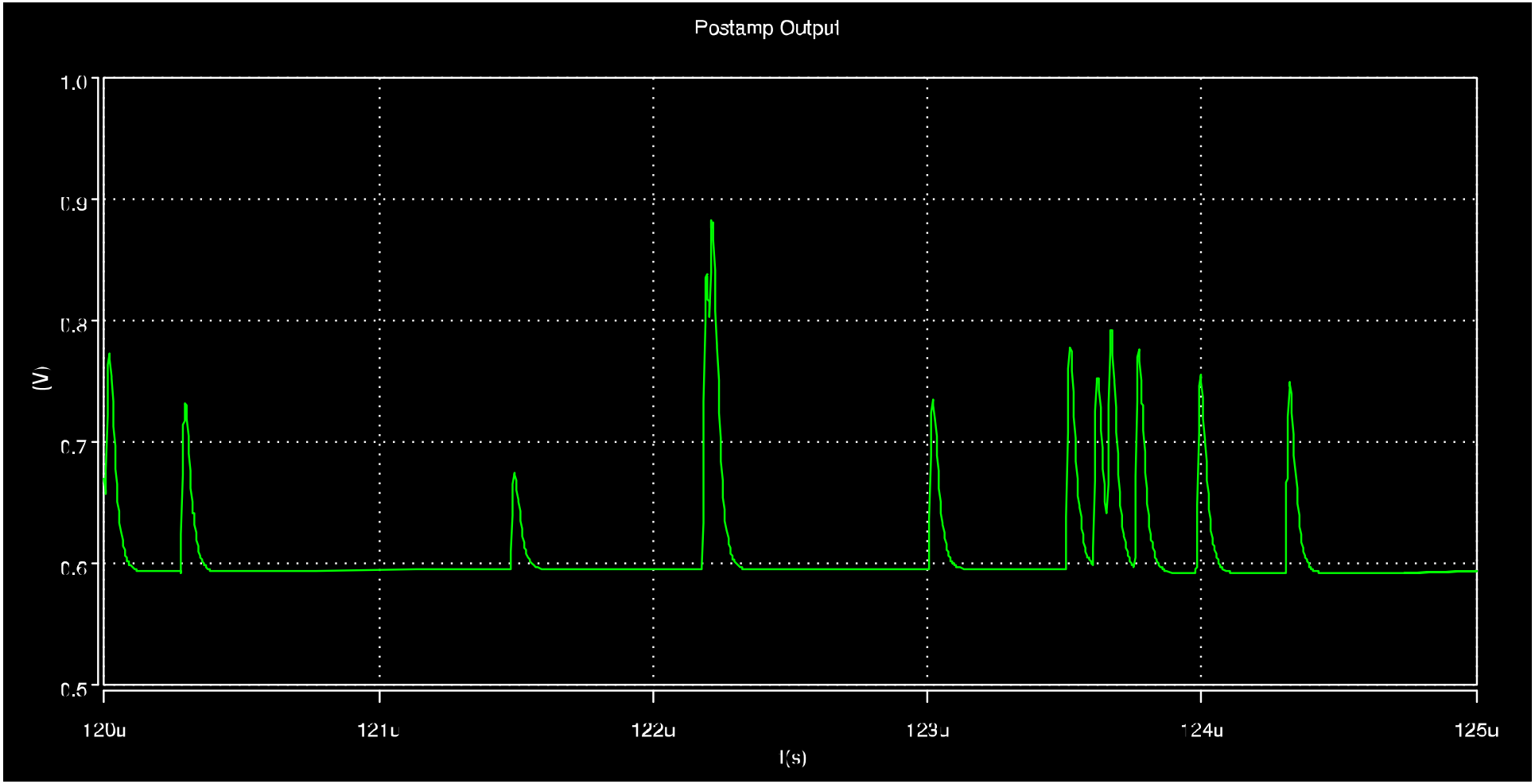




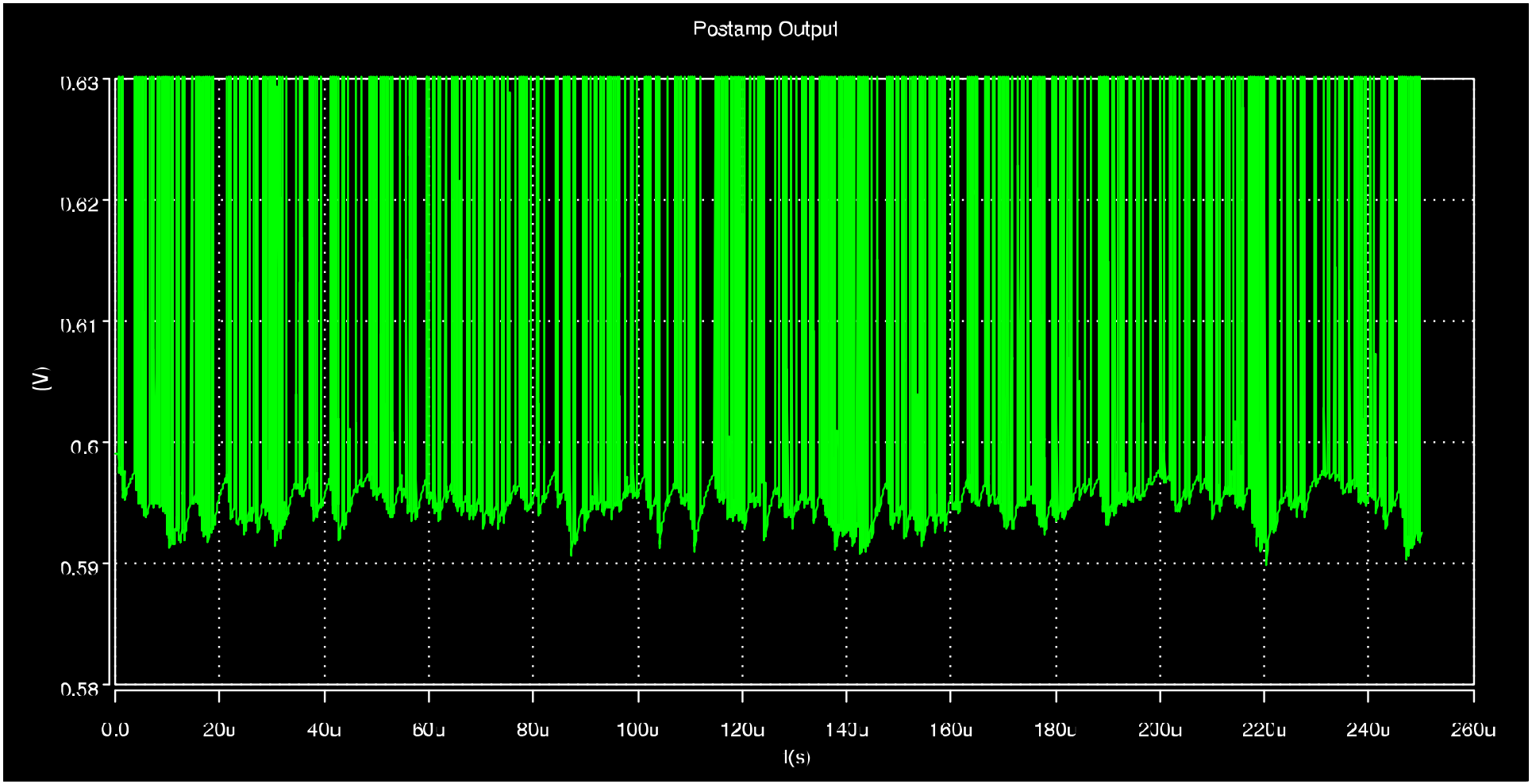
5 % occupancy


Postamp Output
1.0
0.9
0.8
0.7
0.6
0.5
(V)
0.0
20u
40u
60u
80u
100u
120u
140u
160u
180u
200u
220u
240u
260u
t(s)

5 % occupancy

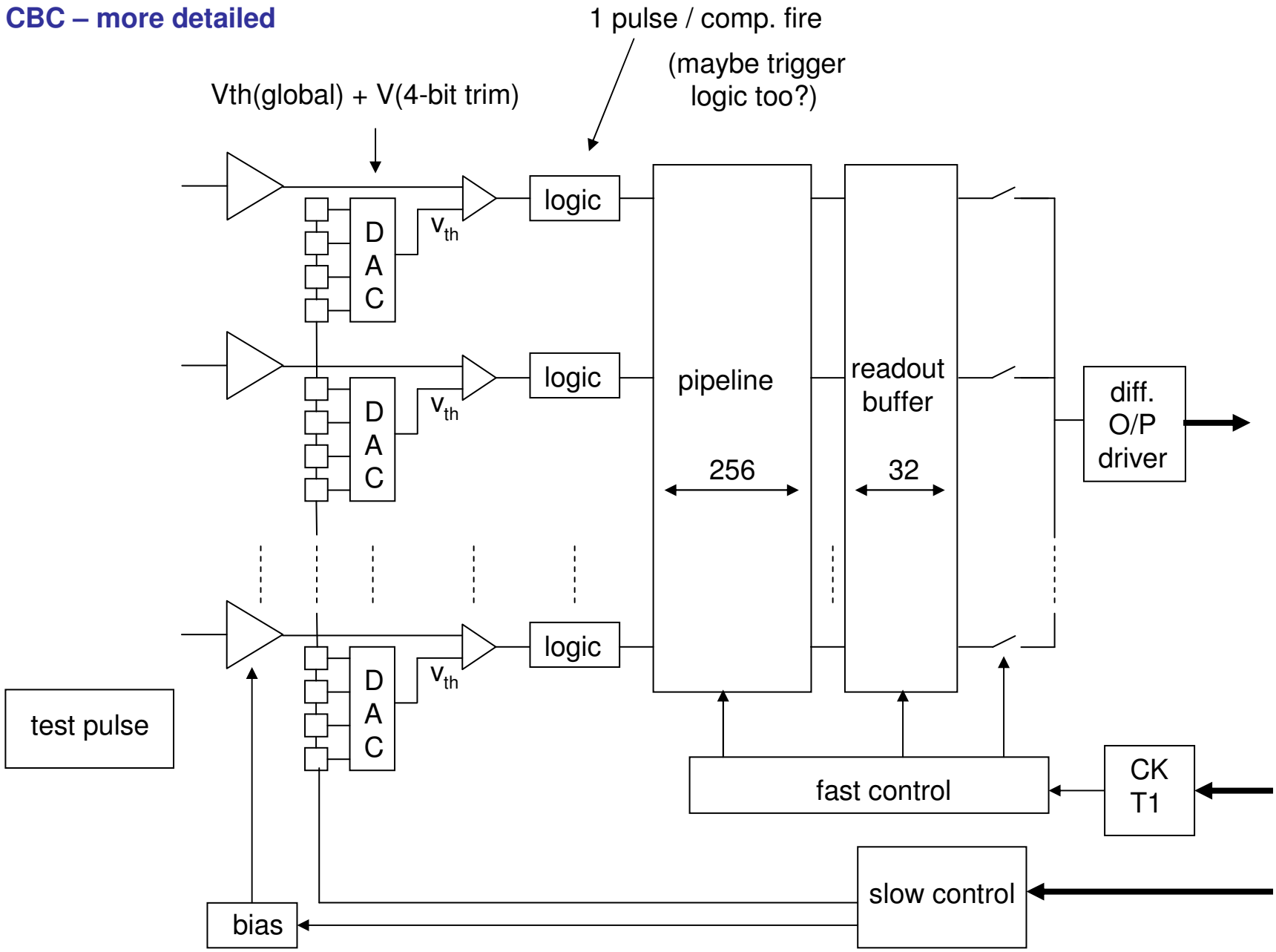

Postamp Output
1.0
0.9
0.8
0.7
0.6
0.5
(V)
120u
121u
122u
123u
124u
125u
t(s)

5 % occupancy

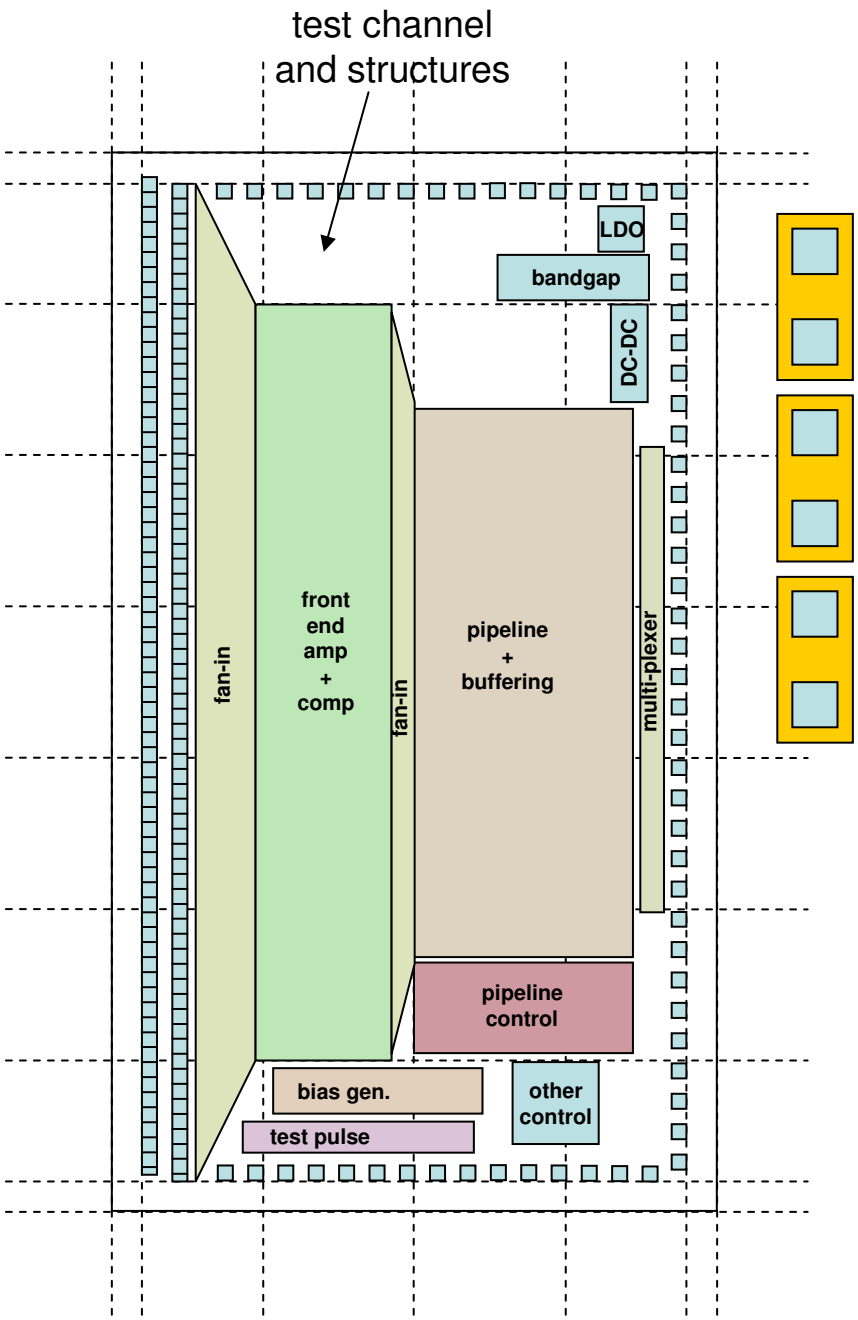

Postamp Output
0.63
0.62
0.61
0.6
0.59
0.58
(V)
0.0
20u
40u
60u
80u
100u
120u
140u
160u
180u
200u
220u
240u
260u
t(s)

THE END

CBC – more detailed



CBC floorplan

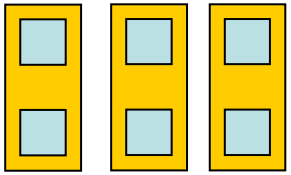


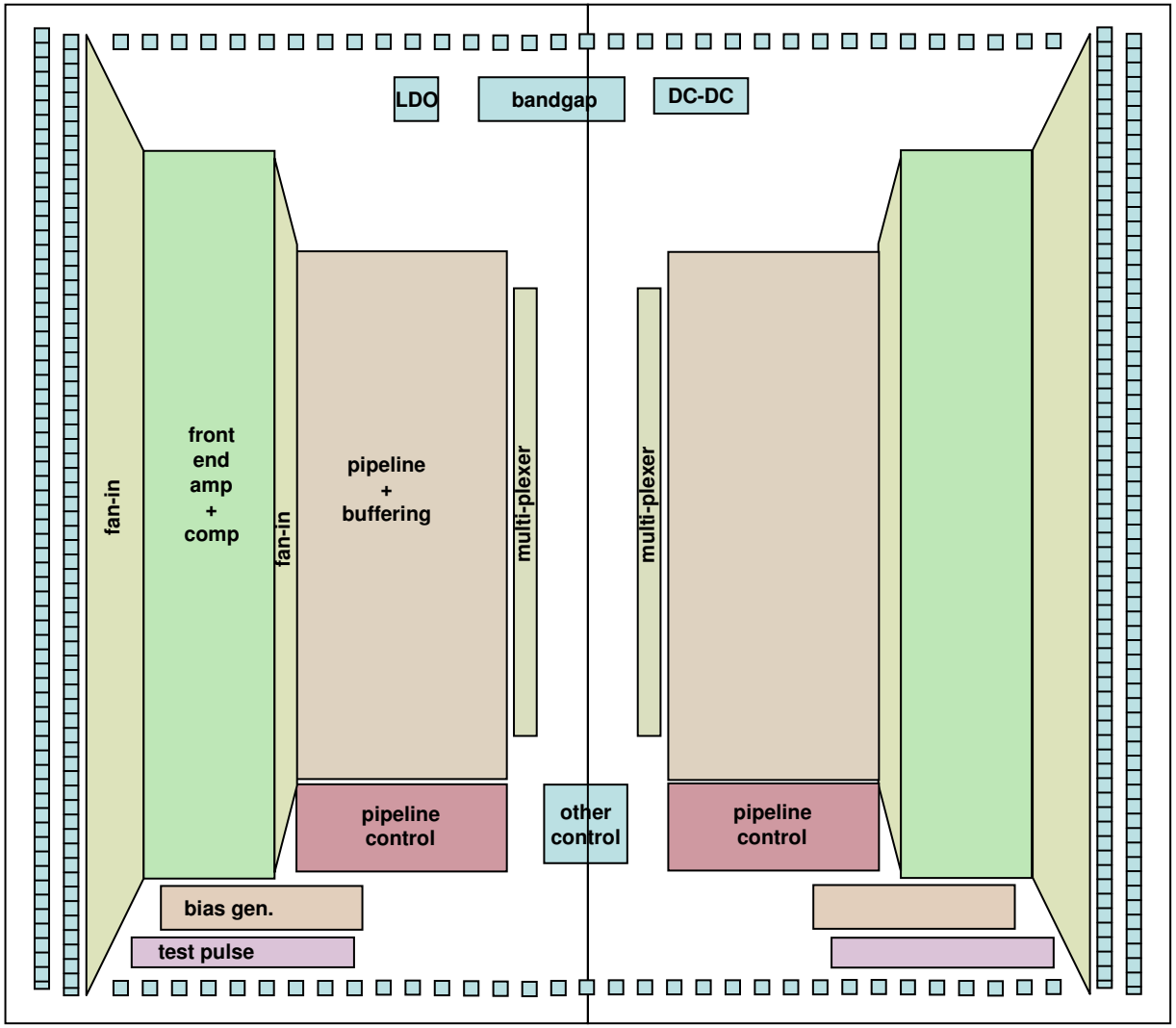
31 backend pads

pads

1. CK-
2. CK+
3. T-
4. T+
5. OUT-
6. OUT+
7. IN-
8. IN+
9. SCK
10. DIN
11. DOUT
12. ADD0
13. ADD1
14. ADD2

CBC floorplan





CBC floorplan