CBC strip chip - power issues

OUTLINE

- CBC architecture summary
- power consumption
- operating voltages
- PSR – simulations and understanding
- common mode rejection
- power circuitry in the chip – some thoughts

Mark Raymond – Imperial College

CBC intro

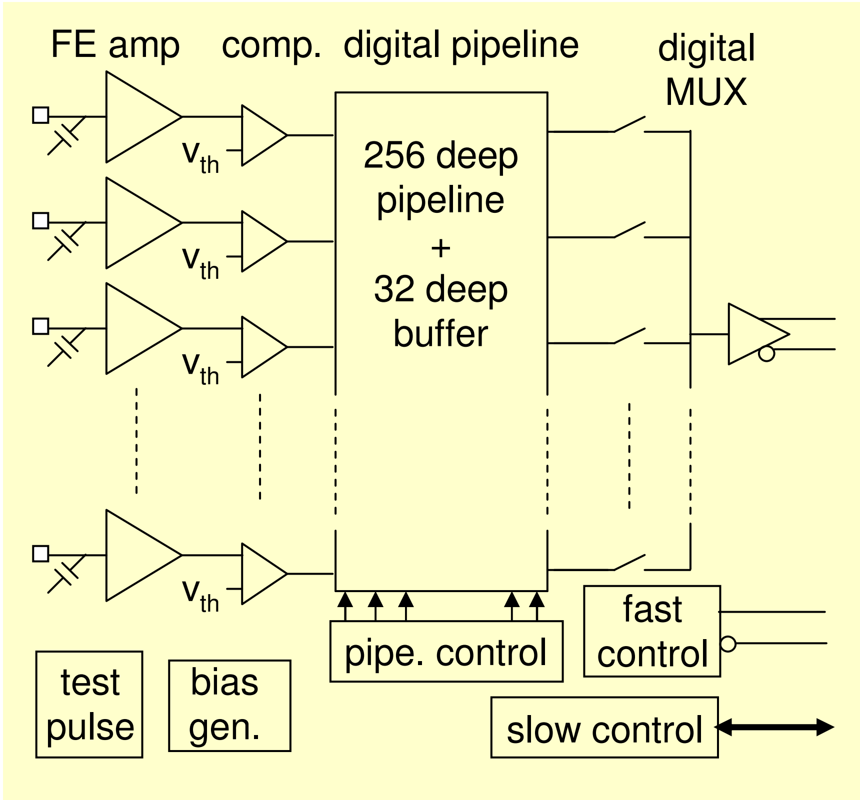
binary un-sparsified architecture for prototype outer tracker short strip readout chip at SLHC

see previous talks for details*

design of CBC now underway in 130 nm

decision now taken to adopt DC-DC powering as SLHC CMS tracker baseline

=> pay attention to front end PSR



CBC – **C**MS **B**inary **C**hip

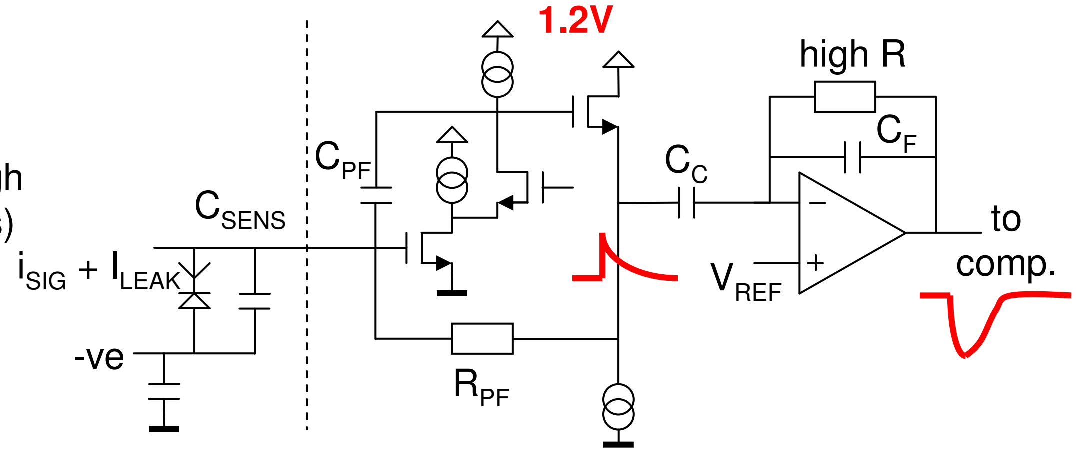
(e.g. May'08 CMS Upgrade, TWEPP'08, Jan'09 Tracker Upgrade, ACES'09 (March))

CBC front end

Preamp

NMOS I/P device

no noise penalty - 1/f corner low enough
(simulation & published measurements)
better connection to sensor for PSR
(sensor bias decoupling and
I/P FET source both at GND)



DC coupling to sensors possible

low Rpf (200k) absorbs DC leakage (1 µA -> 200 mV)
Rpf//Cpf = 200k//100fF = 20 ns decay time constant of preamp (no pile-up)

Postamp

provides gain & risetime provides integrating time constant
opamp (differential) architecture - AC coupled to preamp
blocks DC shift due to leakage (DC coupled sensors)
and blocks low frequency power supply noise coupled into front end

20 nsec peaking time => central frequency of shaping filter ~ 8 MHz

CBC estimated power consumption

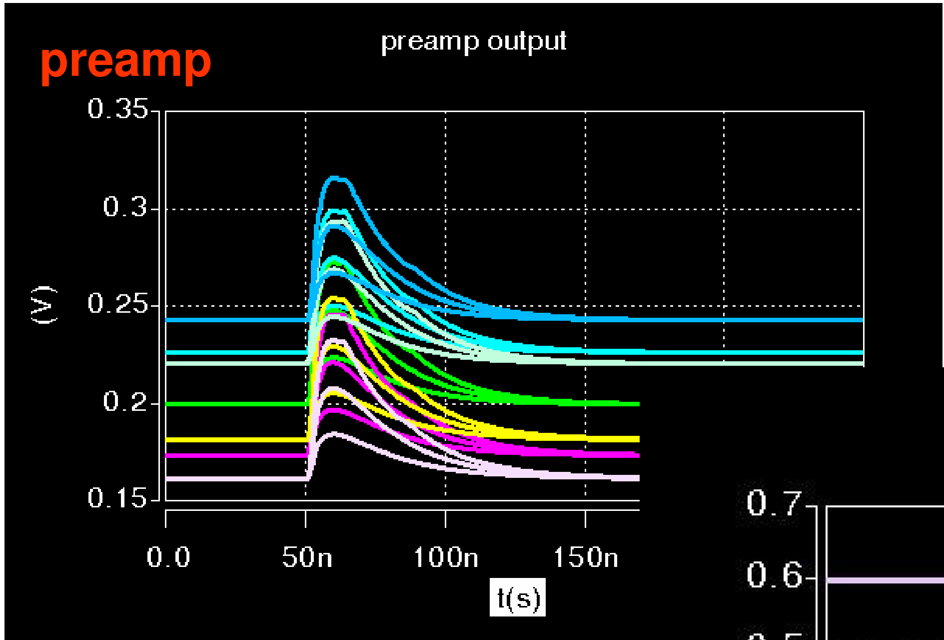
	power/FE chan.	
preamp/postamp		
20 nsec peaking time, short strips C_{SENSOR} ~ 5pF	180 μW	~ 200 μW analogue
(~ 100 + (15 x C_{SENSOR}))		
comparator		
estimate (preliminary simulations)	20 μW	
digital		
take 0.25μm APV25 (digital 400 μW)		
/10 for technology, x3 for SEU	120 μW	~ 300 μW digital
(pessimistic? CBC logic should be simpler)		
output		
LV differential ~ few mW / 128 chans.	30 μW	
contingency		
just guess nominal figure to bring overall power to 0.5 mW	150 μW	

0.5 mW / channel seems like an achievable target (c.f. 2.7 mW for APV25)

digital is biggest uncertainty, and maybe largest contributor
hope to improve estimate as design progresses
can consider running at lower voltage (dig. power ~ V^2) => extra contingency
e.g. 1.2 -> 0.85 power consumption halved
will keep power rails separate on chip to keep option open

using numbers above: 128 chan. chip needs ~ 20 mA analogue, ~30 mA digital

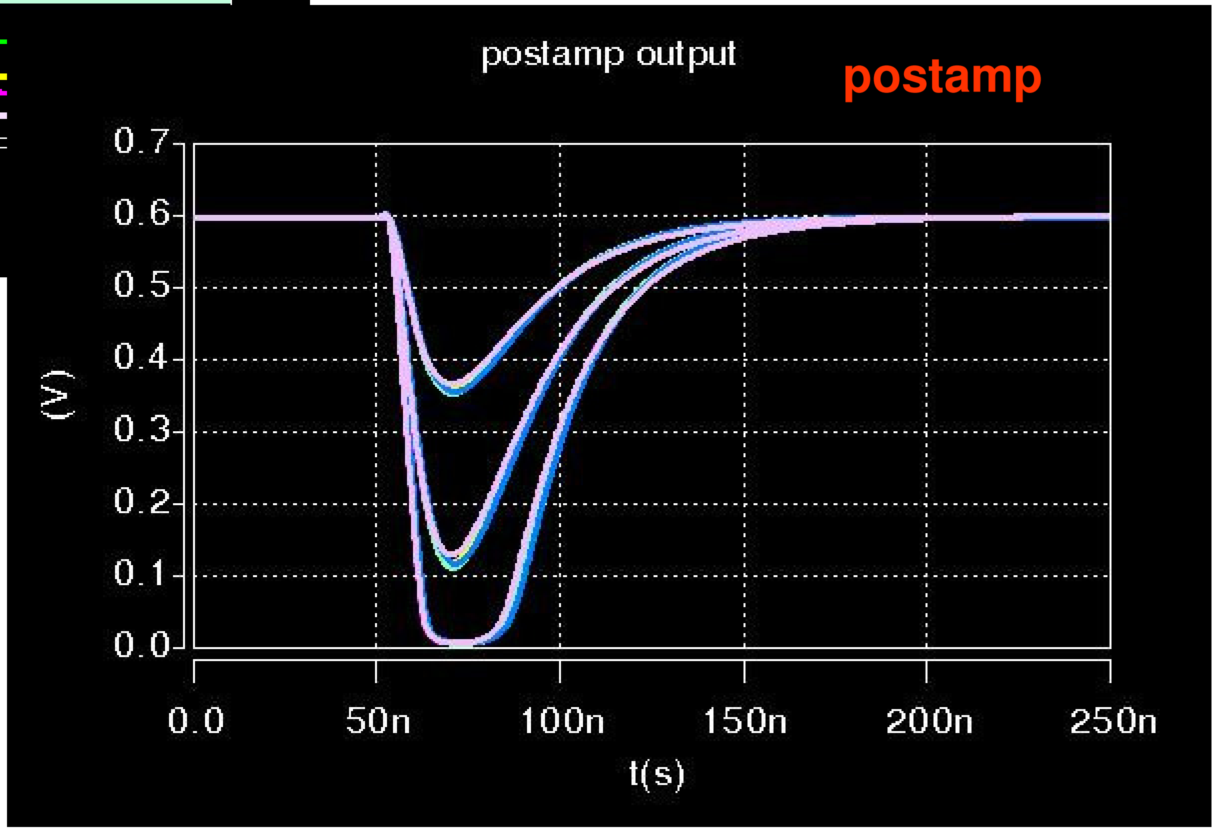
operating voltages & requirements



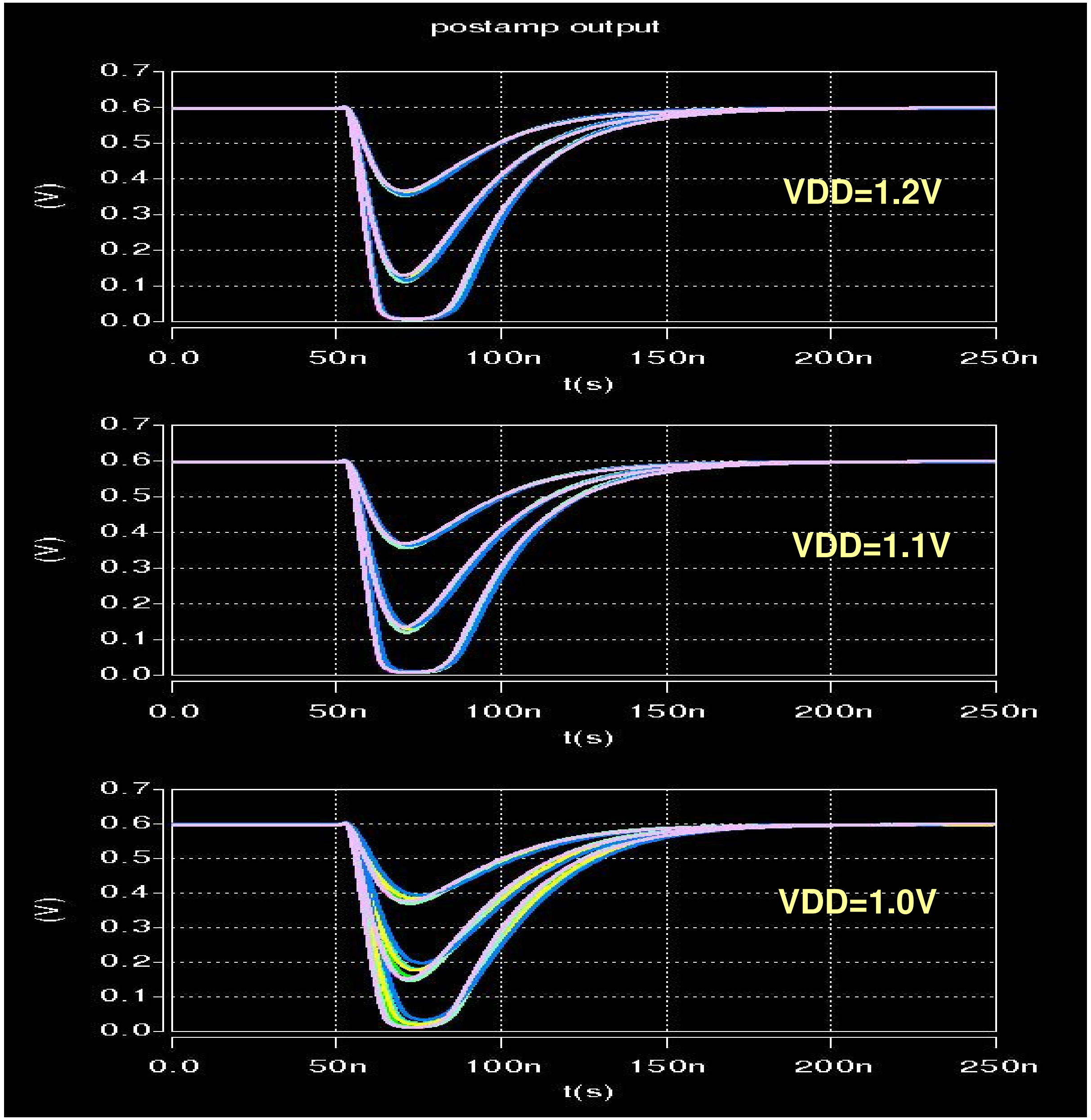
pictures here show 4fC, 8fC, 12fC signals
for VDD = 1.2V & varying process corner parameters

small effect of process variations on postamp output

use this approach to see how robust design is to varying VDD



operating voltages & requirements



effect of reduced VDD on analog performance not significant till more than ~ 10% below nominal 1.2V

could use to allow 10% tolerance on PSU levels

or keep tighter PSU tolerance spec. and exploit margin to allow for drop across passive filtering components

e.g.

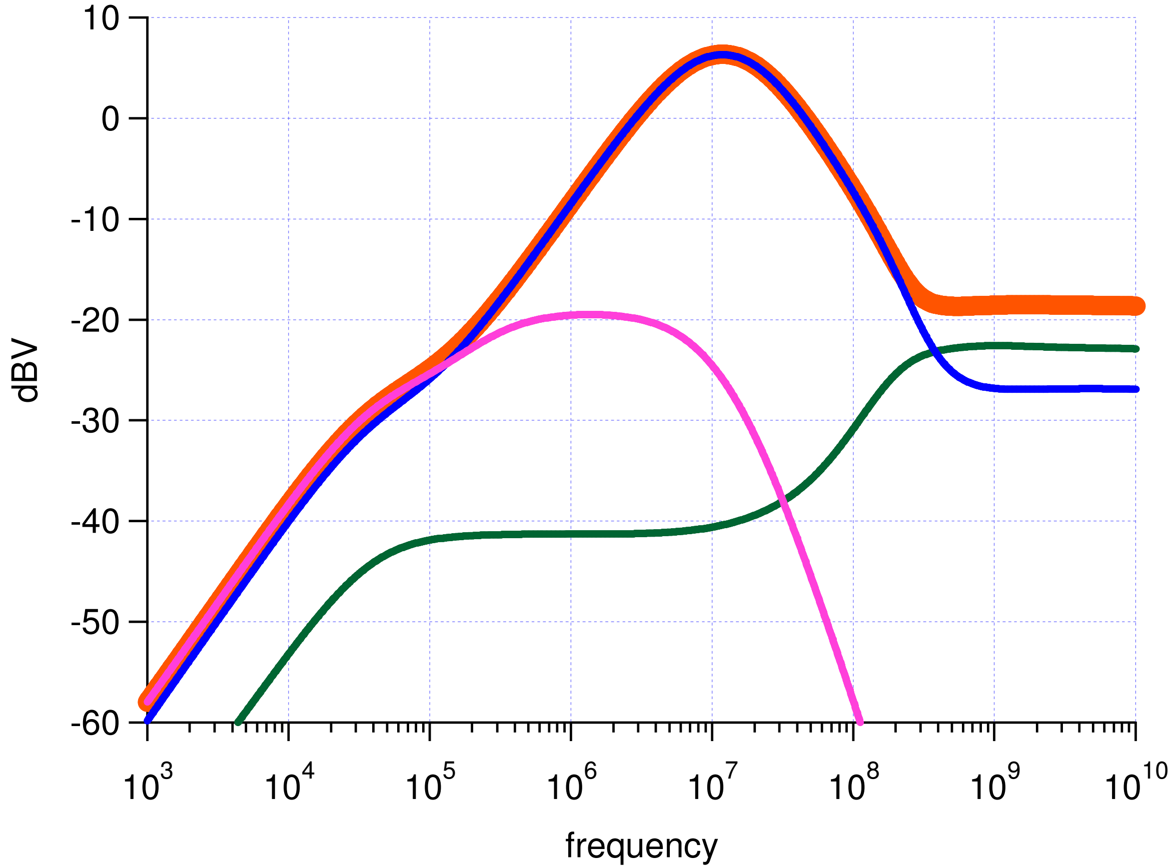
analogue current consumption for 128 chan. chip ~ 20 mA

if allow 50 mV drop across filter resistor => 2.5 ohms

=> not so big C required in RC filter e.g. C=220nF => RC=550 nsec.

could be a useful strategy?

PSR – as it stands



response to sinusoidal ripple on VDD supply to preamp, postamp or both

power supply rejection dominated by preamp response

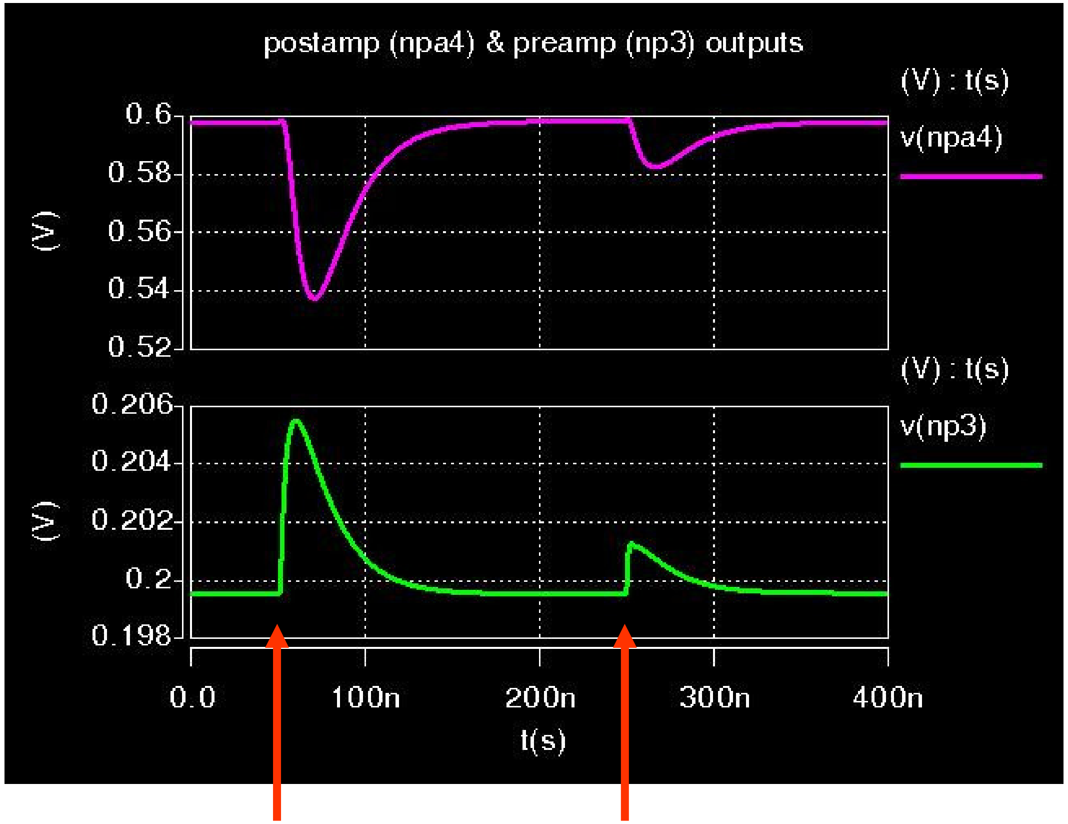
no rejection at ~10 MHz

better at lower frequencies

filtering helps a lot

preamp & postamp (no filtering)
preamp only (postamp supplied separately)
postamp only (preamp supplied separately)
preamp & postamp (with RC = 550ns filter (2.5Ω + 220nF)

time domain picture



1 fC normal signal

10 mV step on supply rail

time domain picture can help to visualise effects of supply disturbance (and helps when investigating effects of circuit changes)

can also superimpose “real” noise signal on VDD rail

PSR – understanding

preamp PSR dominated by current mirror circuits deviation from ideality

power supply voltage change ΔV leads to current change ΔI_{DS} flowing in input transistor

$\Delta I_{DS} = g_m \, \Delta V_{GS}$ so small shift in preamp input voltage

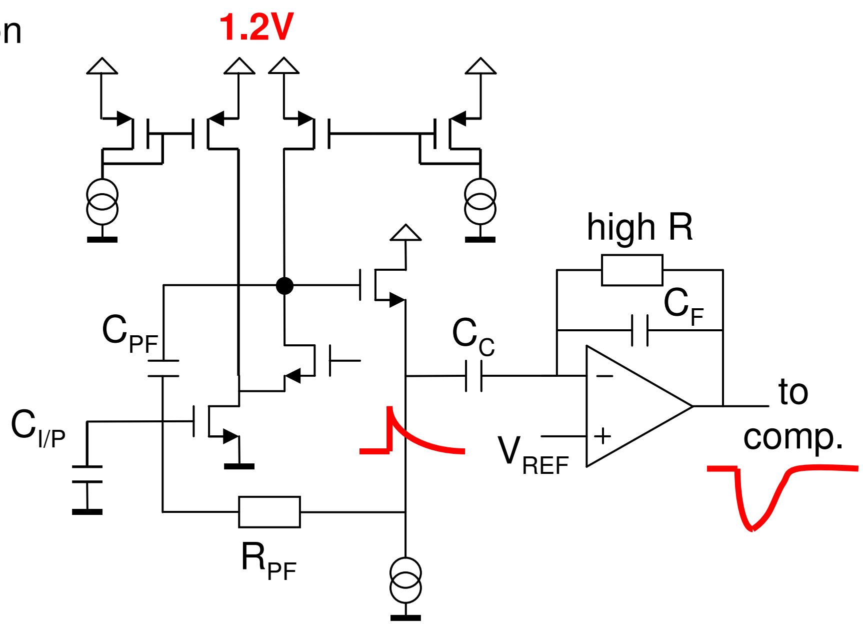
equivalent to an injection of charge $Q = \Delta V_{GS} . C_{I/P}$

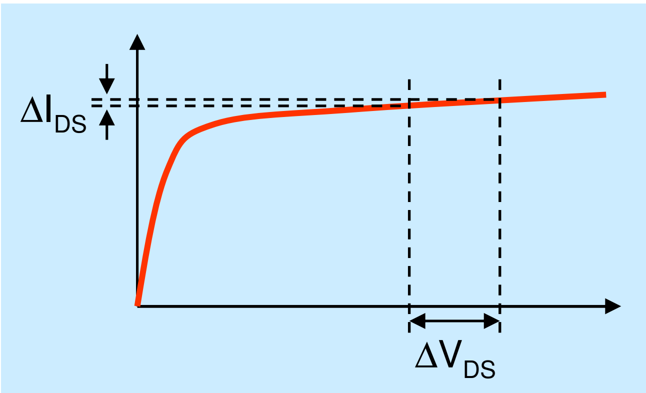
can situation be improved?

have been trying – not much success so far

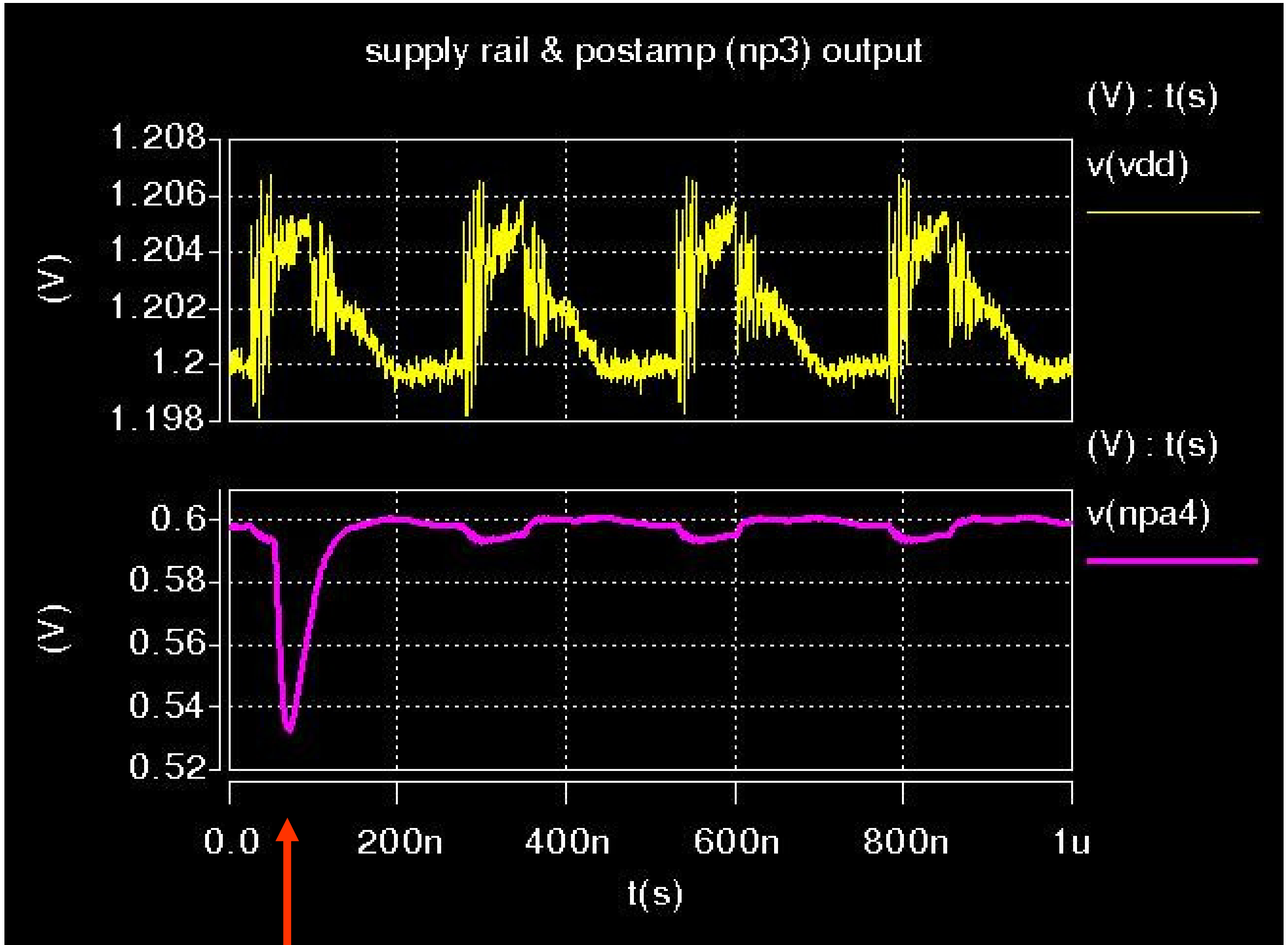
more sophisticated current mirror circuits have drawbacks

> biasing difficulties if don't make current source devices shorter
> … but that leads to extra noise





time domain picture for noise



1 fC normal
signal

measured noise waveform added to VDD rail

200 ps sampled scope data for Enpirion "quiet" converter (provided by Aachen)

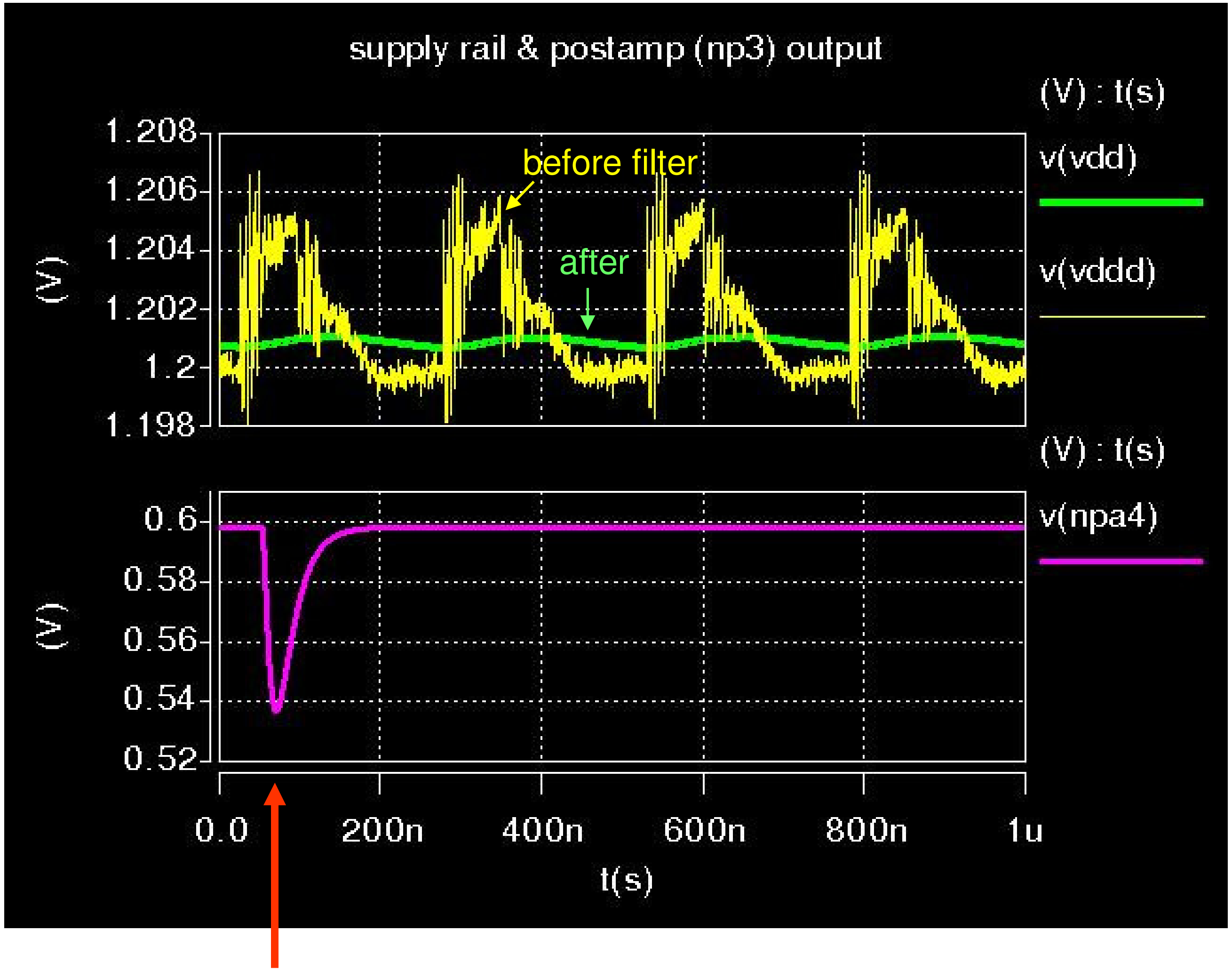
very high frequency components disappear (too high frequency for circuit to respond)

but 4 MHz disturbance clearly visible

~ 7mV pk-pk

(equivalent to ~750 e)

time domain picture – filtered noise



1 fC normal signal

previous noise waveform added to VDD rail

then filtered by ~ 550 nsec RC filter (2.5Ω x 220nF)

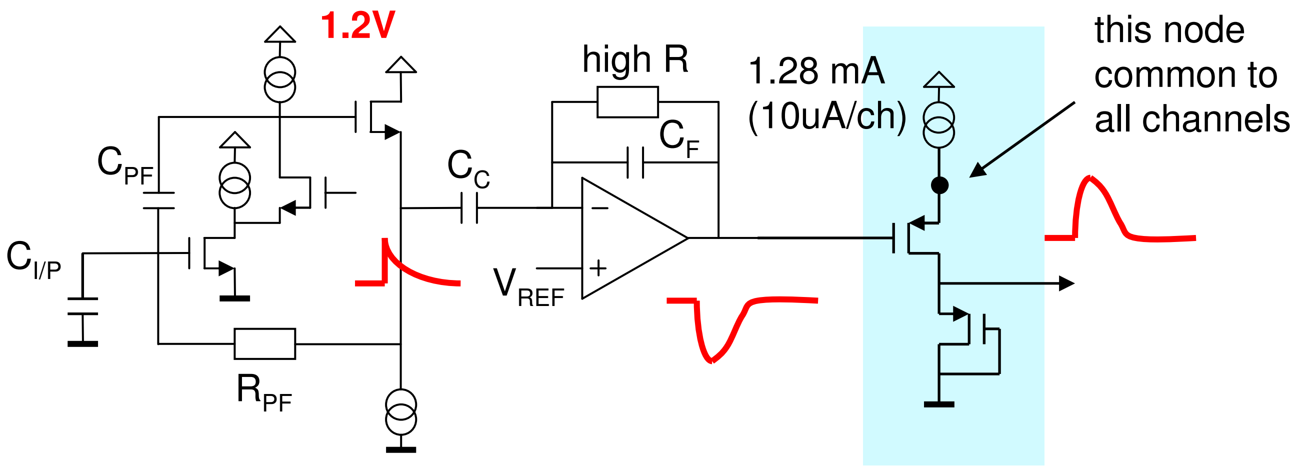
noise on postamp O/P now v. small

~ 0.5mV pk-pk (~ 50 e)

=> simple filtering could be effective

consumes space on hybrid
- but would need decoupling capacitors anyway – just add a series resistor

common mode rejection



power supply noise is a CM effect

=> CM subtraction will remove

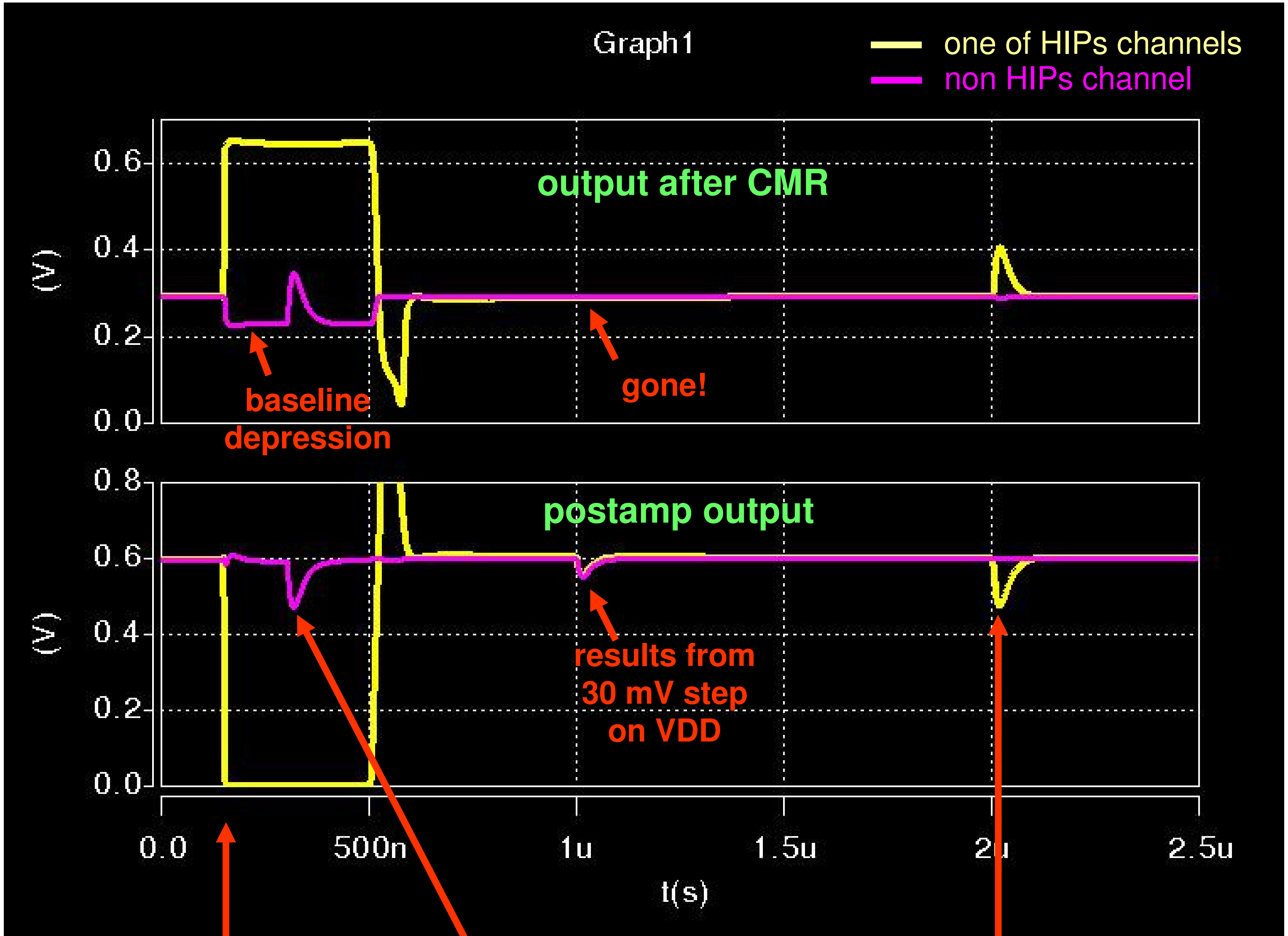
simple inverter circuit with common supply node does the job, see* for circuit operation

(like inverter in APV, but no external resistor, and AC coupled)

works very well, but… (next slide)

*http://icva.hep.ph.ic.ac.uk/~dmray/pptfiles/CMStracker31_10_01.ppt

CMR + HIPs



4pC injected
(shared by 3 “HIPs” channels)

2 fC injected on
non-HIPs channel

2 fC injected on
HIPs channel

128 channel sim.

CMR very effective at removing power supply disturbance

but causes baseline depression until recovery from HIPs saturation

=> potential loss of signal during recovery period (the HIPs effect)

do we really want to do this?
(I don’t think so)

power circuitry in the chip?

my personal thoughts from FE chip perspective

switched capacitor voltage splitter 2.5 -> 1.2 on-chip (12 -> 2.5 done remotely)

concerns

main concern noise injected into chip substrate by switches charging relatively large capacitors

quite a lot of interest in the phenomenon, see* for many references
(there are also techniques to mitigate effects)

external capacitors consume real estate on hybrid

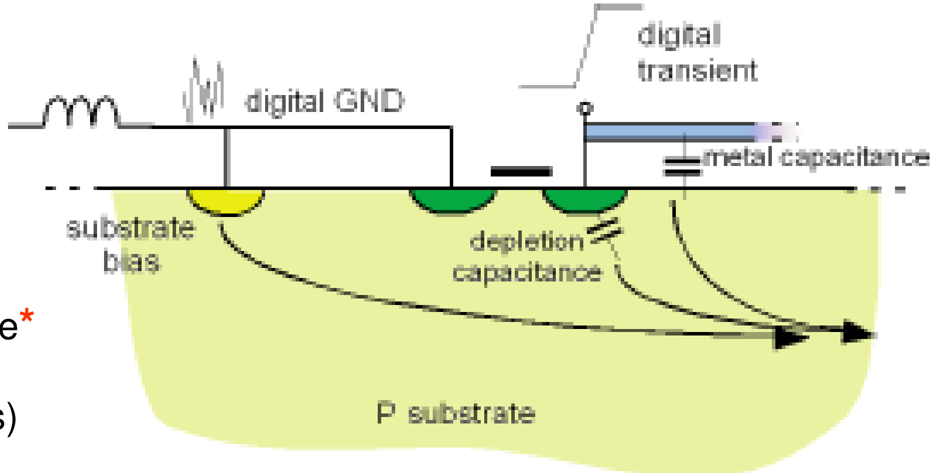


Fig. 1 Scheme of the potential sources of substrate noise.

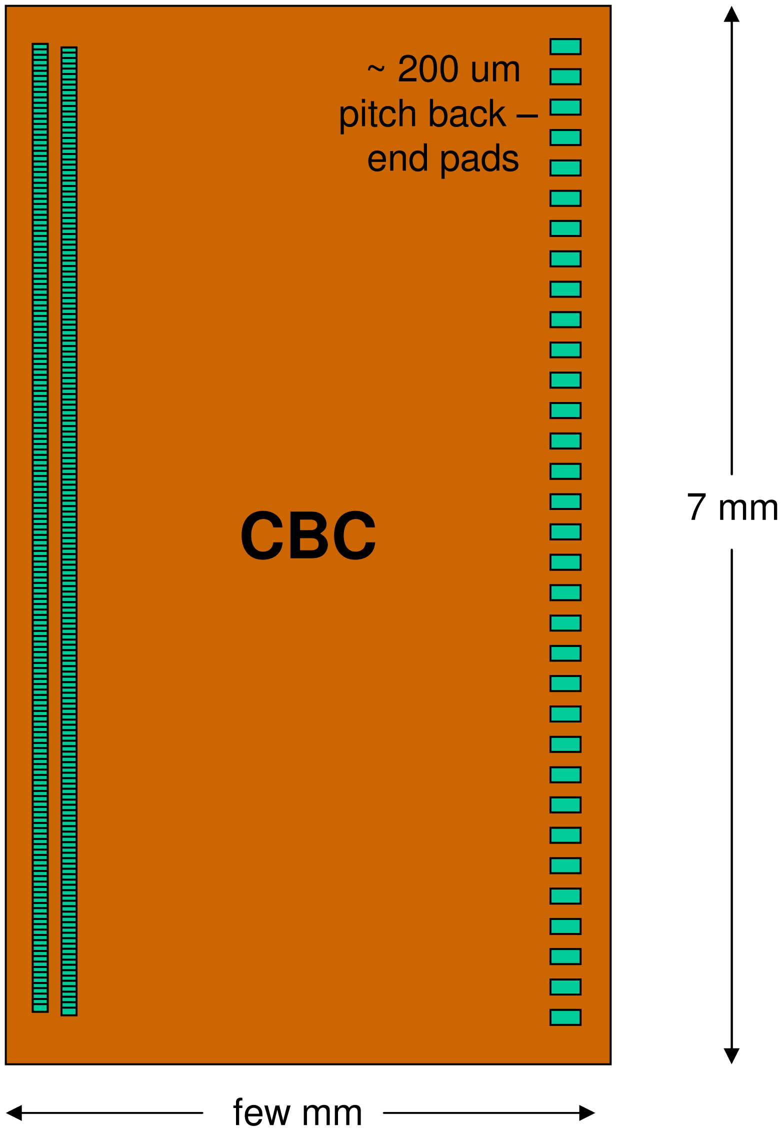
**http://pmos.upc.es/blues/publications/SignalIntegrity/chipps02.pdf*

LDO regulator on chip

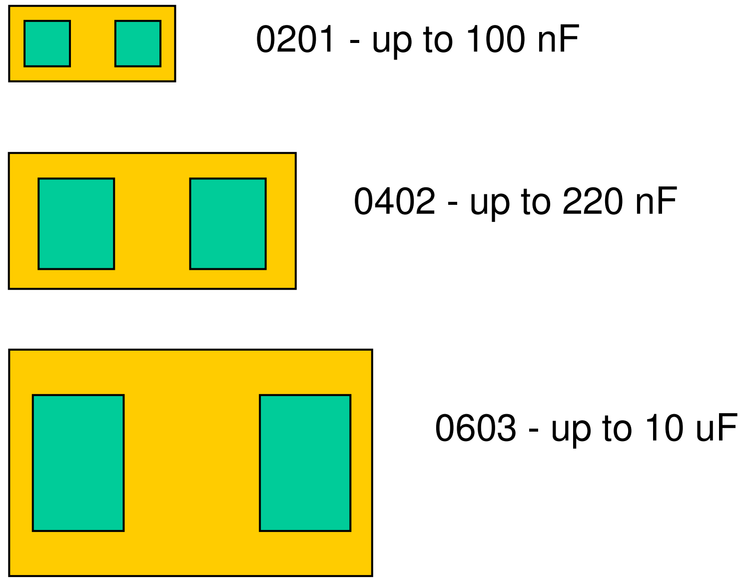
ok for relatively low frequency ripple, not effective for high frequencies

external capacitors also required

chip vs. passives size



approximately to scale

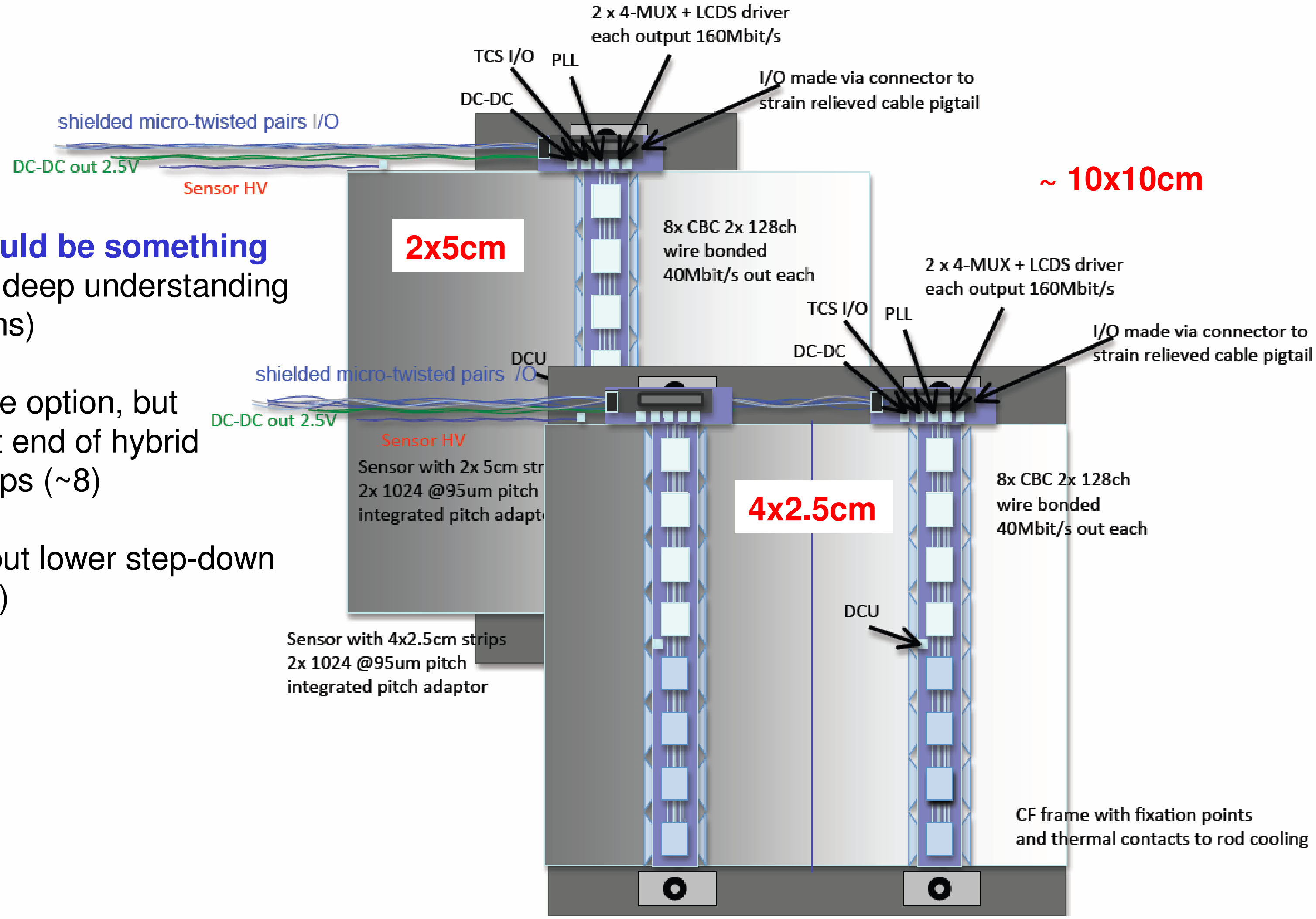


passives take space
don't want too many per chip

decoupling necessary – don't ignore

DC-DC / linear regulation on-chip will
add more passives

Progress in modelling modules for outer Tracker*



my preference would be something like this (without a deep understanding of all the implications)

either retain 2 stage option, but 2nd stage located at end of hybrid serving multiple chips (~8)

or just one stage, but lower step-down ratio (e.g. 6 -> ~1.2)

** from D.Abbaneo: http://indico.cern.ch/getFile.py/access?contribId=1&sessionId=2&resId=0&materialId=slides&confId=47298*

summary

CBC analogue front end has good tolerance to supply voltage variation (DC)

+/- 10% at least

PSR is a concern for single-ended input stage chip

20 nsec shaping has peak sensitivity at ~ 8 MHz

options to improve

design:	hard (… but haven't given up yet)
CMR:	relatively easy - but inherent HIPs sensitivity drawback
filtering:	relatively easy - can use good tolerance to lower analogue supply voltage to allow longer RC time constants