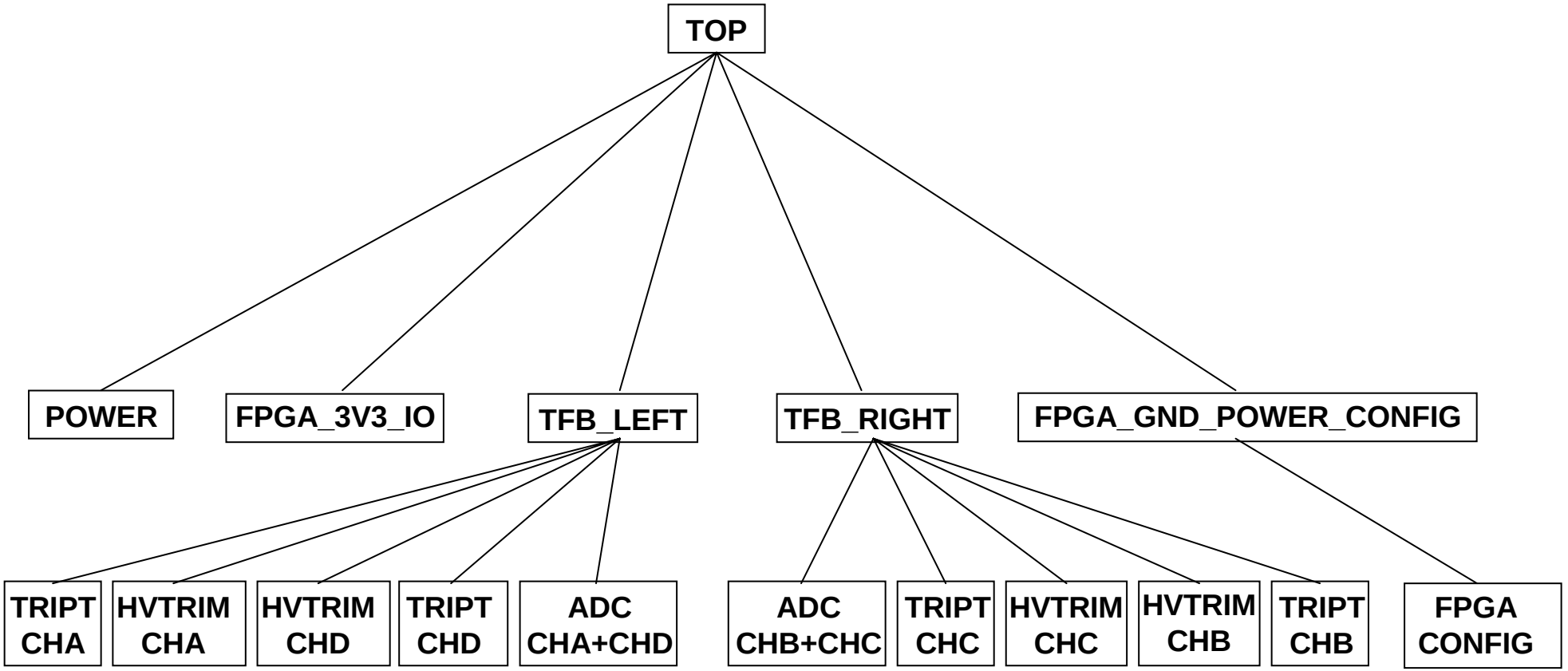
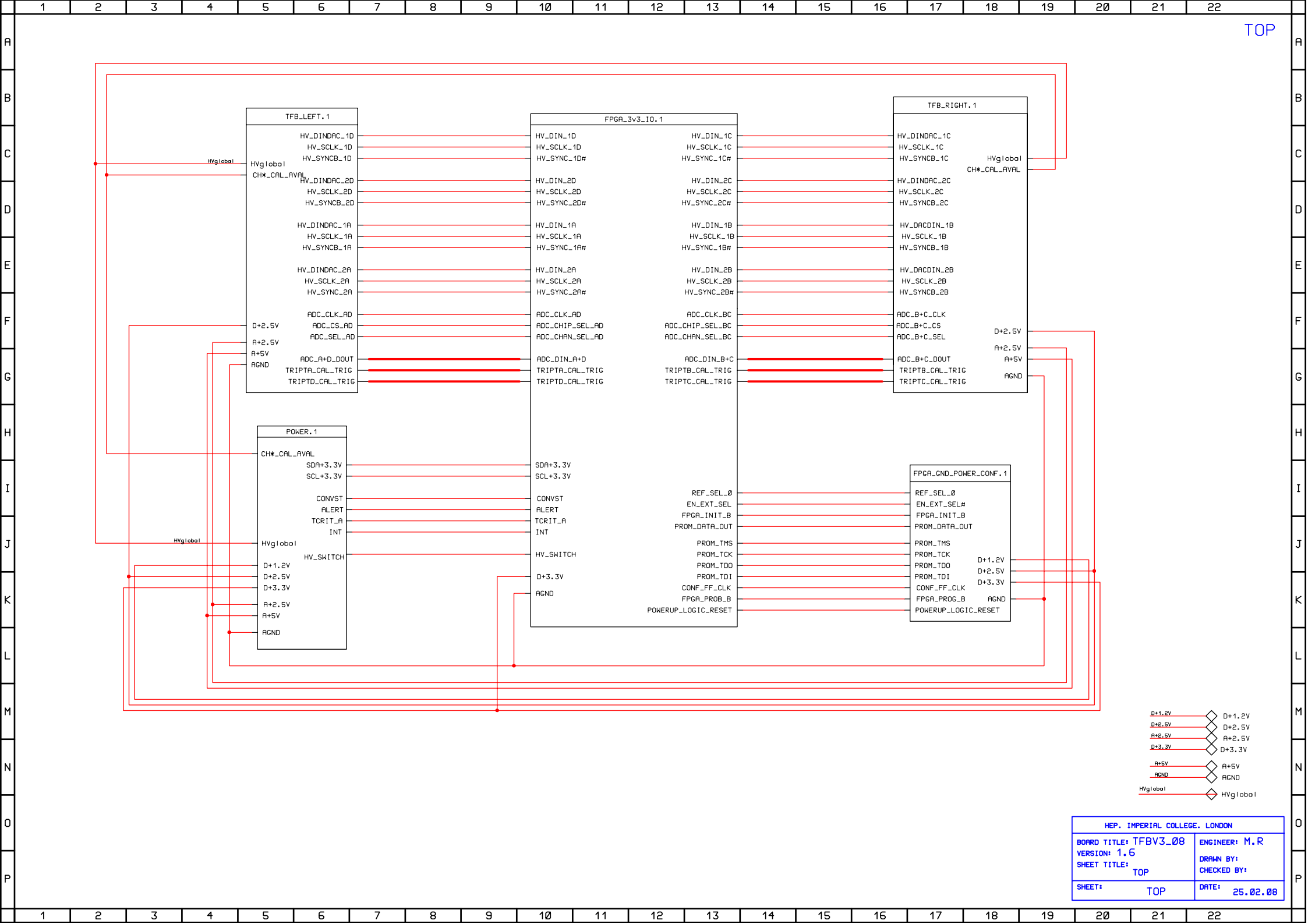
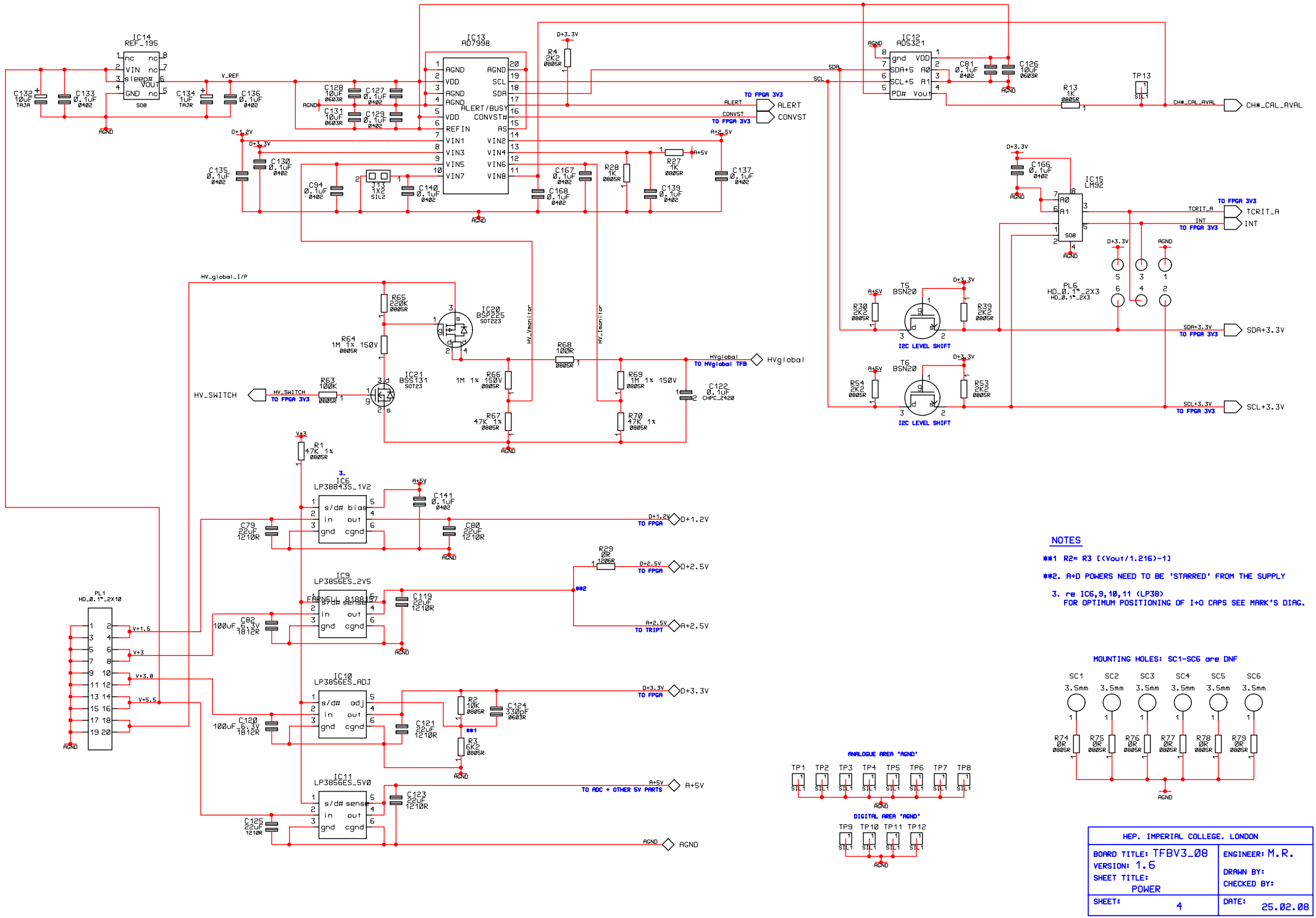

TOP
POWER
FPGA_3V3_IO
TFB_LEFT
TFB_RIGHT
FPGA_GND_POWER_CONFIG
TRIPT CHA
HVTRIM CHA
HVTRIM CHD
TRIPT CHD
ADC CHA+CHD
ADC CHB+CHC
TRIPT CHC
HVTRIM CHC
HVTRIM CHB
TRIPT CHB
FPGA CONFIG


TOP
TFB_LEFT.1
HV_DINDAC_1D
HV_SCLK_1D
HV_SYNCB_1D
HVglobal
CH*_CAL_AVAL
HV_DINDAC_2D
HV_SCLK_2D
HV_SYNCB_2D
HV_DINDAC_1A
HV_SCLK_1A
HV_SYNCB_1A
HV_DINDAC_2A
HV_SCLK_2A
HV_SYNC_2A
ADC_CLK_AD
D+2.5V
ADC_CS_AD
ADC_SEL_AD
A+2.5V
A+5V
AGND
ADC_A+D_DOUT
TRIPTA_CAL_TRIG
TRIPTD_CAL_TRIG
FPGA_3v3_IO.1
HV_DIN_1D
HV_SCLK_1D
HV_SYNC_1D#
HV_DIN_2D
HV_SCLK_2D
HV_SYNC_2D#
HV_DIN_1A
HV_SCLK_1A
HV_SYNC_1A#
HV_DIN_2A
HV_SCLK_2A
HV_SYNC_2A#
ADC_CLK_AD
ADC_CHIP_SEL_AD
ADC_CHAN_SEL_AD
ADC_DIN_A+D
TRIPTA_CAL_TRIG
TRIPTD_CAL_TRIG
HV_DIN_1C
HV_SCLK_1C
HV_SYNC_1C#
HV_DIN_2C
HV_SCLK_2C
HV_SYNC_2C#
HV_DIN_1B
HV_SCLK_1B
HV_SYNC_1B#
HV_DIN_2B
HV_SCLK_2B
HV_SYNC_2B#
ADC_CLK_BC
ADC_CHIP_SEL_BC
ADC_CHAN_SEL_BC
ADC_DIN_B+C
TRIPTB_CAL_TRIG
TRIPTC_CAL_TRIG
TFB_RIGHT.1
HV_DINDAC_1C
HV_SCLK_1C
HV_SYNCB_1C
HVglobal
CH*_CAL_AVAL
HV_DINDAC_2C
HV_SCLK_2C
HV_SYNCB_2C
HV_DACDIN_1B
HV_SCLK_1B
HV_SYNCB_1B
HV_DACDIN_2B
HV_SCLK_2B
HV_SYNCB_2B
ADC_B+C_CLK
ADC_B+C_CS
ADC_B+C_SEL
D+2.5V
A+2.5V
A+5V
AGND
ADC_B+C_DOUT
TRIPTB_CAL_TRIG
TRIPTC_CAL_TRIG
POWER.1
CH*_CAL_AVAL
SDA+3.3V
SCL+3.3V
CONVST
ALERT
TCRIT_A
INT
HVglobal
HV_SWITCH
D+1.2V
D+2.5V
D+3.3V
A+2.5V
A+5V
AGND
FPGA_GND_POWER_CONF.1
REF_SEL_0
EN_EXT_SEL
FPGA_INIT_B
PROM_DATA_OUT
PROM_TMS
PROM_TCK
PROM_TDO
PROM_TDI
CONF_FF_CLK
FPGA_PROG_B
POWERUP_LOGIC_RESET
D+1.2V
D+2.5V
D+3.3V
AGND
HEP. IMPERIAL COLLEGE. LONDON
BOARD TITLE: TFBV3_08
VERSION: 1.6
SHEET TITLE: TOP
ENGINEER: M.R
DRAWN BY:
CHECKED BY:
SHEET: TOP
DATE: 25.02.08

POWER



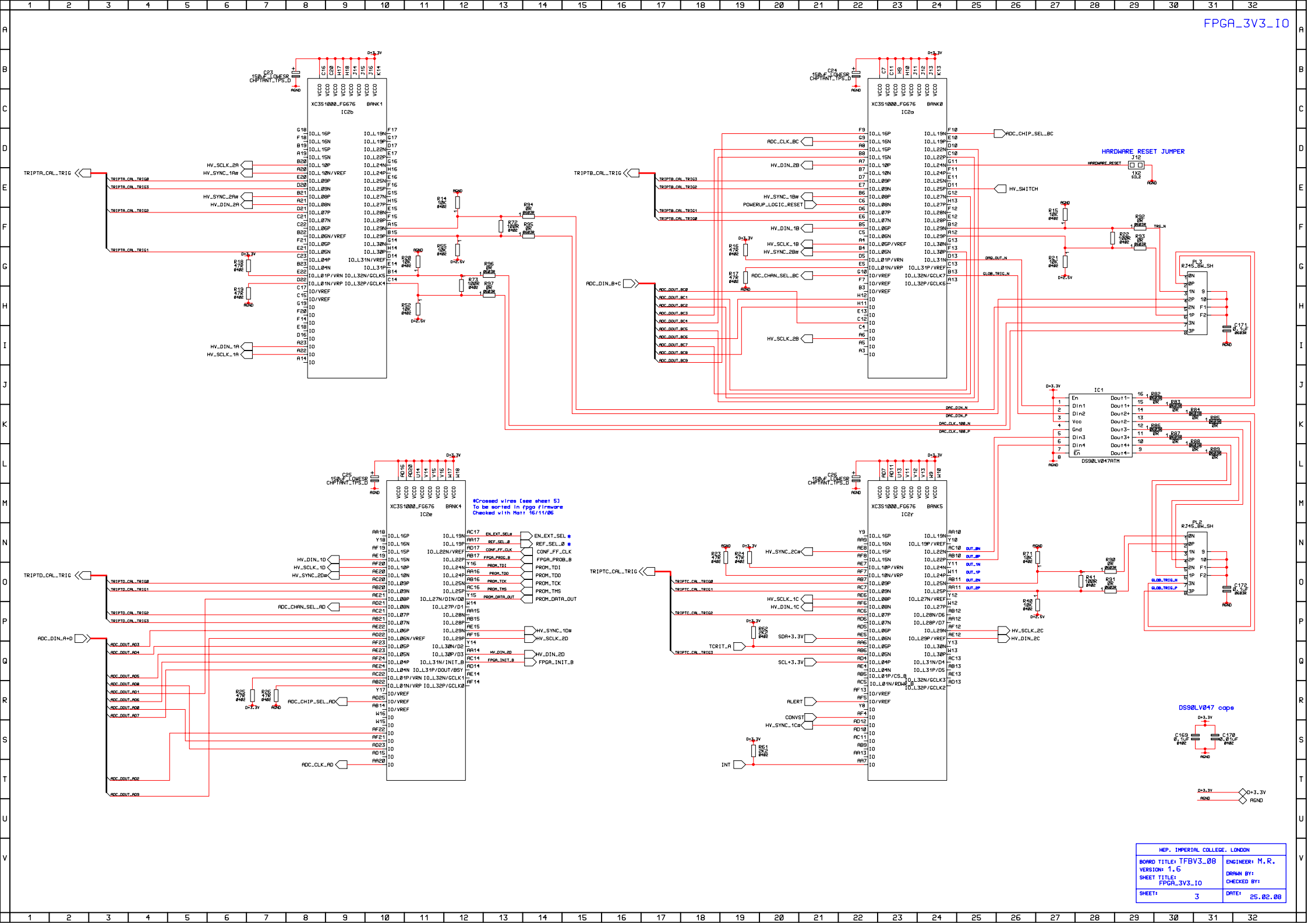
NOTES

**#1 R2= R3 [(Vout/1.216)-1]

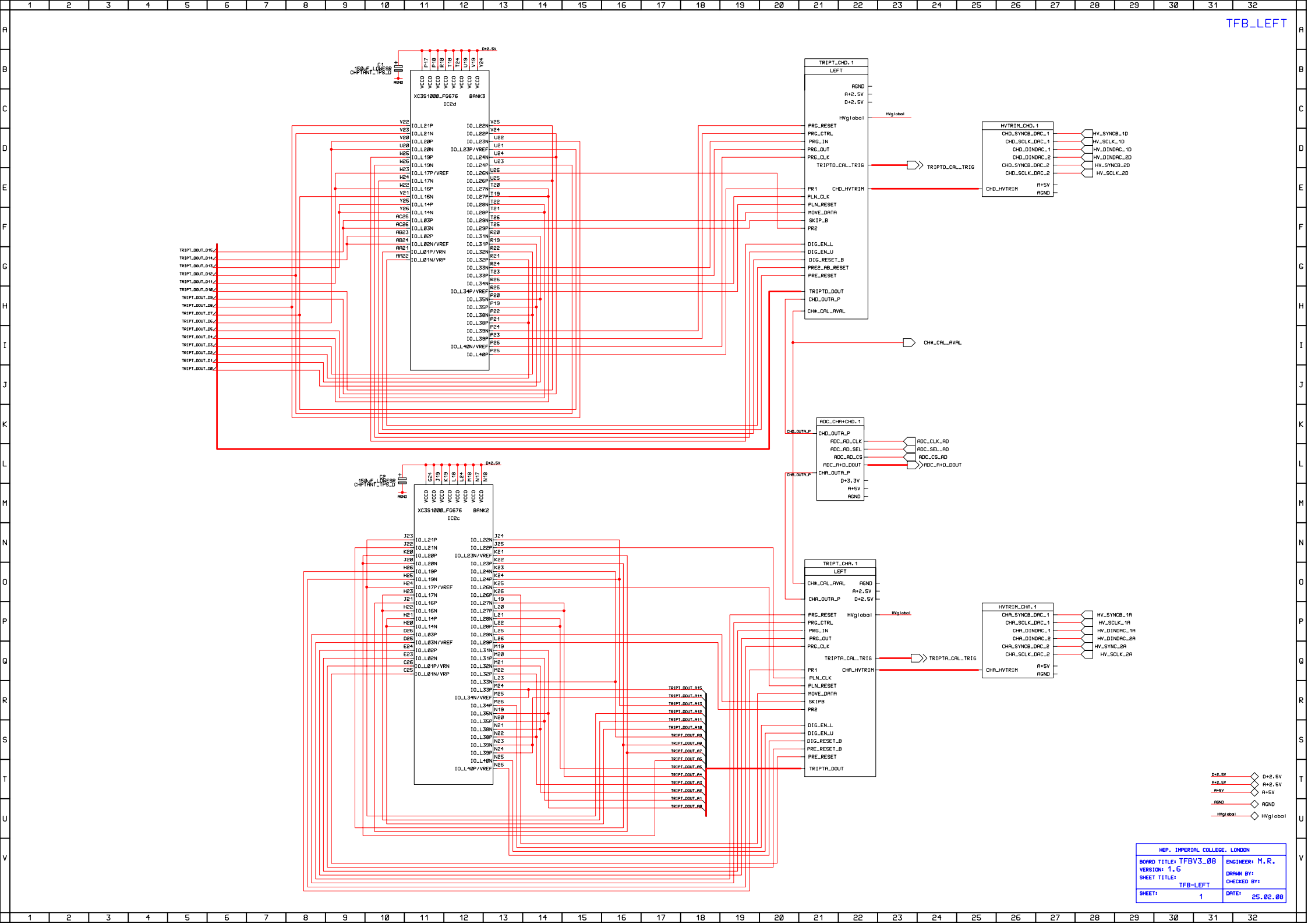
**#2. A+D POWERS NEED TO BE 'STARRED' FROM THE SUPPLY

3. re IC5,9,10,11 (LP38)
FOR OPTIMUM POSITIONING OF I+O CAPS SEE MARK'S DIAG.

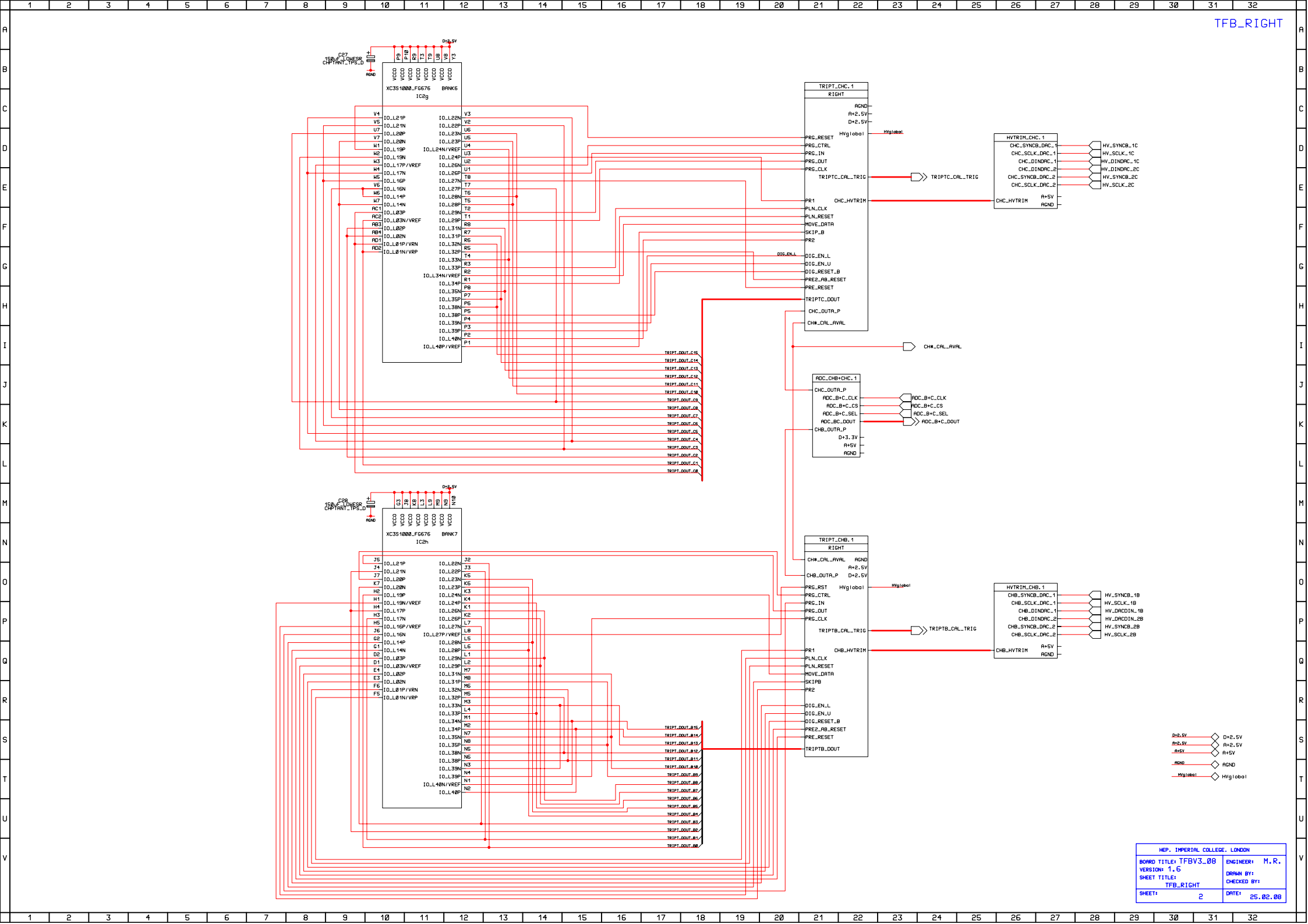
HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: POWER	ENGINEER: M.R. DRAWN BY: CHECKED BY:
SHEET: 4	DATE: 25.02.08



HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: FPGA_3V3_IO	ENGINEER: M.R. DRAWN BY: CHECKED BY:
SHEET: 3	DATE: 25.02.08

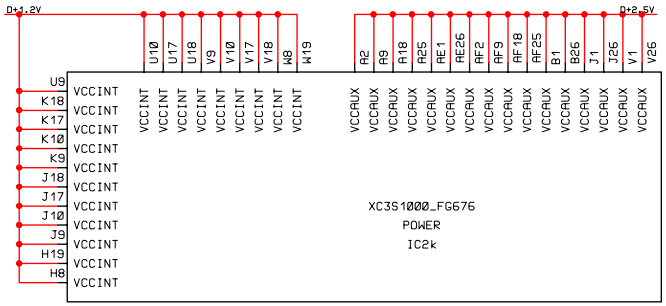

TFB_LEFT
C1
150uF_10VESR
CHIPTANT_TPS_D
D+2.5V
AGND
P17
P18
R18
T18
T24
U19
V19
V24
XC3S1000_FG676
BANK3
IC2d
VCCO
IO_L21P
IO_L21N
IO_L20P
IO_L20N
IO_L19P
IO_L19N
IO_L17P/VREF
IO_L17N
IO_L16P
IO_L16N
IO_L14P
IO_L14N
IO_L03P
IO_L03N
IO_L02P
IO_L02N/VREF
IO_L01P/VRN
IO_L01N/VRP
IO_L22N
IO_L22P
IO_L23N
IO_L23P/VREF
IO_L24N
IO_L24P
IO_L26N
IO_L26P
IO_L27N
IO_L27P
IO_L28N
IO_L28P
IO_L29N
IO_L29P
IO_L31N
IO_L31P
IO_L32N
IO_L32P
IO_L33N
IO_L33P
IO_L34N
IO_L34P/VREF
IO_L35N
IO_L35P
IO_L38N
IO_L38P
IO_L39N
IO_L39P
IO_L40N/VREF
IO_L40P
TRIPT_DOUT_D15
TRIPT_DOUT_D14
TRIPT_DOUT_D13
TRIPT_DOUT_D12
TRIPT_DOUT_D11
TRIPT_DOUT_D10
TRIPT_DOUT_D9
TRIPT_DOUT_D8
TRIPT_DOUT_D7
TRIPT_DOUT_D6
TRIPT_DOUT_D5
TRIPT_DOUT_D4
TRIPT_DOUT_D3
TRIPT_DOUT_D2
TRIPT_DOUT_D1
TRIPT_DOUT_D0
TRIPT_CHD.1
LEFT
AGND
A+2.5V
D+2.5V
HVglobal
PRG_RESET
PRG_CTRL
PRG_IN
PRG_OUT
PRG_CLK
TRIPTD_CAL_TRIG
PR1
CHD_HVTRIM
PLN_CLK
PLN_RESET
MOVE_DATA
SKIP_B
PR2
DIG_EN_L
DIG_EN_U
DIG_RESET_B
PRE2_AB_RESET
PRE_RESET
TRIPTD_DOUT
CHD_OUTA_P
CH#_CAL_AVAL
HVTRIM_CHD.1
CHD_SYNCB_DAC_1
CHD_SCLK_DAC_1
CHD_DINDAC_1
CHD_DINDAC_2
CHD_SYNCB_DAC_2
CHD_SCLK_DAC_2
A+5V
HV_SYNCB_1D
HV_SCLK_1D
HV_DINDAC_1D
HV_DINDAC_2D
HV_SYNCB_2D
HV_SCLK_2D
ADC_CHA+CHD.1
ADC_AD_CLK
ADC_AD_SEL
ADC_AD_CS
ADC_A+D_DOUT
D+3.3V
ADC_CLK_AD
ADC_SEL_AD
ADC_CS_AD
ADC_A+D_DOUT
C2
150uF_10VESR
CHIPTANT_TPS_D
G24
J19
K19
L18
L24
M18
N17
N18
XC3S1000_FG676
BANK2
IC2c
IO_L21P
IO_L21N
IO_L20P
IO_L20N
IO_L19P
IO_L19N
IO_L17P/VREF
IO_L17N
IO_L16P
IO_L16N
IO_L14P
IO_L14N
IO_L03P
IO_L03N/VREF
IO_L02P
IO_L02N
IO_L01P/VRN
IO_L01N/VRP
IO_L22N
IO_L22P
IO_L23N/VREF
IO_L23P
IO_L24N
IO_L24P
IO_L26N
IO_L26P
IO_L27N
IO_L27P
IO_L28N
IO_L28P
IO_L29N
IO_L29P
IO_L31N
IO_L31P
IO_L32N
IO_L32P
IO_L33N
IO_L33P
IO_L34N/VREF
IO_L34P
IO_L35N
IO_L35P
IO_L38N
IO_L38P
IO_L39N
IO_L39P
IO_L40N
IO_L40P/VREF
TRIPT_DOUT_A15
TRIPT_DOUT_A14
TRIPT_DOUT_A13
TRIPT_DOUT_A12
TRIPT_DOUT_A11
TRIPT_DOUT_A10
TRIPT_DOUT_A9
TRIPT_DOUT_A8
TRIPT_DOUT_A7
TRIPT_DOUT_A6
TRIPT_DOUT_A5
TRIPT_DOUT_A4
TRIPT_DOUT_A3
TRIPT_DOUT_A2
TRIPT_DOUT_A1
TRIPT_DOUT_A0
TRIPT_CHA.1
LEFT
CH#_CAL_AVAL
CHA_OUTA_P
PRG_RESET
PRG_CTRL
PRG_IN
PRG_OUT
PRG_CLK
TRIPTA_CAL_TRIG
PR1
CHA_HVTRIM
PLN_CLK
PLN_RESET
MOVE_DATA
SKIPB
PR2
DIG_EN_L
DIG_EN_U
DIG_RESET_B
PRE_RESET_B
PRE_RESET
TRIPTA_DOUT
HVTRIM_CHA.1
CHA_SYNCB_DAC_1
CHA_SCLK_DAC_1
CHA_DINDAC_1
CHA_DINDAC_2
CHA_SYNCB_DAC_2
CHA_SCLK_DAC_2
HV_SYNCB_1A
HV_SCLK_1A
HV_DINDAC_1A
HV_DINDAC_2A
HV_SYNC_2A
HV_SCLK_2A
D+2.5V
A+2.5V
A+5V
AGND
HVglobal
HEP. IMPERIAL COLLEGE. LONDON
BOARD TITLE: TFBV3_08
VERSION: 1.6
SHEET TITLE:
TFB-LEFT
SHEET: 1
ENGINEER: M.R.
DRAWN BY:
CHECKED BY:
DATE: 25.02.08

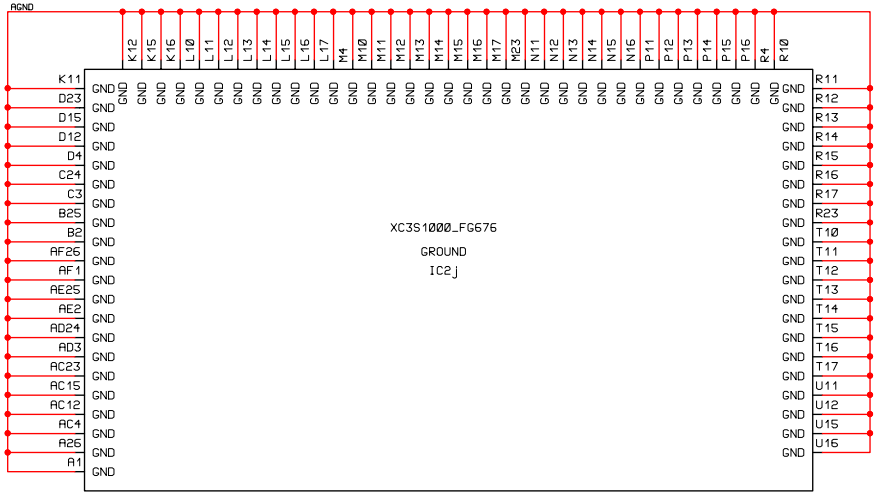
TFB_RIGHT

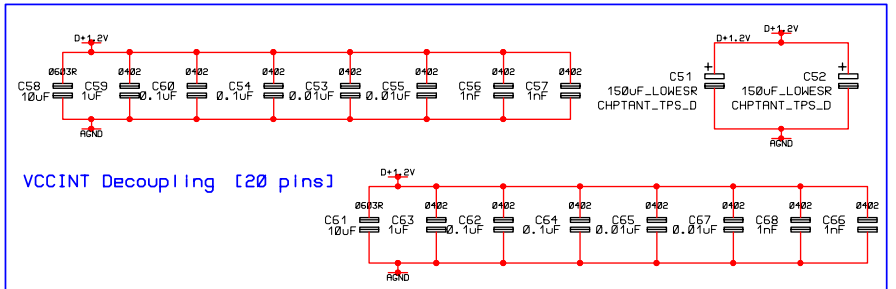


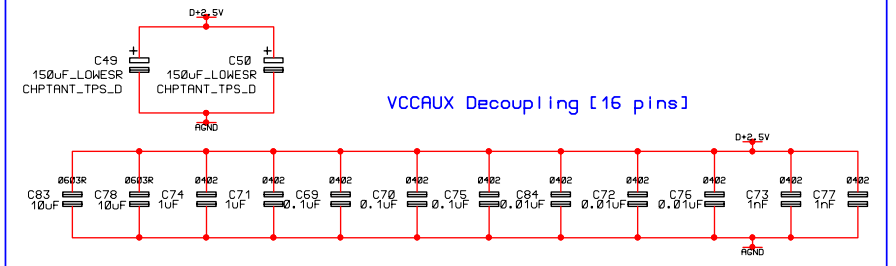
HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08	ENGINEER: M.R.
VERSION: 1.6	DRAWN BY:
SHEET TITLE: TFB_RIGHT	CHECKED BY:
SHEET: 2	DATE: 25.02.08

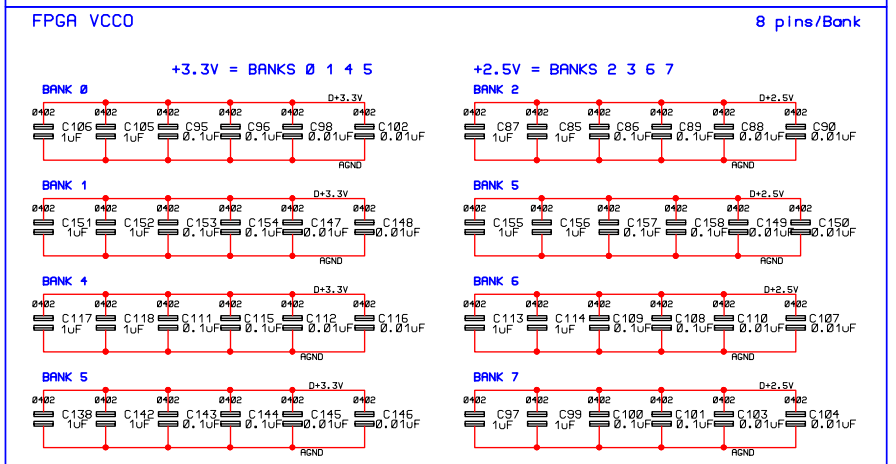
FPGA_GND_POWER_CONF



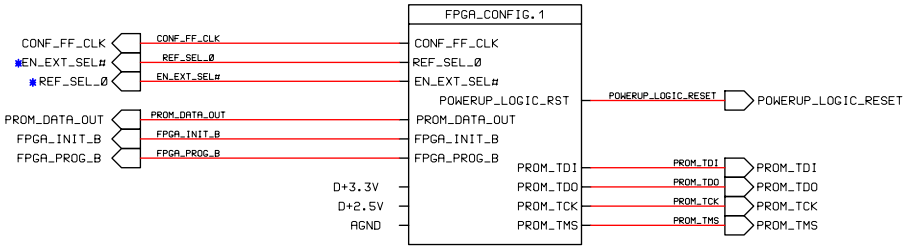


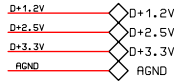






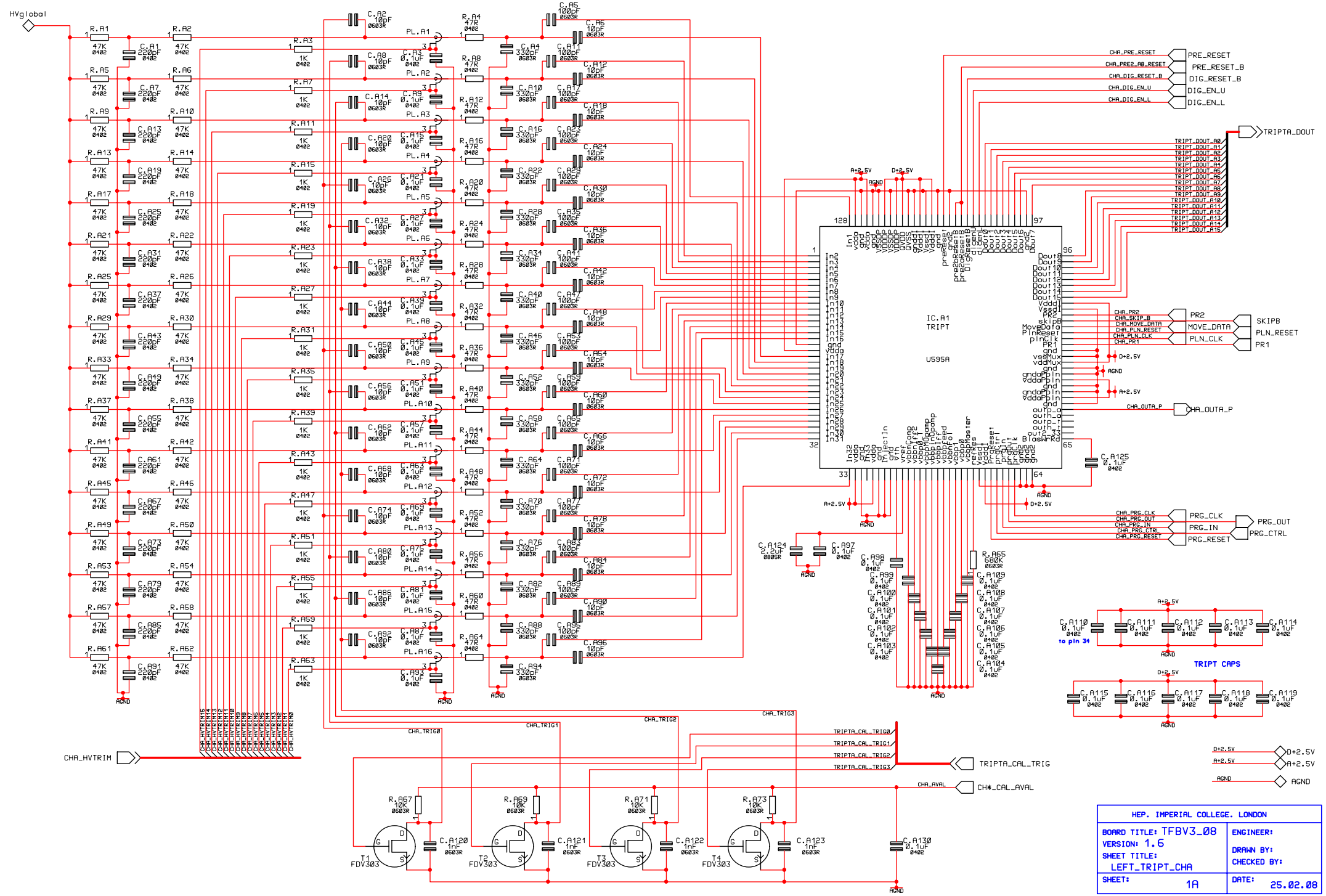
*Crossed wires
To be sorted in fpga firmware
Checked with Matt 16/11/06



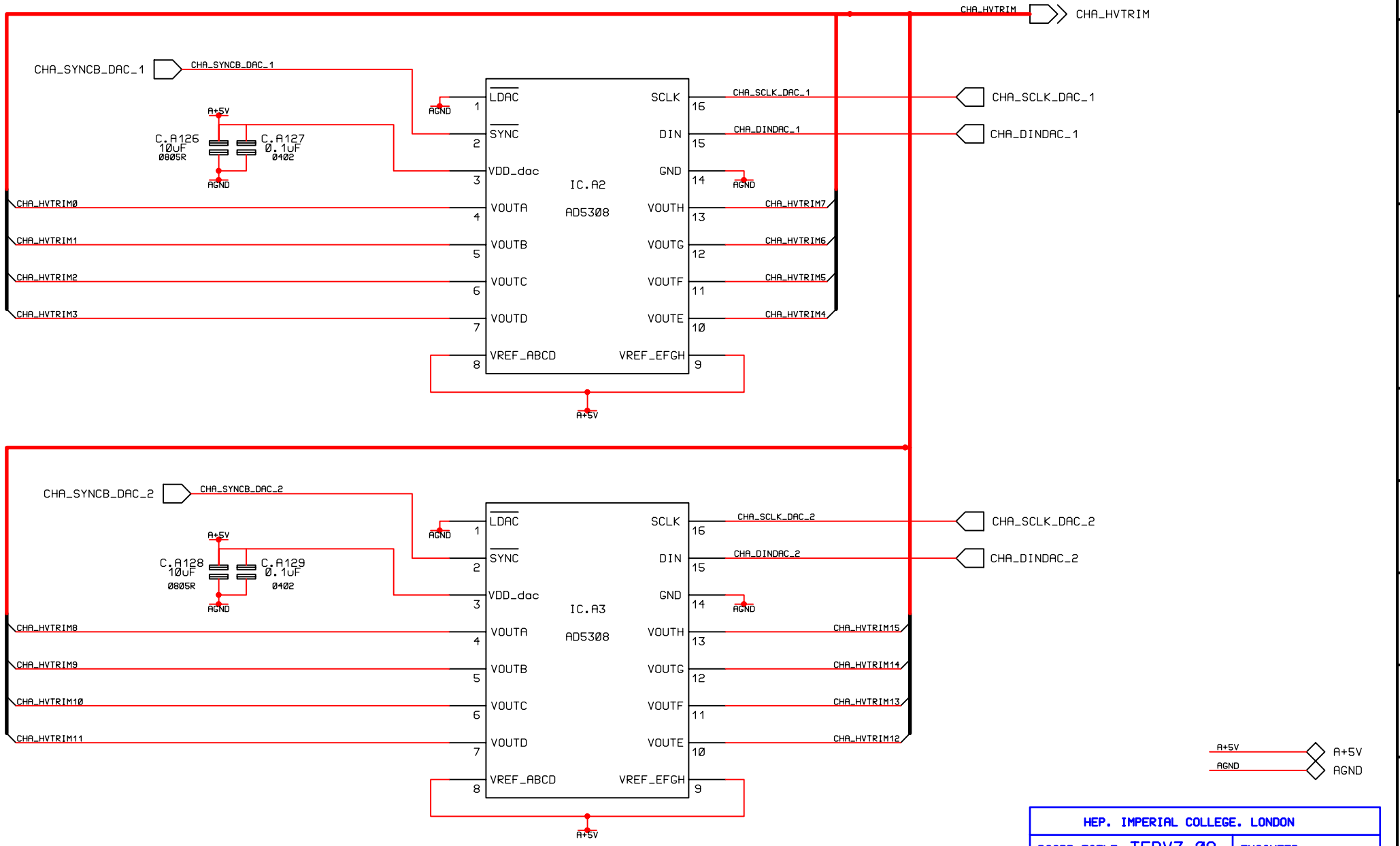


HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: FPGA_GND_POWER_CONF	ENGINEER: M.R. DRAWN BY: CHECKED BY:
SHEET: 5	DATE: 25.02.08

LEFT_TRIPT_CHA

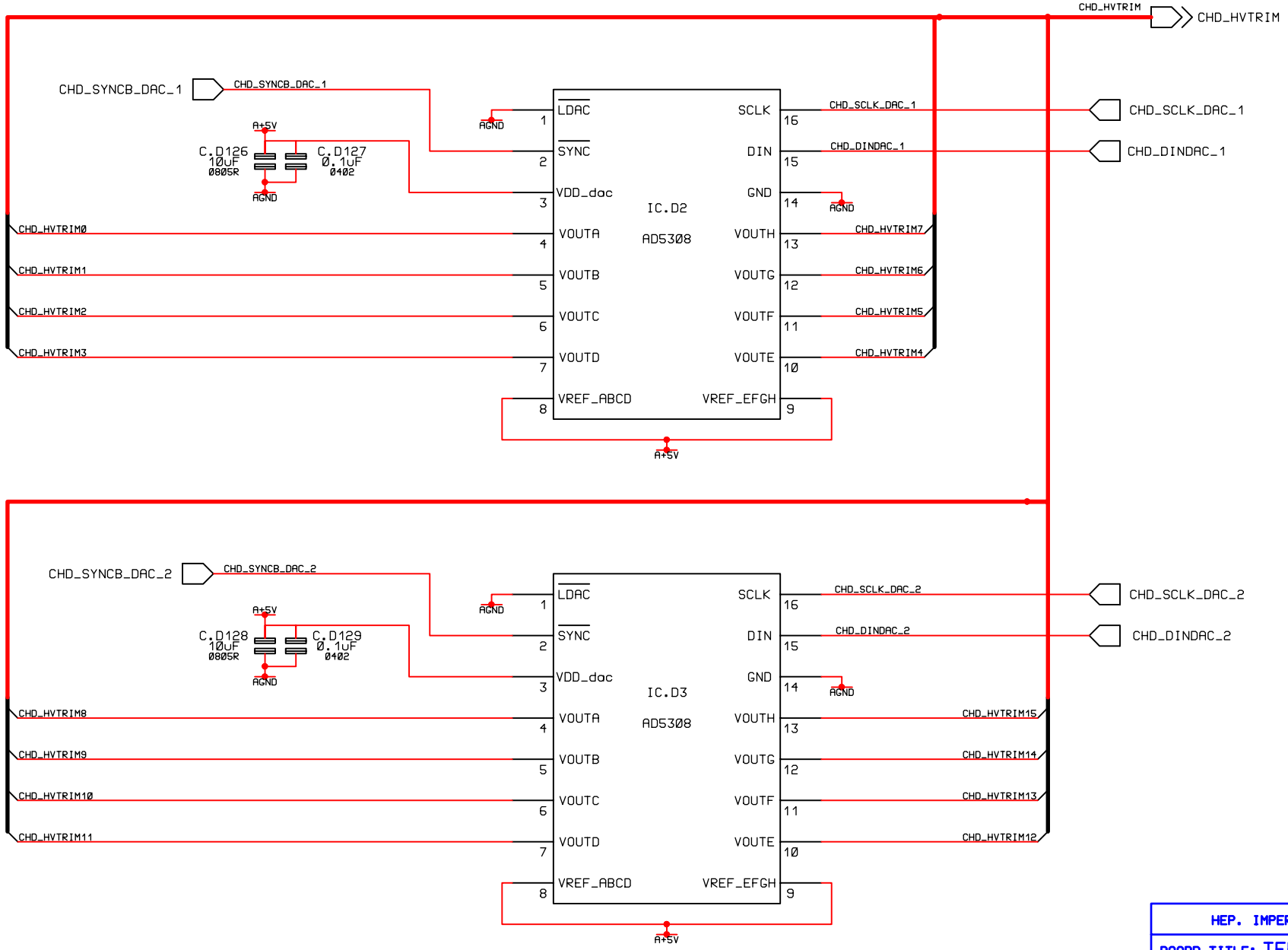


LEFT_HVTRIM_CHA

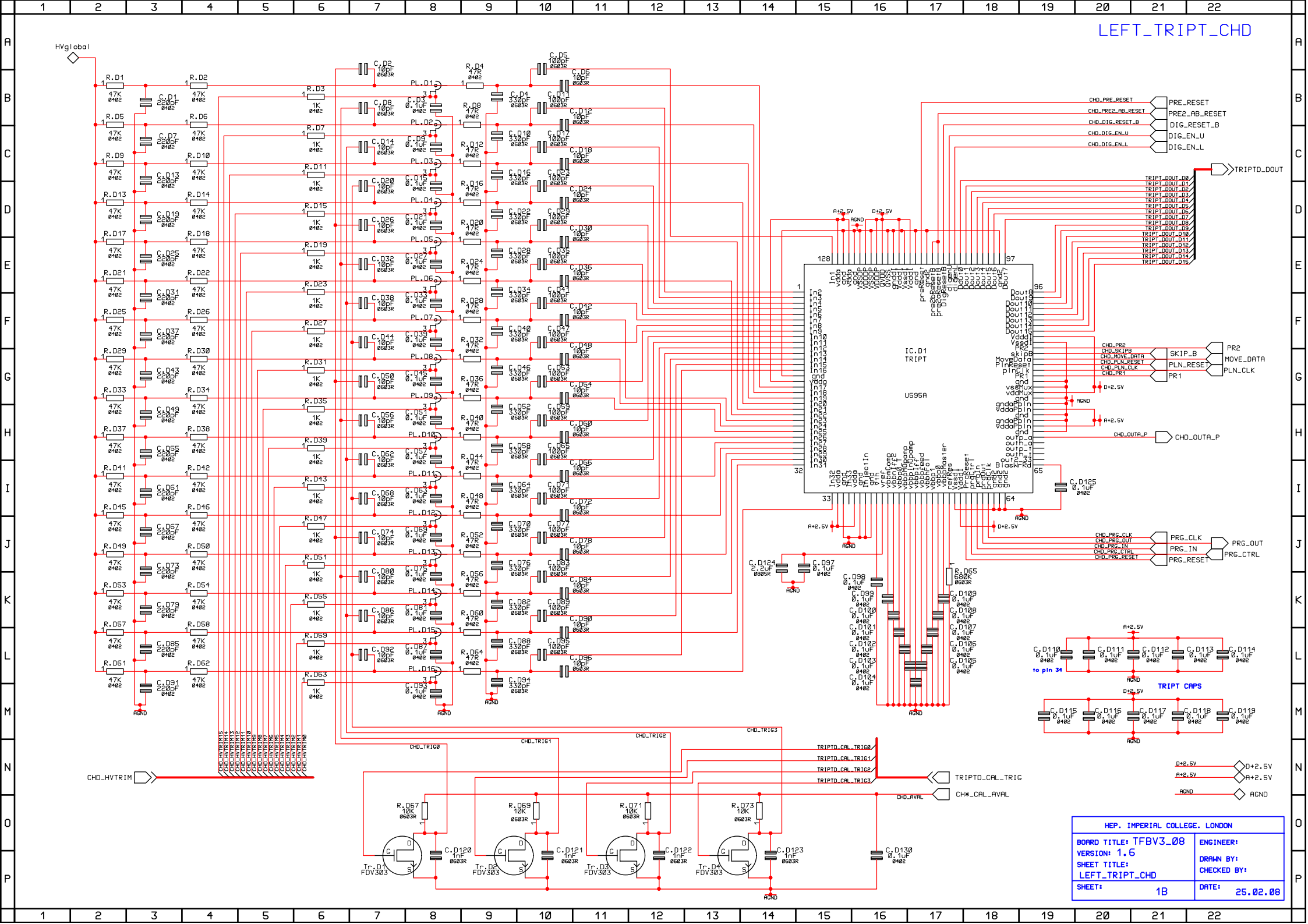


HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: HVTRIM_CHA	ENGINEER: DRAWN BY: CHECKED BY:
SHEET: 1C	DATE: 25.02.08

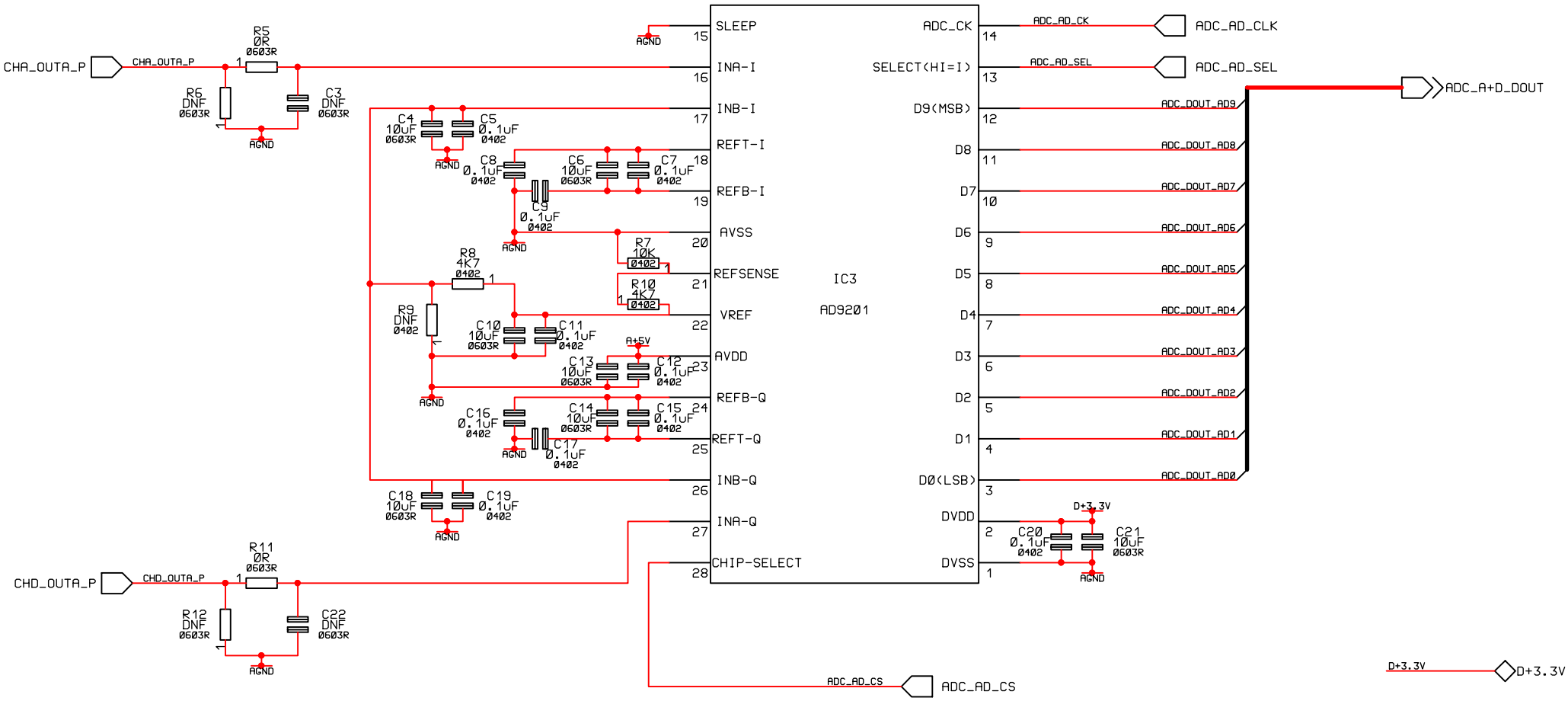
LEFT_HVTRIM_CHD



HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: HVTRIM_CHD	ENGINEER: DRAWN BY: CHECKED BY:
SHEET: 1D	DATE: 25.02.08

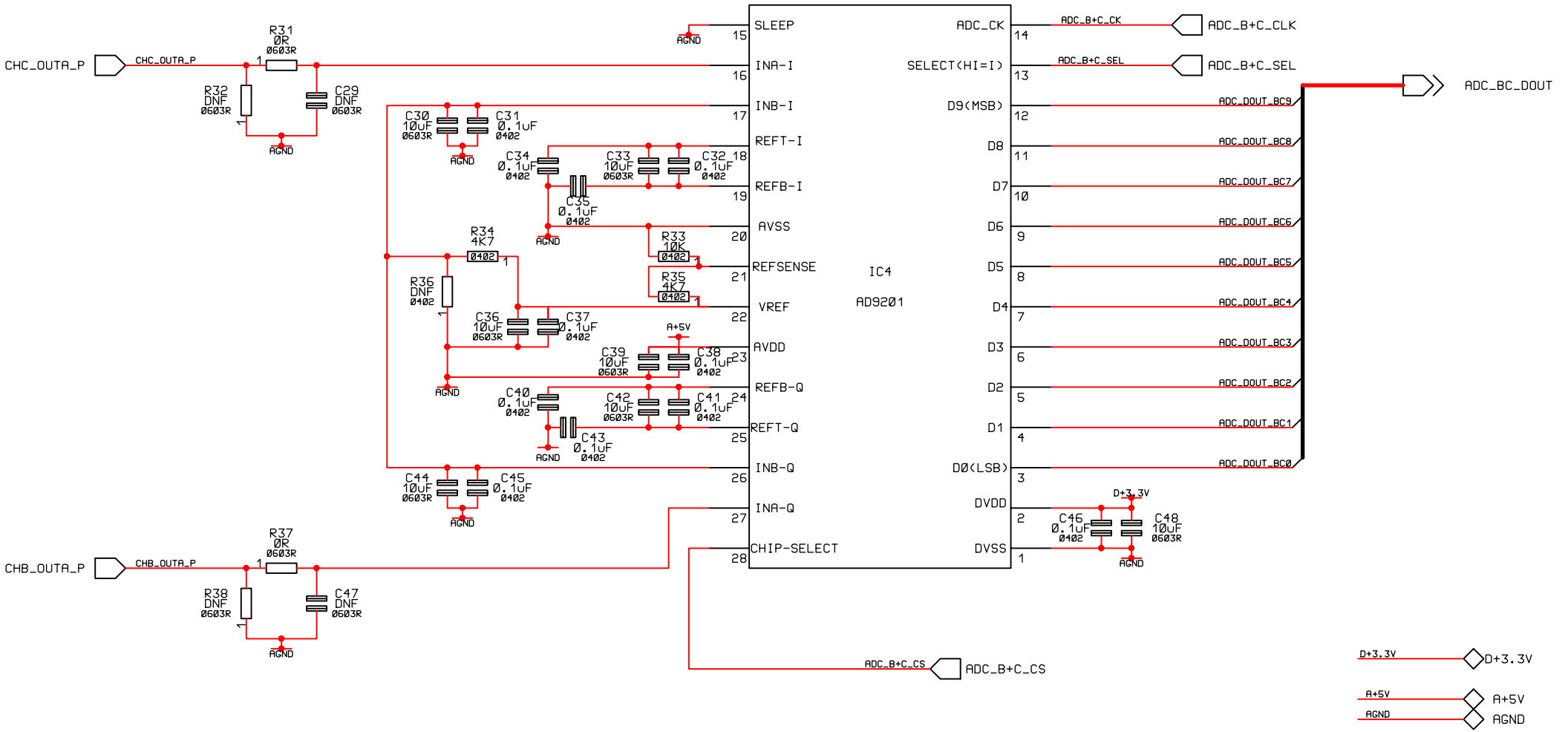

LEFT_TRIPT_CHD
HVglobal
IC.D1
TRIPT
U595A
CHD_HVTRIM
TRIPTD_DOUT
TRIPTD_CAL_TRIG
CH*_CAL_AVAL
TRIPT CAPS
HEP. IMPERIAL COLLEGE. LONDON
BOARD TITLE: TFBV3_08
VERSION: 1.6
SHEET TITLE:
LEFT_TRIPT_CHD
SHEET: 1B
ENGINEER:
DRAWN BY:
CHECKED BY:
DATE: 25.02.08

LEFT ADC_CHA+CHD



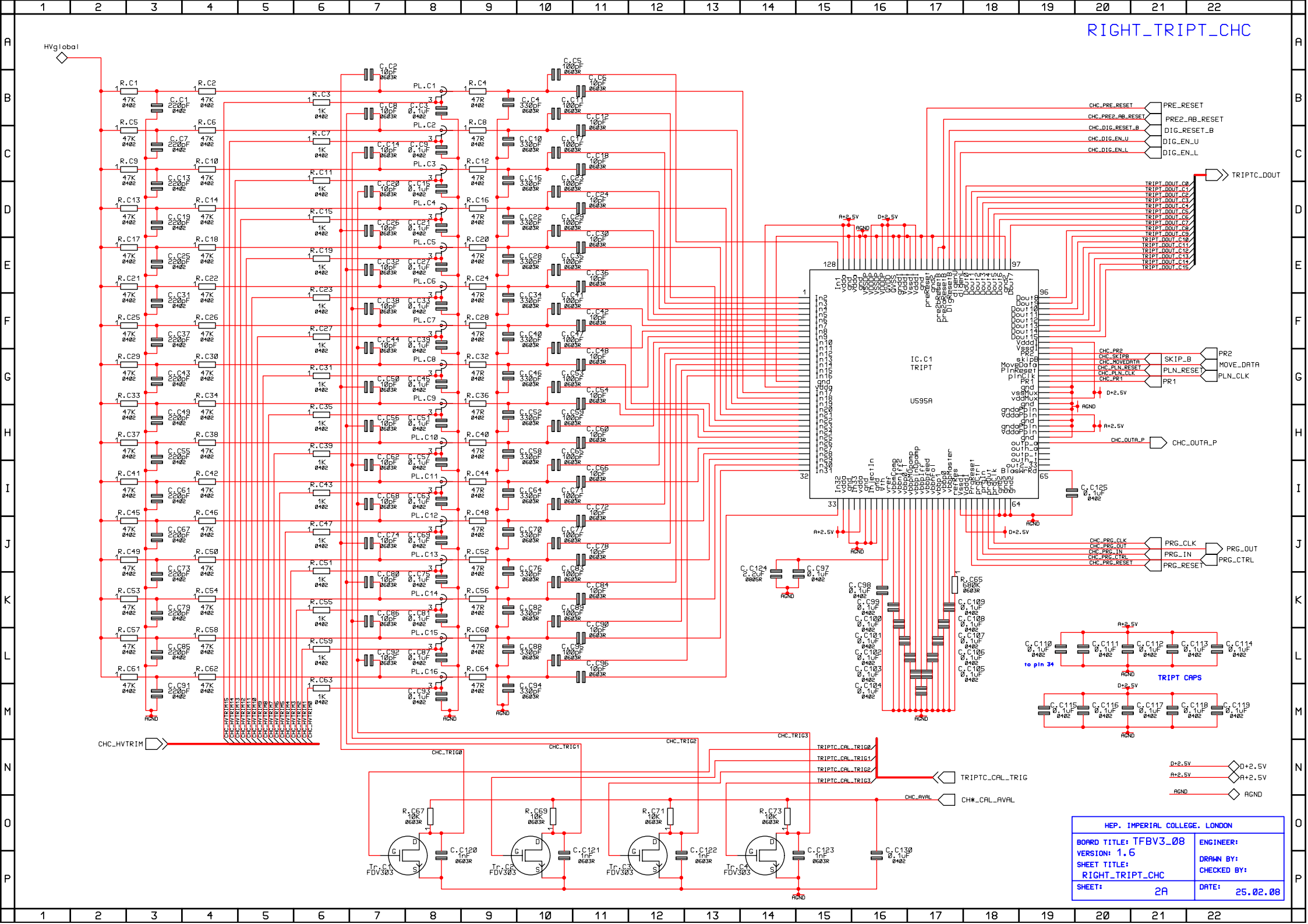
HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: ADC_CHA+CHD	ENGINEER: DRAWN BY: CHECKED BY:
SHEET: 1E	DATE: 25.02.08

RIGHT ADC_CHB+CHC

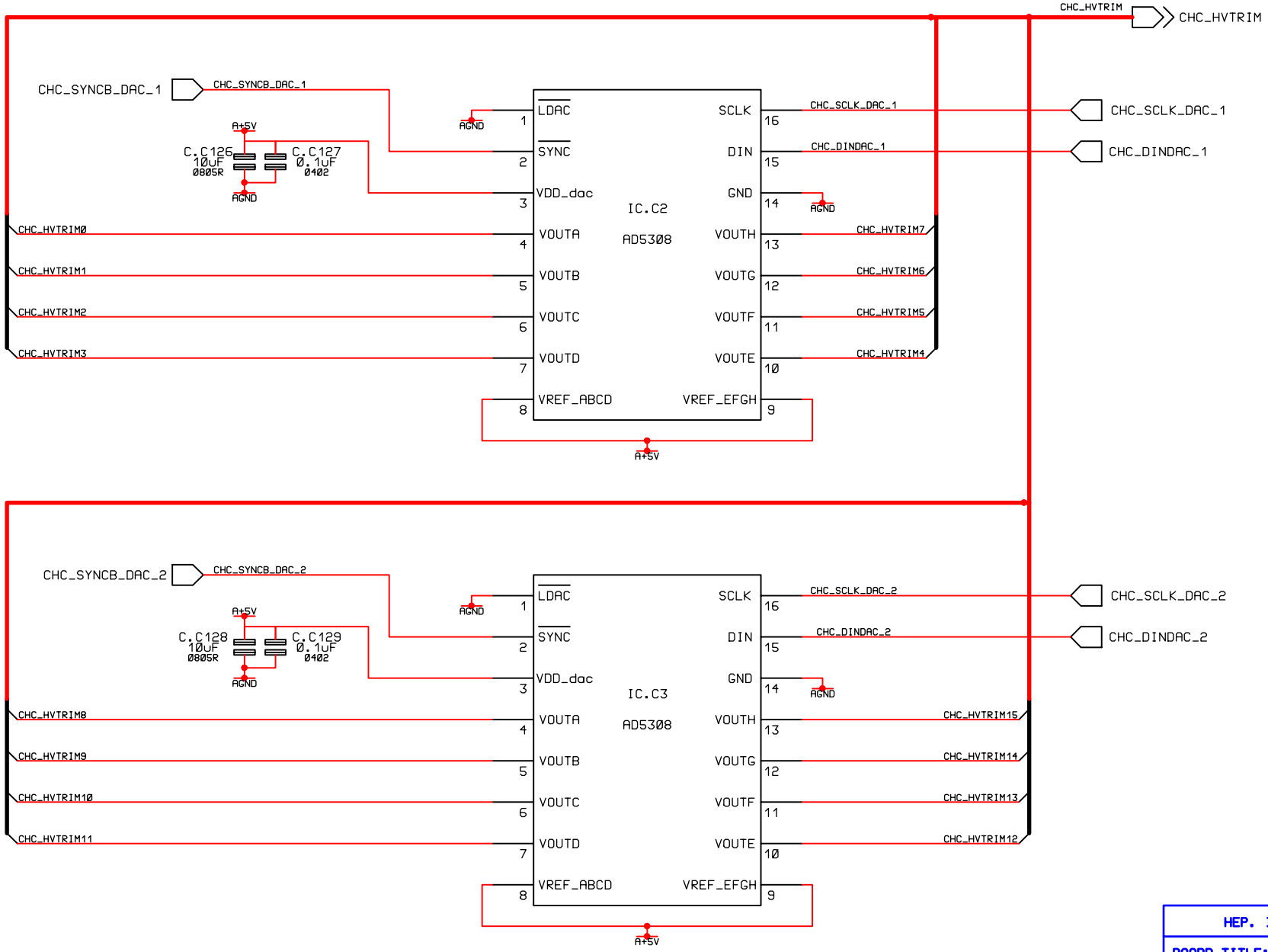


HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: ADC_CHB+CHC	ENGINEER: DRAWN BY: CHECKED BY:
SHEET: 2E	DATE: 25.02.08

RIGHT_TRIPT_CHC

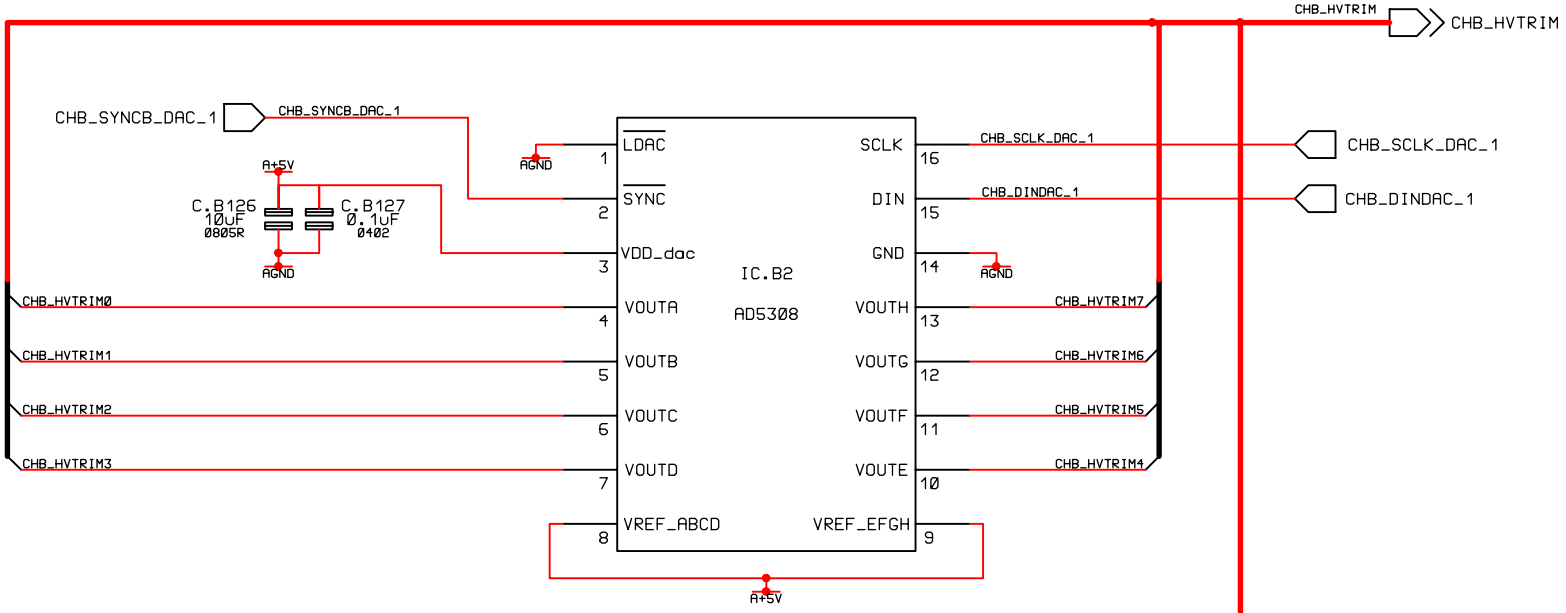


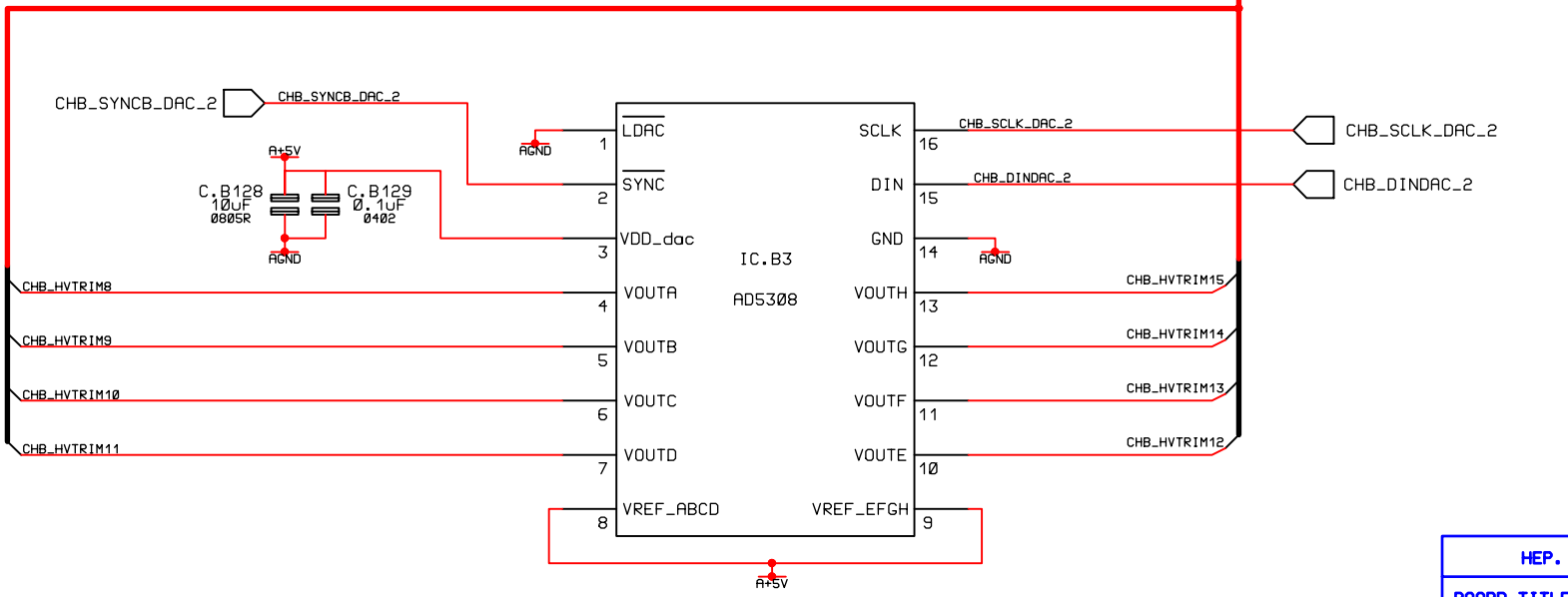
RIGHT_HVTRIM_CHC

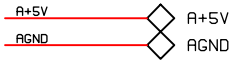


HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: HVTRIM_CHC	ENGINEER: DRAWN BY: CHECKED BY:
SHEET: 2D	DATE: 25.02.08

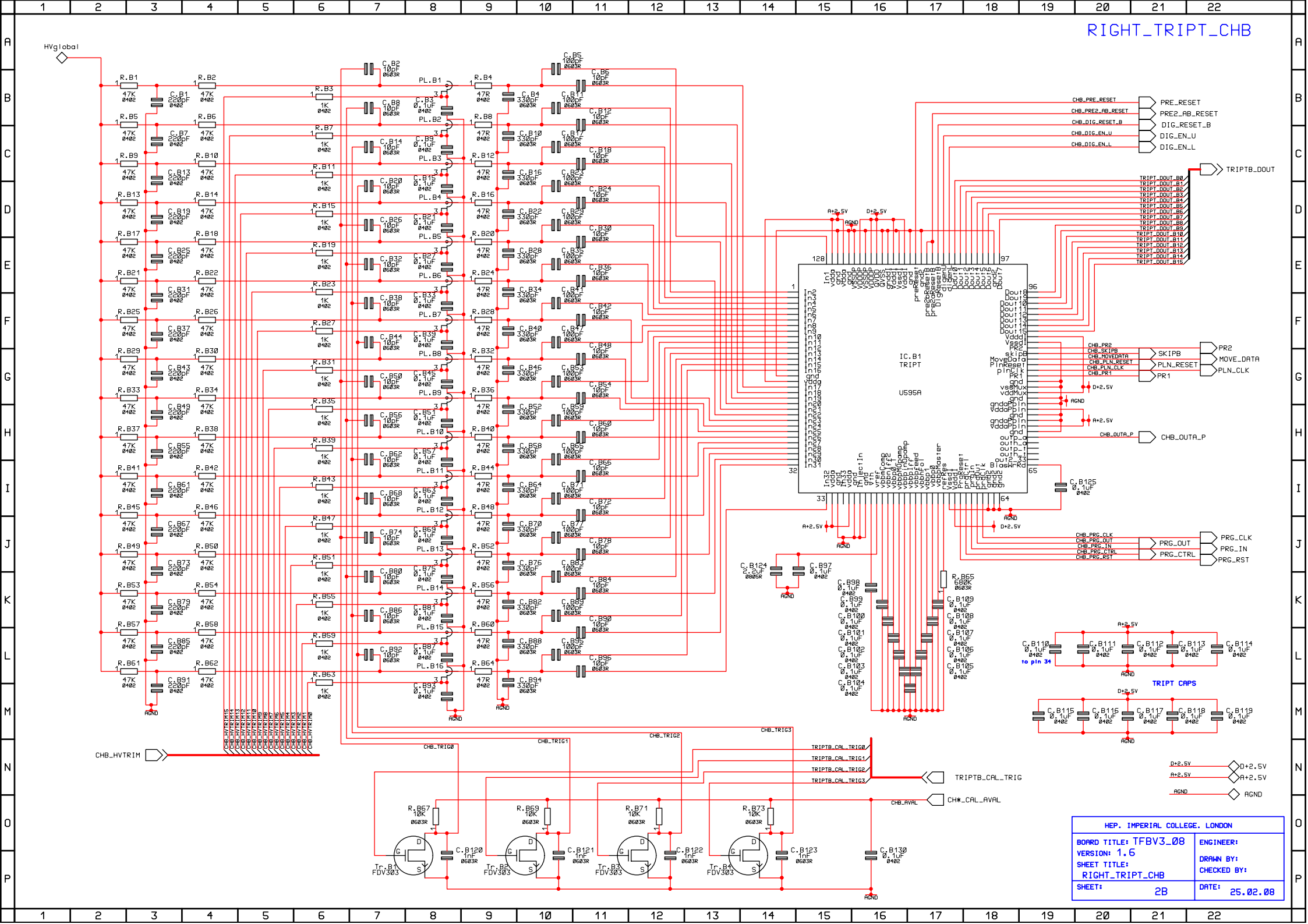
RIGHT_HVTRIM_CHB



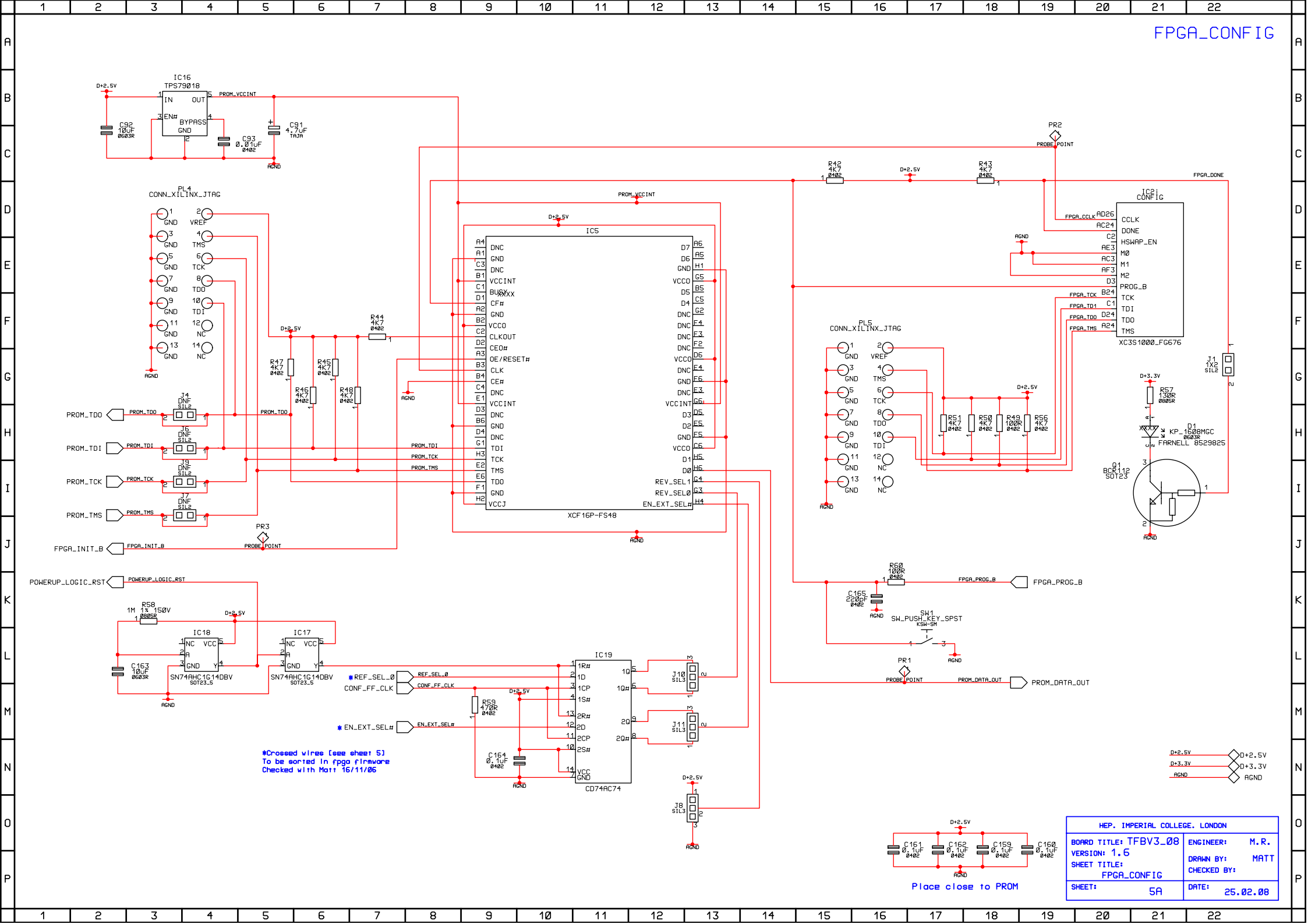




HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08 VERSION: 1.6 SHEET TITLE: HVTRIM_CHB	ENGINEER: DRAWN BY: CHECKED BY:
SHEET: 2C	DATE: 25.02.08


RIGHT_TRIPT_CHB
HVglobal
CHB_HVTRIM
IC.B1
TRIPT
U595A
TRIPTB_DOUT
TRIPTB_CAL_TRIG
CH*_CAL_AVAL
PRE_RESET
PRE2_AB_RESET
DIG_RESET_B
DIG_EN_U
DIG_EN_L
SKIPB
PLN_RESET
PR1
PR2
MOVE_DATA
PLN_CLK
CHB_OUTA_P
PRG_CLK
PRG_IN
PRG_RST
PRG_OUT
PRG_CTRL
TRIPT CAPS
HEP. IMPERIAL COLLEGE. LONDON
BOARD TITLE: TFBV3_08
VERSION: 1.6
SHEET TITLE:
RIGHT_TRIPT_CHB
SHEET: 2B
ENGINEER:
DRAWN BY:
CHECKED BY:
DATE: 25.02.08

FPGA_CONFIG



HEP. IMPERIAL COLLEGE. LONDON	
BOARD TITLE: TFBV3_08	ENGINEER: M.R.
VERSION: 1.6	DRAWN BY: MATT
SHEET TITLE: FPGA_CONFIG	CHECKED BY:
SHEET: 5A	DATE: 25.02.08