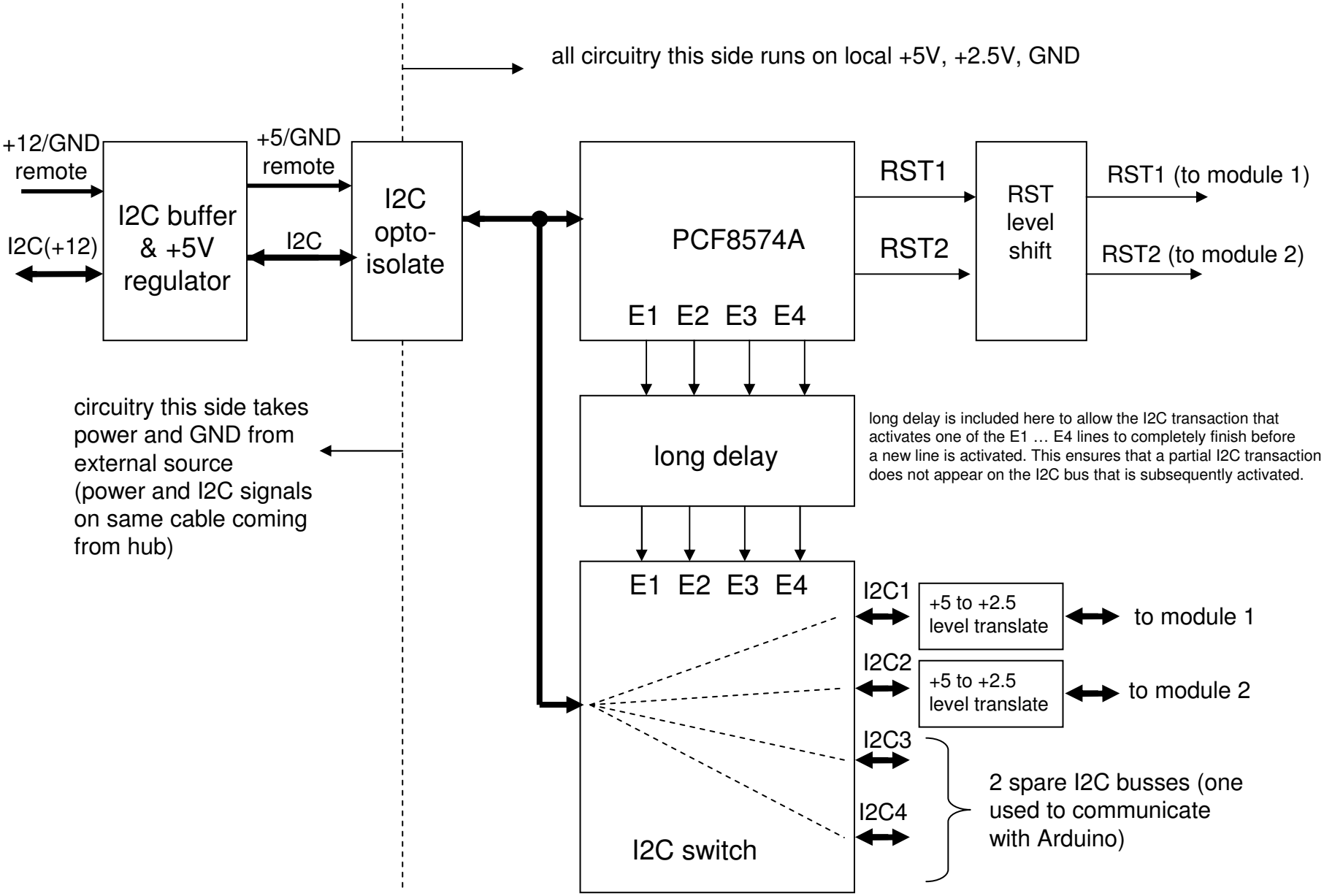
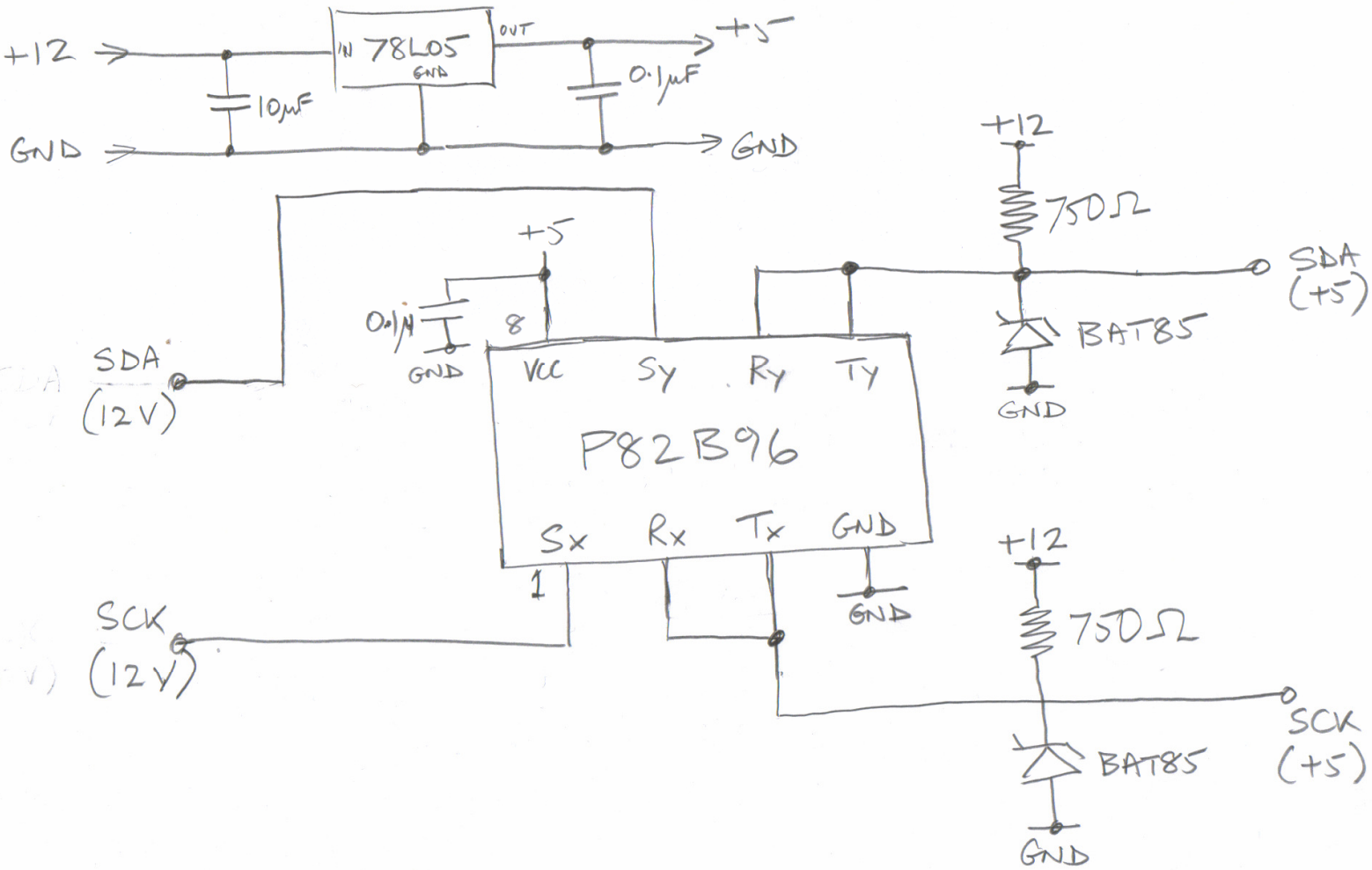
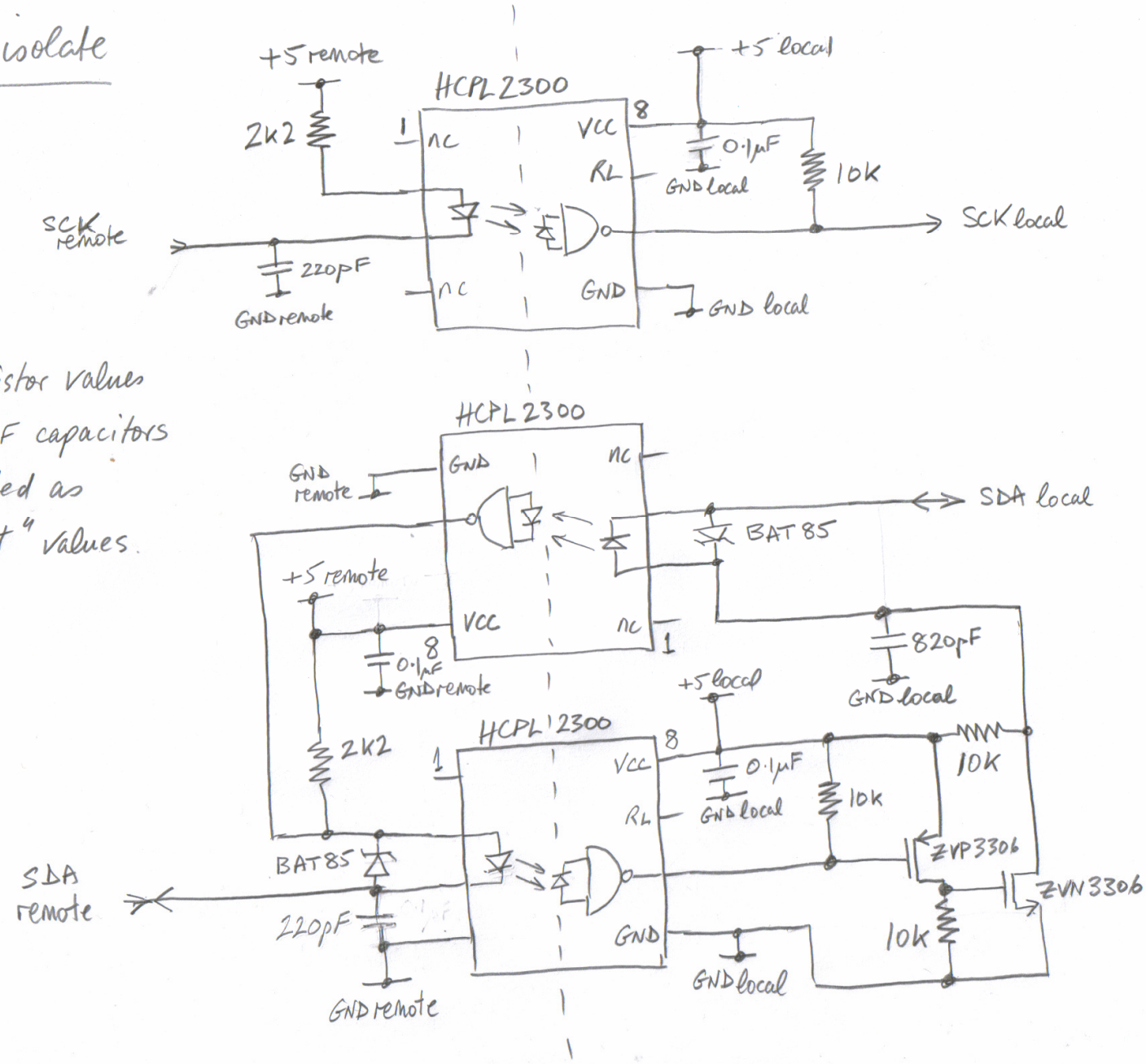
I2C circuitry within XY plane enclosure



I²C buffer

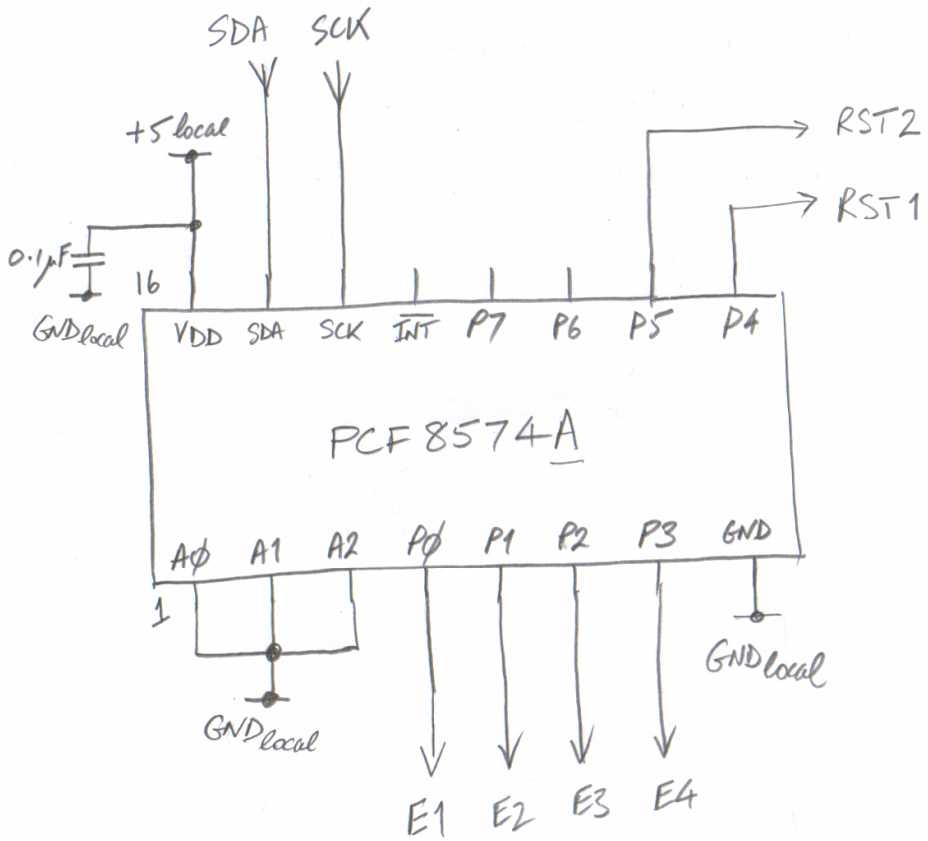

+12
GND
10µF
IN 78L05 GND OUT
+5
0.1µF
GND
+5
0.1µF
8
GND
VCC
Sy
Ry
Ty
P82B96
Sx
Rx
Tx
GND
1
GND
SDA
(12V)
SCK
(12V)
+12
750Ω
SDA
(+5)
BAT85
GND
+12
750Ω
SCK
(+5)
BAT85
GND

I2C opto-isolate



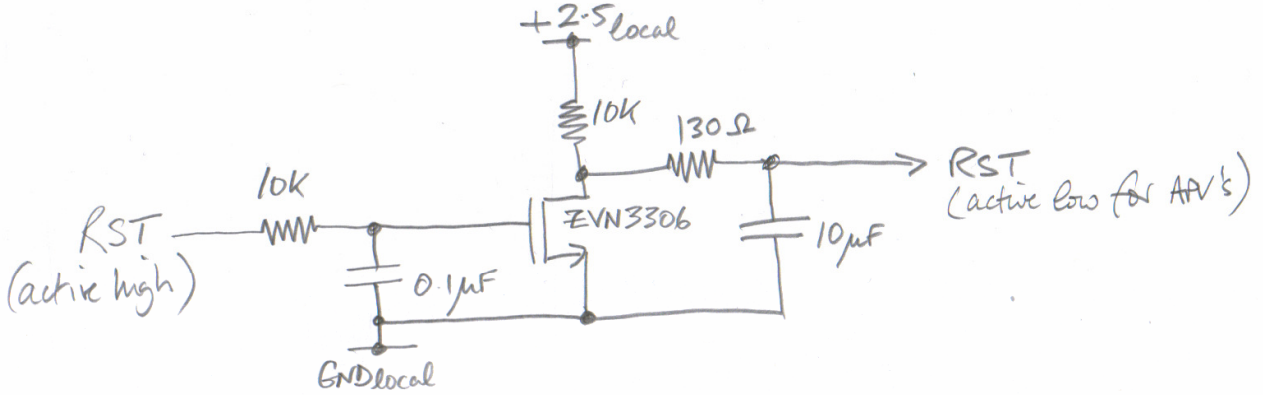
note: pull-up resistor values and 220pF/820pF capacitors should be regarded as "select-on-test" values.

PCF8574A



Note: I^2C address here b0111000 because PCF8574A.
(need to make sure PCF8574 I^2C address in hub different from this one)

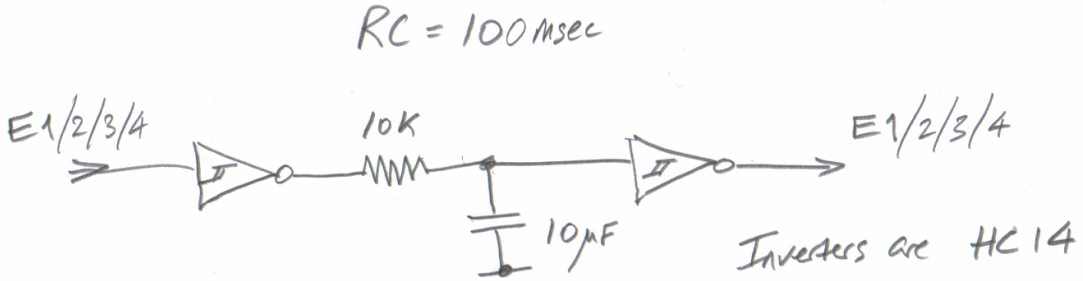
RST level shift



above circuit × 2 (1 for each APV readout hybrid)

10μF included to keep RST line quiet in steady state
130Ω limits current.

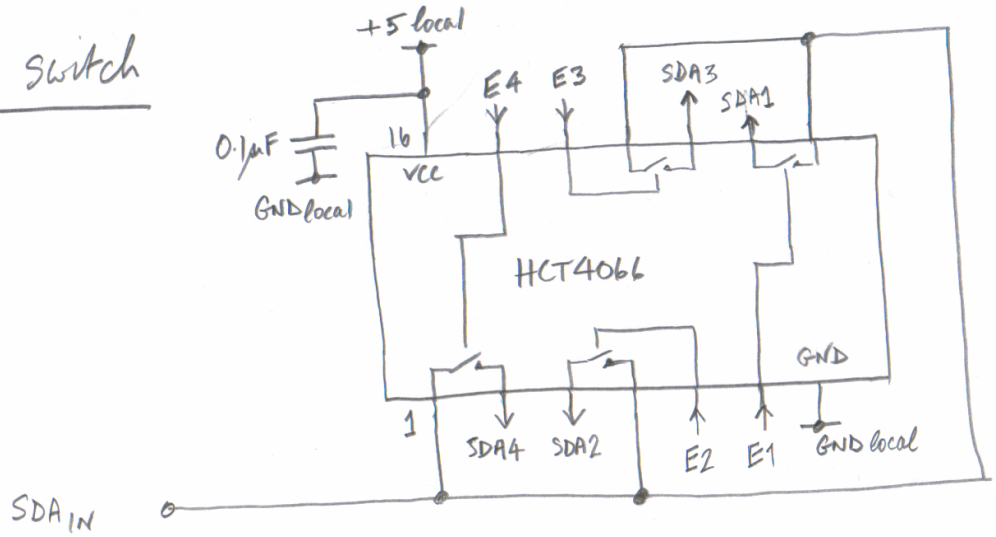
long delay

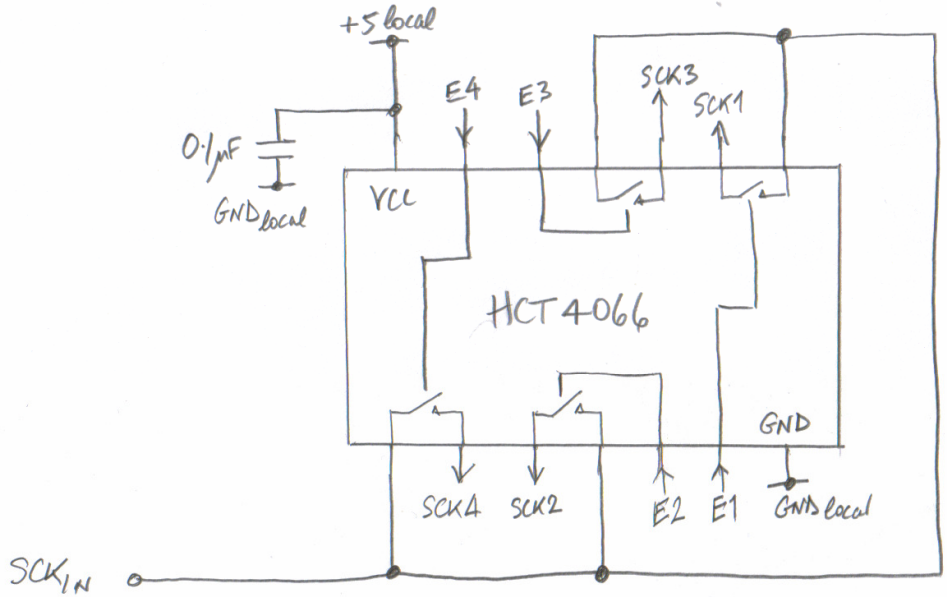


notes

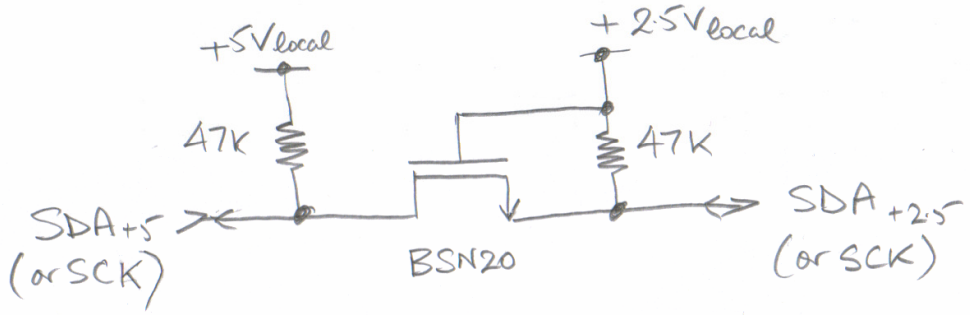
1) Use as many delays as are necessary for the number of I^2C busses you want to switch (6 inverters/package)
2) RC time constant of 100 msec is very long (could be shorter)

I2C Switch


+5 local
0.1μF
GND local
16
VCC
E4
E3
SDA3
SDA1
HCT4066
GND
1
SDA4
SDA2
E2
E1
GND local
SDA IN


+5 local
0.1μF
GND local
VCC
E4
E3
SCK3
SCK1
HCT4066
GND
SCK4
SCK2
E2
E1
GND local
SCK IN

+5 to +2.5 level translate



Pull-up resistor values very high because other pull-up resistors exist external to this circuit. Also the I²C is run very slow (10KHz).

Note: I had to remove the pull-up resistors on the AOH hybrid because the series resistance of the BSN20 meant that the I²C lines were not being pulled low enough. So that leaves only the 47K pull-up on the 2.5V side – but that is OK because the bus runs so slow.

(A better solution for the level shift might be the PCA9306 chip)