APV25 Test Results

0.25 µm APV for AC coupled Si detectors

designed at RAL, CERN and IC

Chips delivered mid October

~20 chips plugged in so far (not all exhaustively tested)
but only 1 found obviously faulty

CONTENTS summary

Brief reminder of chip architecture and layout

Amplifier performance – pulse shape, gain linearity

Pipeline studies

Noise performance

Radiation test results to 20 Mrads

1st result with detector

Mark Raymond (IC) December, 1999.

APV25 chip layout

Chip size:

8.4 x 8 mm^2 (reserved area on wafer)

~ 7.5 x 6.7 mm^2 active area

Input pads:

2 staggered rows of 88 µm pitch each (effective channel pitch 44 µm)

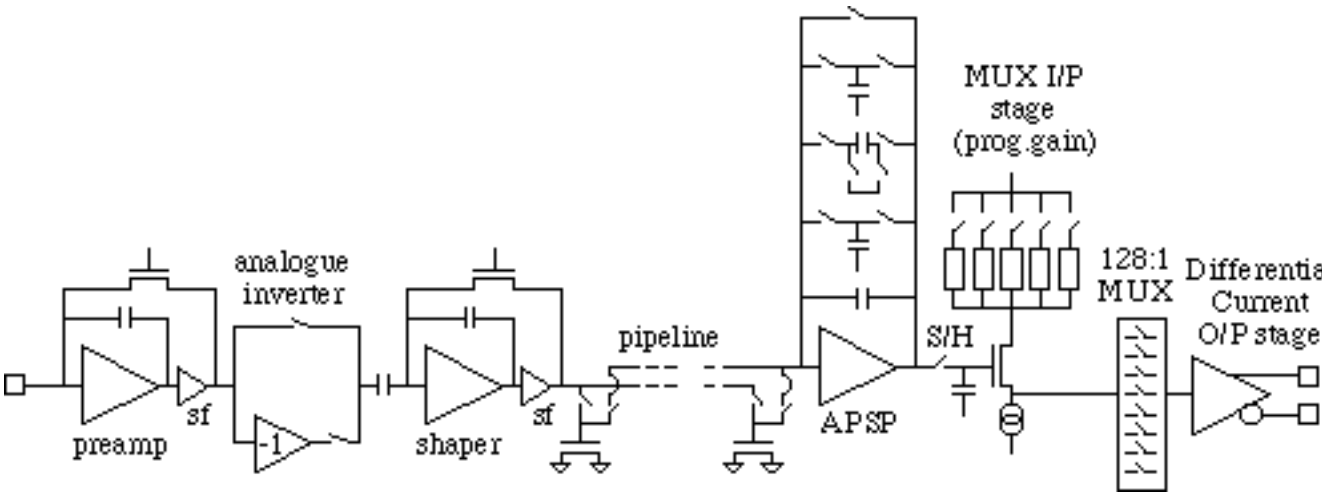
Power brought in on front edge as before

Backend pads:

29 on 225 µm pitch

Pads on top and bottom edges for test purposes, access to bias generator DAC outputs and digital signals

APV25 functional schematic



Preamp designed for AC coupled Si detectors.

New features c.f. previous designs

Switchable inversion at preamp O / P

Needed for optimum use of shaper output range
Switched in for +ve input charge, out for -ve

Pipeline

Implemented using gate capacitance
(metal-metal capacitance would violate design rules for allowable area of this type of capacitor / chip)
192 cells / channel -> 4.8 µsec
(latency up to 4 µsec possible if maximum no. of buffer locations reserved (FIFO depth of 31))

MUX

Programmable gain - 5 values
nominal, ±10%, ±20%

O / P stage

Differential current O / P, 1mA / Mip nominal (design value)
Digital header ± 4 mA

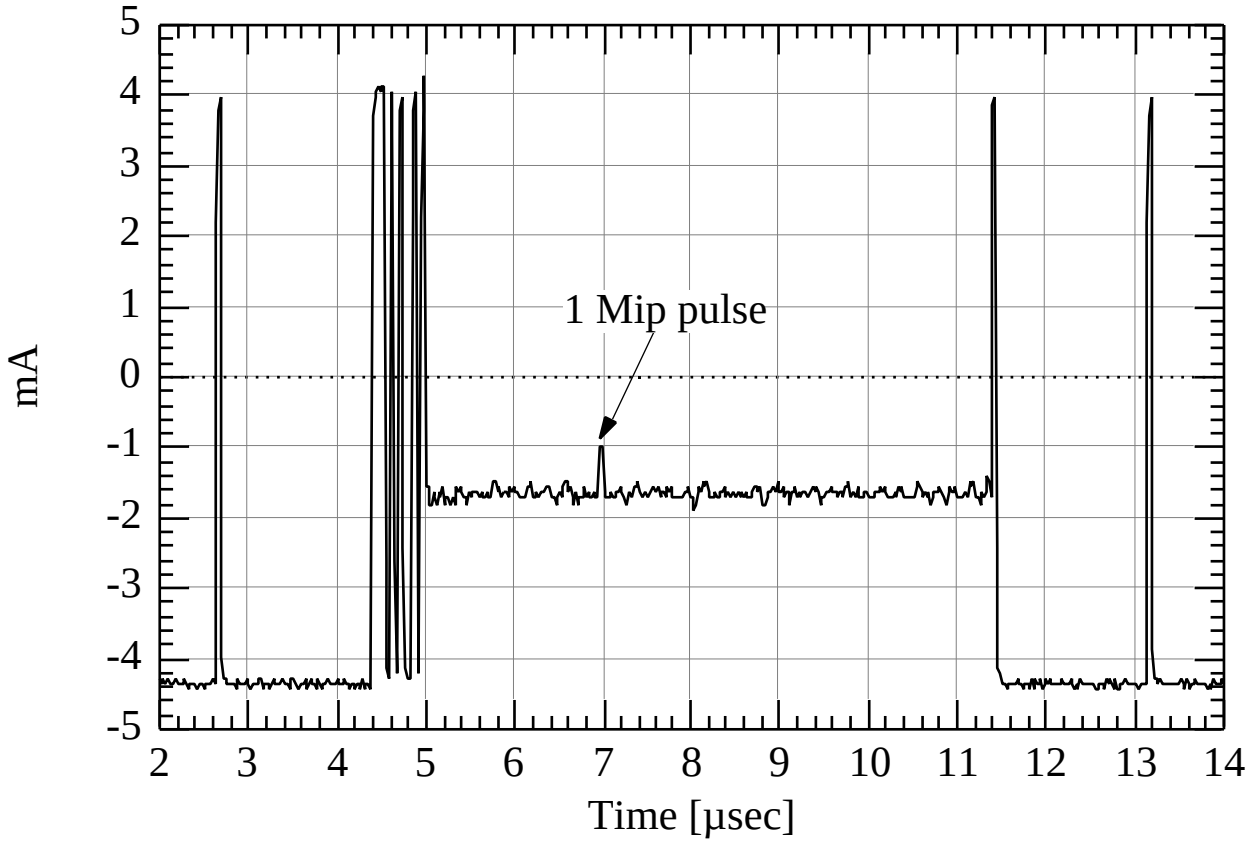
APV25 System Features

As previous APV's except:

- 5 bit I^2C address
  - up to 31 chips / I^2C channel
- FIFO / Pipeline dimensions
  - 31 FIFO locations
    - 31 events bufferable in peak mode
    - 10 in deconvolution (3 cells reserved / trigger)
  - 192 pipeline columns
    - Latency programmable up to 161 (4 µsec) if full 31 cells reserved for buffereing
- Operational Modes
  - Peak / Deconvolution and Multi mode
  - MUX speed 20 or 40 MHz selectable
- Power Supplies
  - +1.25 V (VDD), -1.25 V (VSS) and 0 V

O / P data frame

Scope picture of +ve differential output



Digital header ~ ± 4 mA as expected

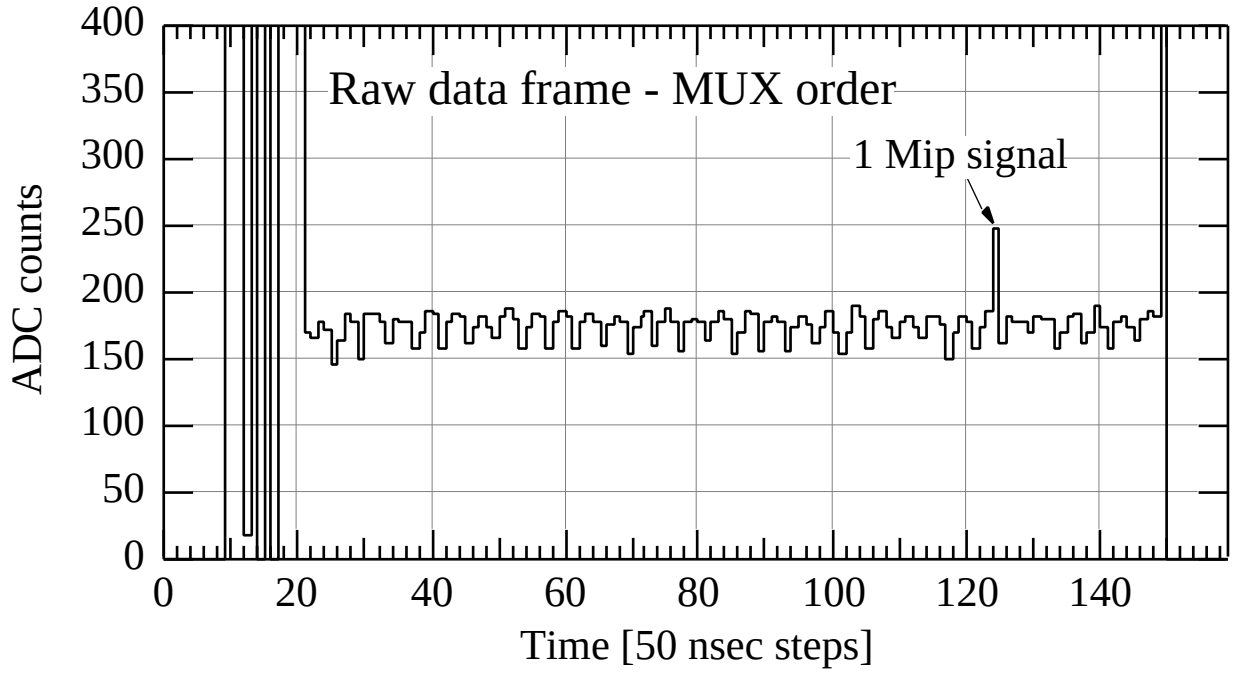
Analogue baseline variable using Vpsp I2C bias register

Tick marks every 1.75 µsec if no data

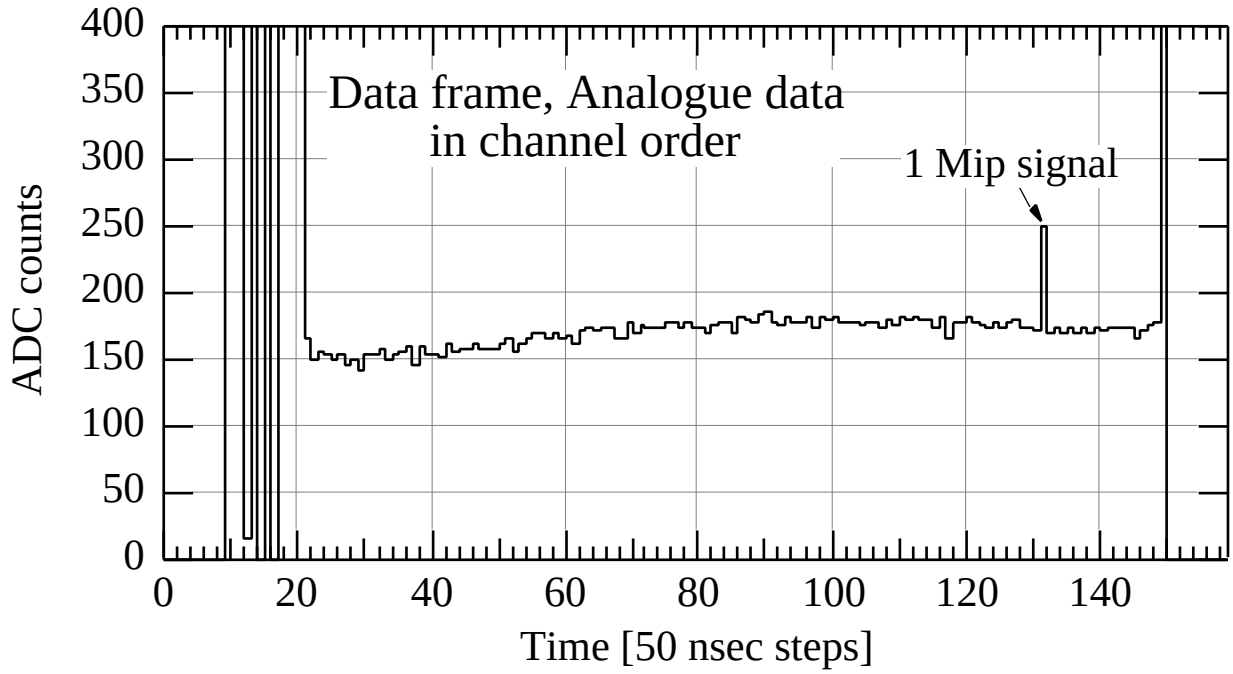
Digital header -> 3 start bits, 8 bit pipeline column triggered address followed by error bit (active low)

Pedestals

APV25 digitised data frame



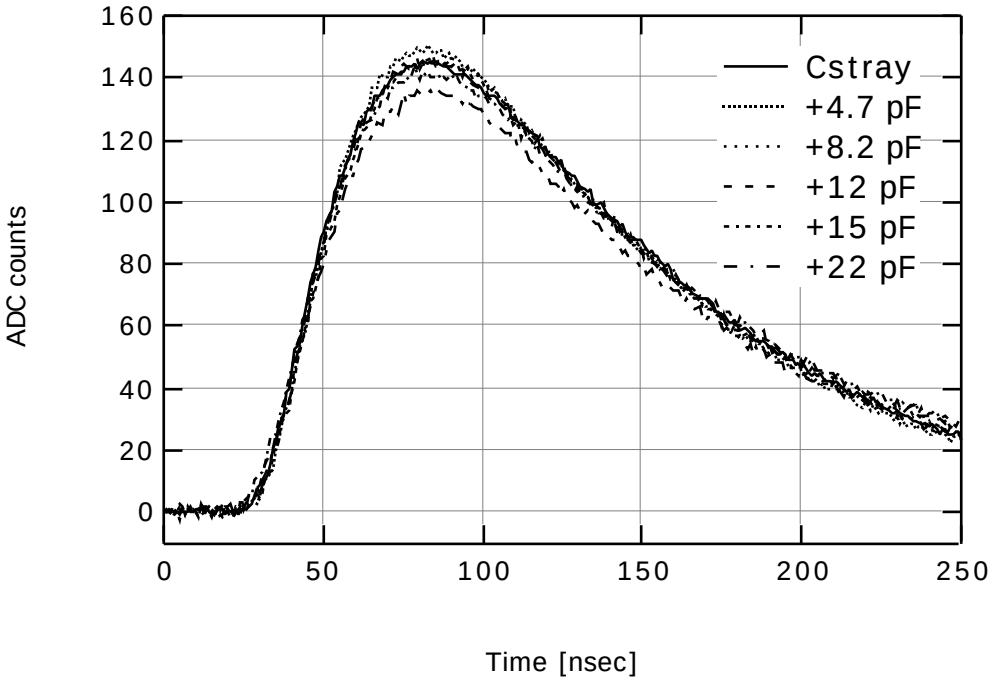
Software reorder analogue part of frame to show channel order (0-127)

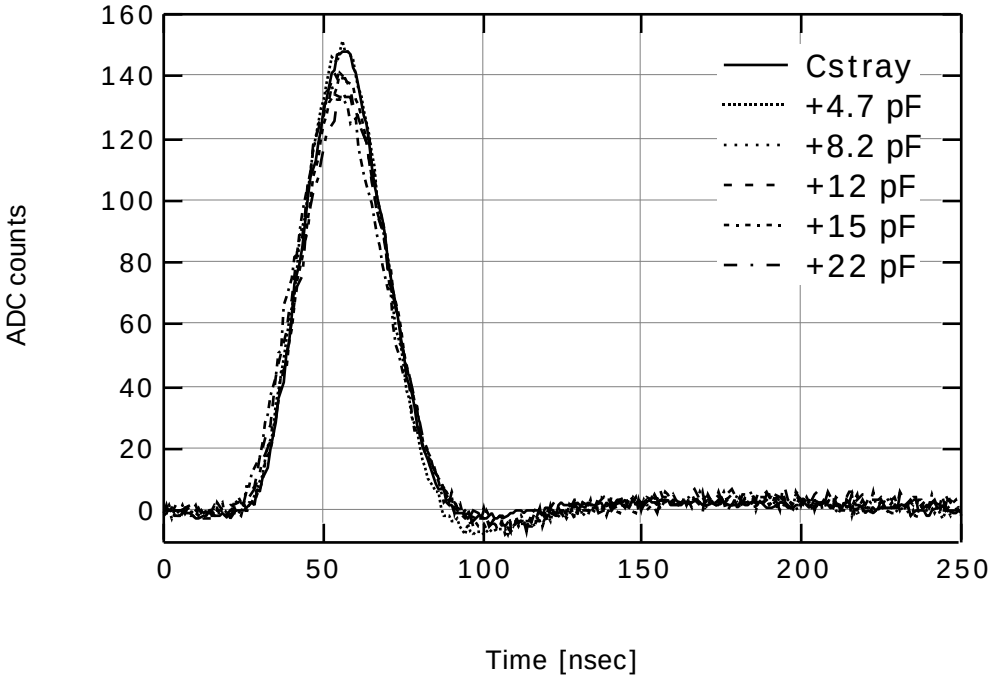


Pk-pk channel pedestal variation ~ 0.5 Mip

Reordered picture shows smooth variation across chip (probably power supply related)

Pulse shapes

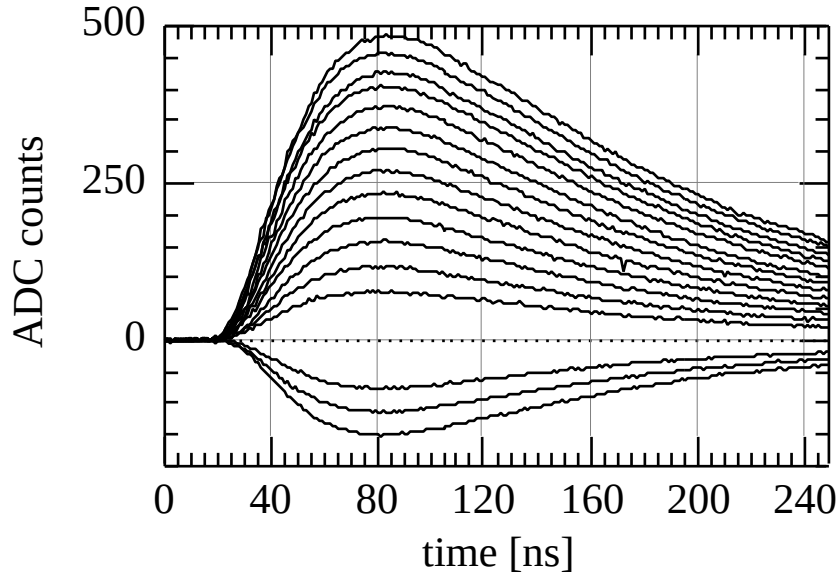


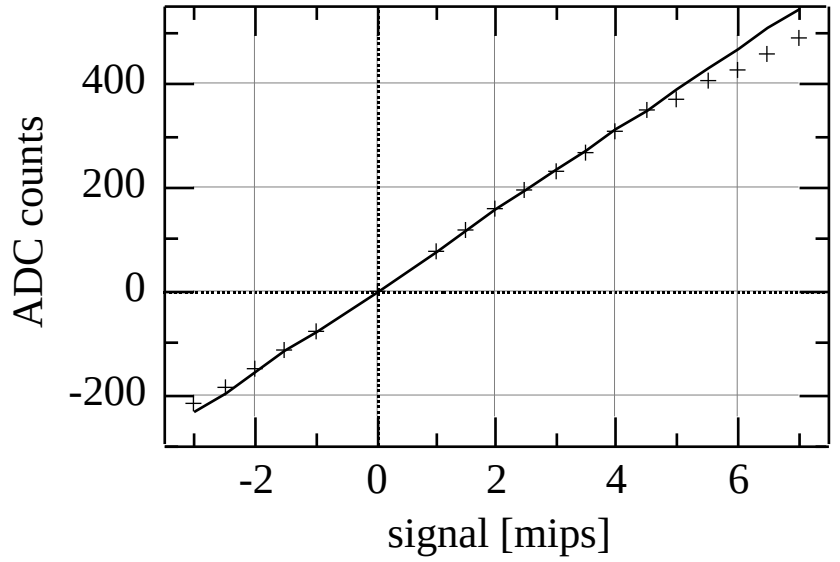


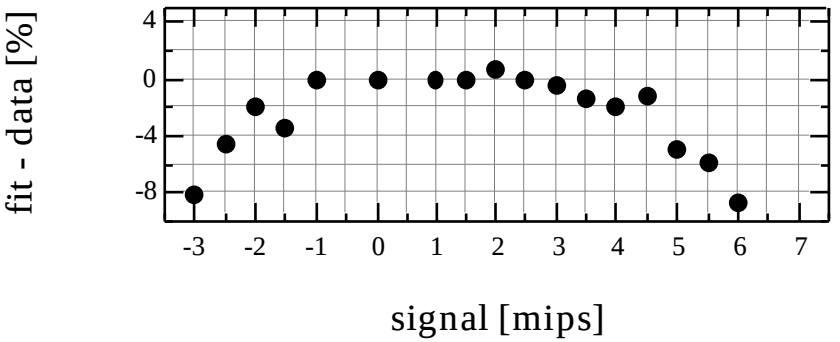
Pulse shape tuned (in peak mode) for 50 ns CR-RC pulse shape for each value of input capacitance. (ISHA: 30 -> 85 µA, VFS: 70 -> 15)

Gain ~ same in peak and deconvolution mode

Gain and Linearity - Peak Mode

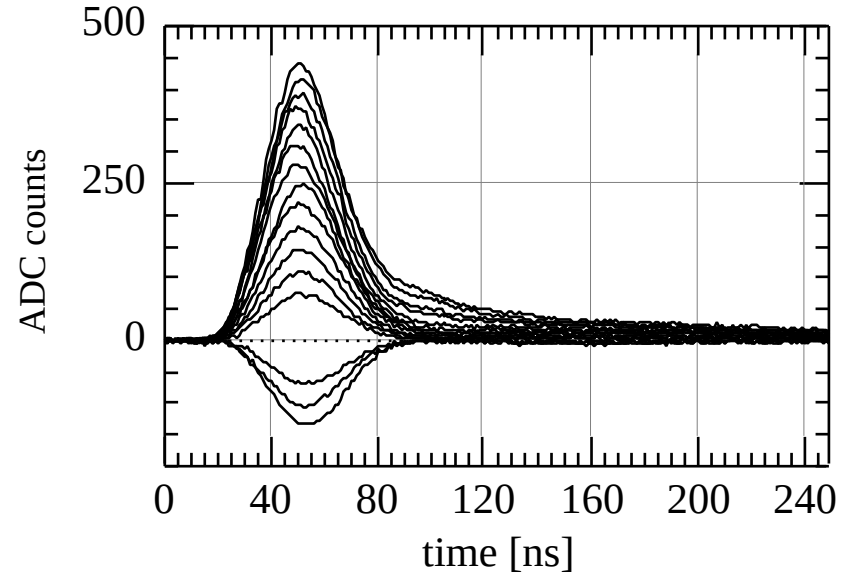


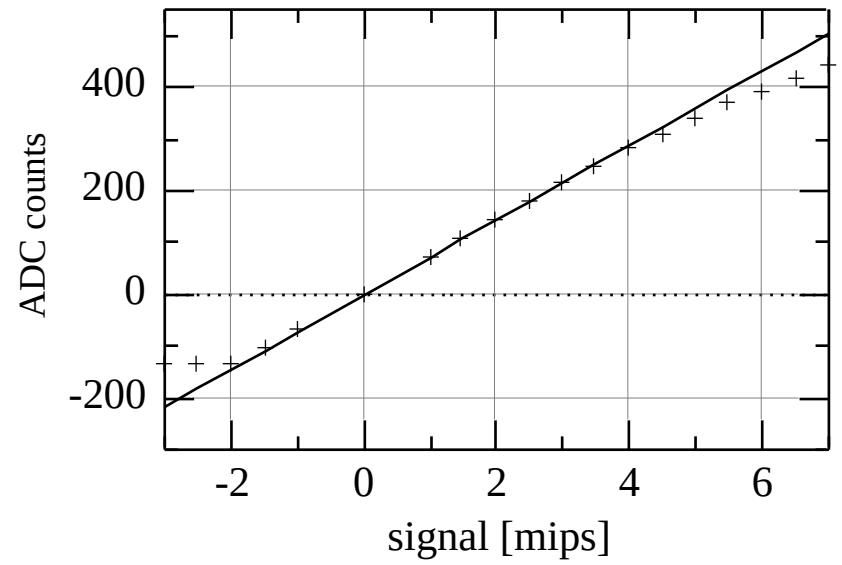


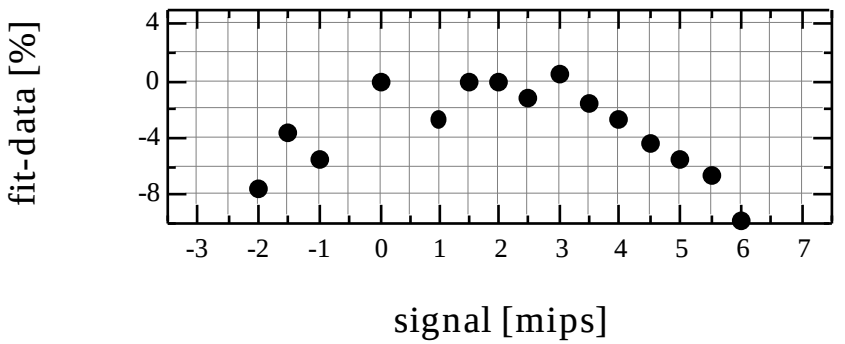


Input signal: -2, -1.5, -1, 1 -> 7 mips (0.5 mip steps)
Linearity: v.good to 3 Mips, ~ 5% down at 5 Mips

Gain and Linearity - Deconvolution

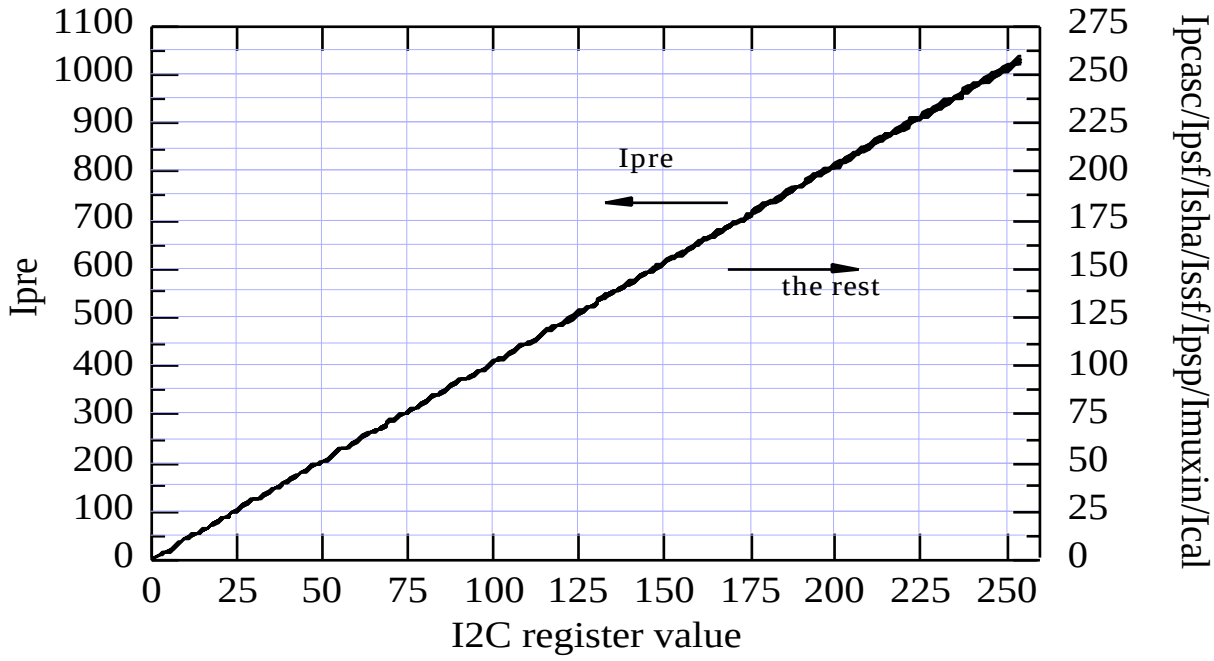


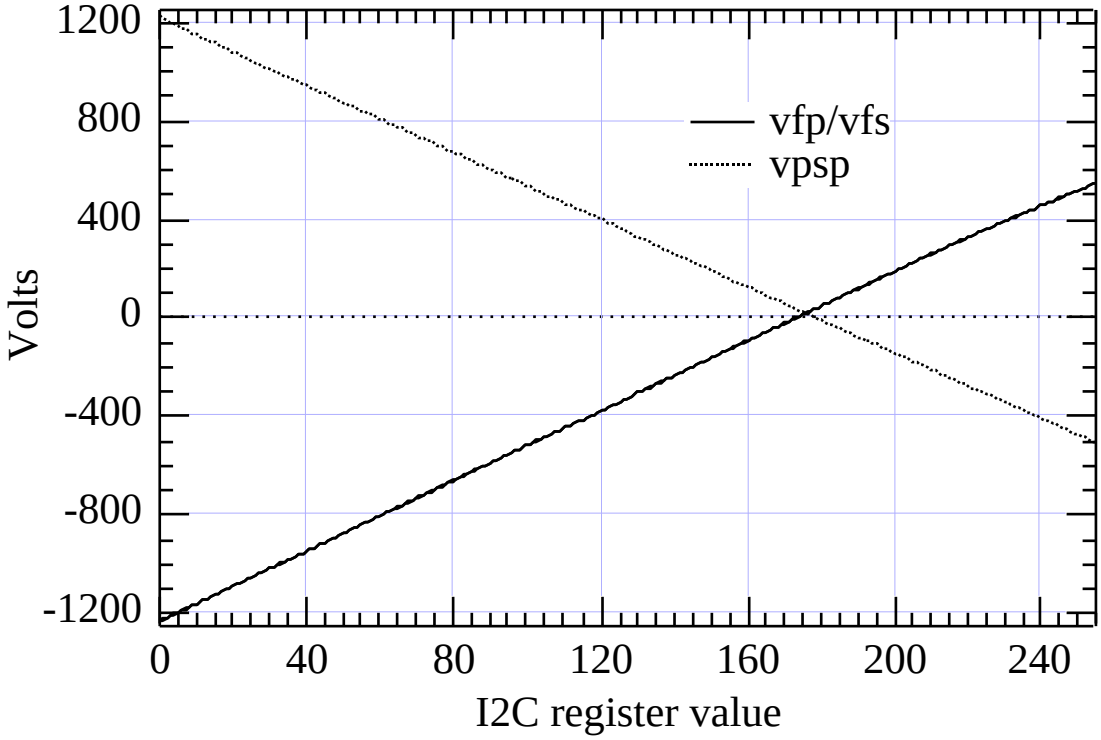




Linearity: v.similar to peak mode result

Bias Generator Operation

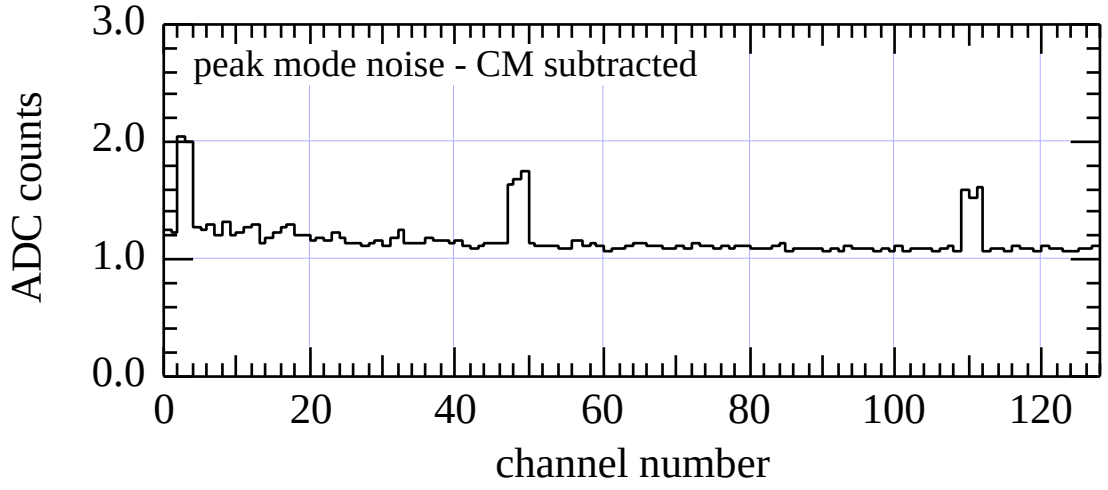




measured on test pads on chip
good linearity and matching

Noise

Plot noise dependence on channel number



Bonded out channels show bigger noise but also a slope across chip

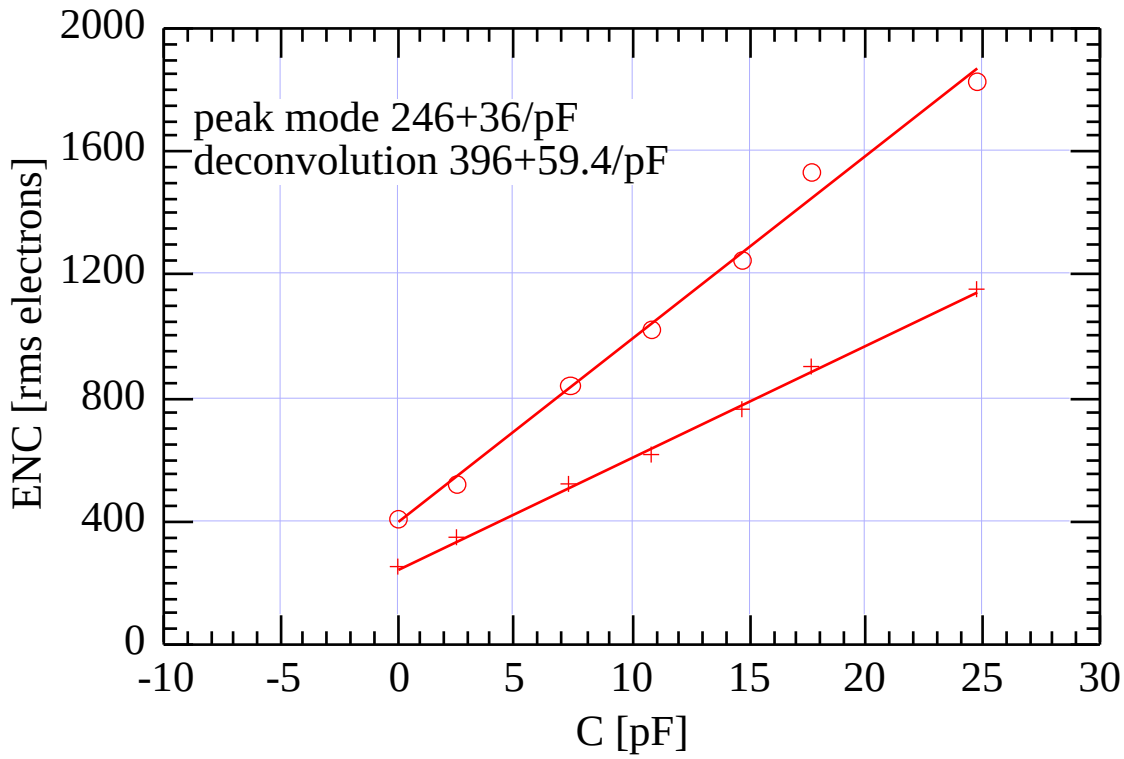
Initially suspect systematic gain variation across chip but not there

Explanation – input pad to input FET track length increases monotonically from top channel (shortest) to bottom channel.

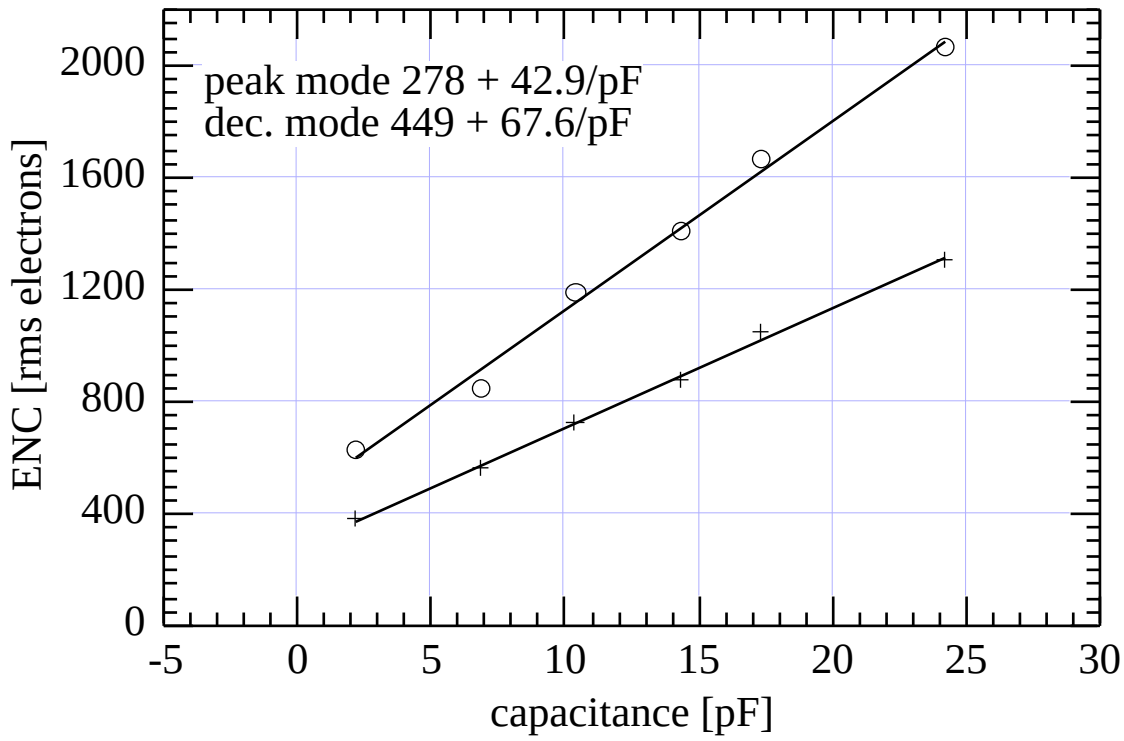
Track resistance 127 mOhm / square -> 13 ohms at top of chip, 70 at bottom. This is a significant noise source for low value channels.

Noise

Channel 109, extra series resistance ≈ 22 ohms



Channel 2, extra series resistance ≈ 70 ohms



~ 20 % extra noise in channel 2 compared with channel 109

Noise

Calculate expectation for 20 pF detector capacitance

Chan 109 (22 ohms)

Peak mode (246+36 / pF) ->	966 electrons
Decon mode (396+59.4 / pF ->	1584 electrons

Chan 2 (70 ohms)

Peak mode (278+42.9 / pF) ->	1136 electrons
Decon mode (449+67.6 / pF) ->	1801 electrons

Note 22 ohms still contributes ~ 4 electrons to the noise slope for channel 109.

Need to find way to minimise track resistance in future

Output signal size

Nominal value should be 1 mA / mip.

Measured value 0.7 mA / mip for nominal gain setting

Gain dependence on MUX I / P stage gain setting (programmable via I2C register)

setting	-20%	-10%	nominal	+10%	+20%
µA / mip (measured)	540 (-23%)	620 (-11%)	700	752 (+7%)	832 (+19%)

Amplifier test structure shows gain as expected

Reason for gain discrepancy still under study -> APSP / pipeline test structure not yet looked at.

Gain uniformity (channel - channel)

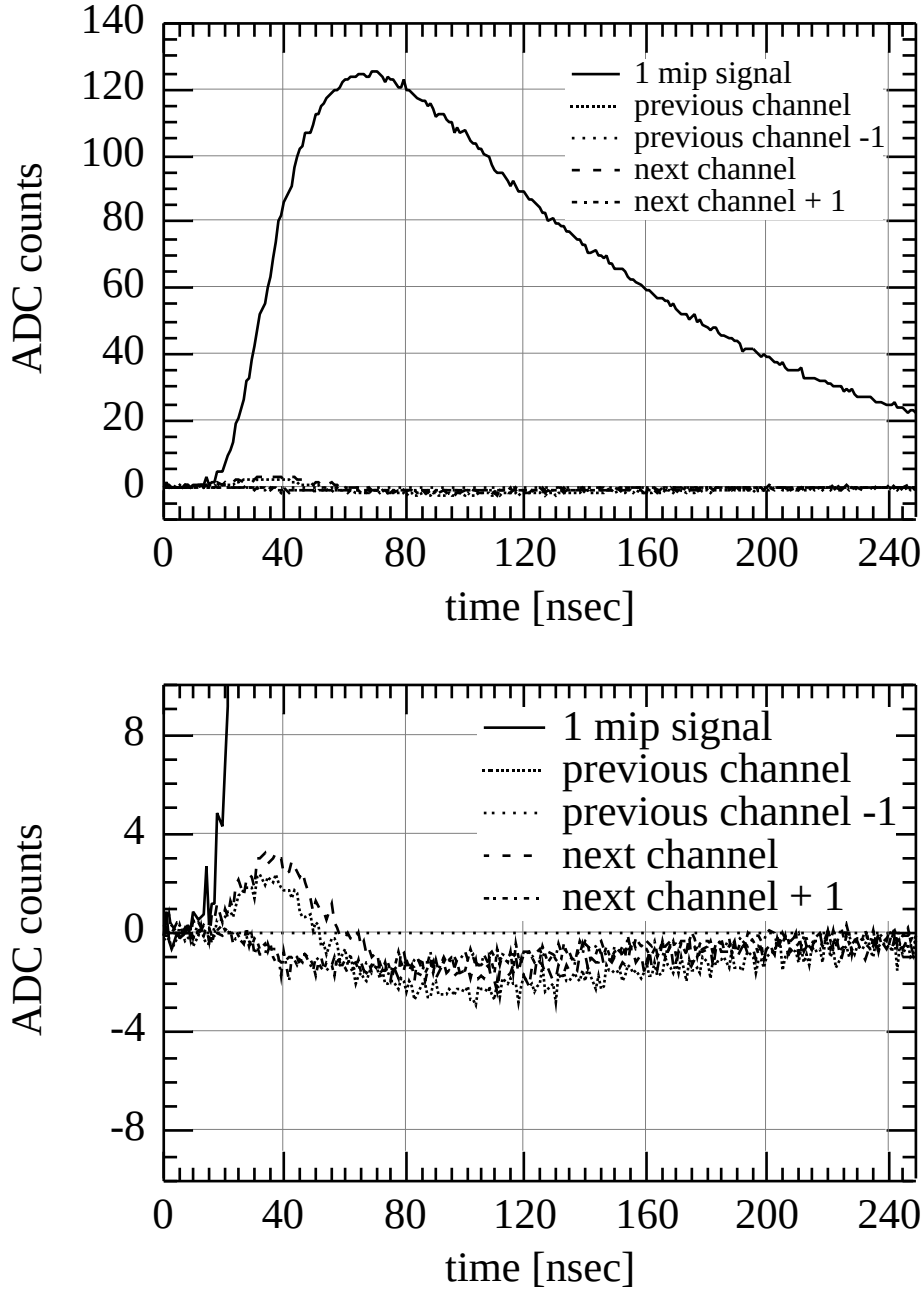
Measured on 8 bonded channels

Channel no.	4	5	47	48	49	109	110	111
peak height 1 mip ADC counts	122	121	124	126	123	124	125	125

pk - pk difference 3.2% for these 8 channels

Crosstalk

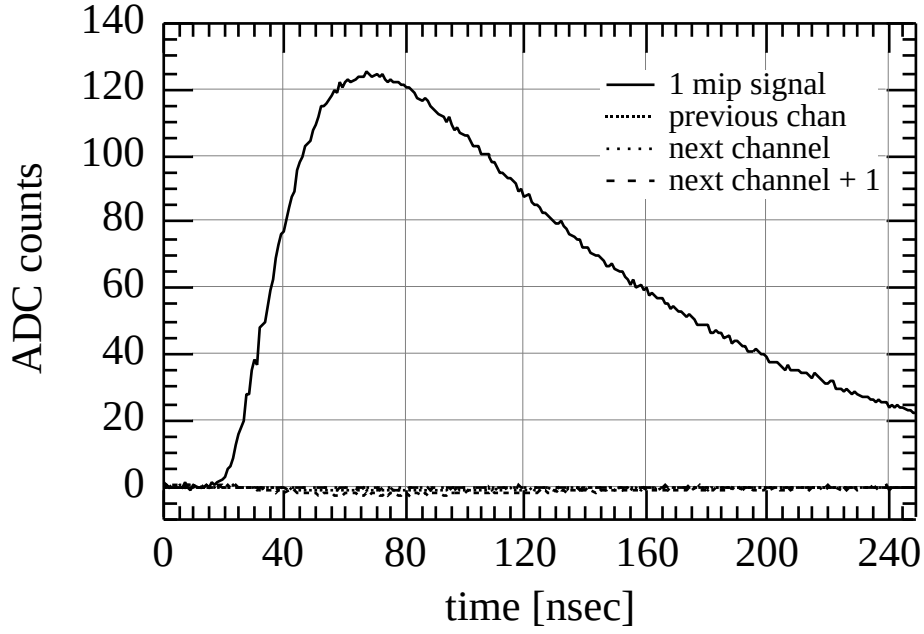
between neighbouring channels in channel order of chip

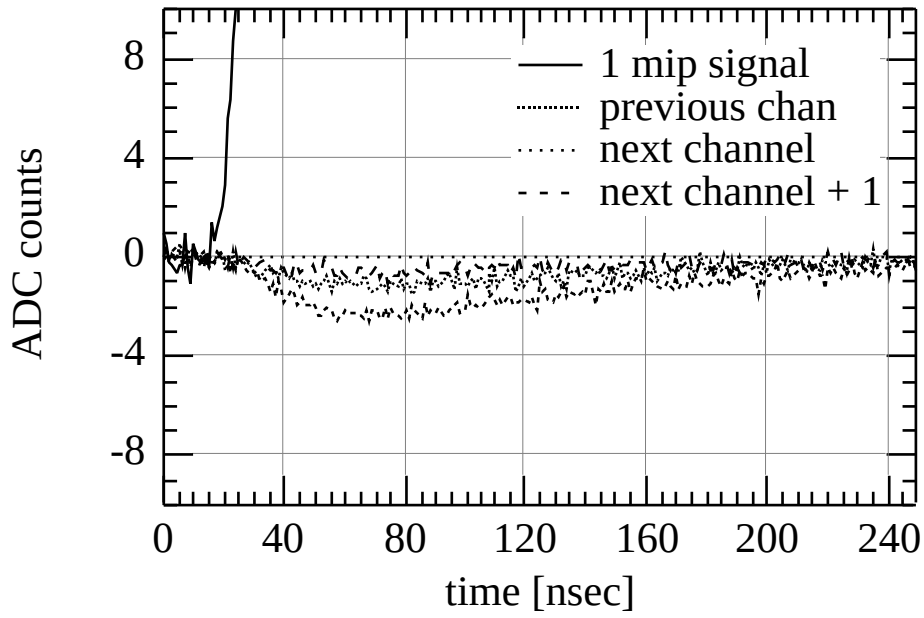


< ~ 2.5 %

Crosstalk

between neighbouring channels in muliplexer order on chip





< ~ 2%

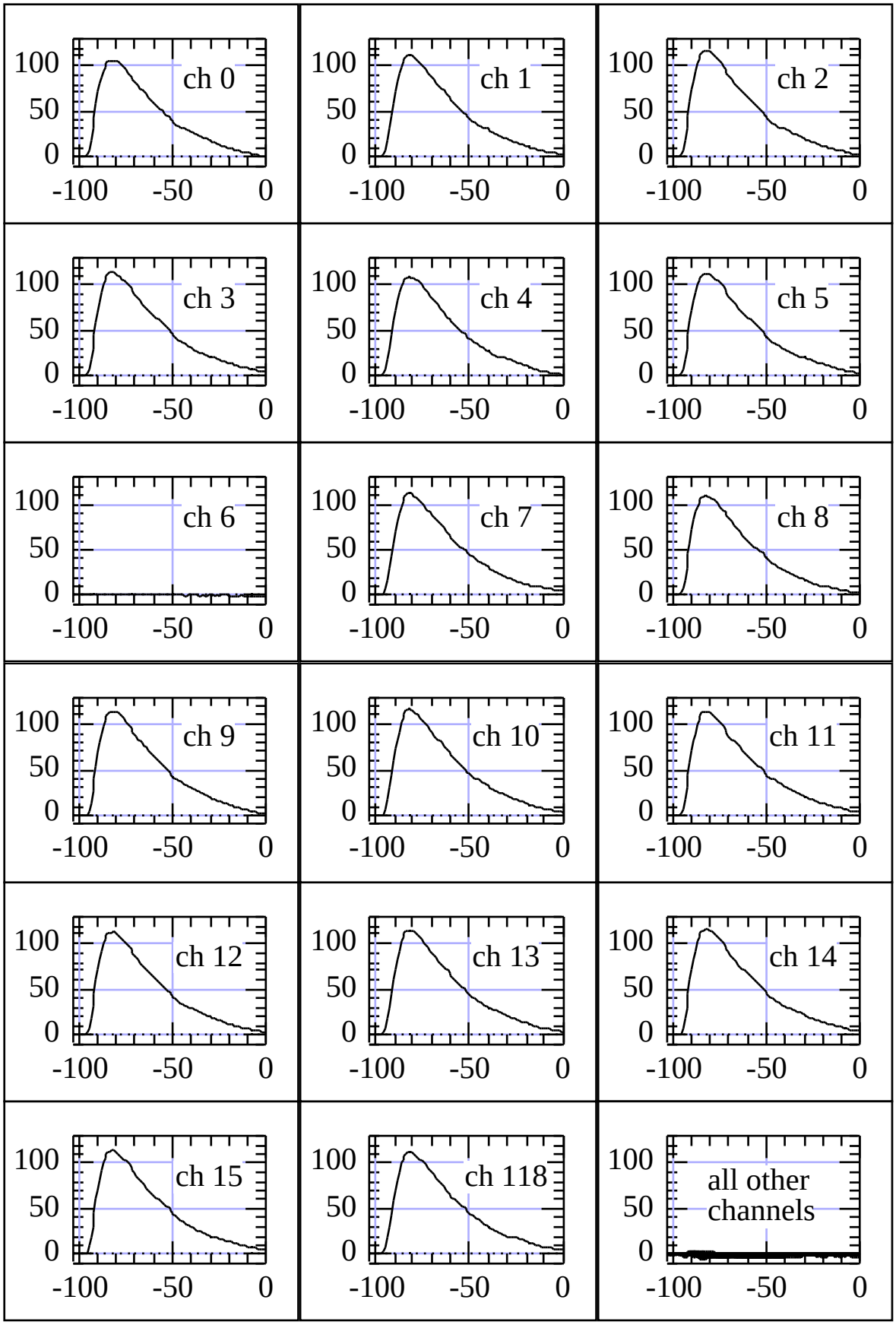
Calibration

On-chip circuit allows pulse shape to mapped in 3.125 nsec increments

Wiring mistake to calibration capacitors results in channels not coming out in the expected order, but all channels connected nevertheless

Cal line	Mux order channels seen		
1	0 - 5,	7 - 15,	and 118
2	16 - 21,	23 – 31	and 102
3	32 - 37,	39 - 47	and 86
4	48 - 53,	55 - 63	and 70
5	64 - 69,	71 - 79	and 54
6	80 - 85,	87 - 95	and 38
7	96 - 101,	103 - 111	and 22
8	112 - 117,	119 - 127	and 6

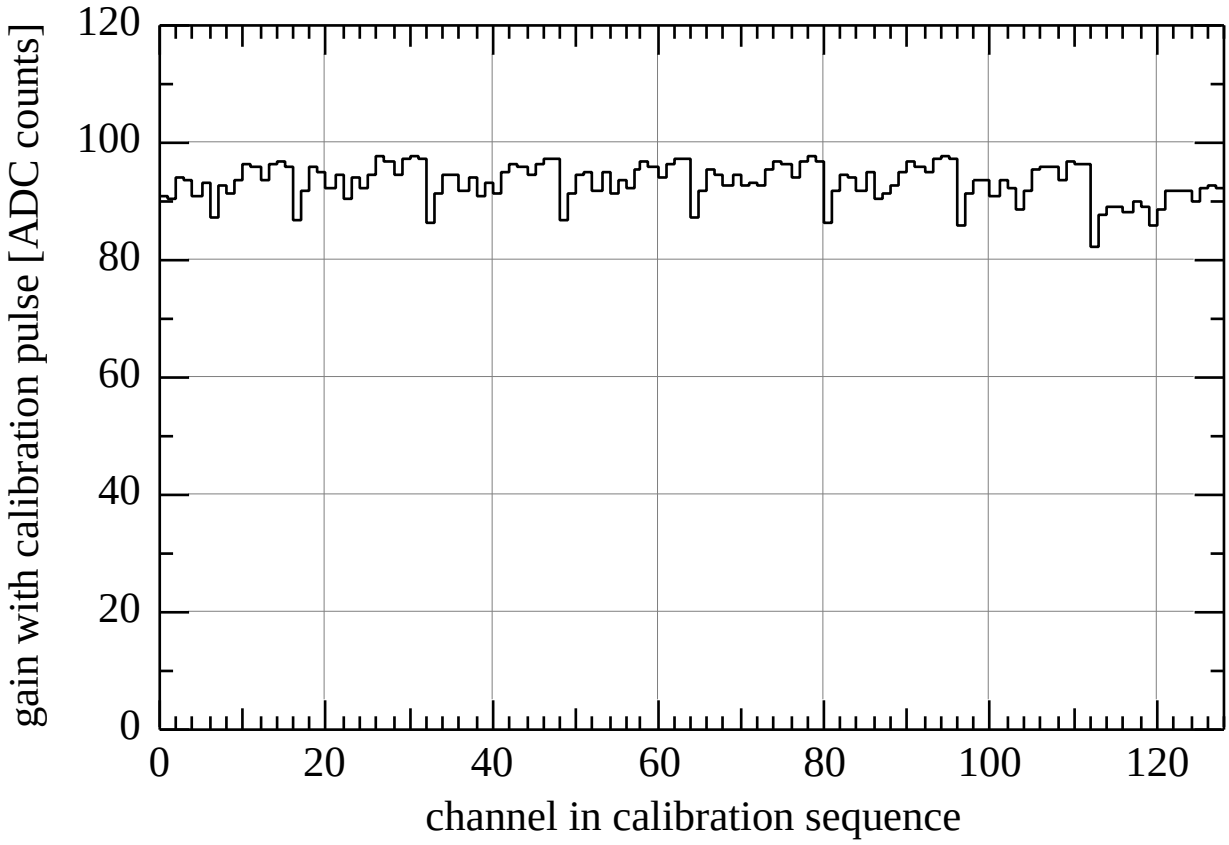
results from a simple reversal of connection order for a group of 8 neighbouring channels. Trivial fix.



Pulse shapes resulting from first calibrate input

Calibration

calibration peak pulse height measured for all channels on chip

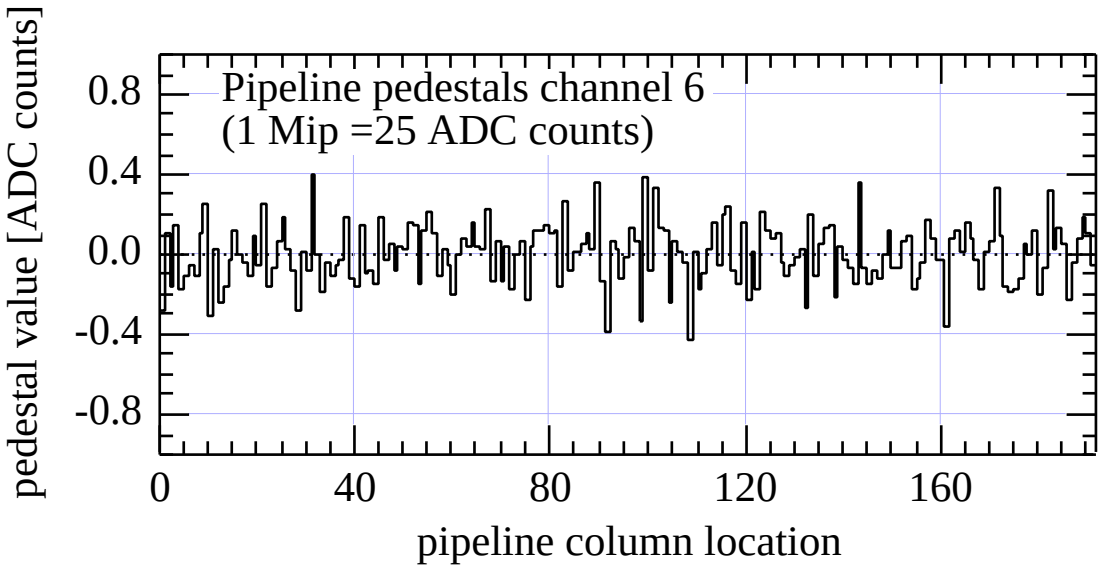


repetitive structure evident - probably due to parasitic couplings in the tracking which connects to each calibrate capacitor at input edge of chip

Pipeline Pedestals

Does channel pedestal vary depending on the pipeline location which stored the signal. Could lead to additional noise contribution

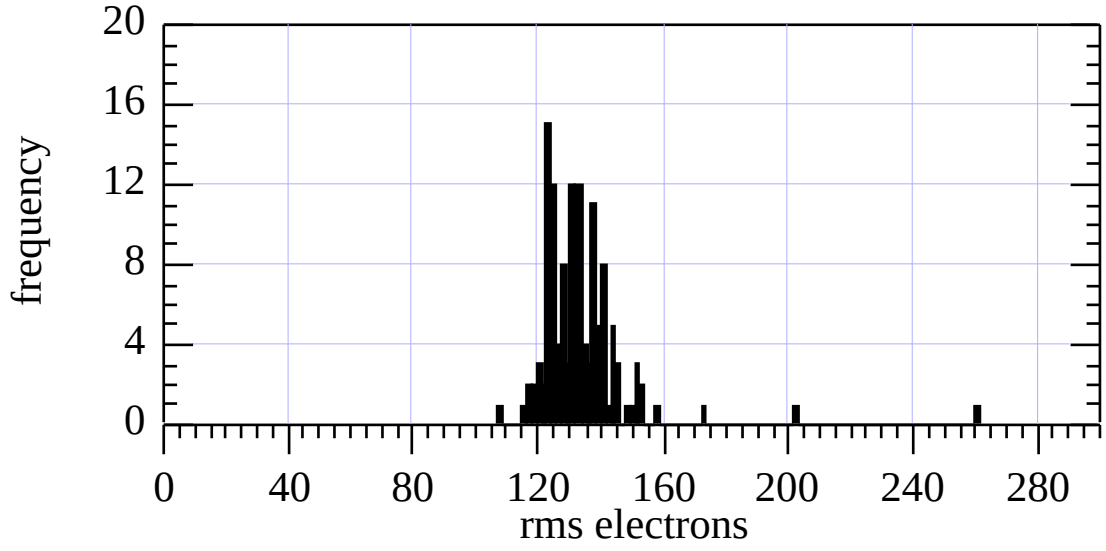
Can measure sytematically by acquiring pedestals for every pipeline location for all channels



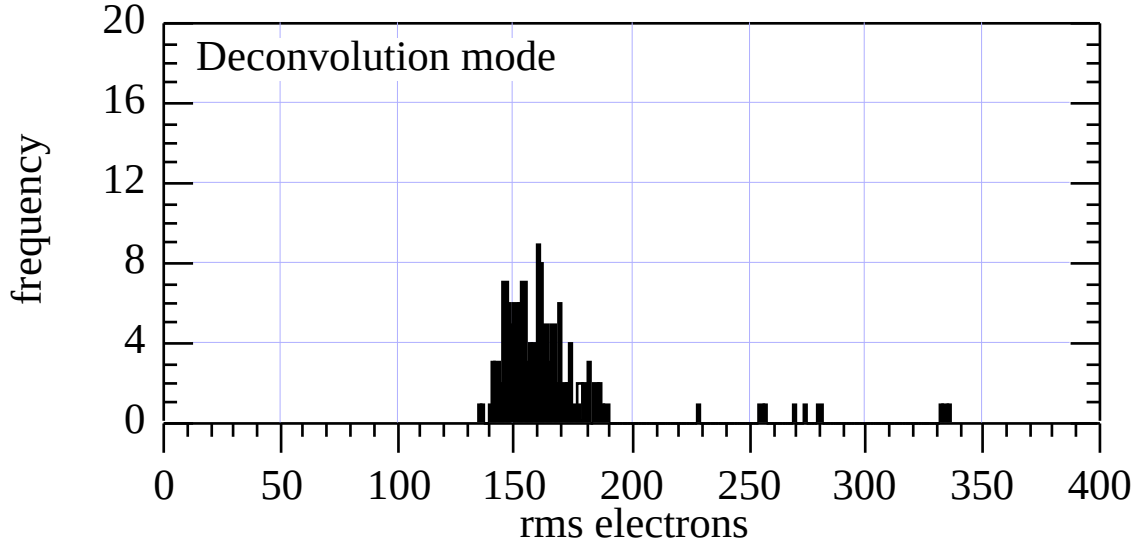
Take rms value for all channels, convert to electrons and histogram

Pipeline Pedestals

Rms pipeline pedestals for all 128 channels – PEAK mode



DECONVOLUTION mode



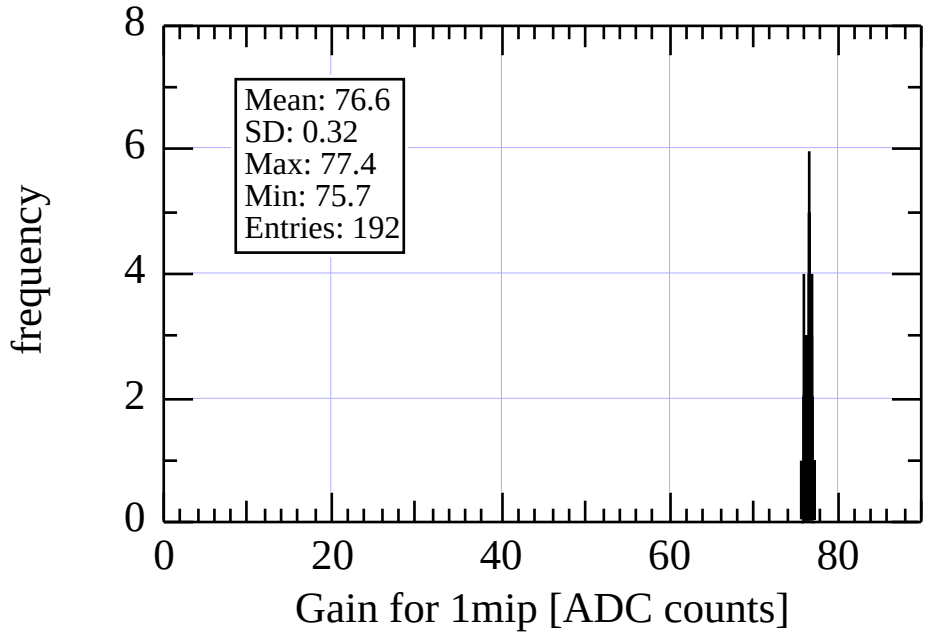
Pipeline pedestal noise contribution effectively negligible

Pipeline Gain Uniformity

If pipeline capacitors not equal in value then gain will depend on pipeline location

Measure by moving charge injection time in 192 25nsec increments (moving trigger as well) hence storing and retrieving signal from every pipeline cell for a channel.

Histogram results



Distribution => very close matching between capacitors in pipeline

Power Consumption

Sub - circuit	current / ch. VDD->VSS [µA]	current / ch. 0V->VSS [µA]	Power / channel [mW]
Preamplifier	60	400	0.65
Preamp source flwr	50		0.125
inverter		100	0.125
shaper	50		0.125
shaper source flwr	50		0.125
APSP	80		0.2
MUX I / P stage	30		.075
O / P stages	188		0.47
Digital	164		0.41
TOTAL	692	500	2.31

Total current / chip

VDD -> VSS (+1.25 -> -1.25): 90 mA
0V -> VSS (0 ->-1.25) 65 mA

Note:

Power saving cf APV6 in Amplifier / APSP areas (1.35 cf 1.89 mW / ch)
Digital(APV25) / Digital(APV6) = .41 / .55 mW / chan

But o / p stages add significant extra power. However this chip now has sufficient gain to remove amplification requirements in subsequent chips (APVMUX) which would probably otherwise have consumed significant power.

Irradiations

One chip irradiated in steps using 50 kV X-rays
1, 4, 10, 20, + anneal

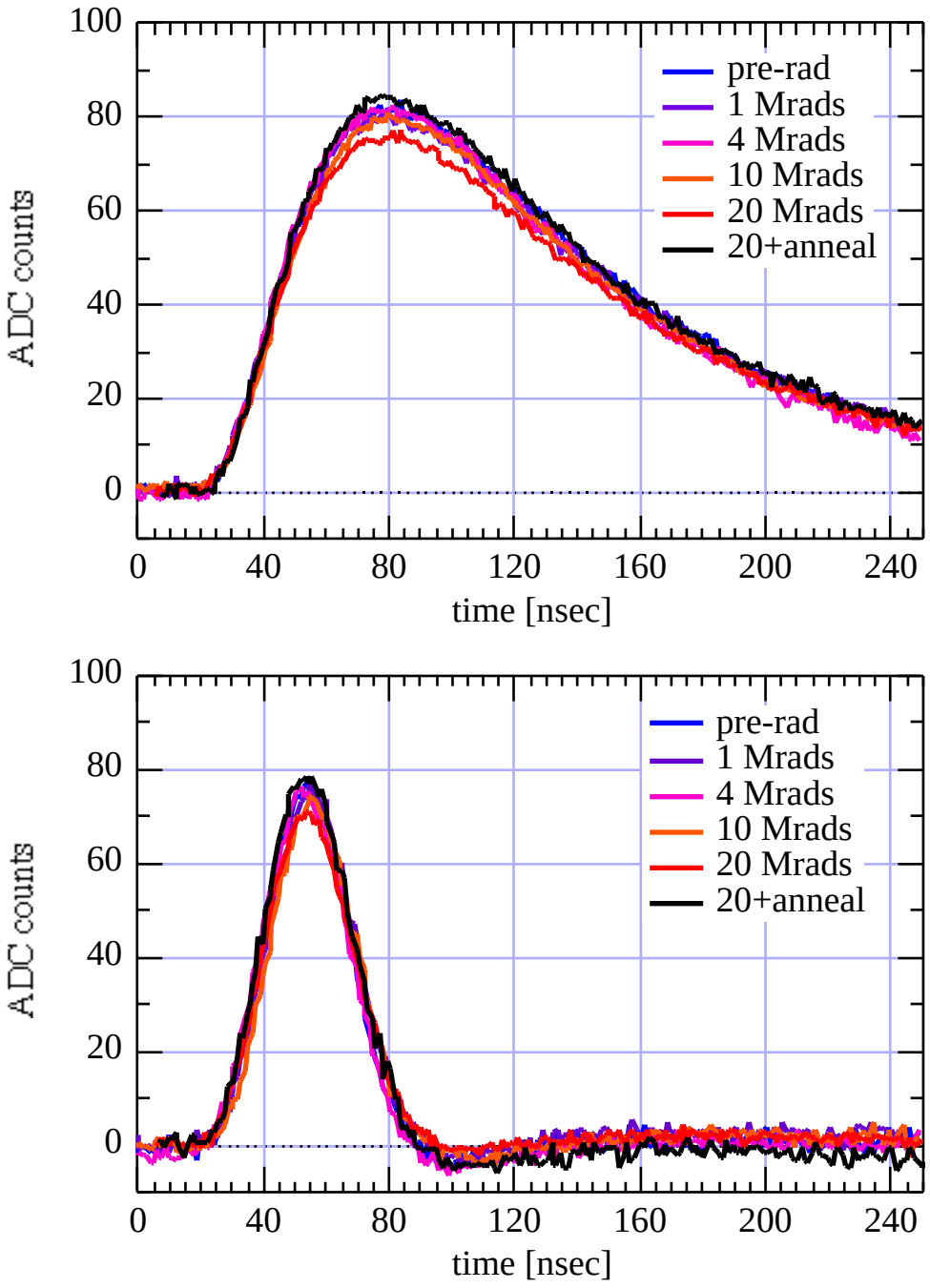
Dosimetry using calibrated Si diode accurate to ~ ± 10%

Chip biased during irradiations, clocked and triggered (same conditions during anneal step)

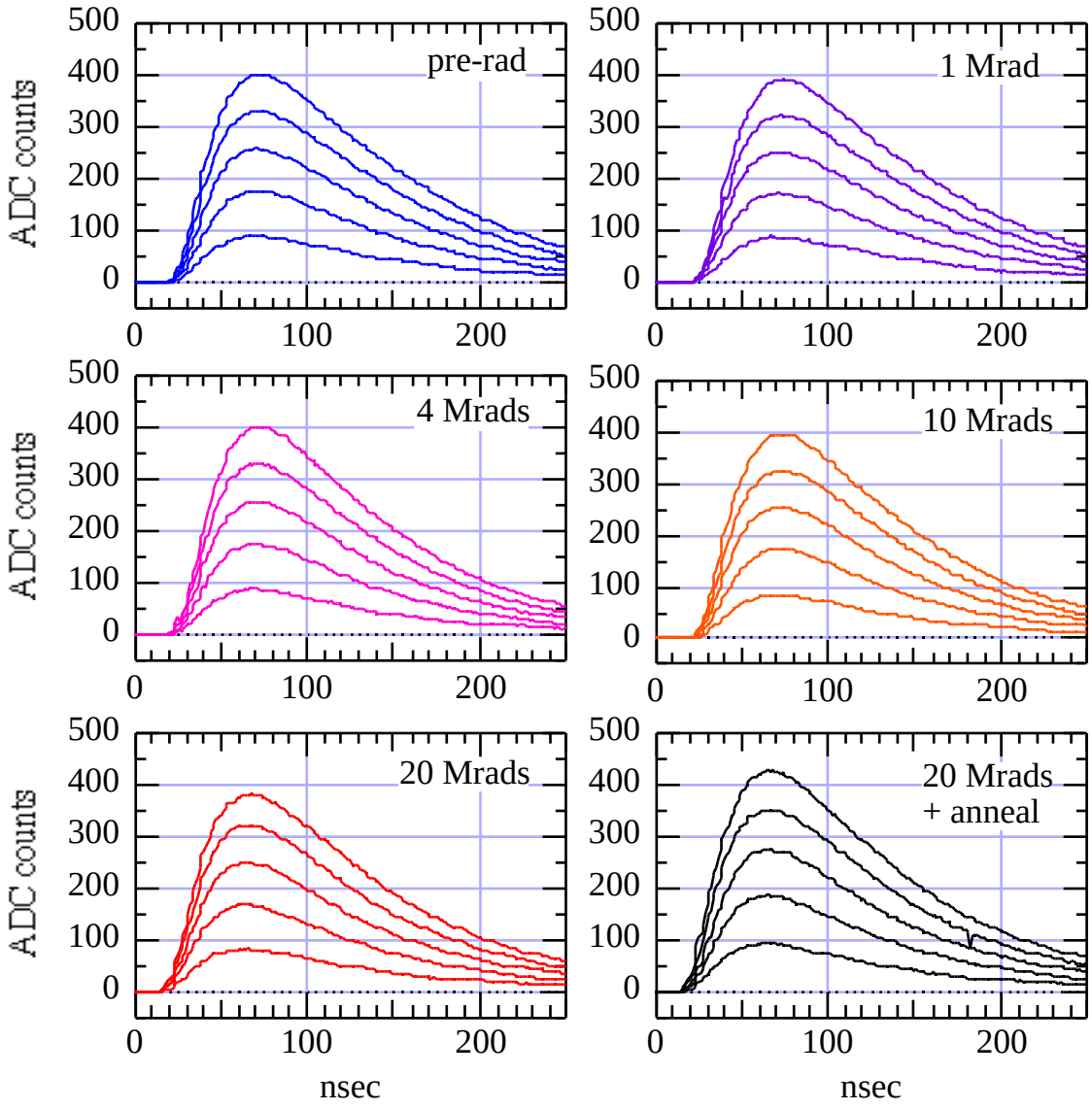
Annealing at 100 deg. C for 7 days

Measurements performed after each step

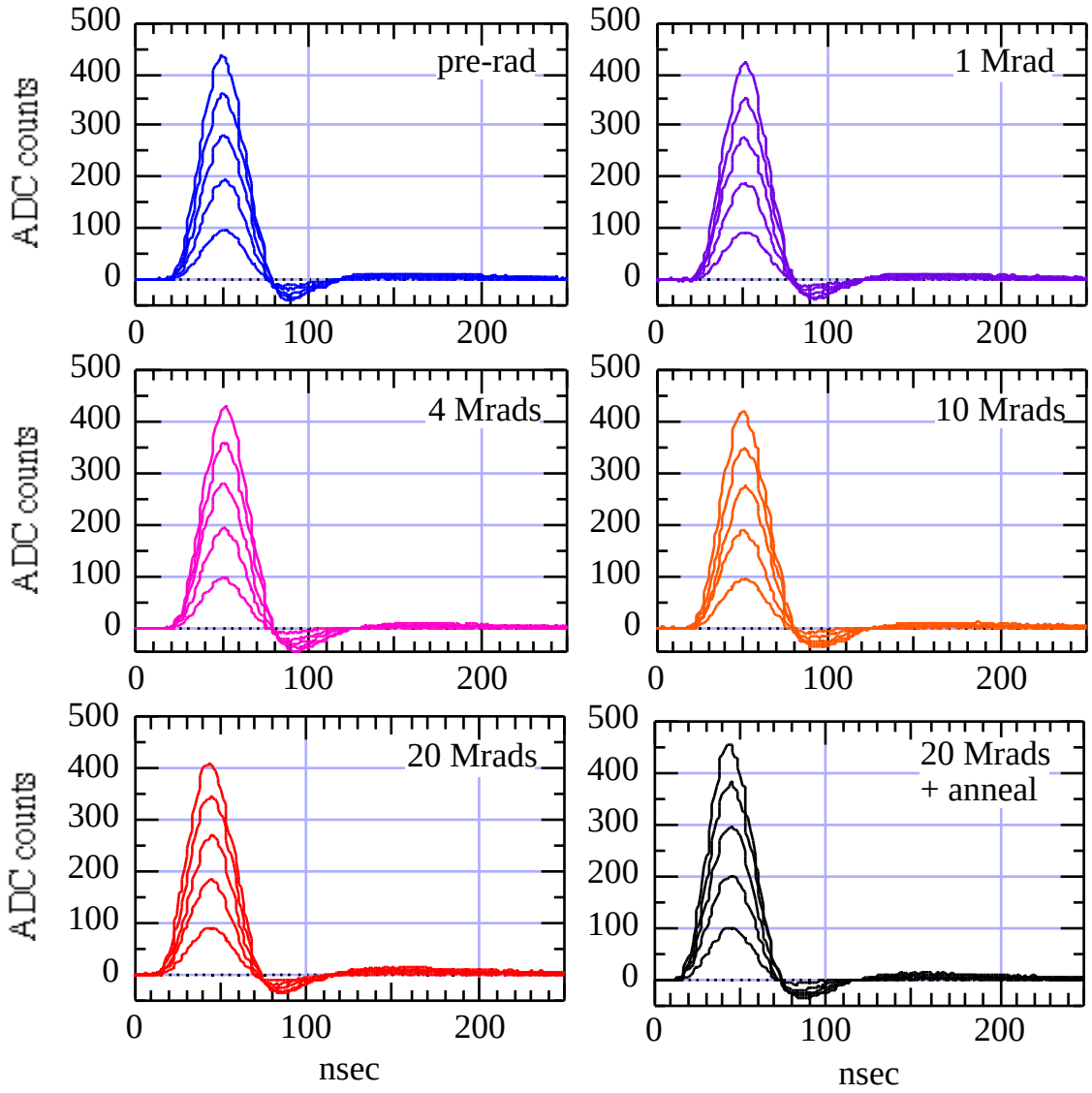
Peak and Deconvolution mode pulse shapes (1 mip) before and after irradiation (Cin ≈ 16 pF)



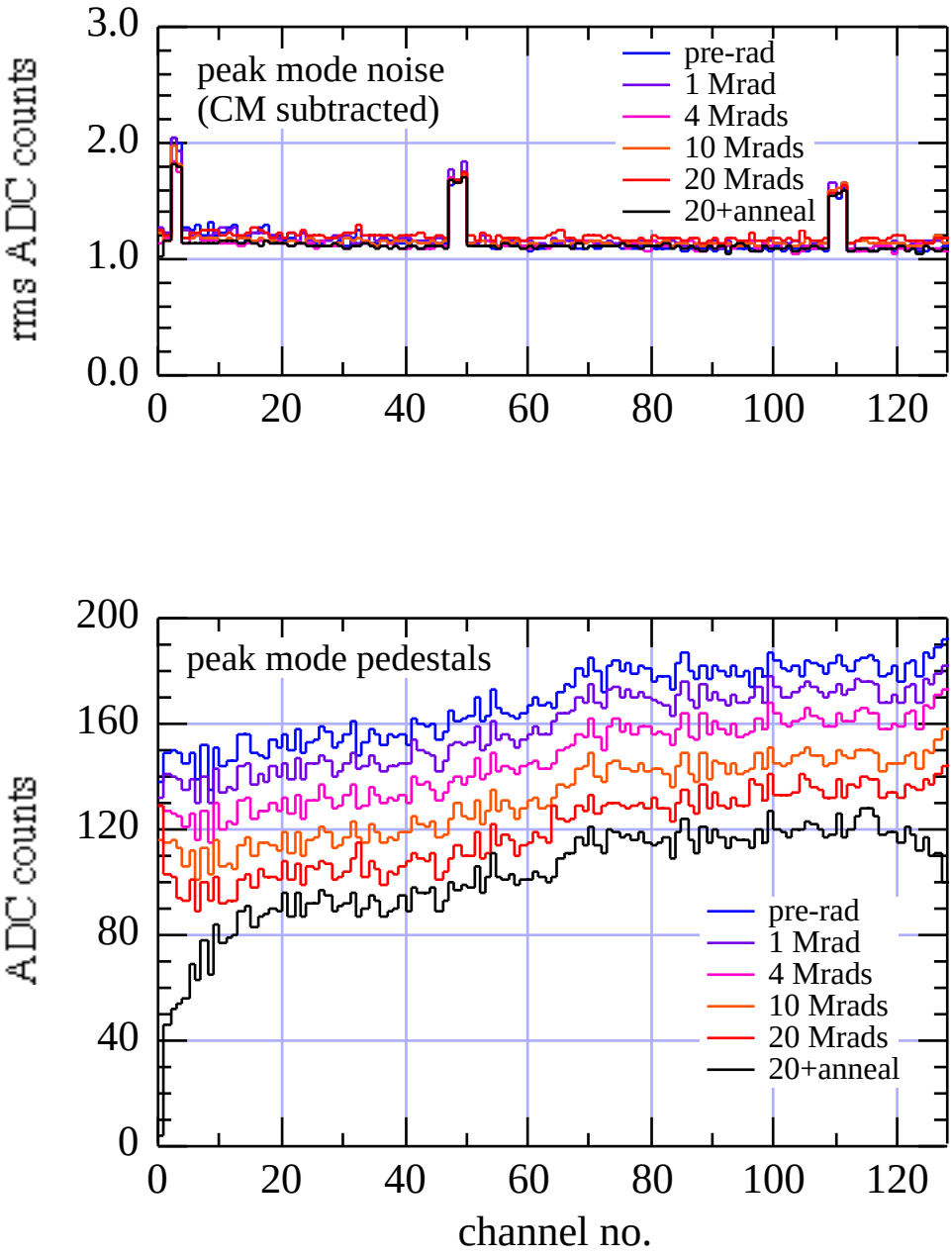
Peak Mode Pulse Shapes for 1 - 5 mips before and after irradiation



Deconvolution Mode Pulse Shapes for 1 - 5 mips before and after irradiation



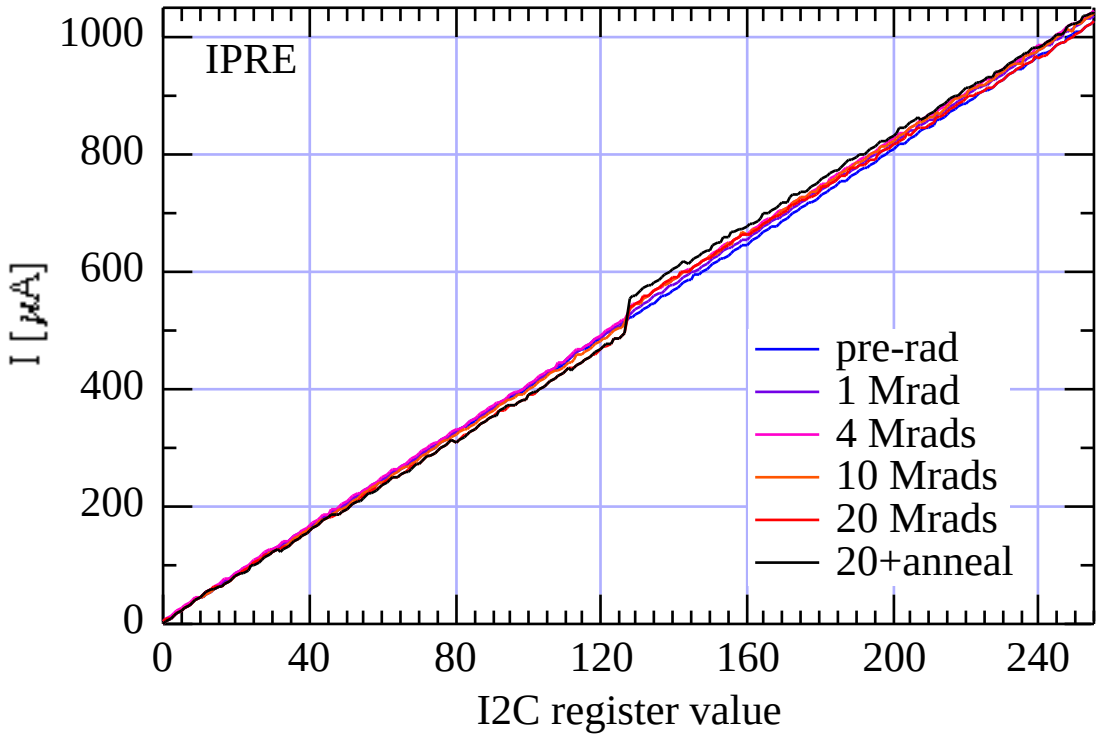
Peak Mode Noise and Pedestals before and after irradiation

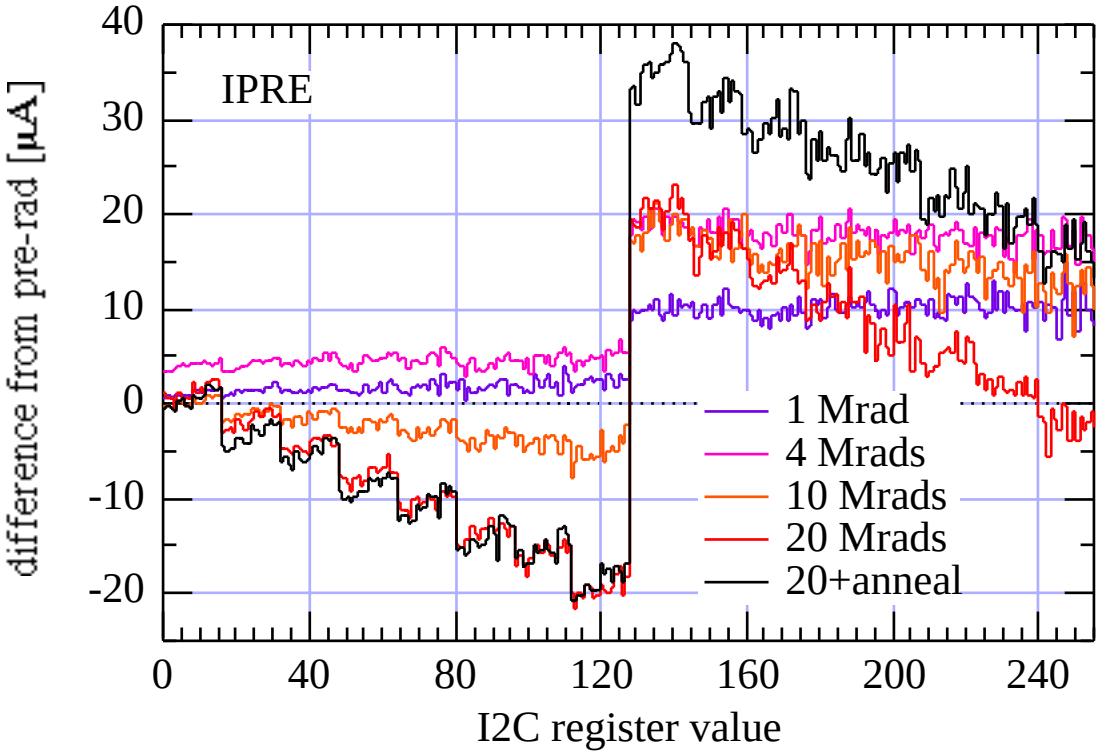


artificial offset added to pedestals for clarity

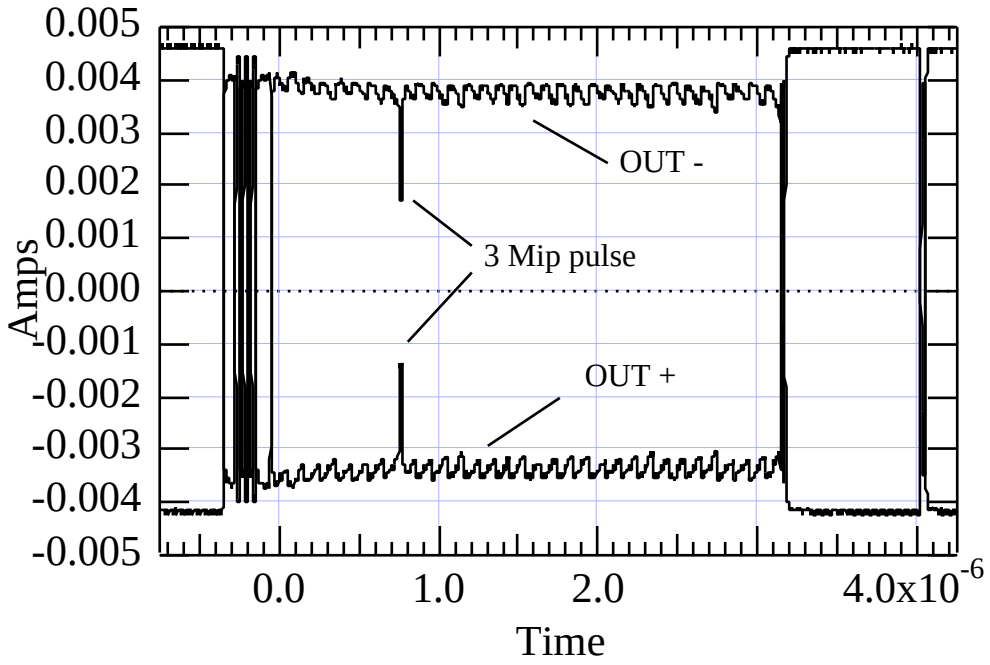
noticeable droop for low and high channel pedestals after anneal

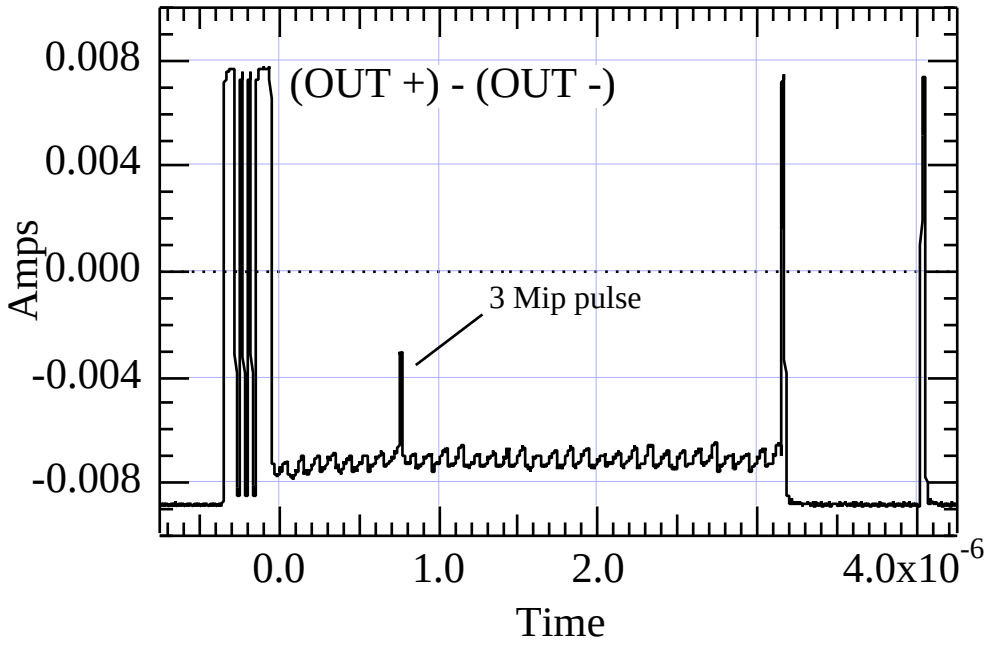
IPRE bias current measurement before and after irradiation



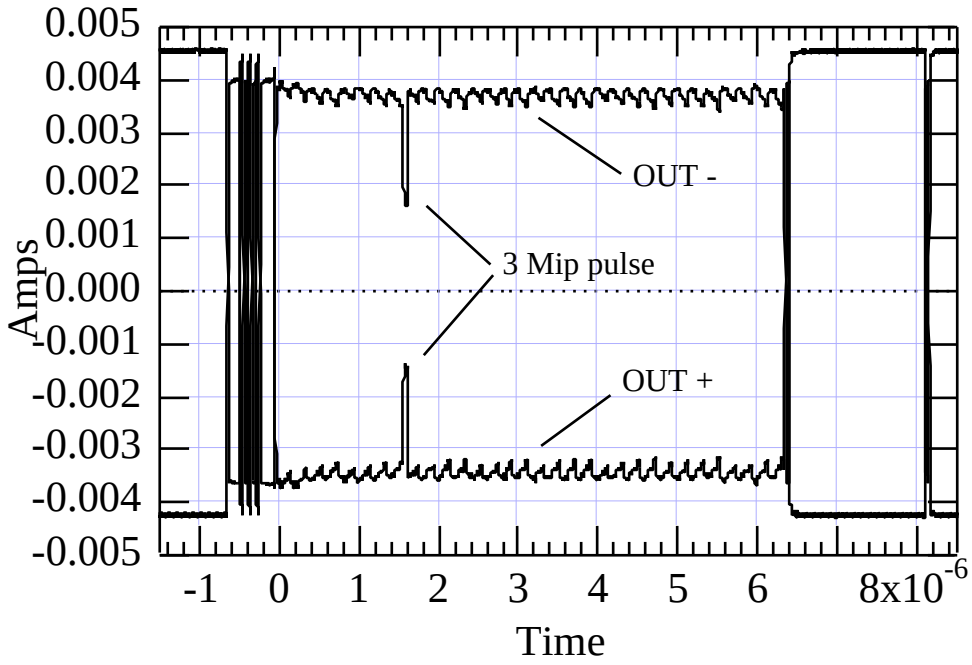


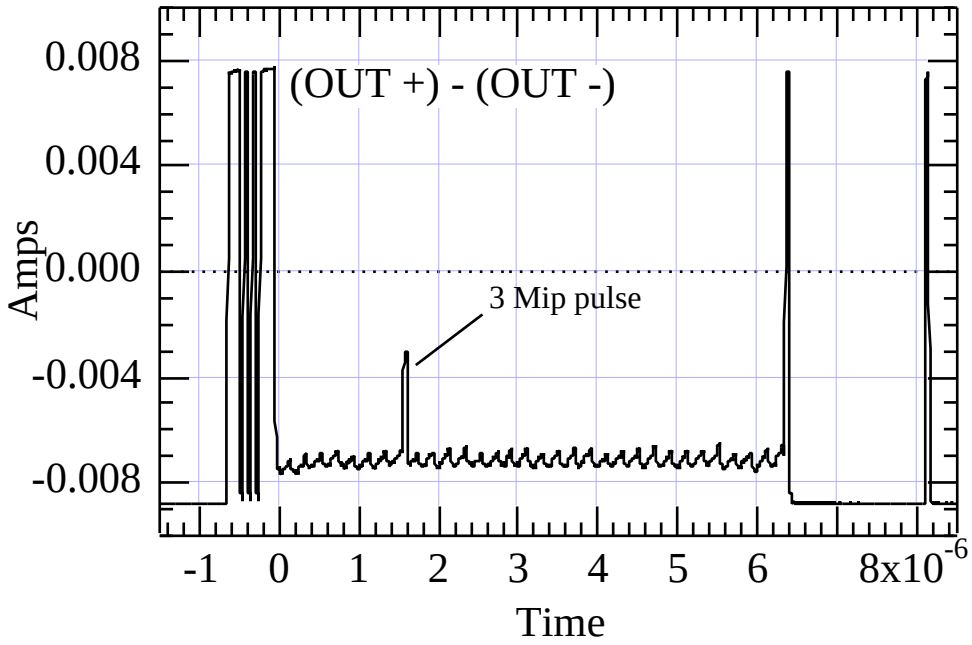
Output Data Frame (40 MHz MUX speed)

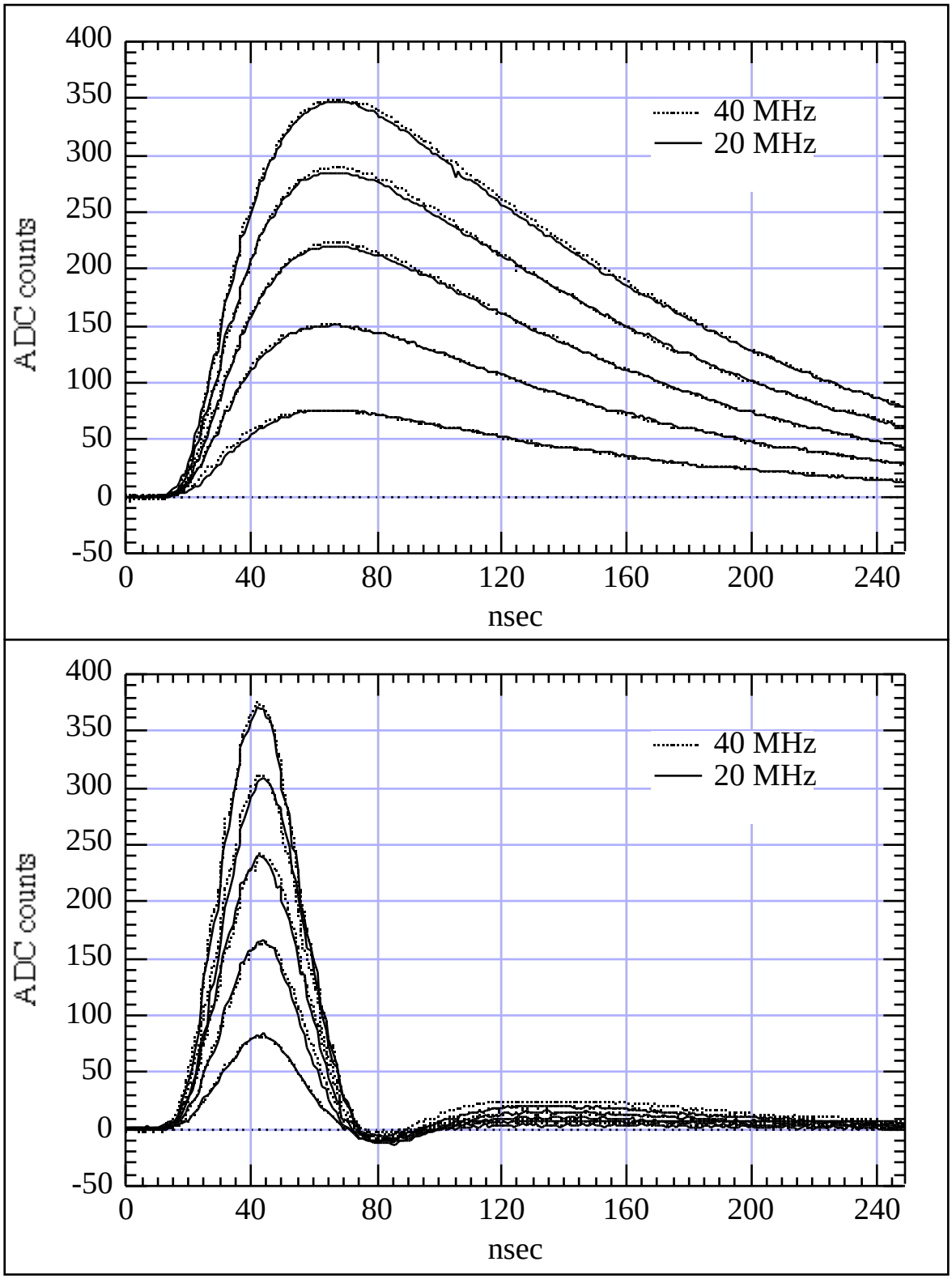


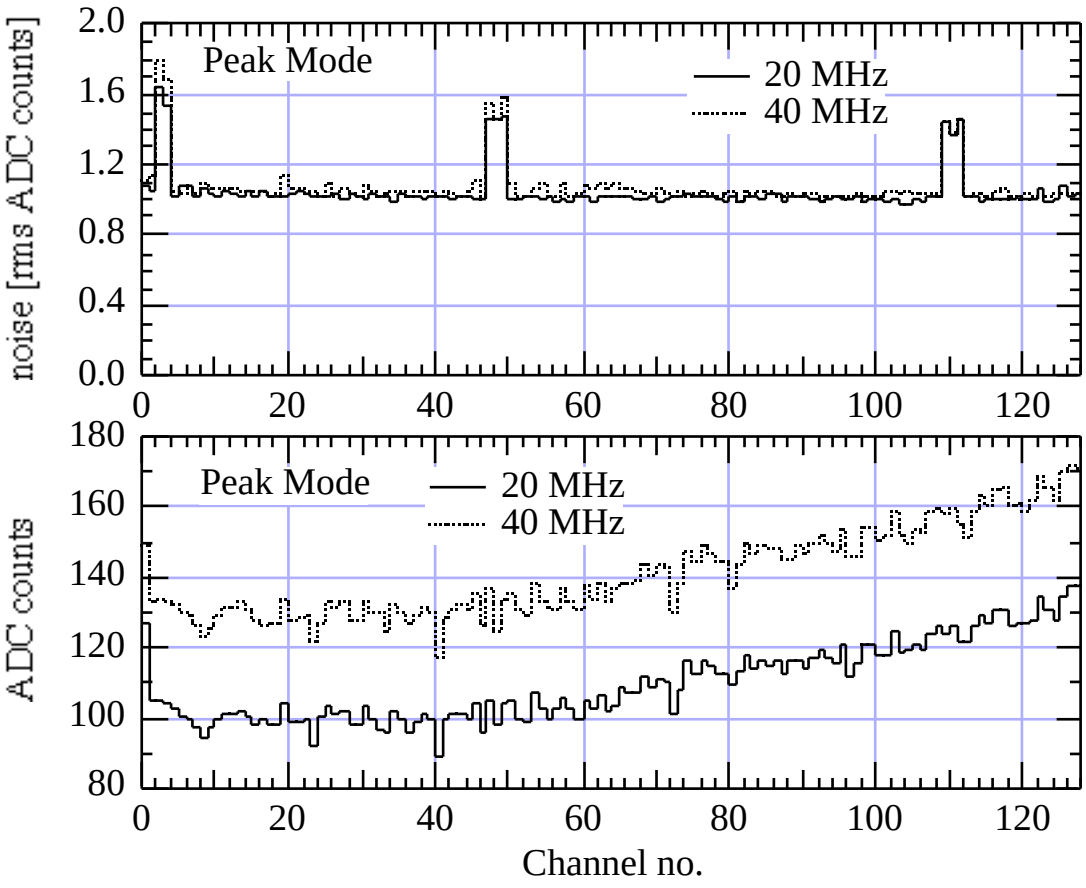


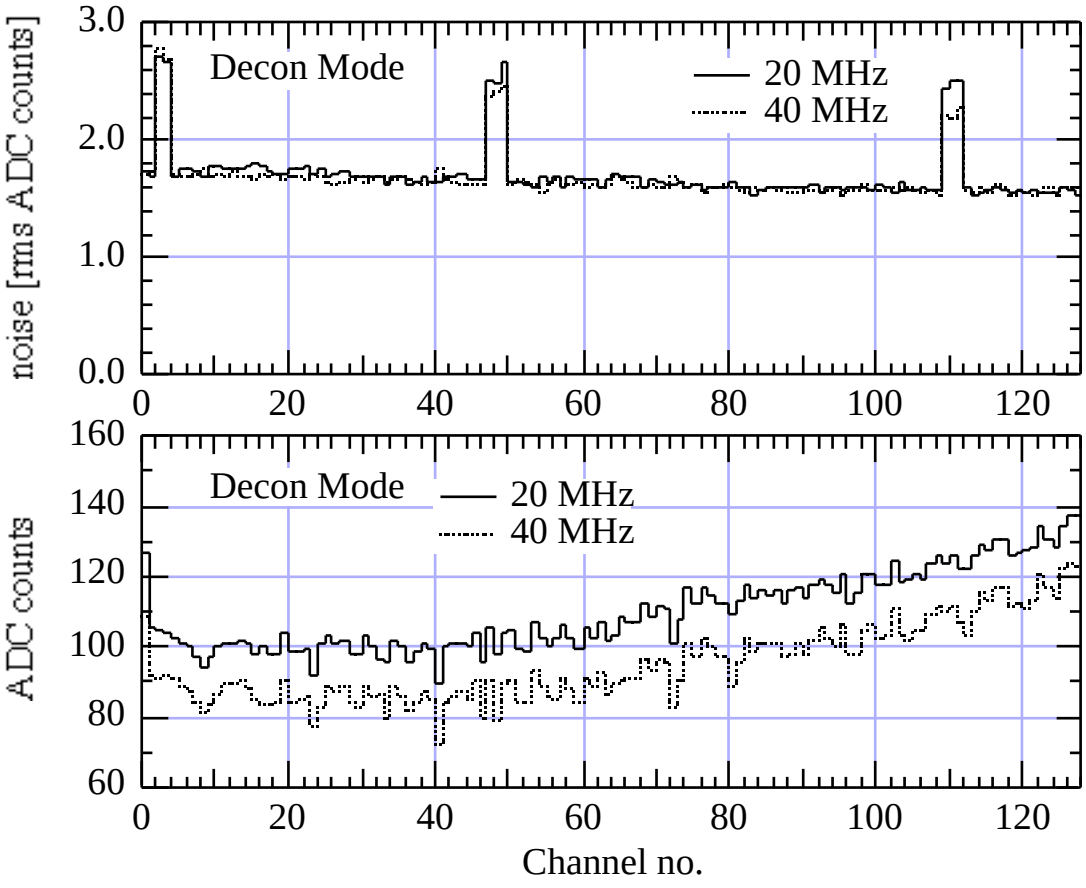
Output Data Frame (20 MHz MUX speed)

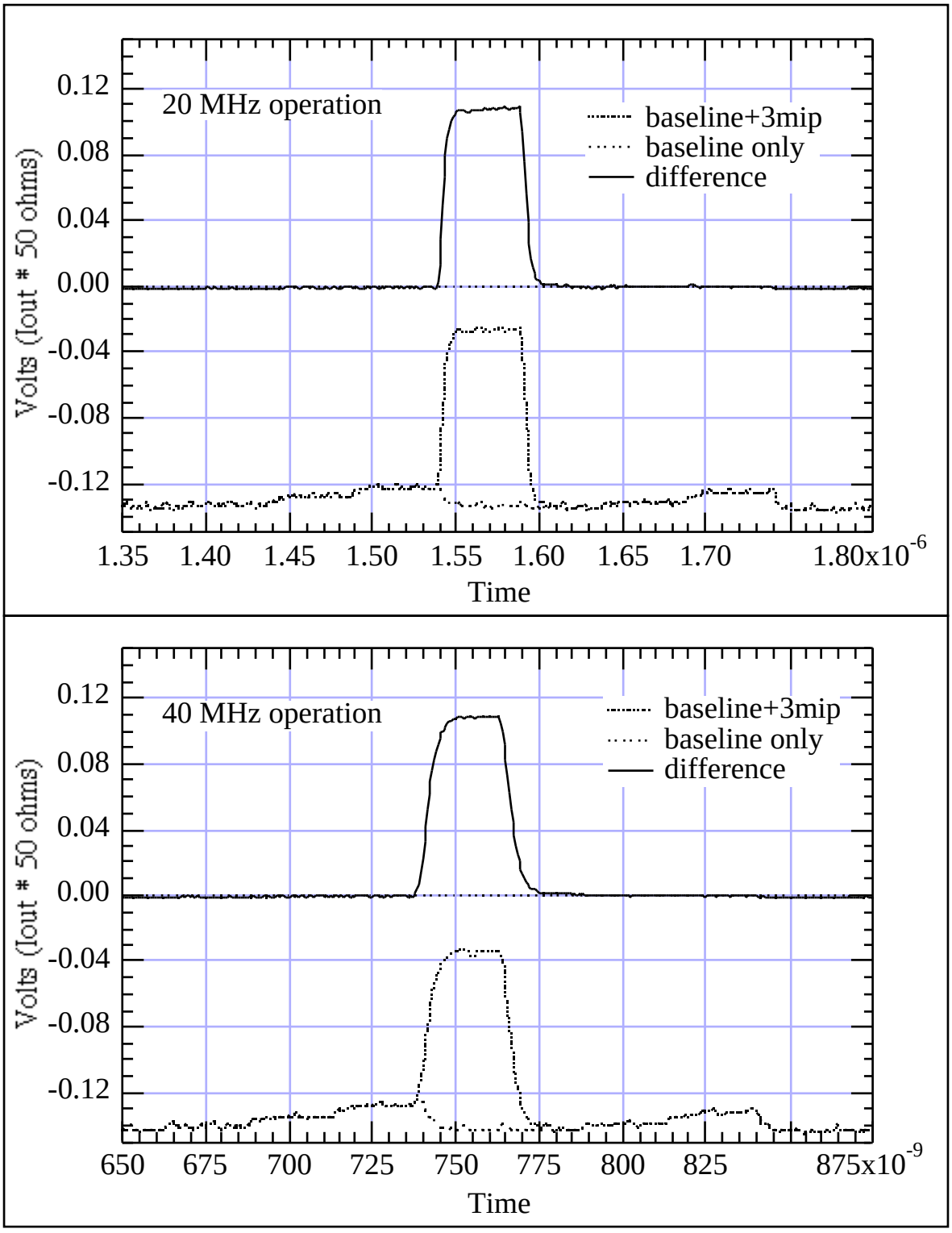




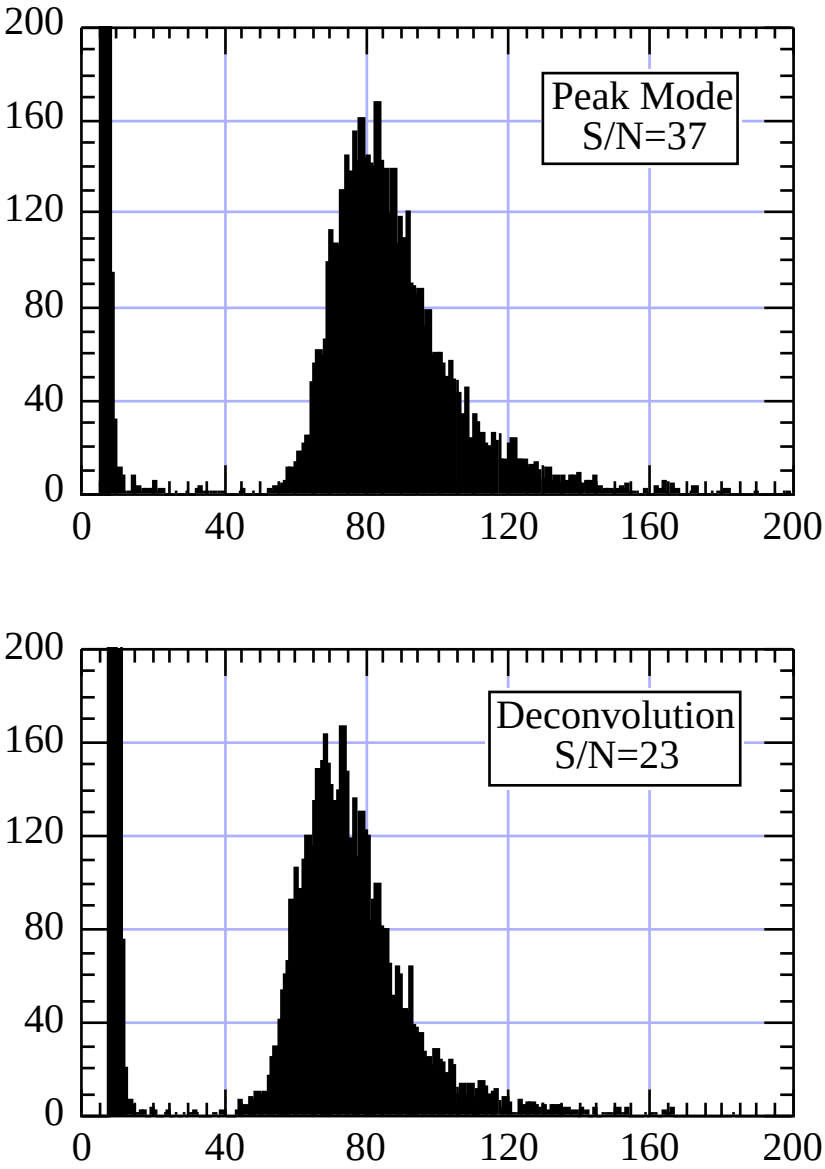

400
350
300
250
200
150
100
50
0
-50
ADC counts
0
40
80
120
160
200
240
nsec
40 MHz
20 MHz
400
350
300
250
200
150
100
50
0
-50
ADC counts
0
40
80
120
160
200
240
nsec
40 MHz
20 MHz


Peak Mode
20 MHz
40 MHz
noise [rms ADC counts]
ADC counts
Channel no.


Decon Mode
20 MHz
40 MHz
noise [rms ADC counts]
ADC counts
Channel no.


20 MHz operation
baseline+3mip
baseline only
difference
Volts (Iout * 50 ohms)
0.12
0.08
0.04
0.00
-0.04
-0.08
-0.12
1.35
1.40
1.45
1.50
1.55
1.60
1.65
1.70
1.80x10-6
Time
40 MHz operation
baseline+3mip
baseline only
difference
Volts (Iout * 50 ohms)
0.12
0.08
0.04
0.00
-0.04
-0.08
-0.12
650
675
700
725
750
775
800
825
875x10-9
Time

Sr-90 ß Pulse Height Spectra taken with APV25 bonded to Silicon Detector



5 cm Si detector, 350 µm thick, 50 µm strip pitch, 100 V bias.
Strip signal included in spectrum if no signal present in neighbouring strips.
Synchronization: scintillator trigger accepted if occurs within ~ 7 nsec of APV clock edge

Conclusions

Detailed results confined to a few chips so far

Very good performance for 1st iteration

Analogue performance close to expectation
=> accurate models

Noise good – hope to improve further

Pipeline good – gate capacitance works well

Radiation tolerance good to beyond requirements

Further work

Repeat measurements for more chips

Some features need deeper understanding (e.g. gain)\

Correct problems already identified

SEU studies (February – Legnaro)

Test structures need study
DC/MSGC amplifiers, APSP+pipeline test structure

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