APV25 Production Testing Status

Outline

Yield studies

current status of ongoing investigations into causes of low yield on latest and previous production lots

Future production plan

Mark Raymond, Imperial College

History - 2002

Jan 1st two production lots showed low yield
manufacturer found evidence of problems with silicide layer
– both lots returned for replacement

March 3rd lot -> much better, 79% yield (few patchy wafers)

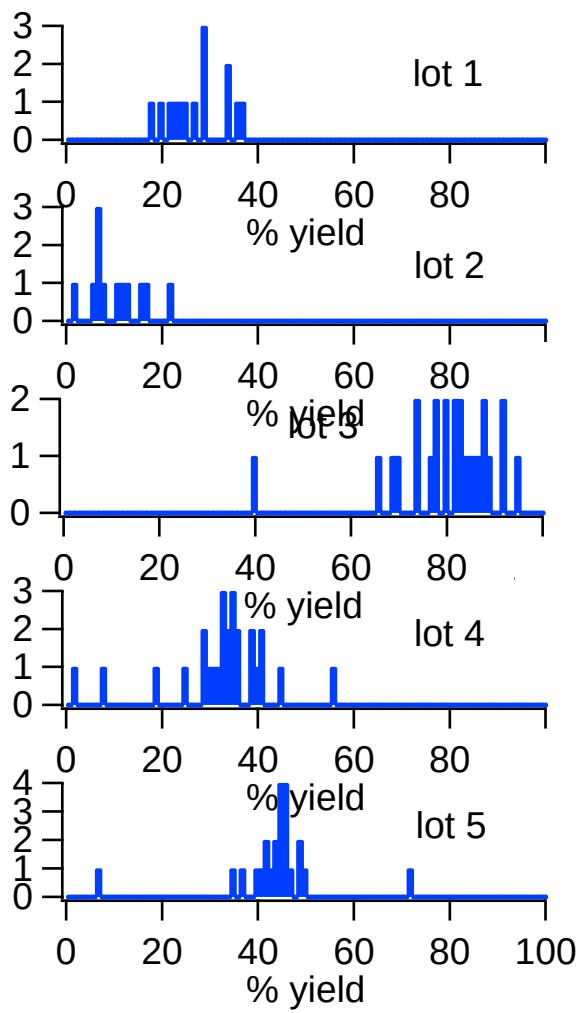
May 4th and 5th (replacements for 1 and 2) -> 33% and 44%
=> still some processing problem

other HEP designs also experiencing variable yield
causes unclear but long metal lines common to HEP designs
(possible ESD damage during processing due to antenna effect)

Sept Test structures (CERN) included on MPW run to try and prove/disprove theories

Nov MPW run back -> all structures showing high yield
no sig. difference between “low expected” and “high expected” yield designs => nothing proven

see http://www.hep.ph.ic.ac.uk/~dmray/pptfiles/CMS_TK_ELEC_July2002.ppt
and http://www.hep.ph.ic.ac.uk/~dmray/pdffiles/APV_LECC02_HEP.pdf

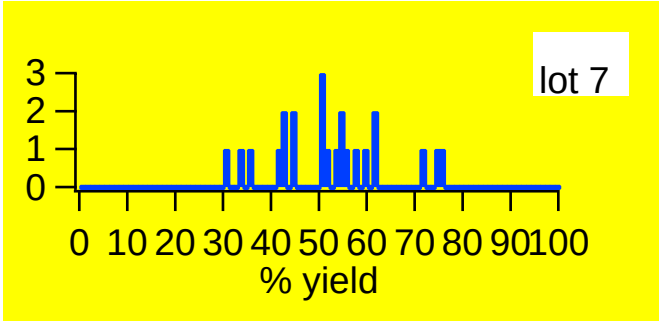


Up to date - 2003

Jan: APV lots 6 and 7 delivered

lot 7 -> average 52%, but lot 6 close to zero

manufacturers notified (via CERN)



Feb: wafers from all 4 lower yield lots sent for failure analysis (FA)

weekly telephone conference set up to monitor progress including participants from:

Manufacturers: FA teams on 2 sites

Imperial and RAL: APV design and test

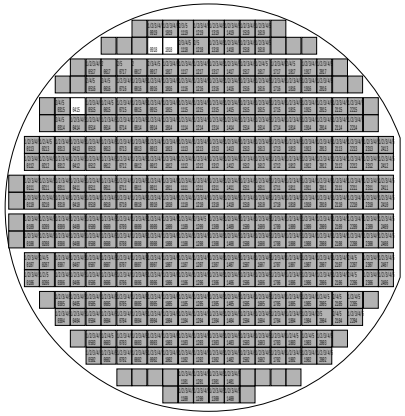
CERN: coordinating team and Medipix engineers

(Medipix project also experiencing yield problems on several lots – design not very similar to APV but might be common root cause – understood on all sides that FA on APV takes priority)

Problem Lots

lot 4 – ave. yld. 33%

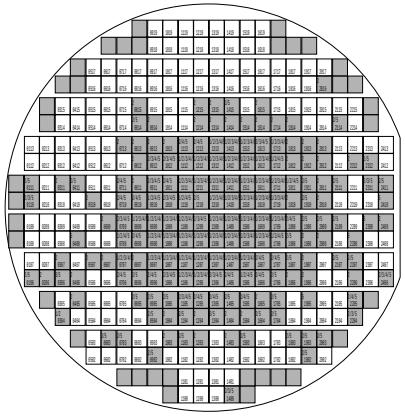
Wafer Map: WG8P4CT



Date probed:	Wed 26 Feb 2003
Chips passed:	3/360
Yield:	1%
Digital failures:	351
Power supply failures:	1
Channel defects (Peds & Cal):	4
Pipeline defects:	1

lot 5 – ave. yld. 44%

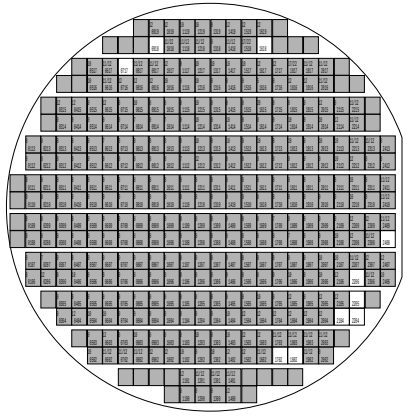
Wafer Map: W28P77T



Date probed:	Thu 27 Feb 2003
Chips passed:	170/360
Yield:	47%
Digital failures:	111
Power supply failures:	1
Channel defects (Peds & Cal):	77
Pipeline defects:	1

lot 6 – ave. yld. ~ 0%

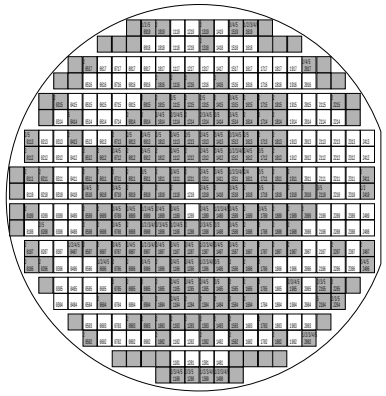
Wafer Map: A7BCG1T



Date probed:	Wed 29 Jan 2003
Chips passed:	10/360
Yield:	3%
Digital failures:	220
Power supply failures:	7
Channel defects (Peds & Cal):	123
Pipeline defects:	0

lot 7 – ave.yld. 52%

Wafer Map: KKM3K2T



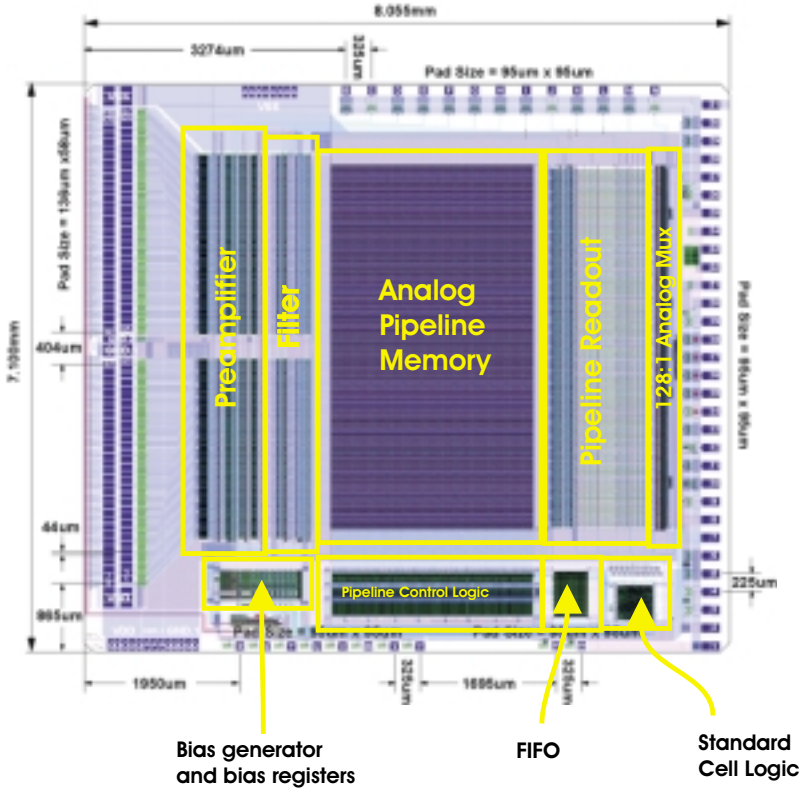
Date probed:	Tue 18 Feb 2003
Chips passed:	150/360
Yield:	42%
Digital failures:	77
Power supply failures:	2
Channel defects (Peds & Cal):	127
Pipeline defects:	4

sample wafers from each of 4 problem lots sent to manufacturers failure analysis team

Lot 4 wafer extreme example but hopefully indicative of failure mode of other wafers in same lot
other wafers from this lot already with hybrid company

to assist failure analysis wafers re-probed with modified test protocol – trying to extract as much info as possible from failing sites

Modified wafer test protocol



test continues to end even if gross defect found early on to provide as much info as possible to FA team

sort failures into 5 categories:

- power
- channel (pedestal or response to CAL)
- bias register (stuck bits)
- pipeline logic (digital header incorrect)
- other digital

try to associate failure with particular functional area on chip

high power failure can be useful in localising faults

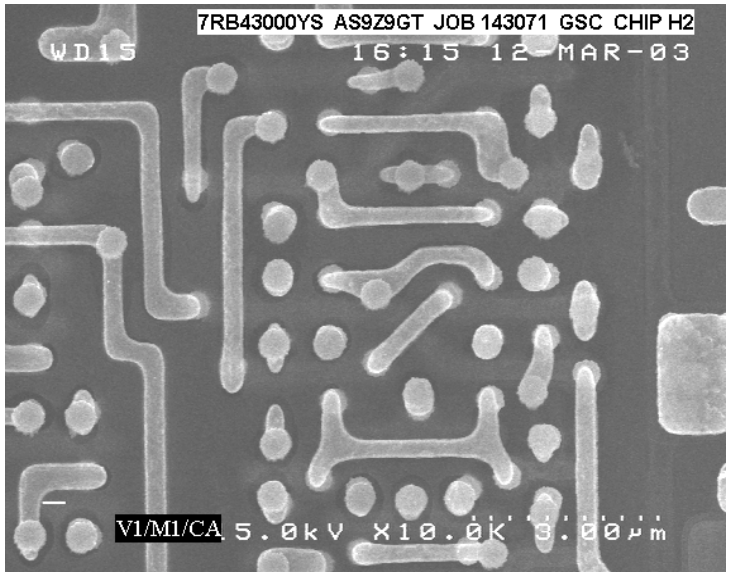
chips can (and often do) fail on more than one (sometimes all) categories

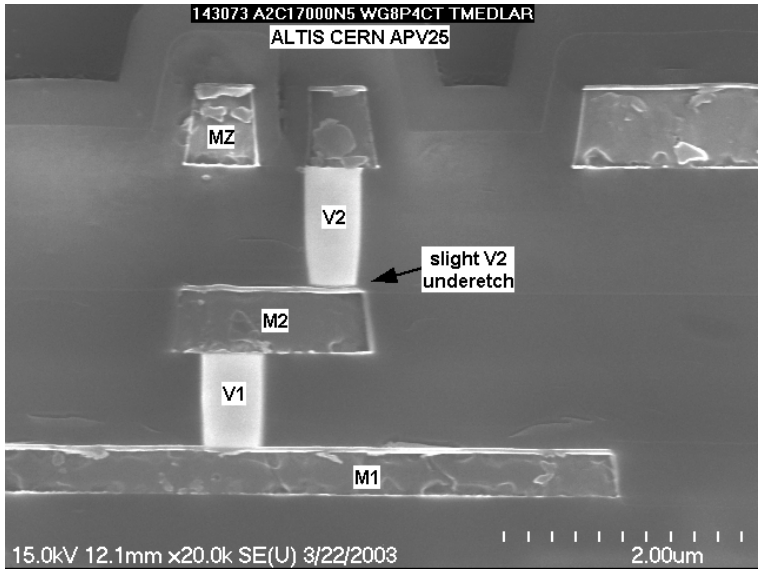
Failure Analysis (FA) techniques

liquid crystal
- wafer coated with temperature sensitive layer
- probes used to apply power to a particular chip
- coating changes colour over any hot spots – allows localization of fault

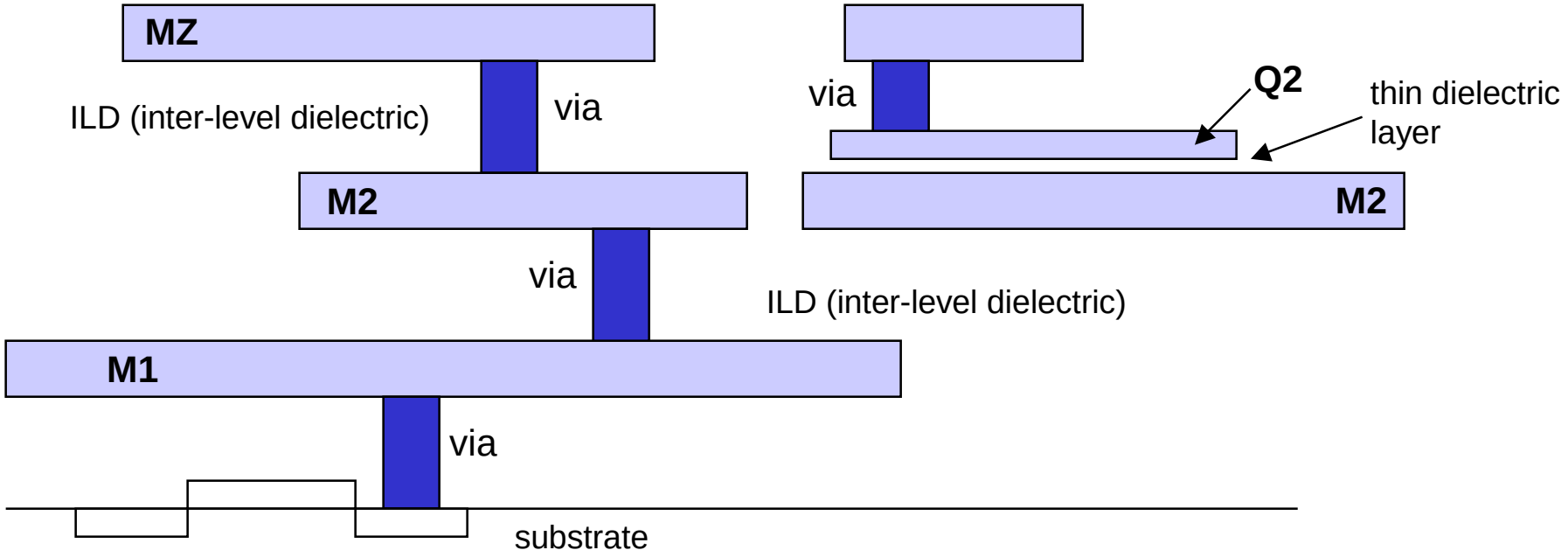
delayering (top down)
- gradual removal of layers, looking for problems along the way

cross section
- cut through wafer in suspect location





Metallization X section



APV uses 3 metal layers (up to 6 possible)

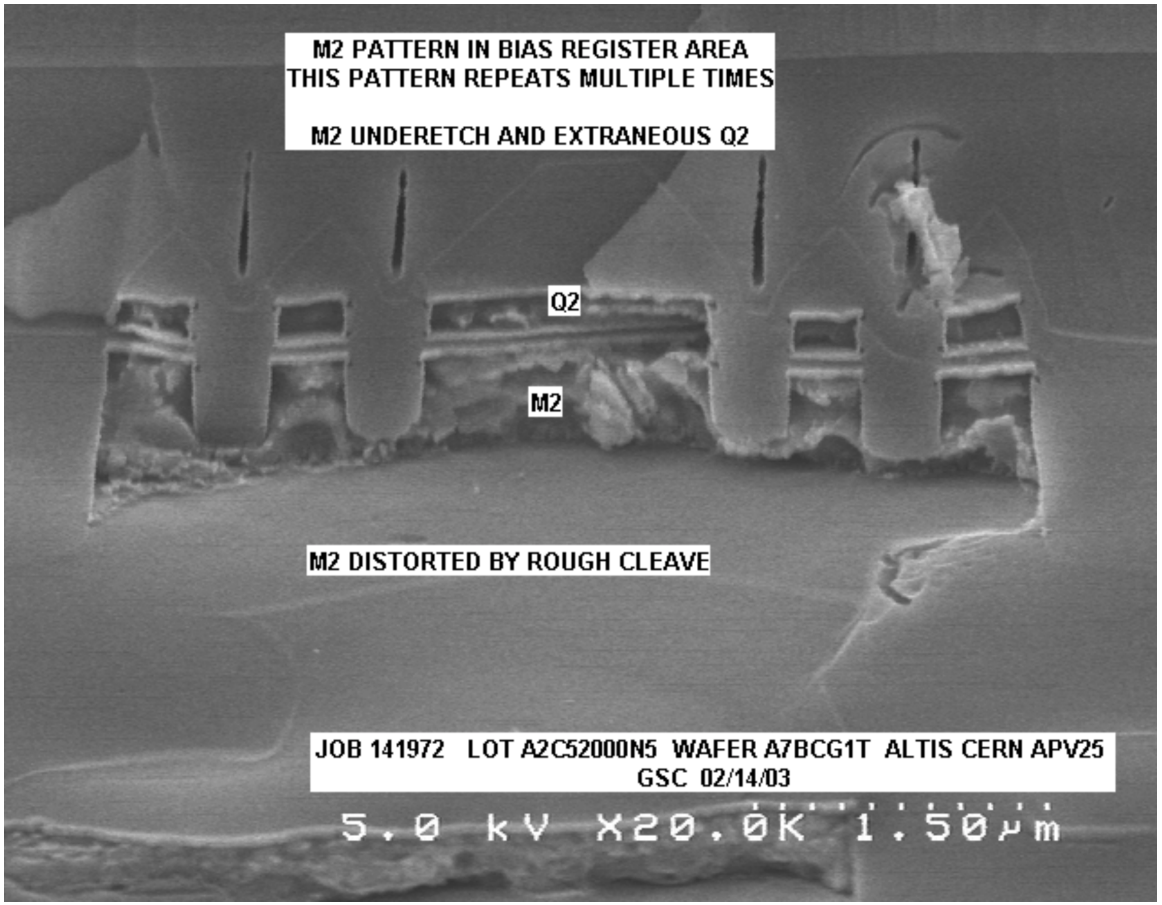
floating capacitors implemented by Q2/M2 structure – only used in analogue parts of chip

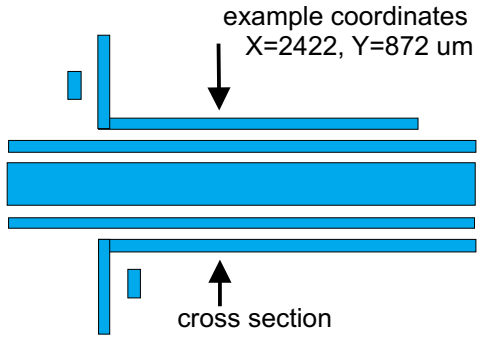
production process divided into 2 distinct phases

Front end of line – transistors defined

Back end of line – metal layers and interconnecting vias added

Fault Diagnosis – Lot 6





severity of problem with this lot allowed fairly rapid diagnosis

X-section through metal tracking shows shorts between tracks, and Q2 (capacitor top-plate metal) where it shouldn't be

Q2 should have been stripped off (in areas where it is not supposed to be) prior to patterning of underlying M2

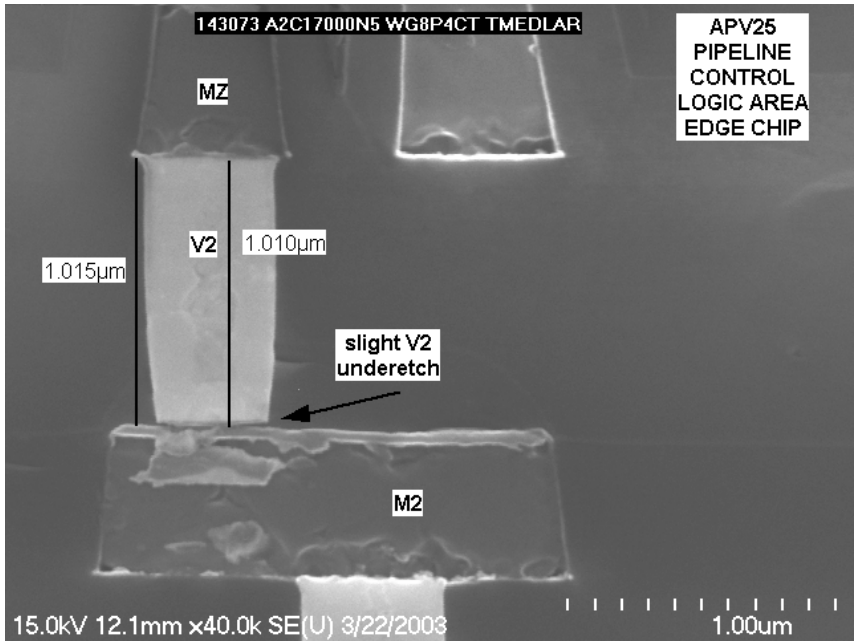
problem thought to be incomplete removal of photo-resist layer used to pattern Q2

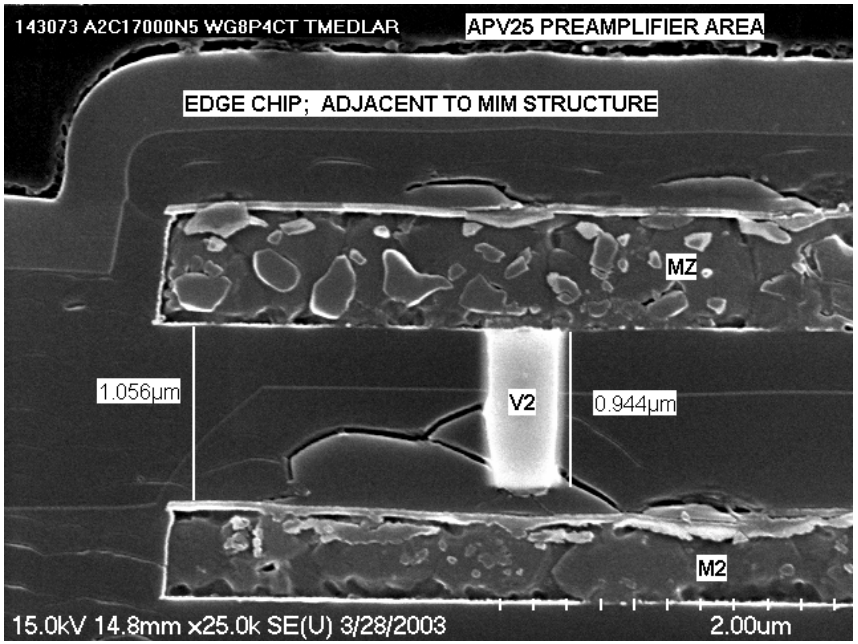
=> Q2 layer not removed properly (in areas where it should be)

=> subsequent M2 etch had to go through Q2 first and so didn't get all the way through

Fault Diagnosis – lot 4

this wafer showed high power consumption failures – liquid crystal technique showed hotspots in pipeline control logic area





non-contacting vias => transistors which should be **off** can float to **on** condition => high power consumption

reasons for via underetch not clear, but separation between metal layers close to maximum allowed
=> points to possible problem with Inter-Level Dielectric (ILD) layer thickness control (etch time is fixed)

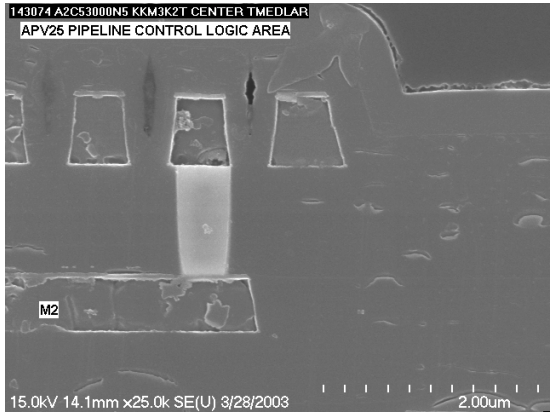
this problem now confirmed on chips in centre and at edge of wafer

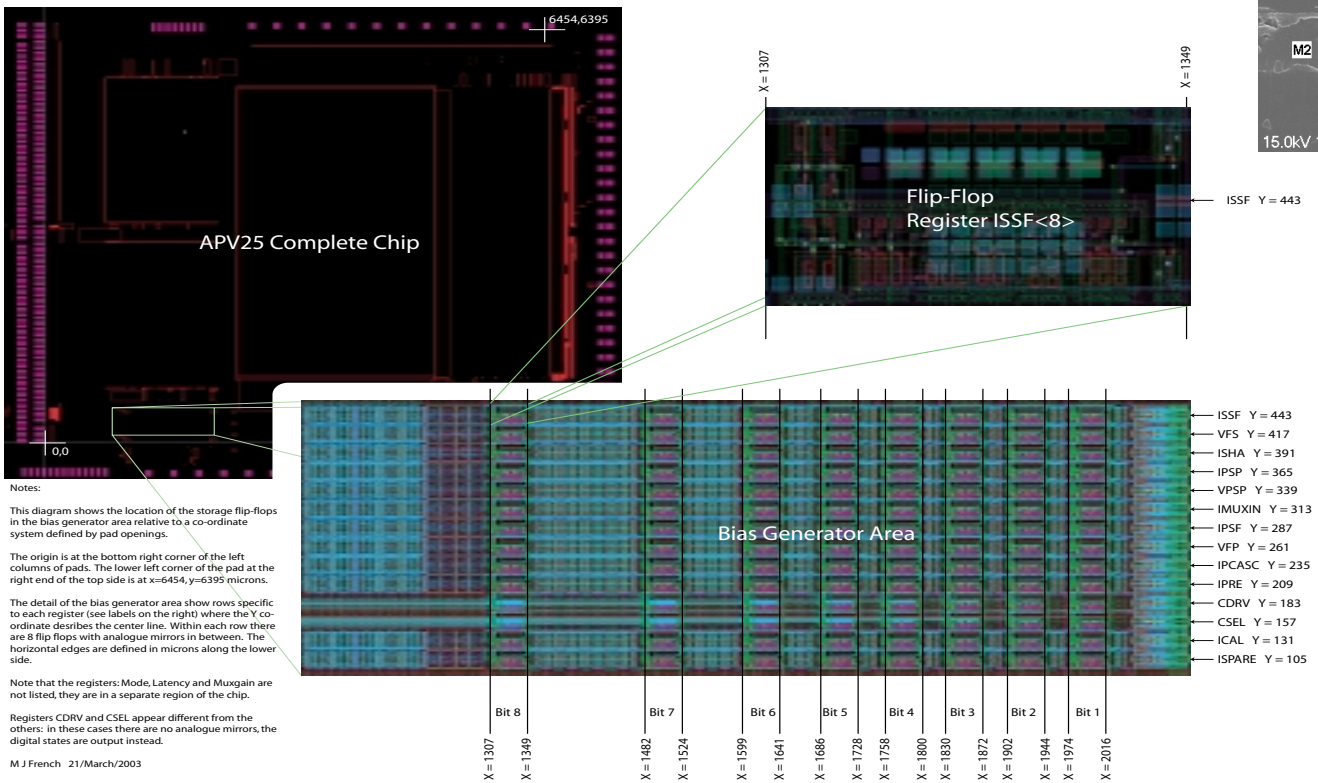
Fault Diagnosis – lots 5 & 7

lot 7 wafer FA just started - this lot showed average 52% yield, so not such severe problem

no definite problem found so far (but ILD thickness also large)

physical coordinates of stuck bit locations in bias registers provided for both these lots – may be helpful





APV Production Plan

no. of wafers	latest delivery date	
24	June 03	
24	July	
48	Sept.	
48	Oct.	
48	Nov.	**2003**
48	Jan 04	**2004**
48	Feb.	
(48)	(March)	

288 (336)

wafer volume will cover our needs assuming 60% yield
~ 62,000 (72,500) chips

~ 40 wafers/month
high but manageable, 2 wafers/day

Summary

Progress in understanding causes for low yields

2002 lots

Lot 4 (33%): V2 underetch (non-contacting vias), ILD thickness close to maximum
Lot 5 (44%): not yet begun

2003 lots

Lot 6 (~0%): M2 layer shorts and extraneous Q2 metal layer
Lot 5 (52%): FA started, no problem found so far, but ILD thickness also large

Manufacturer's efforts have been substantial, still ongoing

All problems identified so far associated with "back-end-of-line" production phase

2 free production lots offered and now in fabrication (delivery in ~ few weeks time)
foundry proposes to vary ILD thickness (5 steps between process extremes) on one lot with additional measurements after each ILD stage

=> lower overall yield for this lot but valuable information for further production

hope that results of these studies will lead to reduction of low-yield lots