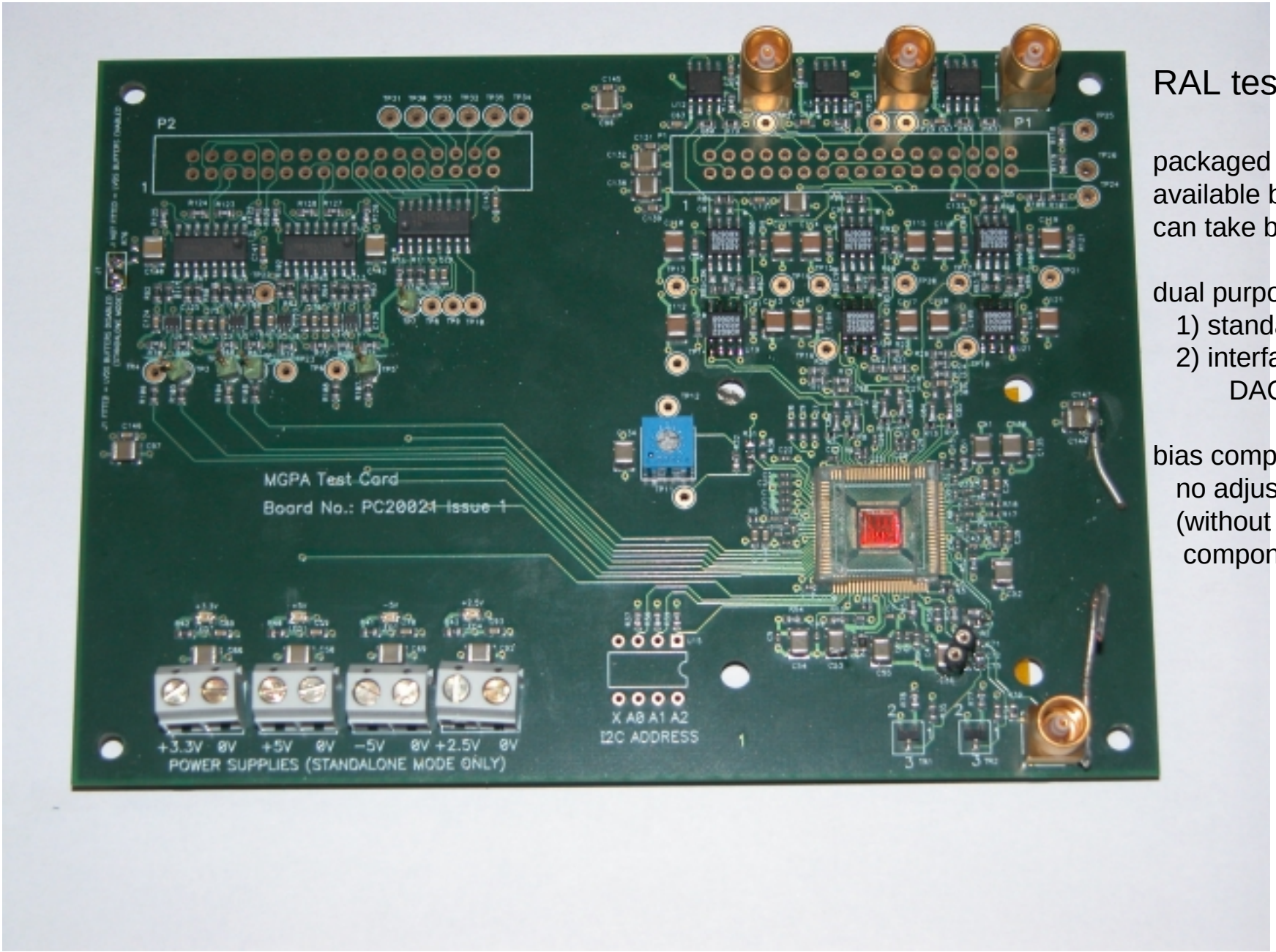
MGPA first results

testing begun 29th May on bare die (packaging still underway)

two chips looked at so far – both working (all results here from one only)

OUTLINE

- test setup description
- analogue performance
  - gain
  - linearity
  - matching
  - noise
- I2C offset adjust
- calibration feature
- power consumption



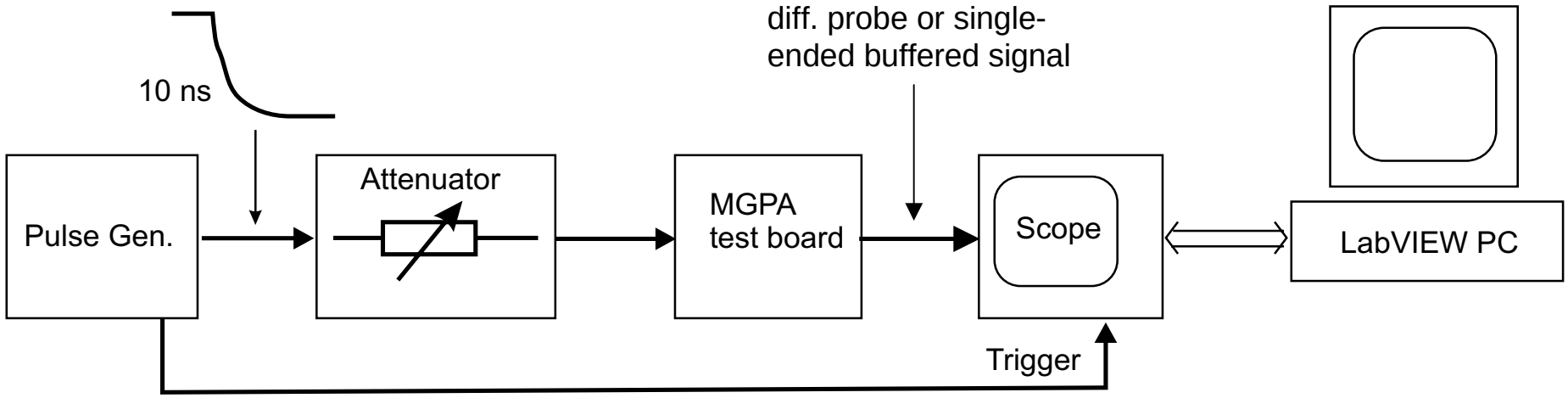
RAL test board

packaged chips not yet available but RAL board can take bare die

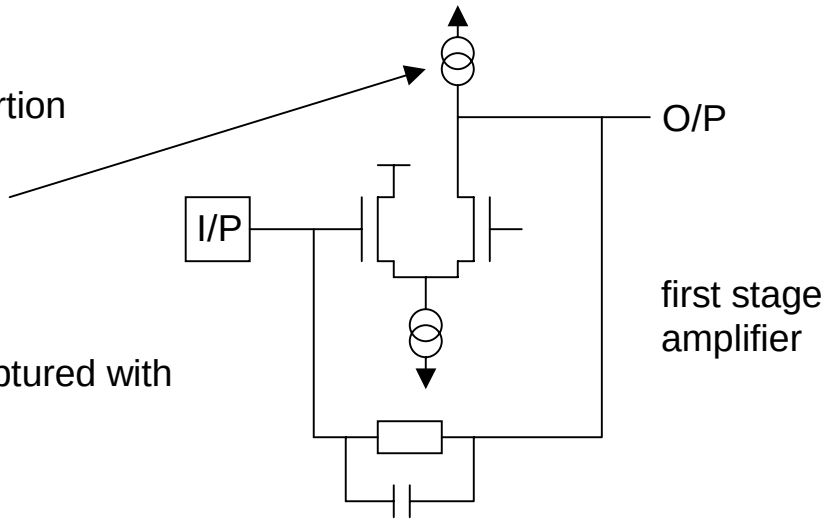
dual purpose design
1) standalone–used here
2) interface to standard DAQ system

bias components fixed – no adjustment possible (without changing 0402 components)

Test setup for pulse shape measurements



note: very fast risetime charge injection -> pulse shape distortion on rising edge due to slew rate limitation at O/P of first stage current source magnitude OK for 10 nsec exponential edge



Scope averaging -> 16 bit resolution. Multiple waveforms captured with different DC offsets to remove scope INL effects.

Pulse shapes – low gain channel

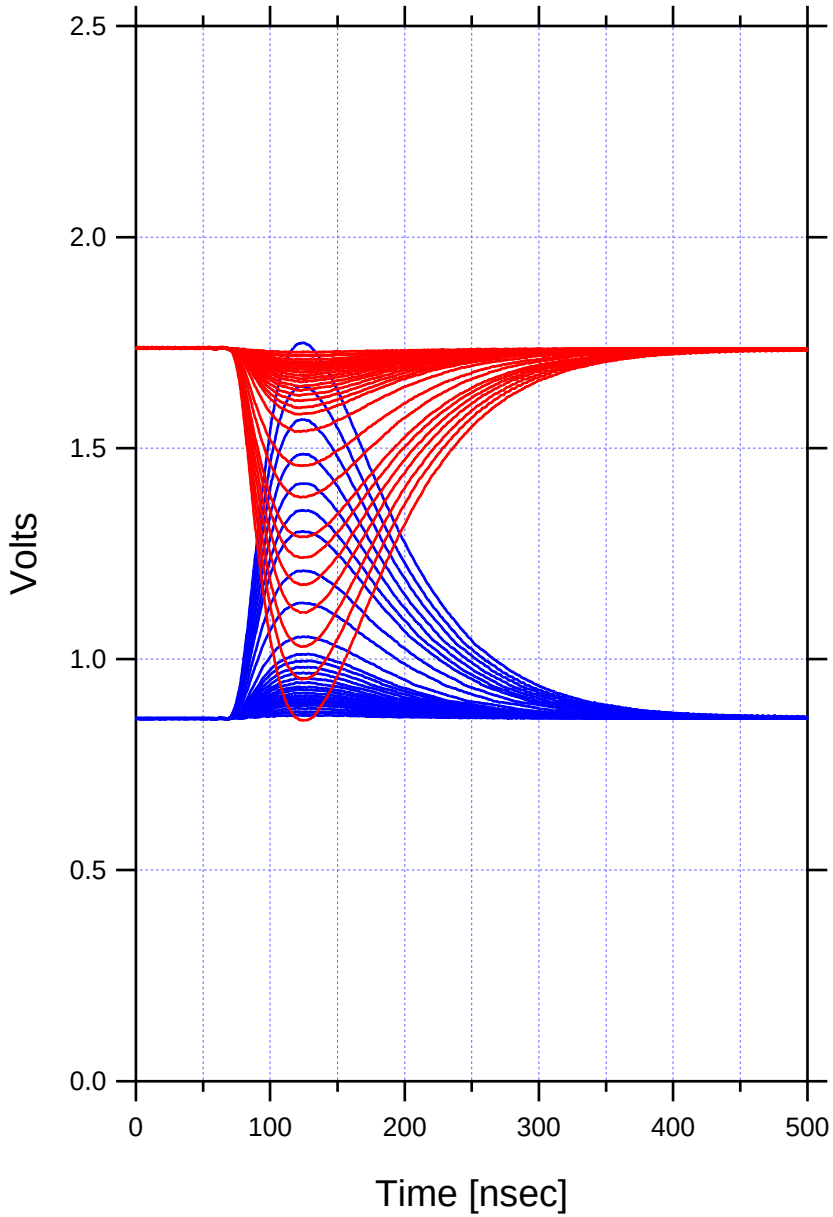
signals up to 60 pC (feedback components for barrel application: 1.2k//33pF)

steps not equally spaced (log attenuator)

2 active probes on +ve and –ve outputs (before any buffering)

linear range +/- 0.45 V around Vcm (1.25 V nom.)

note: Vcm defined by external pot'l divider (5% resistors) so not exactly 1.25 V

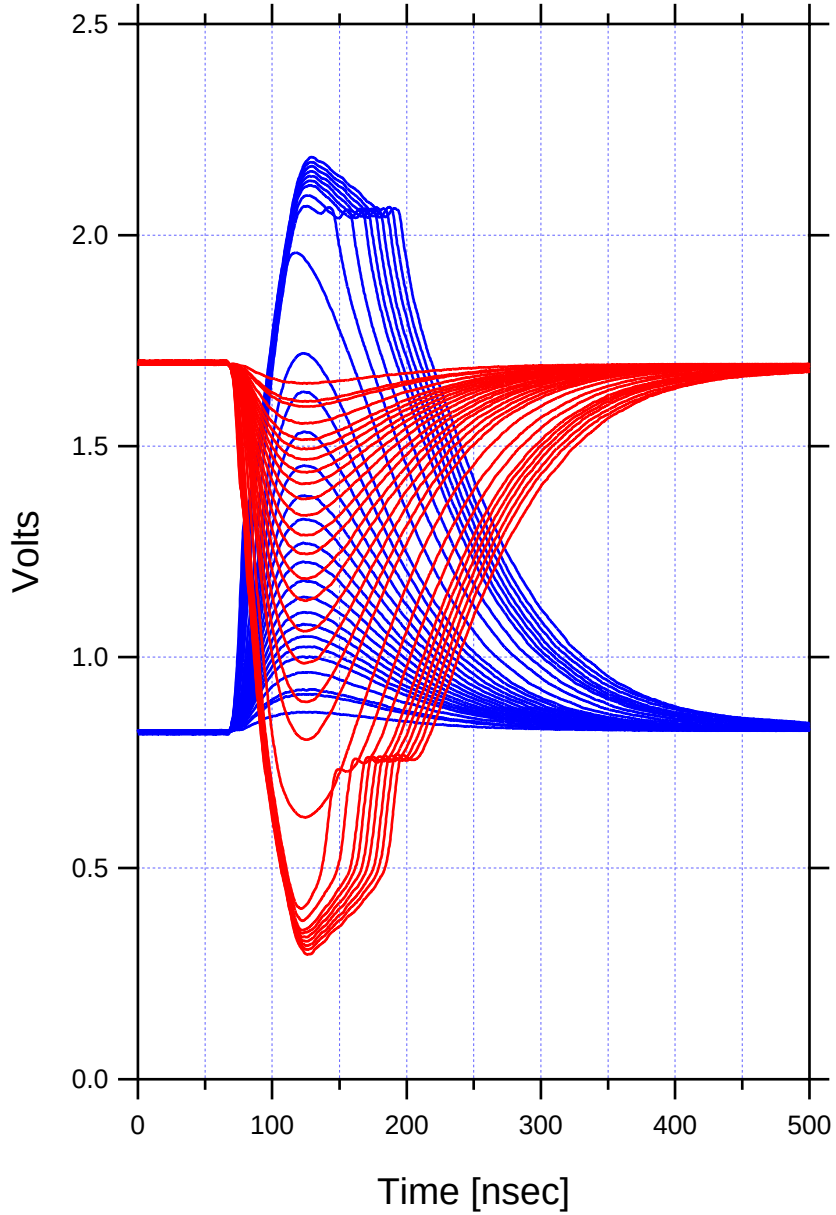


Pulse shapes – mid gain channel

same signal steps as before (up to 60 pC)

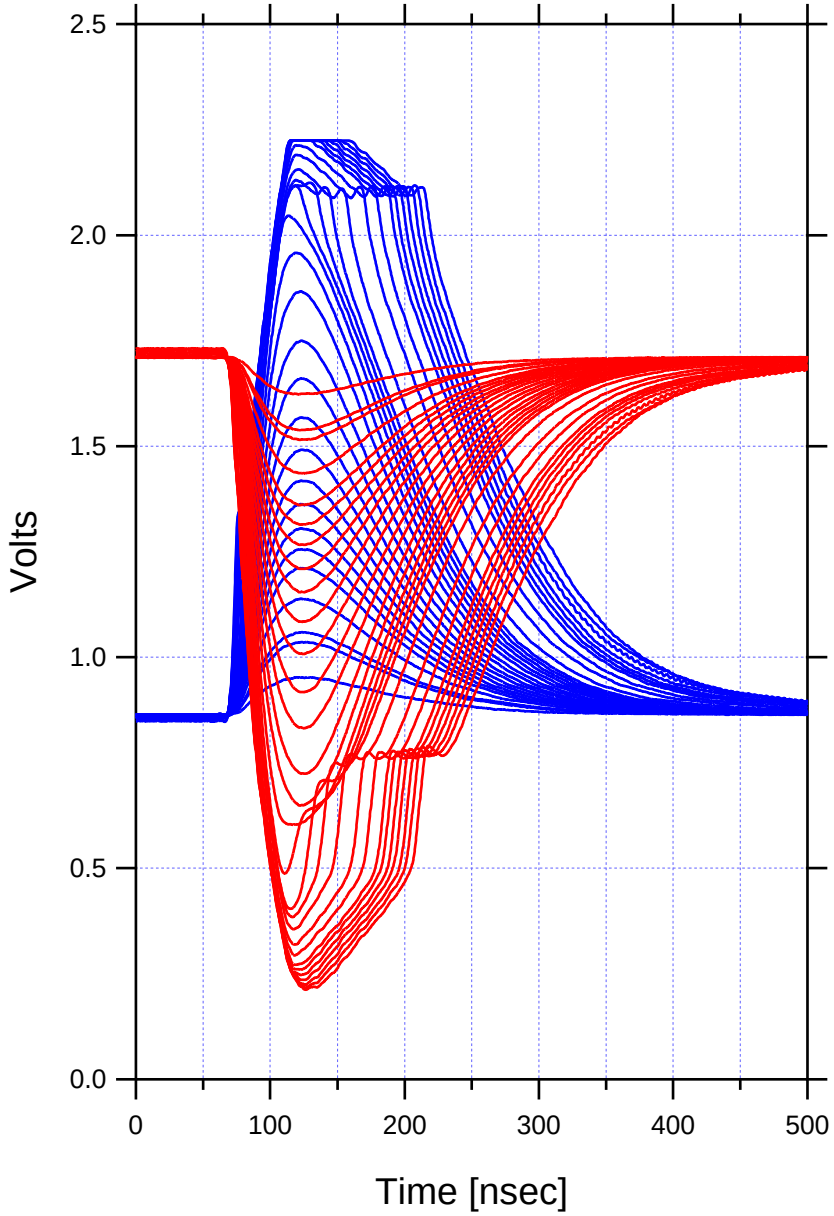
this range only linear up to ~ 10 pC

shows saturation effects for out of range signals

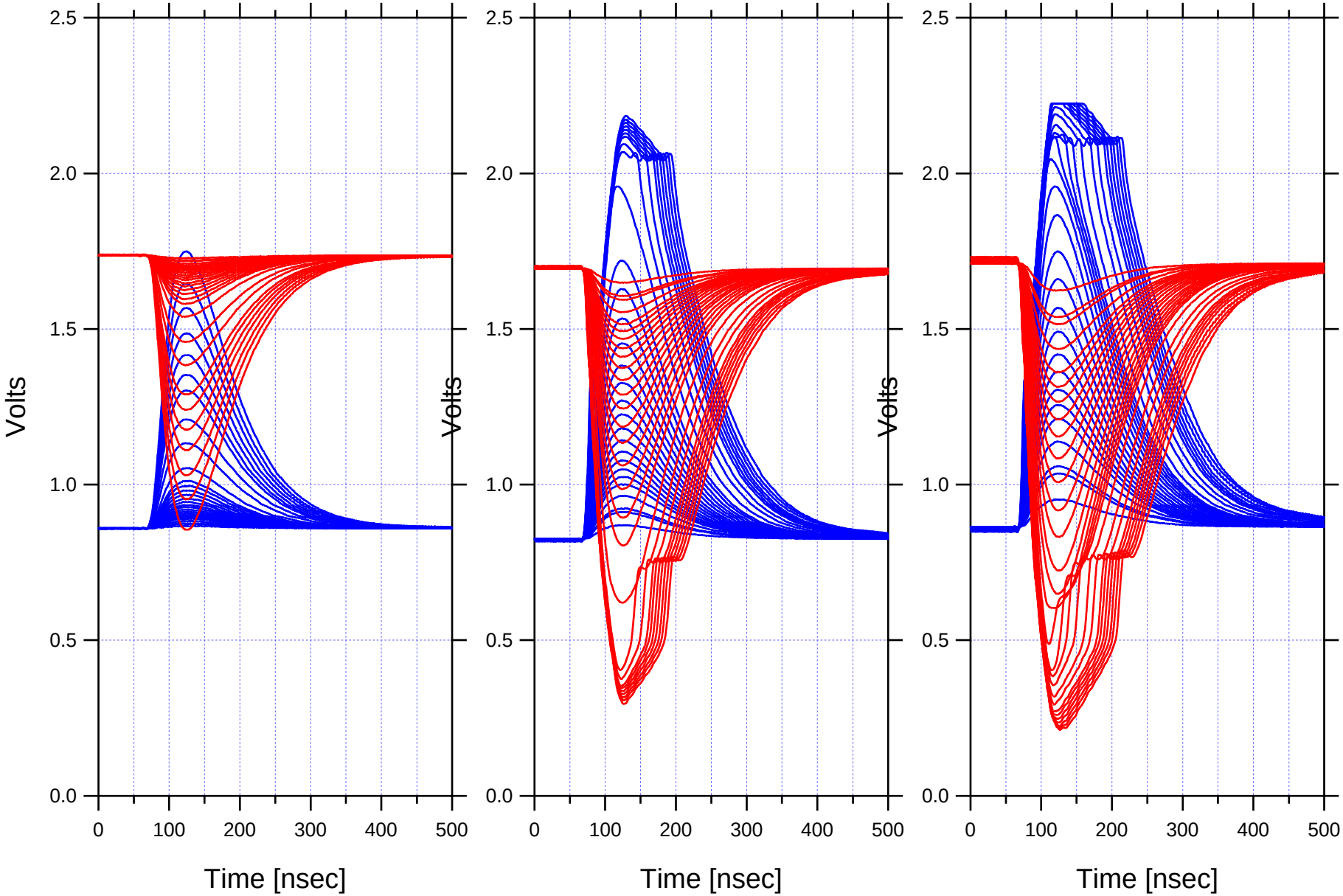


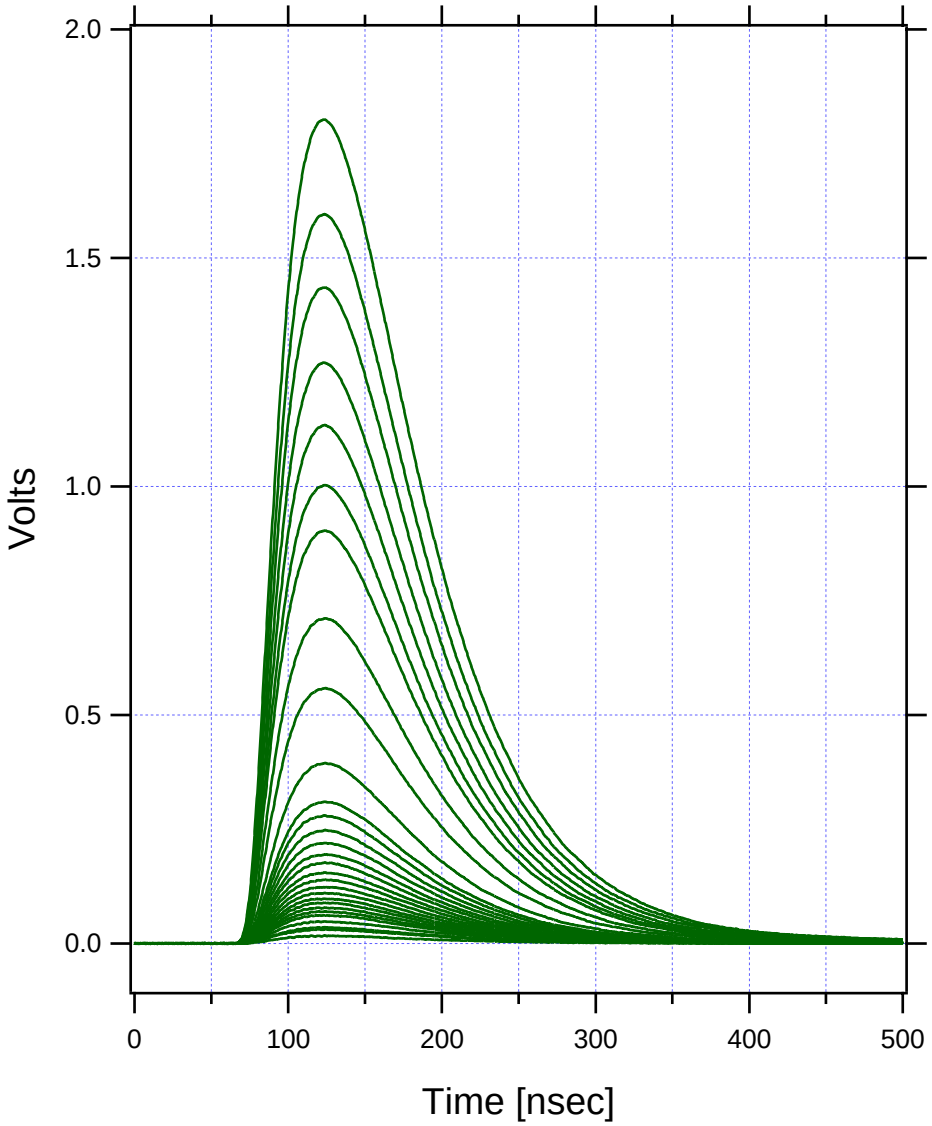
Pulse shapes – high gain channel

this range only linear up to ~ 5 pC



Pulse shapes – all 3 gain ranges for comparison





Differential pulse shape – low gain channel

differential probe on chip outputs (before buffering)

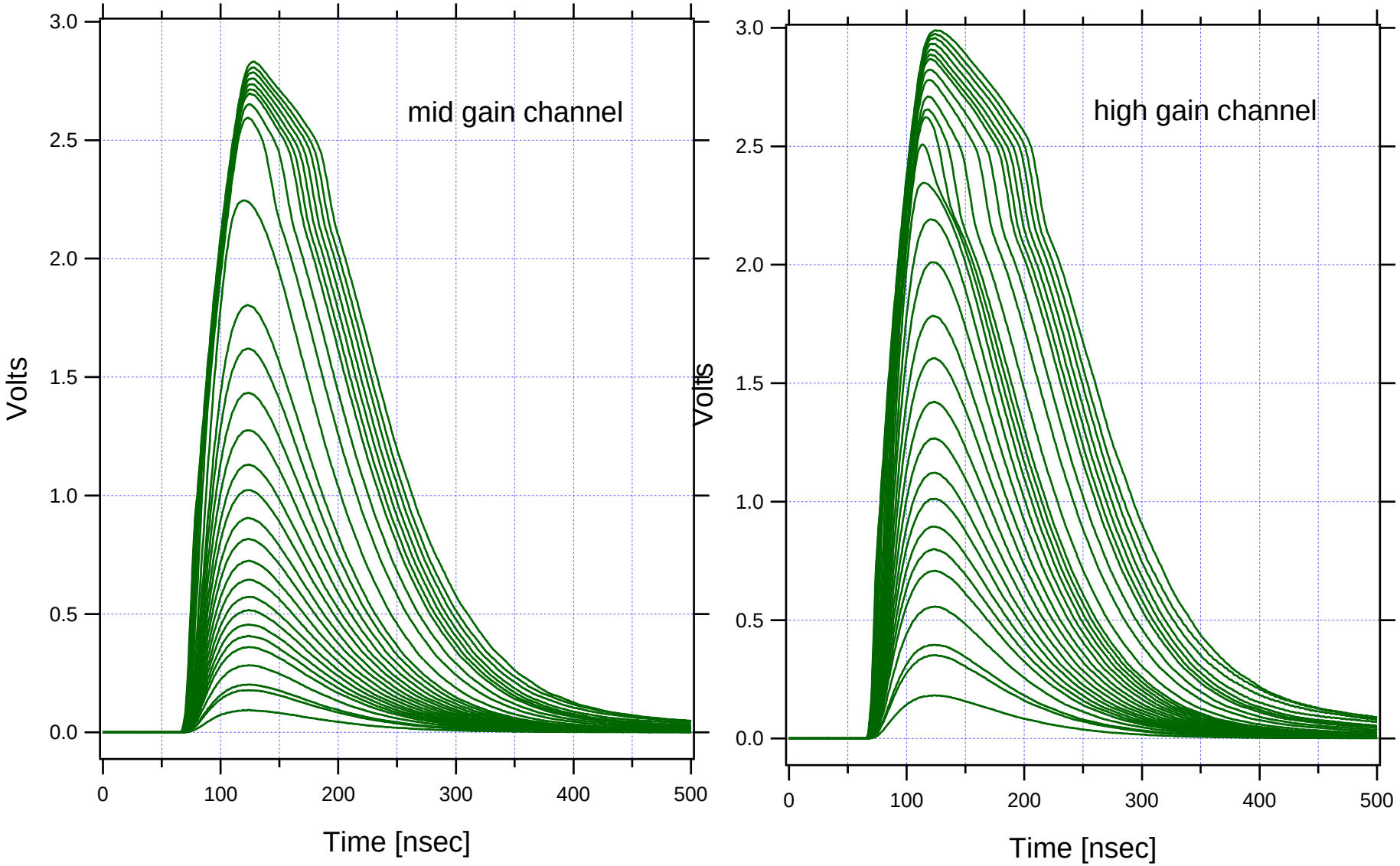
60 pC fullscale signal as before

differential swing +/- 0.45 V around Vcm
corresponds to ~1.8 Volt linear range

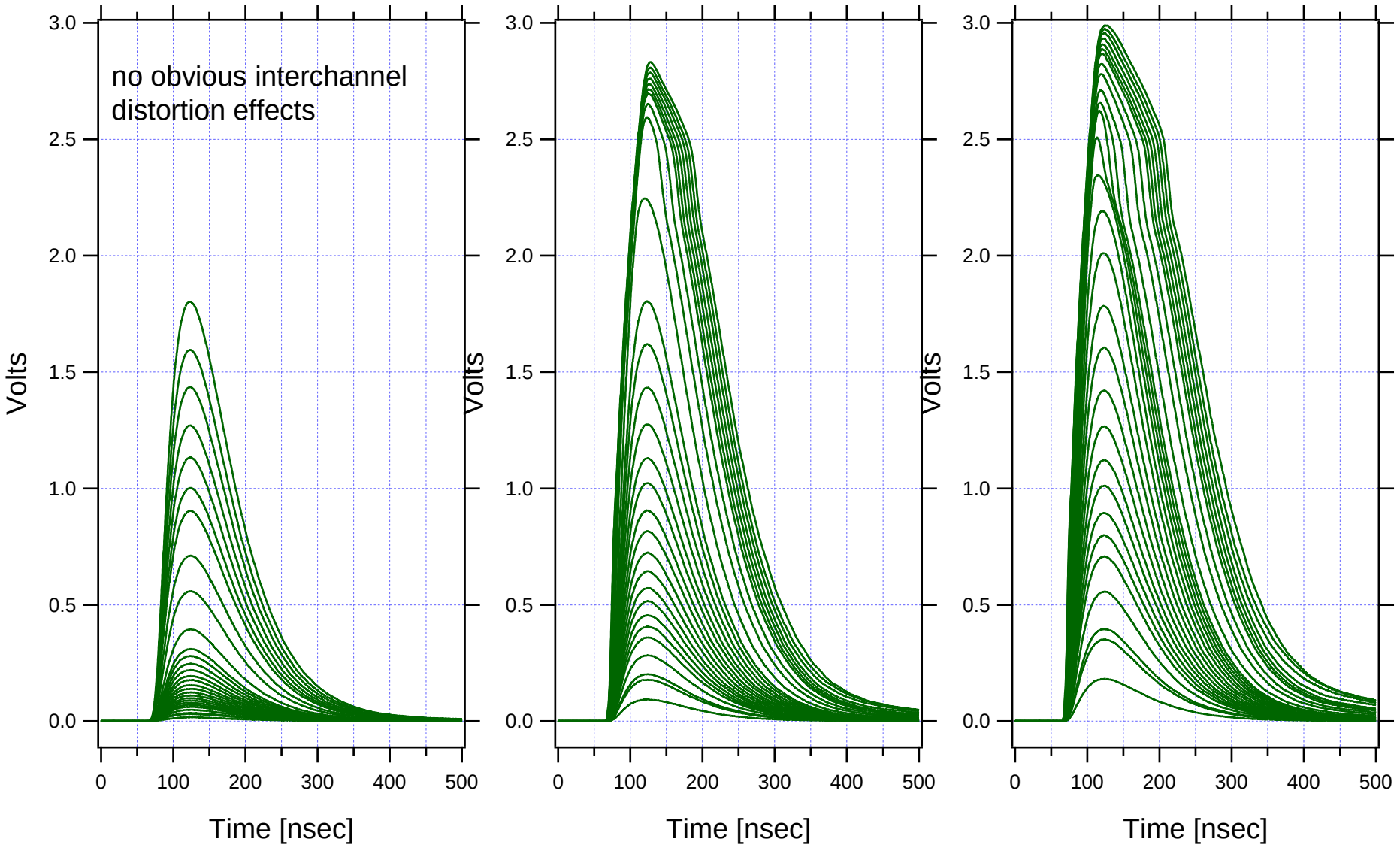
pedestal subtracted

no “obvious” pulse shape distortion due to higher gain channels saturating

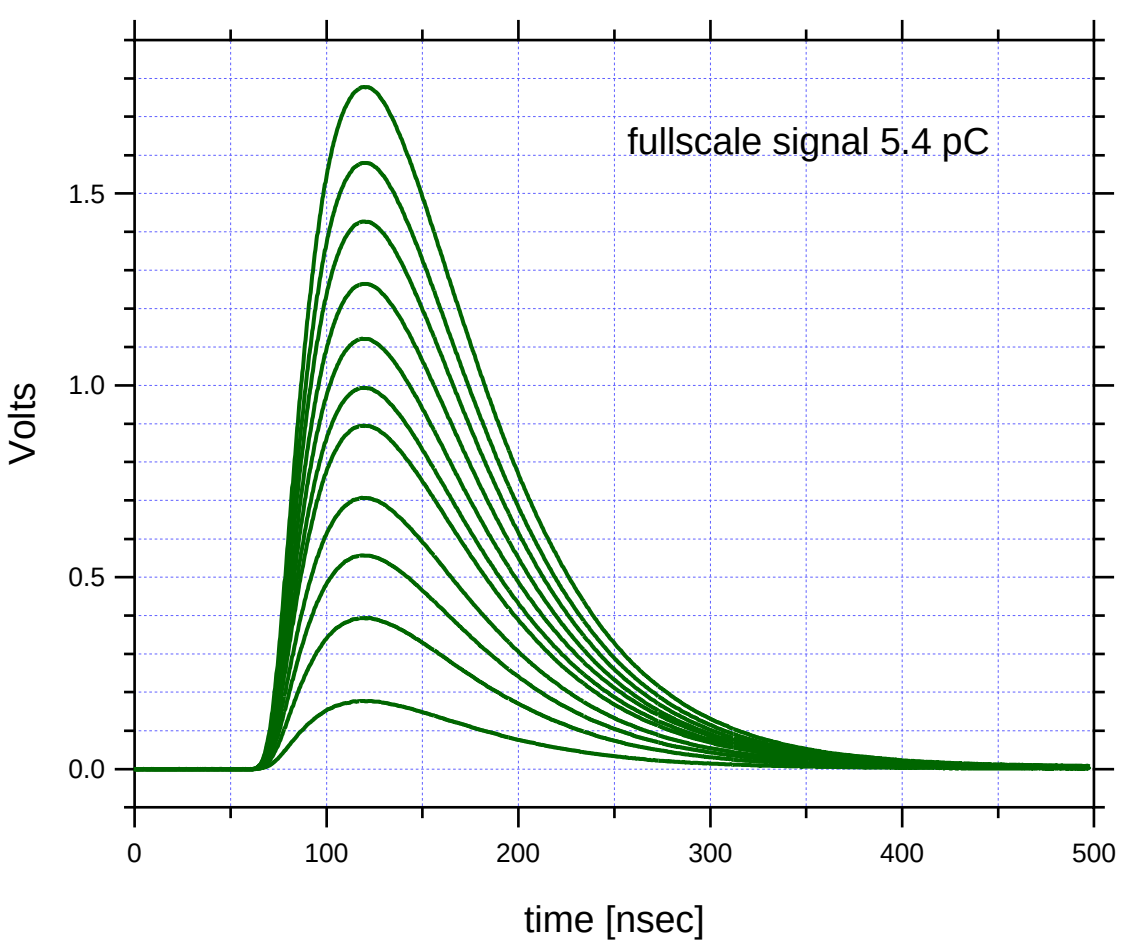
Differential pulse shape – mid and high gain channels (60 pC fullscale signal)

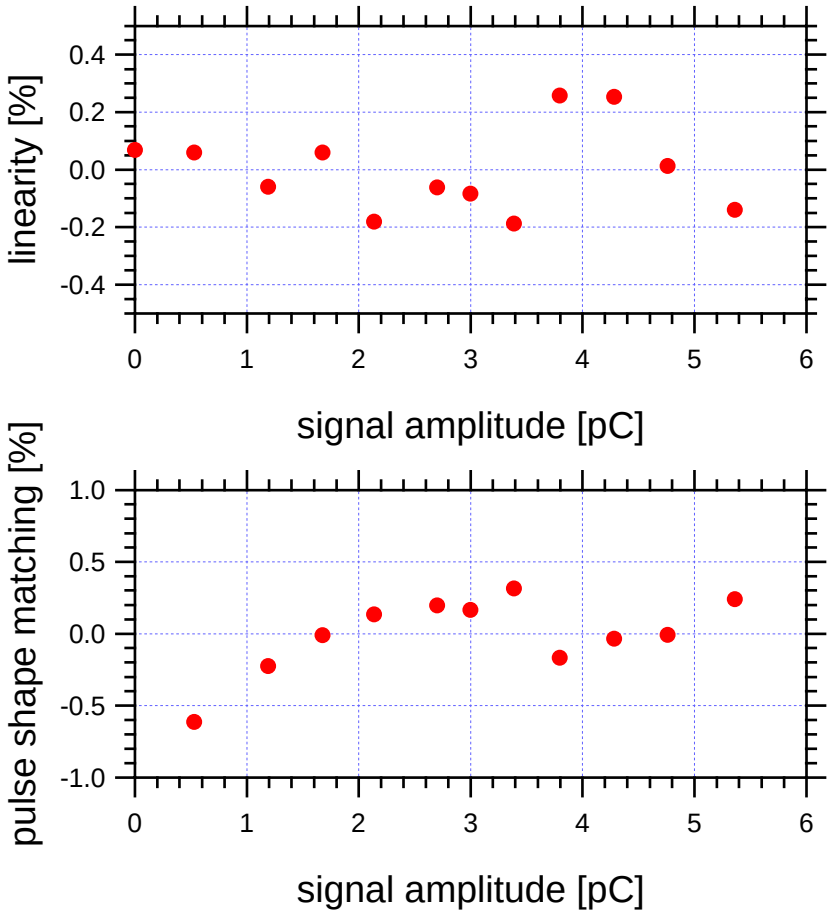


Differential pulse shapes – all 3 gain channels compared – **gain ratios 1 : 5.6 : 11.3** (cf 1 : 6 : 12)



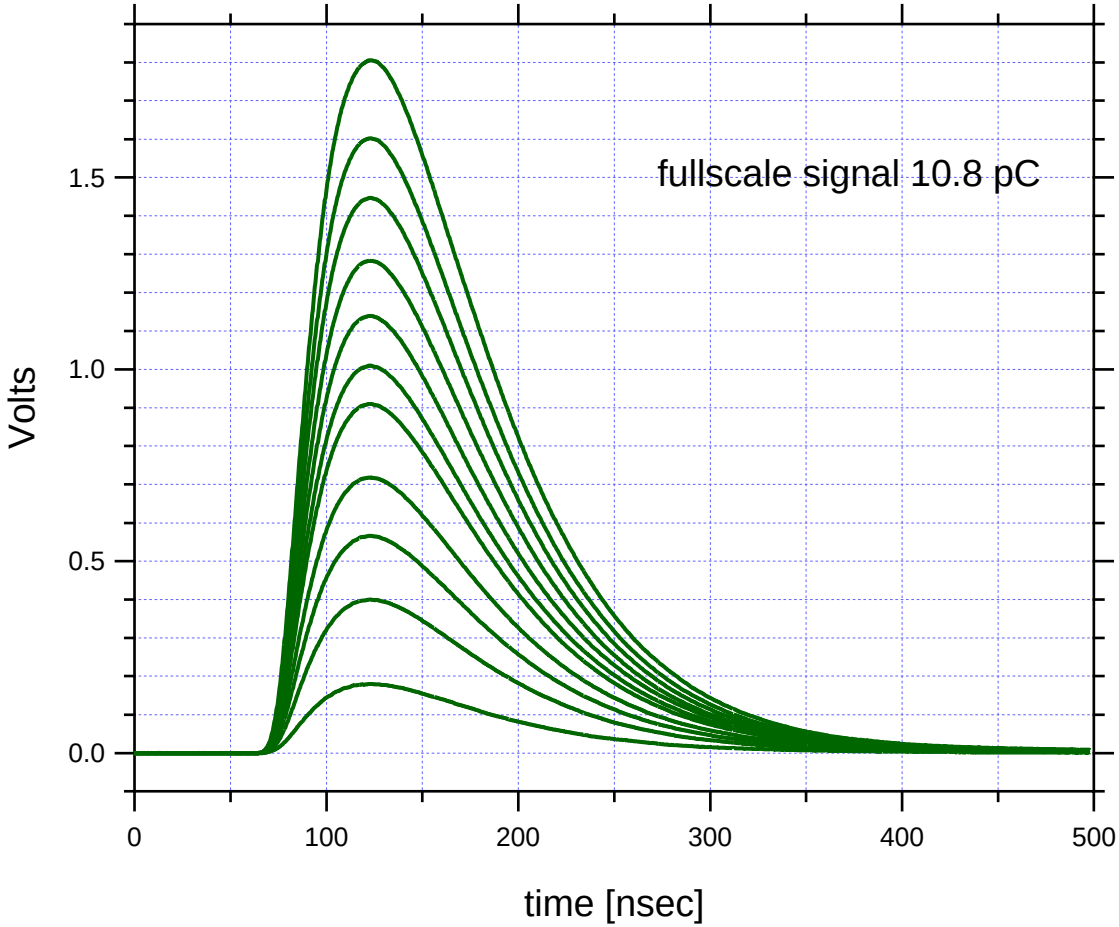
Linearity and pulse shape matching – high gain channel

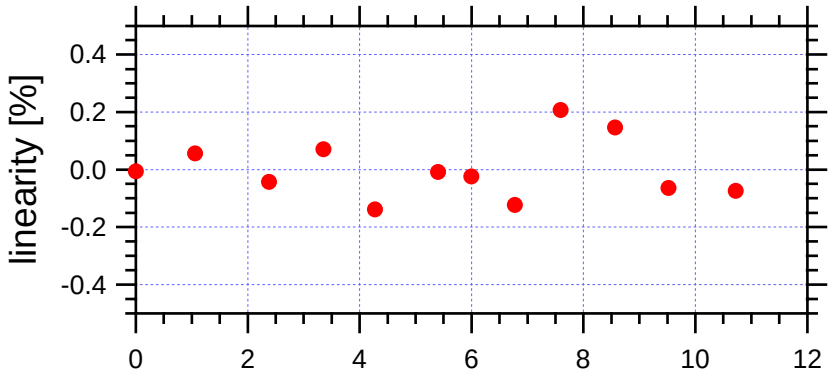


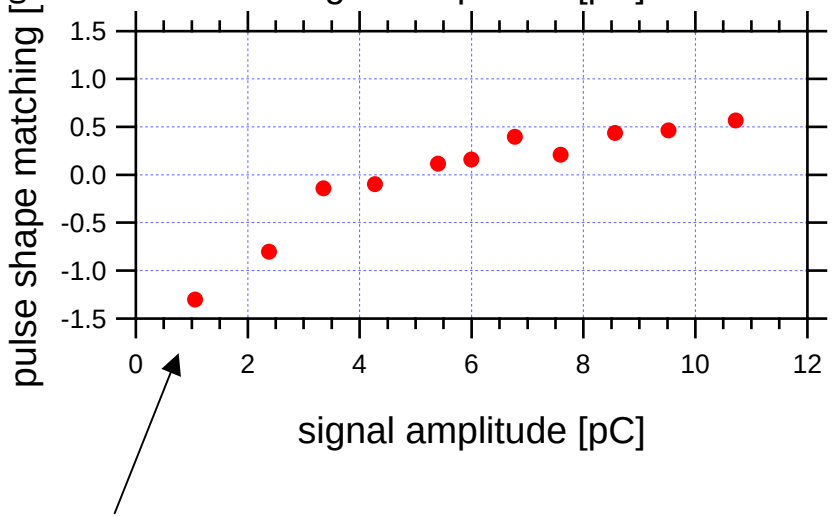


pulse shape matching in spec., linearity outside by factor ~2

Linearity and pulse shape matching – mid gain channel

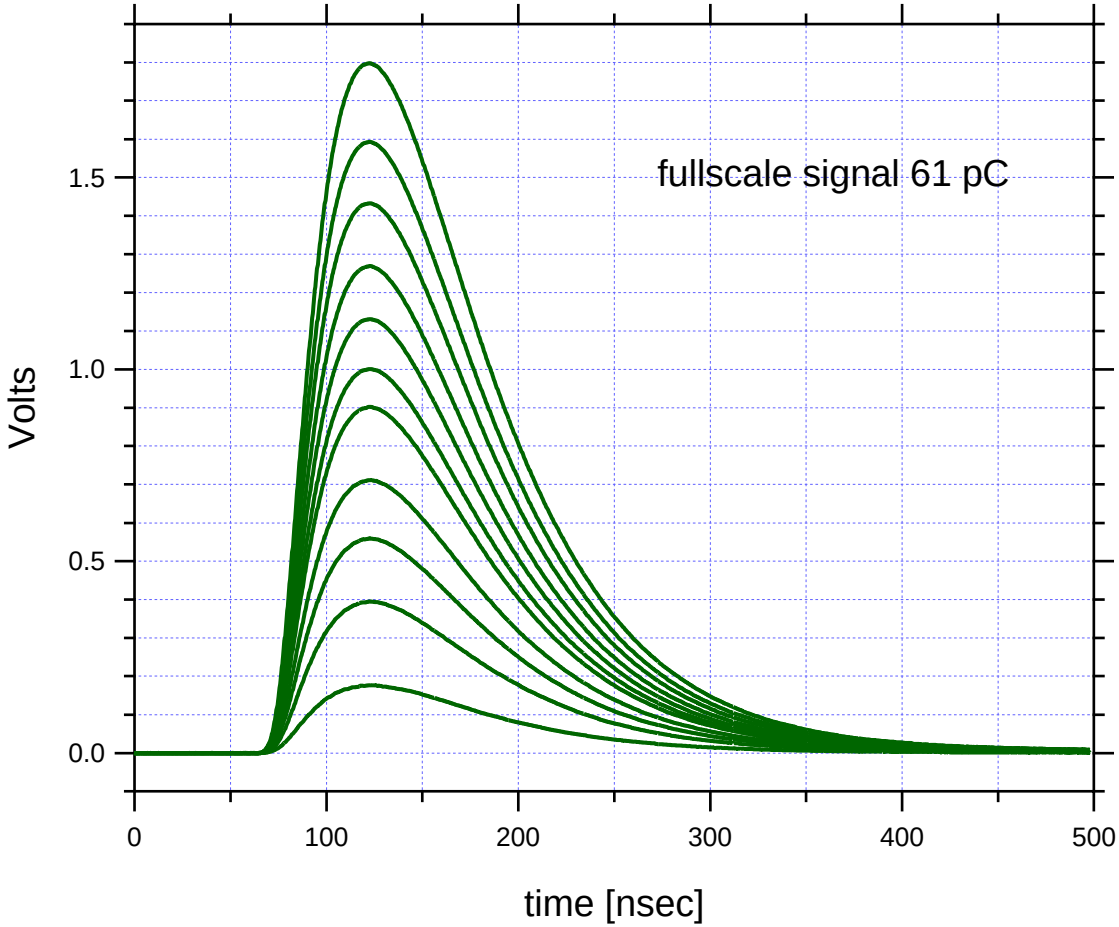


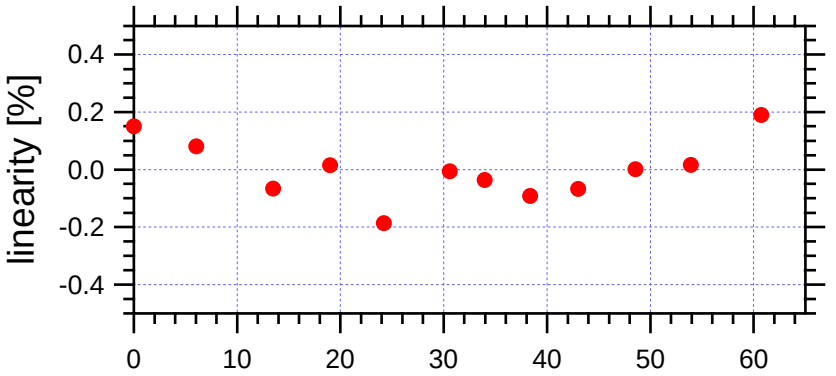


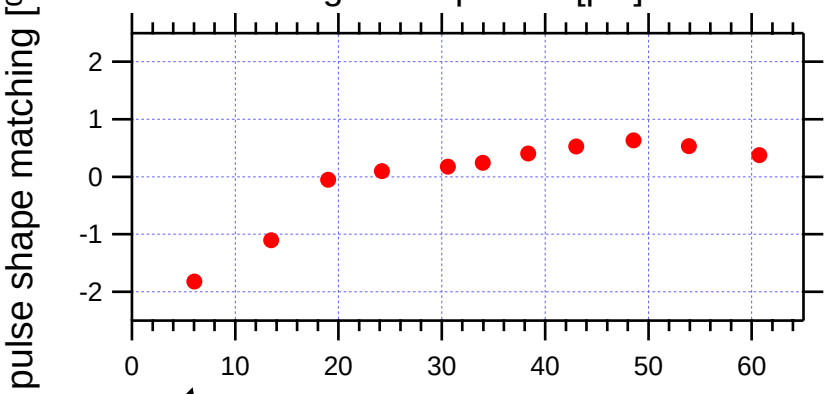


smallest signals show slower risetime – needs further investigation

Linearity and pulse shape matching – low gain channel







similar (but worse) effect as for mid-gain channel

Pulse shape matching between gain channels

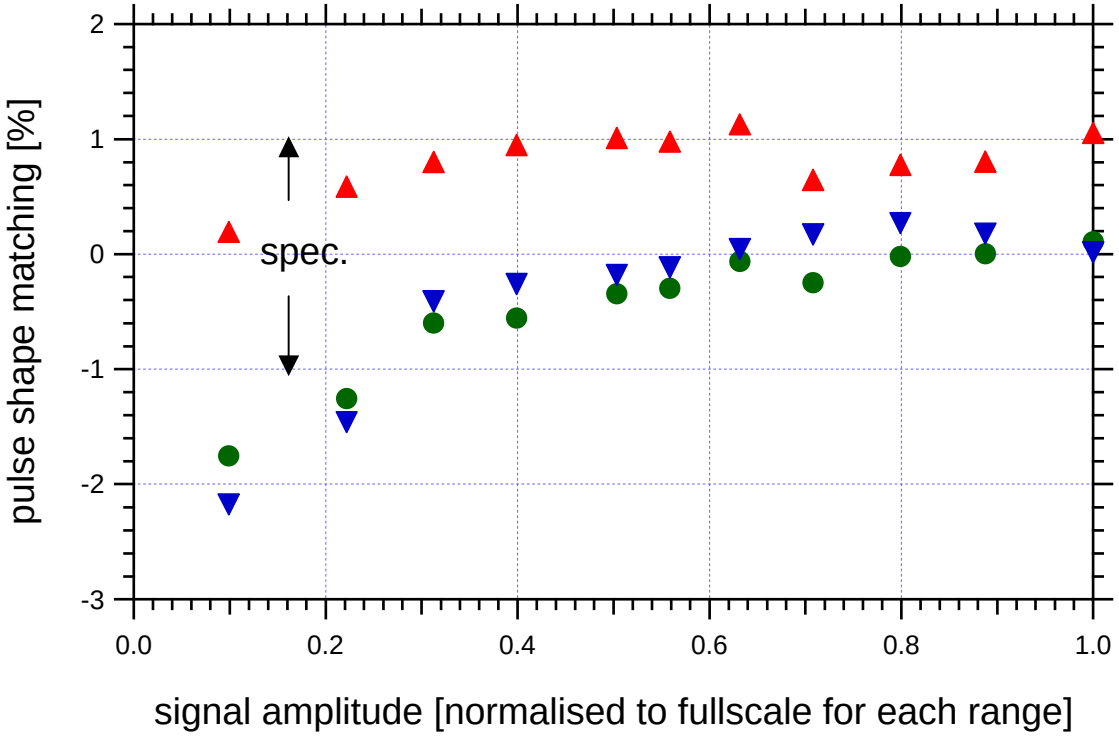
Pulse shape matching definition:

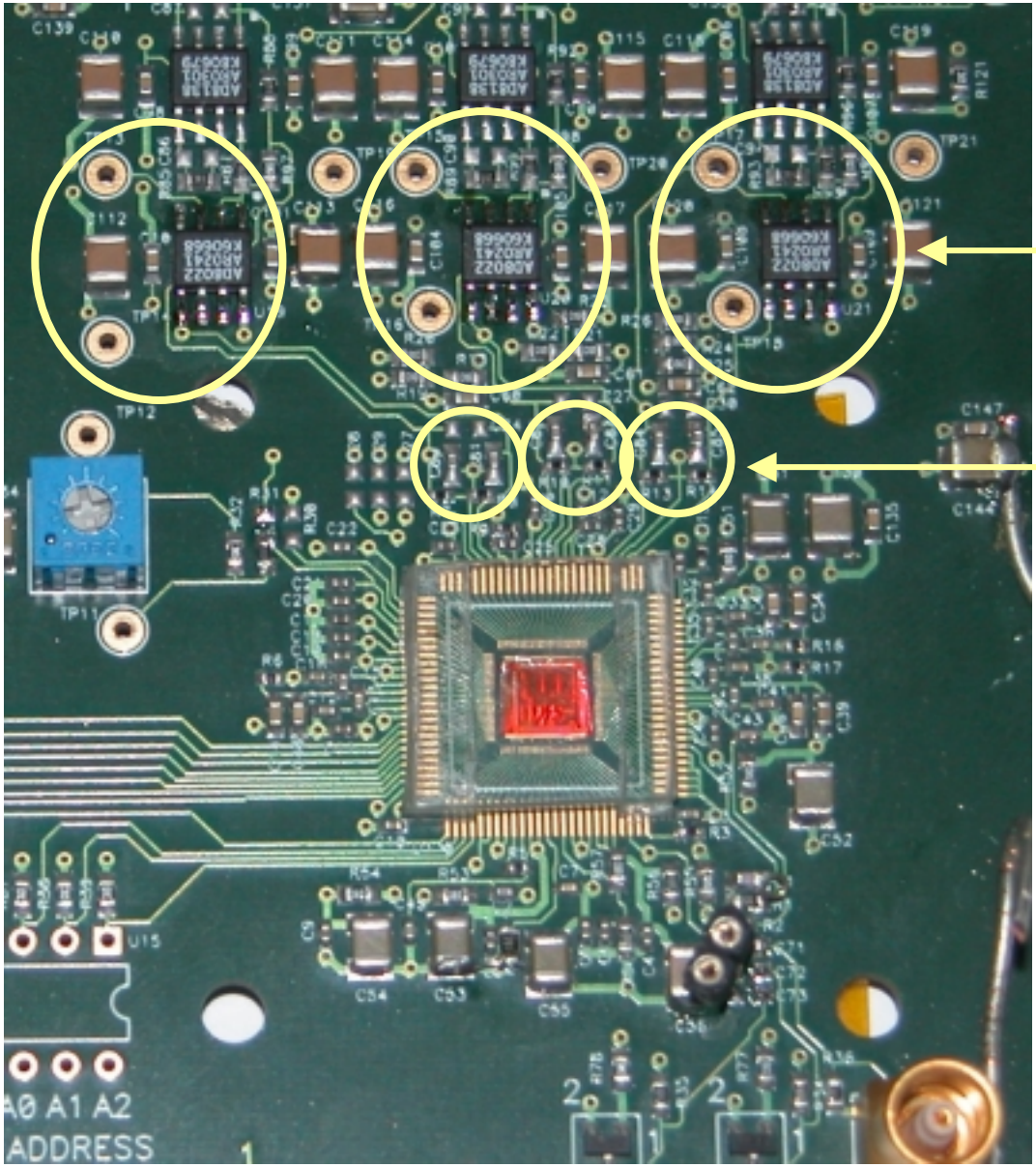
Pulse Shape Matching Factor
PSMF=V(pk-25ns)/V(pk)

Pulse shape matching =
[(PSMF-Ave.PSMF)/Ave.PSMF] X 100

Ave.PSMF = average for all signal sizes and gain ranges

systematic discrepancies between channels can be due to mismatch in diff. O/P termination components or (more likely here) difference in stray capacitance from PCB layout



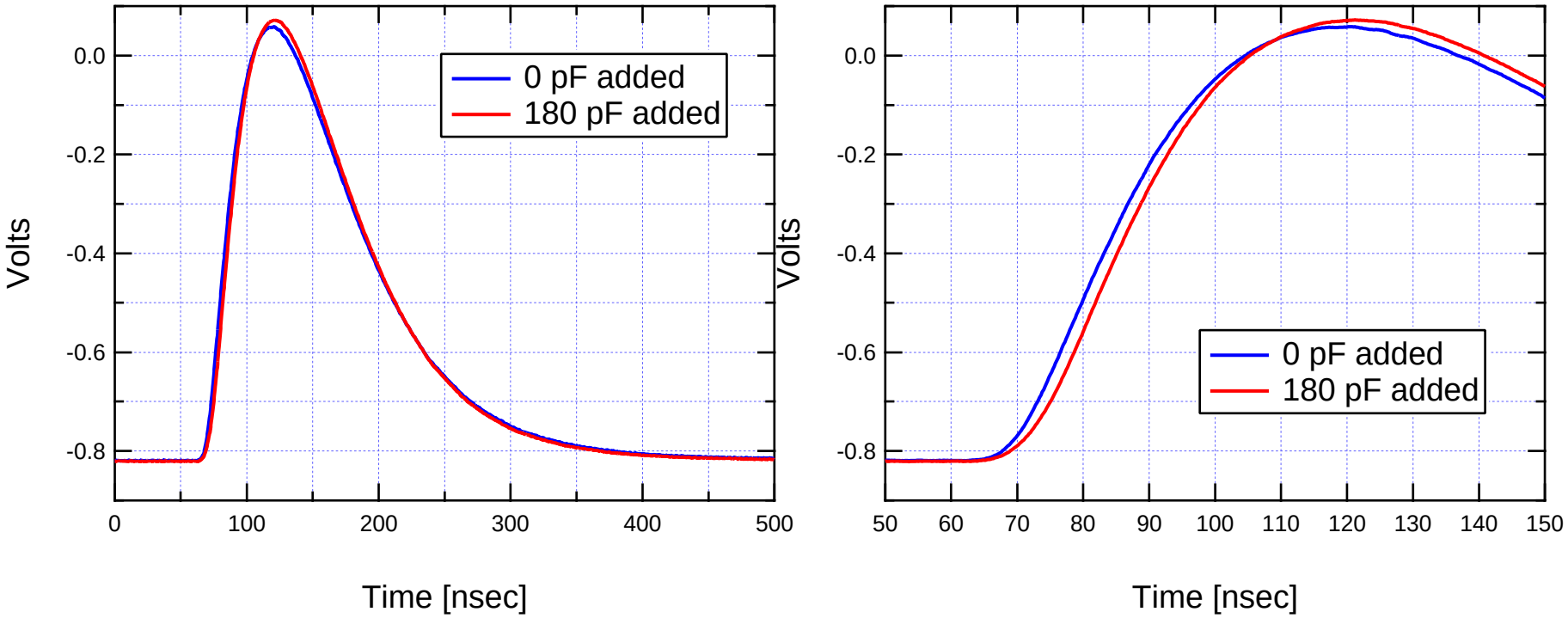


mismatch of stray O/P capacitance likely due to signal routing on test card

1st stage of buffering

differential O/P termination components (1% tolerance)

effect of input capacitance on pulse shape

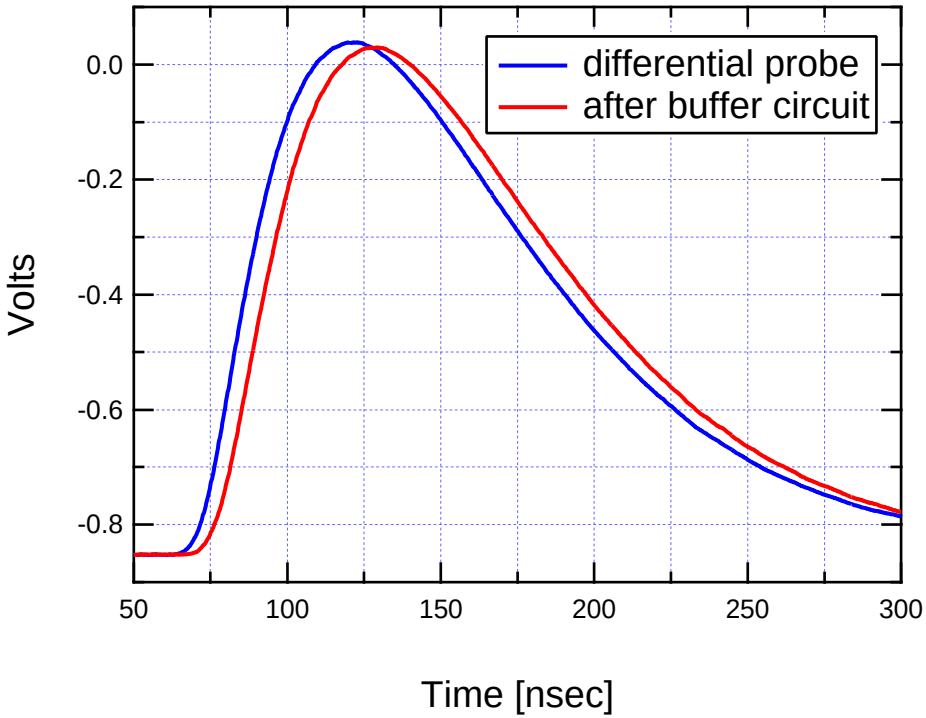


pulse peak shifts by ~ 3 nsec.

Noise measurements

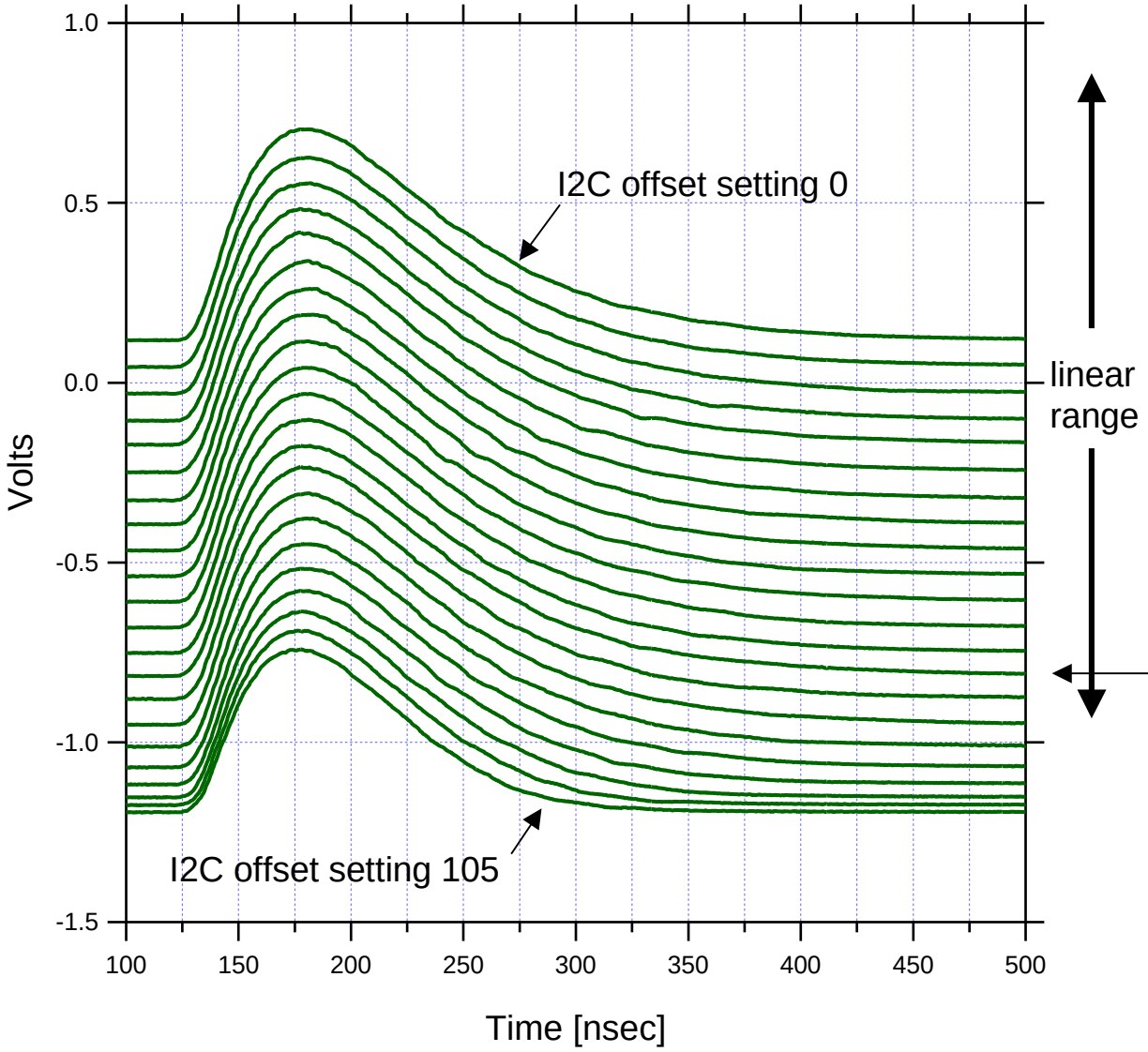
use wide bandwidth true rms meter (single ended I/P)
=> need diff. to singled ended buffer circuitry
=> extra noise contribution to subtract
and extra noise filtering →

	Cstray (~20pF)	Cstray +180pF	simulation (200pF)
high gain	7,000	7,850	6,200
mid gain	8,250	9,100	8,200
low gain	~28,000	~28,000	35,400



weak dependence on input capacitance as expected

note: large uncertainty for low gain channel - buffer circuitry dominates here



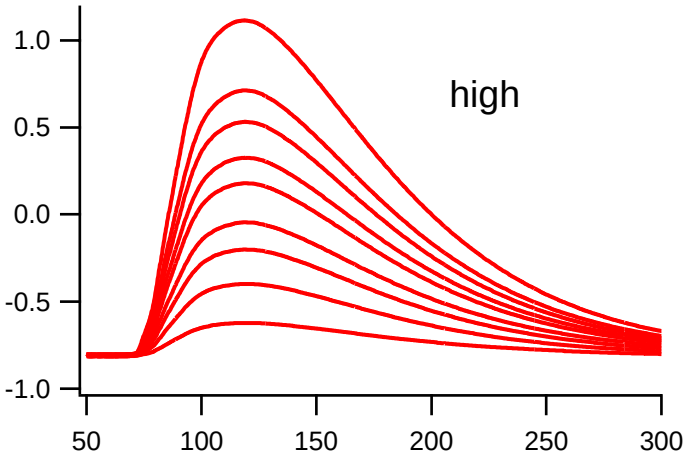
I2C pedestal offset adjustment

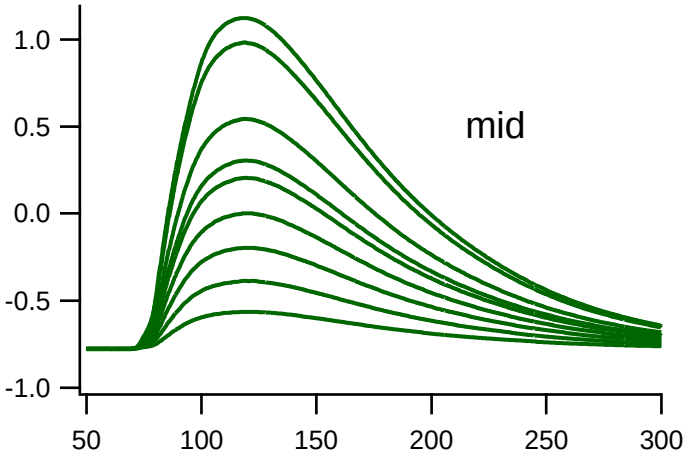
high gain channel shown here
(other channels similar)

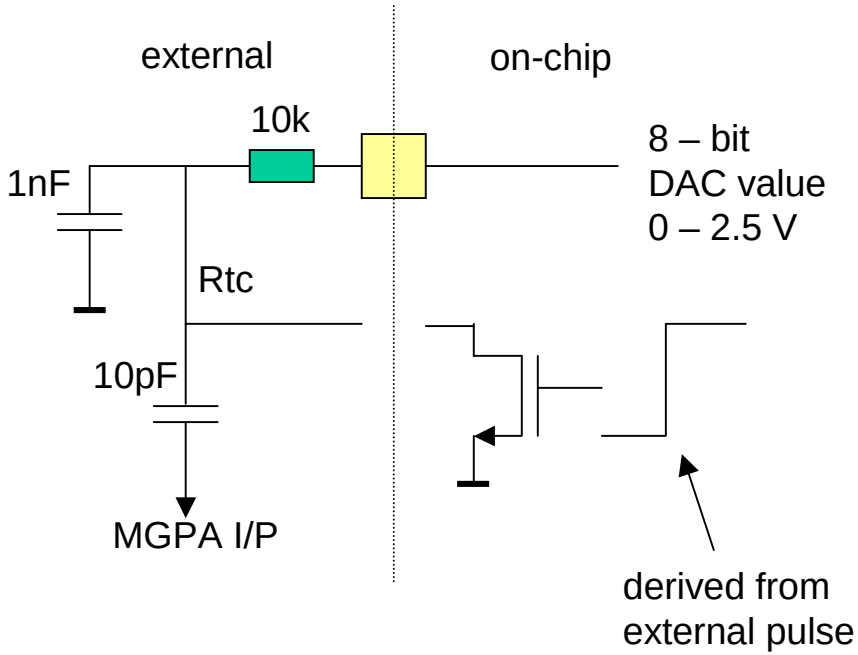
offset setting 0 -> 105 in steps of 5 (decimal)

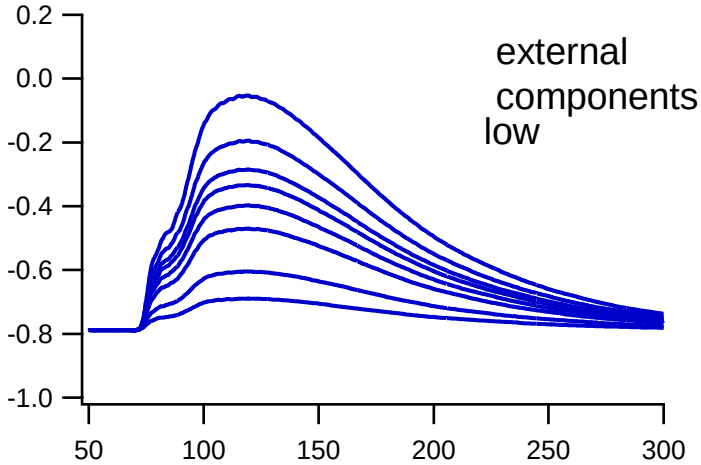
~ optimum baseline setting here
corresponds to I2C setting ~70

Calibration circuit functionality (1)



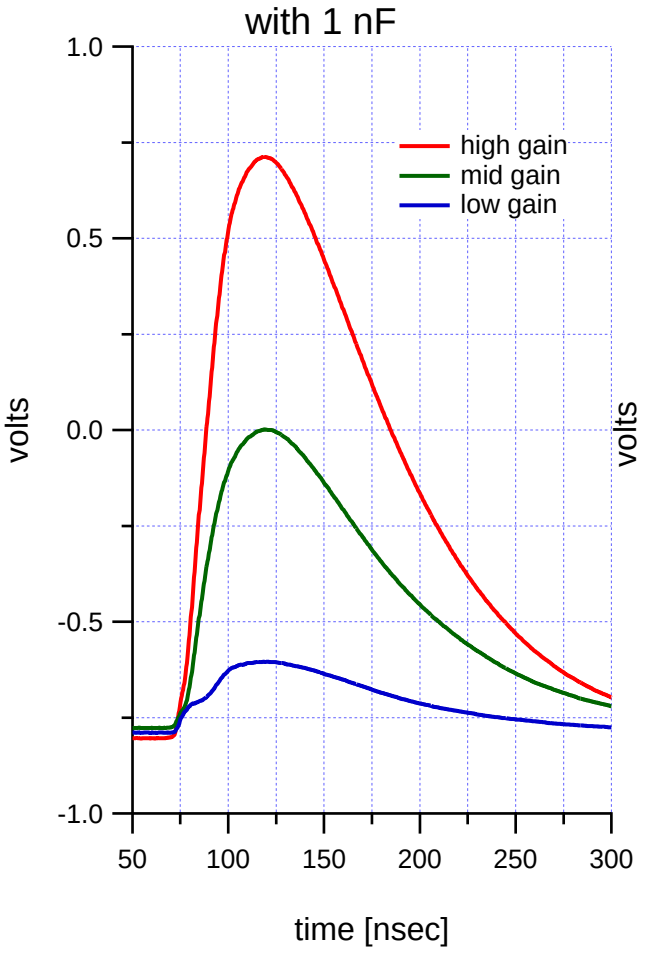


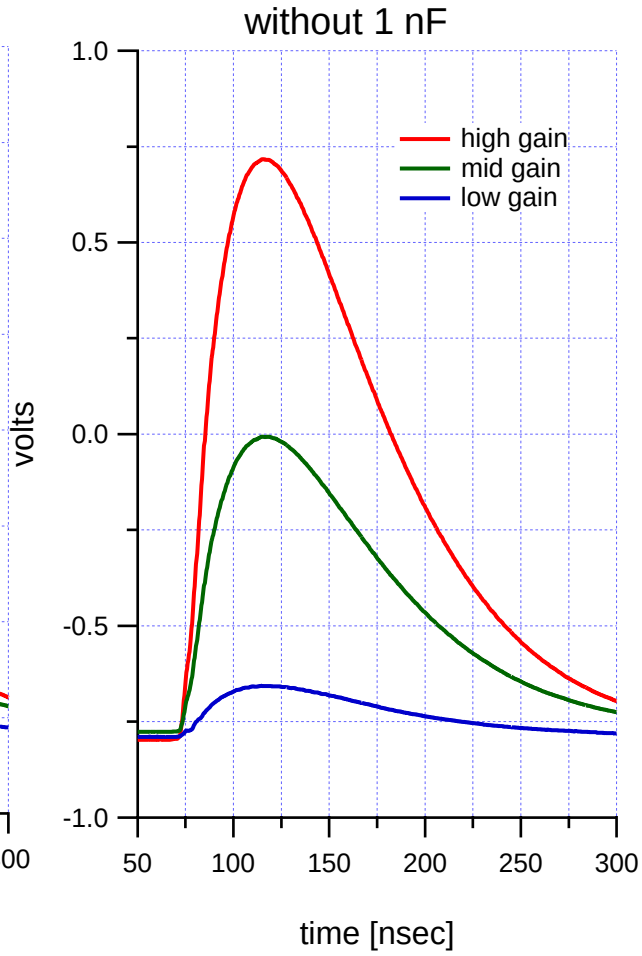


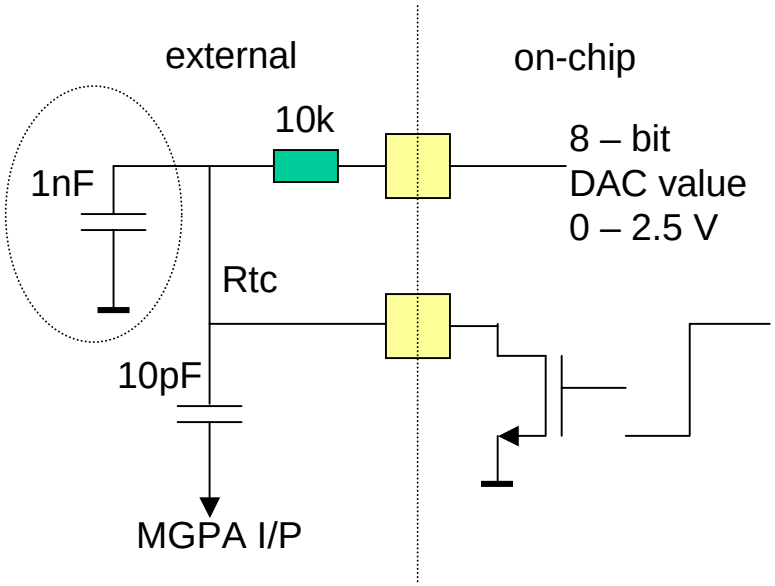


distortion on rising edge for low gain channel – somehow related to external 1 nF cap.

Calibration circuit functionality (2)

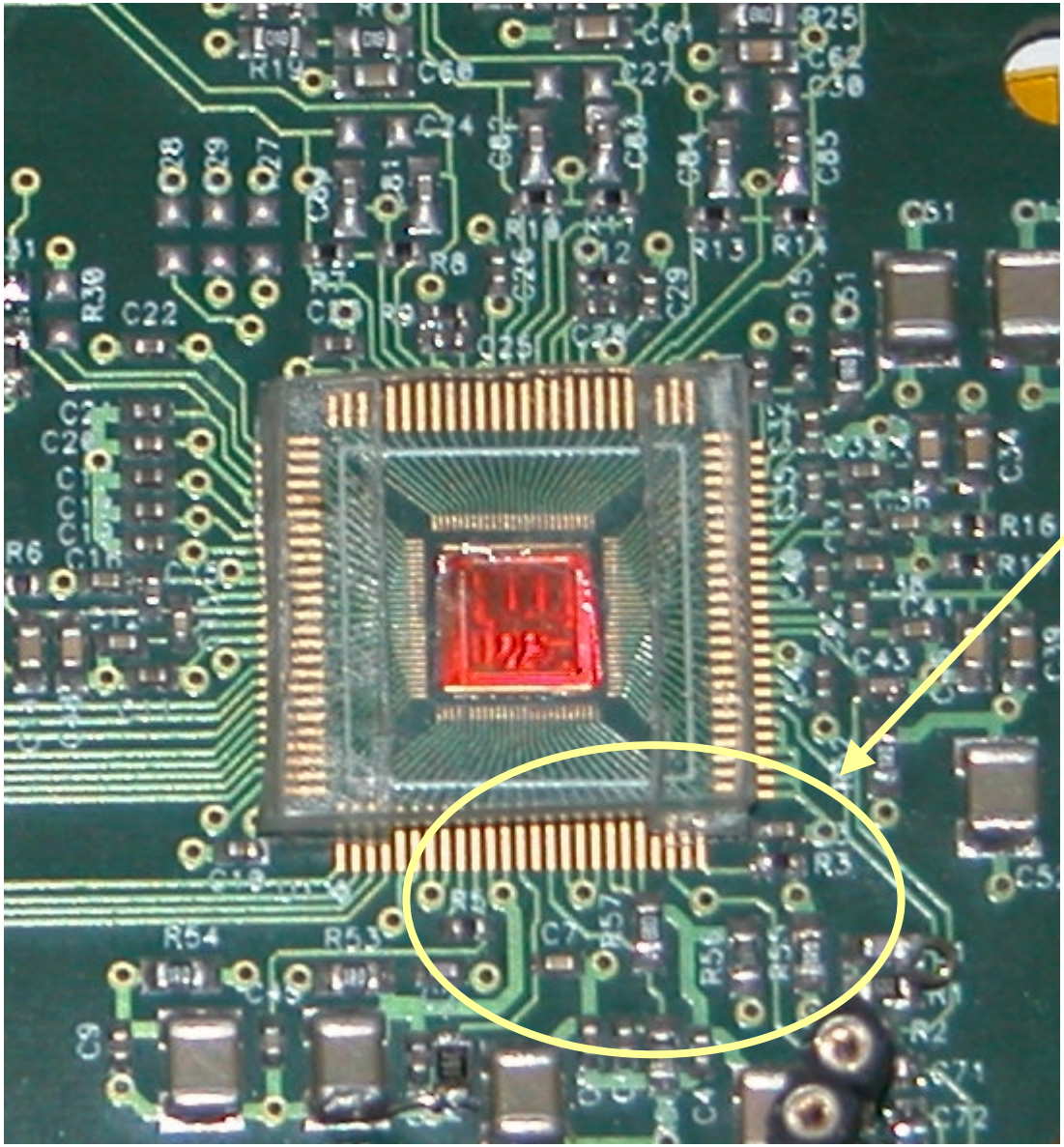






calibration pulse shapes with/without external 1 nF show improvement if removed

effect needs further investigation



main concern so far:

high frequency instability (~ 250 MHz) can be introduced on first stage O/P when probing

not clear whether problem on chip
(no hint during simulation)

or could be test board related
decoupling components around first stage not as close in as would like
VDDP, VS in particular

test board for packaged chips should help with diagnosis
decoupling closer in (may be cure?)
bias currents easy to vary (should give clues)

Power consumption

Current measured in 2.5 V rail supplying test board -> ~ 245 mA

-> chip current + Vcm divider (4mA) + power LED (3mA)

$\Rightarrow$chip current = 238 mA

measuring bias currents and multiplying by mirroring ratios -> 235 mA

may change if further testing indicates changing bias conditions -> performance improvements worth having

Summary

all results so far for one unpackaged chip, barrel feedback components to first stage

gains close to specification (1 : 5.6 : 11.3)

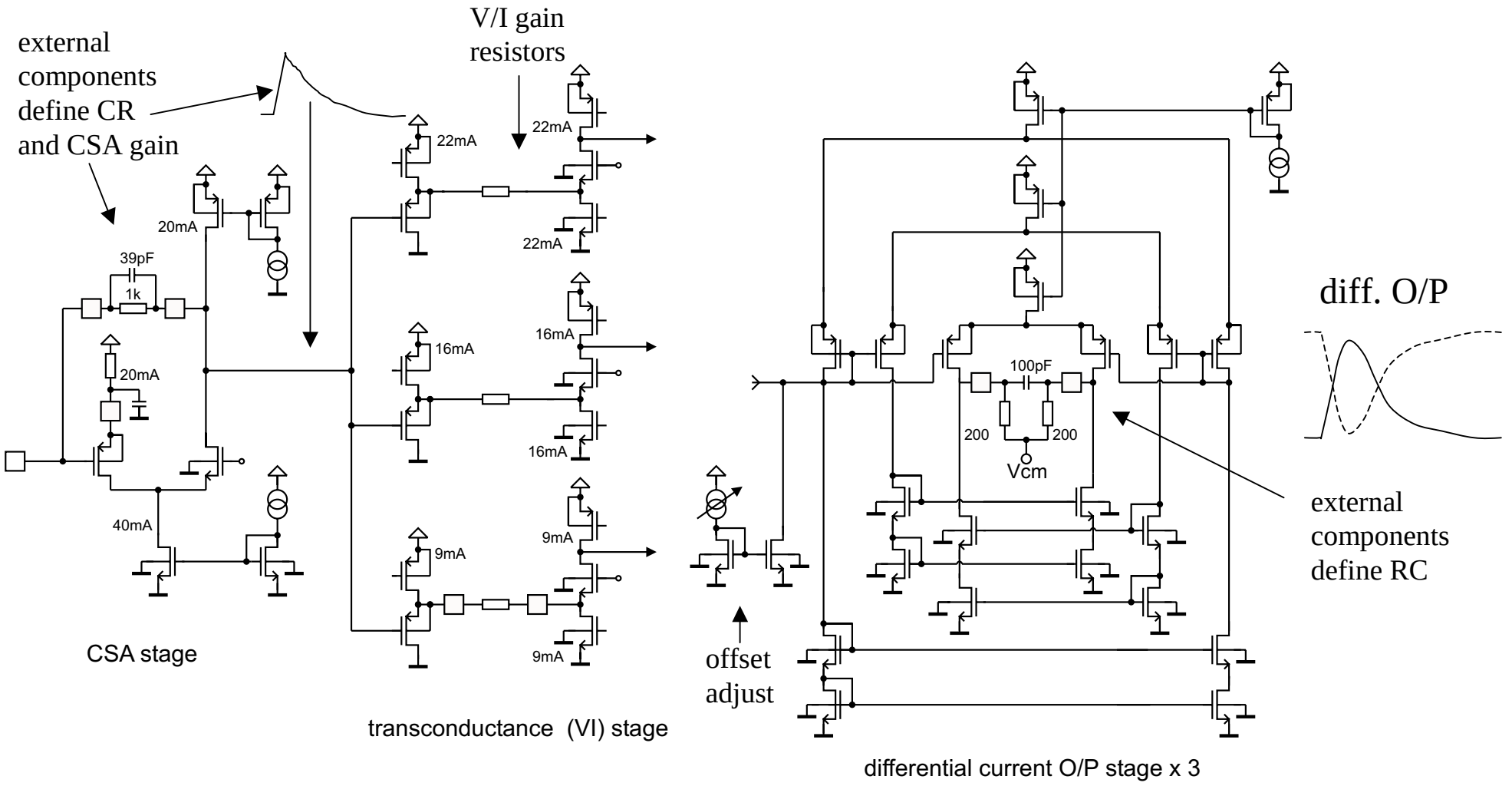
pulse shapes good
- linearity ~ +/- 0.2% (~ 2 x spec.)
- pulse shape matching within spec. apart from lowest end of mid and low gain ranges
- no obvious distortion introduced on lower gain channels by higher gain channels saturating
  - => good chip layout

noise close to simulation values (< 10,000 electrons for mid and high gain ranges)

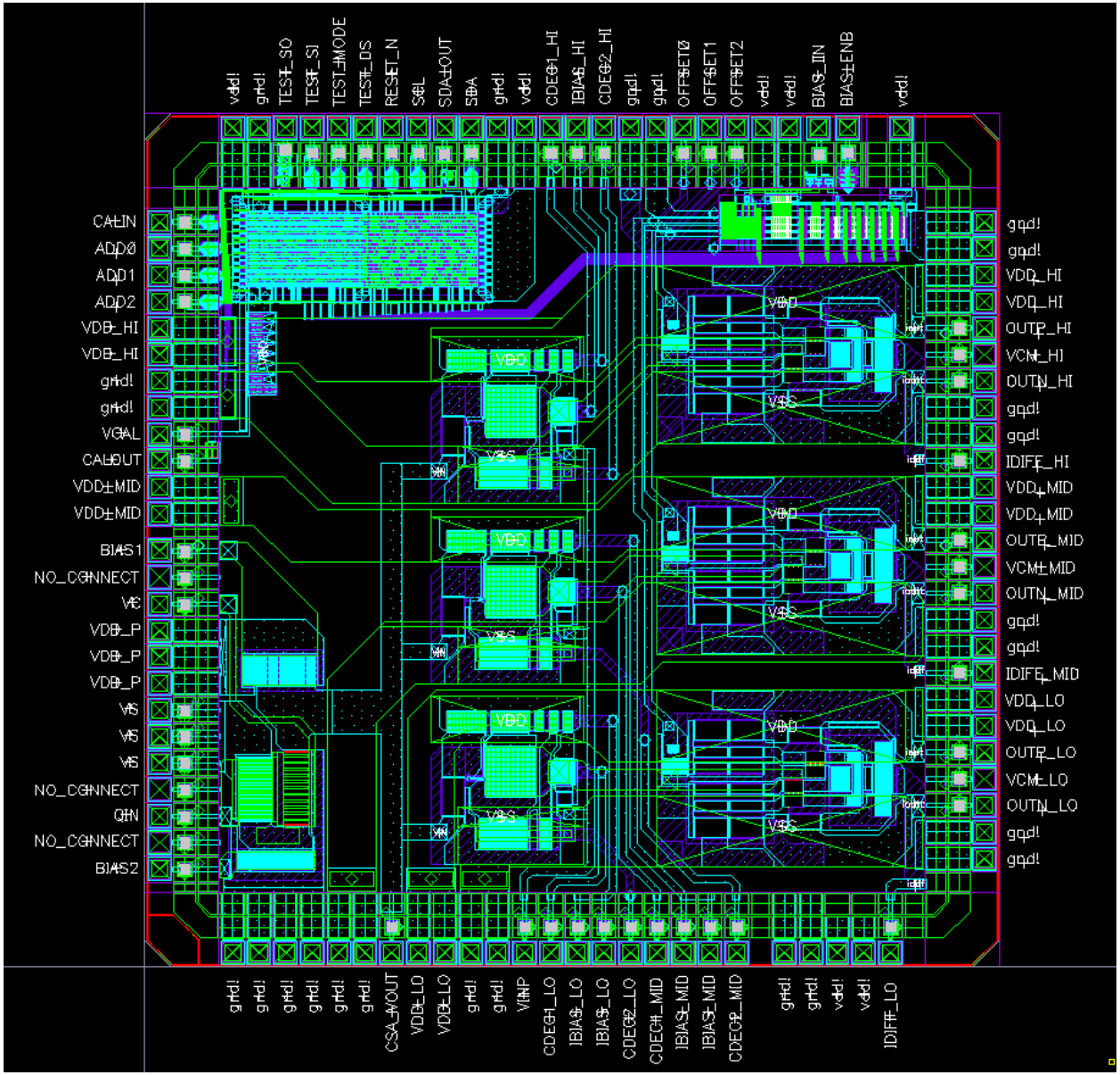
I2C features (channel offsets, calibration) fully functioning

plan to move to packaged chips as soon as available

MGPA – architecture overview



I2C interface → offset & CAL pulse generation


vdd!
gnd!
TEST_SO
TEST_SI
TEST_MODE
TEST_DS
RESET_N
SCL
SDA_OUT
SDA
gnd!
vdd!
CDEG1_HI
IBIAS_HI
CDEG2_HI
gnd!
gnd!
OFFSET0
OFFSET1
OFFSET2
vdd!
vdd!
BIAS_IN
BIAS_ENB
vdd!
CAL_IN
ADD0
ADD1
ADD2
VDD_HI
VDD_HI
gnd!
gnd!
VCAL
CAL_OUT
VDD_MID
VDD_MID
BIAS1
NO_CONNECT
VC
VDD_P
VDD_P
VDD_P
VSS
VSS
VSS
NO_CONNECT
CIN
NO_CONNECT
BIAS2
gnd!
gnd!
OUTP_HI
VCM_HI
OUTN_HI
gnd!
gnd!
IDIFF_HI
VDD_MID
VDD_MID
OUTP_MID
VCM_MID
OUTN_MID
gnd!
gnd!
IDIFF_MID
VDD_LO
VDD_LO
OUTP_LO
VCM_LO
OUTN_LO
gnd!
gnd!
gnd!
gnd!
gnd!
gnd!
gnd!
gnd!
CSA_MOUT
VDD_LO
VDD_LO
gnd!
gnd!
VTMP
CDEG1_LO
IBIAS_LO
IBIAS_LO
CDEG2_LO
CDEG1_MID
IBIAS_MID
IBIAS_MID
CDEG2_MID
gnd!
gnd!
vdd!
vdd!
IDIFF_LO