MGPA1

Multiple Gain Pre-Amplifier

CMS ECAL

User Manual

Version 1.1 Preliminary

15th May 2003

Jamie Crooks

1. INTRODUCTION

This manual describes the Multiple Gain Pre-Amplifier (MGPA) chip, which is a three gain-channel amplifier matched to the requirements of the Electromagnetic Calorimeter (ECAL) readout for the CMS experiment at the CERN LHC accelerator.

Three gain ranges are required to achieve the required dynamic range for the ECAL detector with sufficient resolution in each gain range. In the CMS ECAL system the MGPA outputs connect to a multi-channel ADC and a digital logic decision is made following the conversions as to which output is in range (the highest gain channel that has not saturated the ADC).

The CMS ECAL uses Lead Tungstate crystals read out using Avalanche Photodiodes (APD) and Vacuum Phototriodes (VPT) in the barrel and end-cap regions respectively. The MGPA is intended for both barrel and end-cap, external gain components to the first stage allowing the two different overall gains required because of the different light-to-charge conversion gains of the two photodetectors. The output of the first stage feeds the three different gain stages, and three subsequent output stages provide the outputs in differential current form. Simple CR-RC pulse shaping is implemented by the first stage resistor-capacitor feedback components, and the resistive and capacitive termination components of the differential output stages.

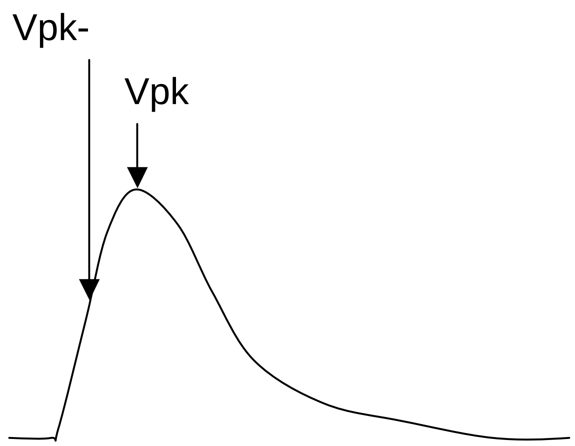
Operational bias currents are externally defined by resistors, and the output offset (pedestal) levels are programmed by an I2C protocol. A simple calibration facility is provided where a programmable (I2C) amplitude charge pulse is injected into the first stage input on receipt of an external edge trigger.

This version of the manual is preliminary, since the first prototypes of the MGPA have not yet been received and tested at the time of writing.

1.1 Specifications

Parameter	Barrel	End-Cap
full-scale signal	60 pC	16 pC
noise level [electrons]	10,000 electrons	3,500 electrons
noise level [C]	1.6 fC	0.56 fC
input capacitance	~ 200 pF	~ 50 pF
output signals to match ADC	differential 1.8 V, +/- 0.45 V around Vcm = (Vdd-Vss)/2 = 1.25 V	
gain ranges	1, 6, 12	
gain tolerance (each range)	+/- 10 %	
linearity (each range)	0.1 % full-scale	
pulse shaping (impulse response)	40 nsec CR-RC	
channel/channel pulse shape matching	< 1 %	

1.2 Pulse Shape



2. PHYSICAL SIZE, PACKAGE & PAD LAYOUT

The MGPA chip (not including scribe channels) measures 4025 x 4025 microns. For MPW-10 (March 2003) the MGPA chip will be cut to 4500 x 5000 microns. This chip is fabricated on a 0.25um, 3-layer metal IBM process. The chip comprises 25 pads on each side for bonding into a 100-pin package.

2.1 Package Information

The MGPA is housed in a 100 pin TQFP package provided by Atlantic Technology.

Description	100LD TQFP 260x260 CU64T
Drawing (package)	DGMF14141
Drawing (lead frame)	QPL-100-TQFP-0014-R1
Part No	18100223

The package measures 14mm $\times$ 14mm. The upper surface of the package sits 1.8mm above the surface of the PCB. Refer to manufacturer drawings for precise package details.

All 100 pads are bonded to the 100 pins in a straight 1:1 assignment. A bonding diagram is available.

2.2 Pad Layout

Pad centres are arranged on a 5um pitch, at a minimum spacing of 125um. Refer to the bonding diagram for pad layout.

2.3 Power Supplies

The MGPA provides separated positive power supplies for the following:

- Input preamplifier: *"VDD_P"*
- VI-stage & Differential output stage (High gain channel): *"VDD_HI"*
- VI-stage & Differential output stage (Mid gain channel): *"VDD_MID"*
- VI-stage & Differential output stage (Low gain channel): *"VDD_LO"*
- Digital I2C, Bias current generator, Calibration DAC, Pad ring: *"VDD"*

Ground connections (by metal) to these circuits are also identified: Note that all ground pins are connected to the substrate so these pins are not isolated.

3. PIN DEFINITIONS

Pin	Name	Type	Value	Function
1	CALIN	Digital input		Full scale digital input calibration pulse
2	ADD0	Digital input		Sets the 3 LSBs of the unique I2C address of this chip. The upper 4 bits are tied to logic '1' internally.
3	ADD1	Digital input		
4	ADD2	Digital input		
5	VDD_HI	Power	2.5v	Positive power supply for high gain channel
6	VDD_HI	Power	2.5v	Positive power supply for high gain channel
7	GND	Ground	0v	Negative (ground) connection for high gain channel
8	GND	Ground	0v	Negative (ground) connection for high gain channel
9	VCAL	Analogue output		Voltage reference defined by calibration DAC
10	CALOUT	Analogue output		Open drain o/p controlled by CALIN for calibration
11	VDD_MID	Power	2.5v	Positive power supply for mid gain channel
12	VDD_MID	Power	2.5v	Positive power supply for mid gain channel
13	BIAS1	Analogue output	2mA	Input preamplifier bias current
14	NO CONNECT			To facilitate board design
15	VC	Analogue input		Input preamplifier bias
16	VDD_P	Power	2.5v	Positive power supply for input preamplifier
17	VDD_P	Power	2.5v	Positive power supply for input preamplifier
18	VDD_P	Power	2.5v	Positive power supply for input preamplifier
19	VS	Analogue input	20mA	Input preamplifier bias
20	VS	Analogue input		
21	VS	Analogue input		
22	NO CONNECT	No connect		To allow guarding of input signal if required
23	QIN	Analogue input		Charge input signal
24	NO CONNECT	No connect		To allow guarding of input signal if required
25	BIAS2	Analogue input	4mA	Input preamplifier bias current
26	GND	Ground	0v	Negative (ground) connection for input preamplifier
27	GND	Ground	0v	Negative (ground) connection for input preamplifier
28	GND	Ground	0v	Negative (ground) connection for input preamplifier
29	GND	Ground	0v	Negative (ground) connection for input preamplifier
30	GND	Ground	0v	Negative (ground) connection for mid gain channel
31	GND	Ground	0v	Negative (ground) connection for mid gain channel
32	CSA_VOUT	Analogue output		Output voltage from preamplifier
33	VDD_LO	Power	2.5v	Positive power supply for low gain channel
34	VDD_LO	Power	2.5v	Positive power supply for low gain channel
35	GND	Ground	0v	Negative (ground) connection for low gain channel
36	GND	Ground	0v	Negative (ground) connection for low gain channel
37	VINP	Analogue input		Voltage reference for VI-stage circuits
38	CDEC1_LO	Analogue input		VI-stage bias for low gain channel
39	IBIAS_LO	Analogue output		VI-stage bias for low gain channel
40	IBIAS_LO	Analogue output		
41	CDEC2_LO	Analogue output		VI-stage bias for low gain channel
42	CDEC1_MID	Analogue input		VI-stage bias for mid gain channel
43	IBIAS_MID	Analogue output		VI-stage bias for mid gain channel
44	IBIAS_MID	Analogue output		
45	CDEC2_MID	Analogue output		VI-stage bias for mid gain channel
46	GND	Ground	0v	Negative (ground) connection to power ring
47	GND	Ground	0v	Negative (ground) connection to power ring
48	VDD	Power	2.5v	Positive power supply to power ring
49	VDD	Power	2.5v	Positive power supply to power ring
50	IDIFF_LO	Analogue output	1.5mA	Differential stage bias current for low gain channel

Pin	Name	Type	Value	Function
51	GND	Ground	0v	Negative (ground) connection for low gain channel
52	GND	Ground	0v	Negative (ground) connection for low gain channel
53	OUTN_LO (B1)	Analogue output		Differential output signal from low gain channel
54	NO CONNECT			For connection to VCM node
55	OUTP_LO (B1)	Analogue output		Differential output signal from low gain channel
56	VDD_LO	Power	2.5v	Positive power supply for low gain channel
57	VDD_LO	Power	2.5v	Positive power supply for low gain channel
58	IDIFF_MID	Analogue output	1.5mA	Differential stage bias current for mid gain channel
59	GND	Ground	0v	Negative (ground) connection for mid gain channel
60	GND	Ground	0v	Negative (ground) connection for mid gain channel
61	OUTN_MID (A2)	Analogue output		Differential output signal from mid gain channel
62	NO CONNECT			For connection to VCM node
63	OUTP_MID (A2)	Analogue output		Differential output signal from mid gain channel
64	VDD_MID	Power	2.5v	Positive power supply for low mid channel
65	VDD_MID	Power	2.5v	Positive power supply for low mid channel
66	IDIFF_HI	Analogue output	1.5mA	Differential stage bias current for high gain channel
67	GND	Ground	0v	Negative (ground) connection for high gain channel
68	GND	Ground	0v	Negative (ground) connection for high gain channel
69	OUTN_HI (A1)	Analogue output		Differential output signal from high gain channel
70	NO CONNECT			For connection to VCM node
71	OUTP_HI (A1)	Analogue output		Differential output signal from high gain channel
72	VDD_HI	Power	2.5v	Positive power supply for low high channel
73	VDD_HI	Power	2.5v	Positive power supply for low high channel
74	GND	Ground	0v	Negative (ground) connection for bias generator
75	GND	Ground	0v	Negative (ground) connection for bias generator
76	VDD	Power	2.5v	Positive power supply for bias generator
77	BIAS_ENB	Digital input		Bias generator disable (active high, int. pull-down)
78	BIAS_IIN	Analogue input	128uA	Reference current for bias generator
79	VDD	Power	2.5v	Positive power supply for bias generator
80	VDD	Power	2.5v	Positive power supply for bias generator
81	OFFSET2	Analogue input		Offset current for high gain differential output
82	OFFSET1	Analogue input		Offset current for mid gain differential output
83	OFFSET0	Analogue input		Offset current for low gain differential output
84	GND	Ground	0v	Negative (ground) connection for bias generator
85	GND	Ground	0v	Negative (ground) connection for bias generator
86	CDEC2_HI	Analogue input		VI-stage bias for high gain channel
87	IBIAS_HI	Analogue output		VI-stage bias for high gain channel
88	CDEC1_HI	Analogue output		VI-stage bias for high gain channel
89	VDD	Power	2.5v	Positive power supply for digital I2C logic
90	GND	Ground	0v	Negative (ground) connection for digital I2C logic
91	SDA	Digital input		I2C Data input signal
92	SDA_OUT	Digital output		I2C Data output signal
93	SCL	Digital input		I2C Clock input signal
94	RESET_N	Digital input		I2C Reset (active low)
95	TEST_DS	Digital input		Scan chain clock
96	TEST_MODE	Digital input		Scan chain enable (active high)
97	TEST_SI	Digital input		Scan chain input
98	TEST_SO	Digital output		Scan chain output
99	GND	Ground	0v	Negative (ground) connection for digital I2C logic
100	VDD	Power	2.5v	Positive power supply for digital I2C logic

4. CONTROL INTERFACE

The MGPA is fitted with an I2C interface containing 6 read / write registers. The logic is designed to be protected against single-event upset (SEU): All registers are triplicated within the design, their outputs passing through voting logic which selects the majority vote.

4.1 Device Address

I2C protocol implements a 7 bit chip address, where for the MGPA the upper 4 bits are tied to logic ‘1’. The lower three bits are available on pins 2,3,4 allowing for eight MGPA devices to be individually addressed on any one I2C bus. These pins should be tied low / high on the PCB, to give chip addresses in the range 0x78 → 0x7F.

4.2 I2C Pins

SCL	Input	The I2C clock signal, driven by the master controller (CCU) I2C operation is specified at 400kbit/s This signal will be held high by the master controller when the I2C interface is not in use
SDA	Input	The I2C data signal, driven by the master controller (CCU). This signal is held high by an PCB mounted pull-up resistor and pulled low by the master controller.
SDA_OUT	Output	The I2C data signal, driven by the slave device This signal is held high by an PCB mounted pull-up resistor and pulled low by the master controller. The SDA and SDA_OUT signals may be shorted together for a 2-wire I2C interface.

4.3 I2C Registers

Address	**Name**	**Function**	**Reset value**
0x00	GENERAL	<0> Calibrate Pulse enable <7:1> Spare	00000000
0x01	OFFSET0	<7:0> Low gain channel offset current	00000000
0x02	OFFSET1	<7:0> Mid gain channel offset current	00000000
0x03	OFFSET2	<7:0> High gain channel offset current	00000000
0x04	OFFSET3	<7:0> Spare	00000000
0x05	DACCAL	<7:0> Calibration pulse magnitude	00000000

4.4 I2C Protocol

The I2C operation is designed for compatibility with the CCU chip and therefore employs “RAL-MODE” functionality as used in the APV design. This mode of operation is governed primarily by the Philips standard for I2C communications. “RAL-MODE” in particular defines an extended addressing scheme for reading and writing as defined below. Note also that acknowledge signals are assumed to be ignored by the controller and therefore incremental addressing is unavailable: Only single register read / write operations are possible.

4.4.1 I2C Write

Data is written to the MGPA in three 8-bit words, each followed by an acknowledge sent by the receiving device. The words are defined as follows

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CHIP ADDRESS [6:0]							0
REGISTER ADDRESS [6:0]							0
DATA VALUE [7:0]							

4.4.2 I2C Read

Data is transferred from the MGPA as a two part operation. First, a device is accessed for writing, and a particular register in that device is addressed for reading. In the following operation the same device now is accessed for reading and it responds by sending back the previously defined register.

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CHIP ADDRESS [6:0]							0
REGISTER ADDRESS [6:0]							1

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CHIP ADDRESS [6:0]							1
DATA VALUE [7:0]							

5. SCAN CHAIN FUNCTIONALITY

The digital I2C unit is synthesised with scan-chain flip-flops for testing purposes. The scan path comprises 176 registers.

The four digital signals associated with the scan chain are detailed below:

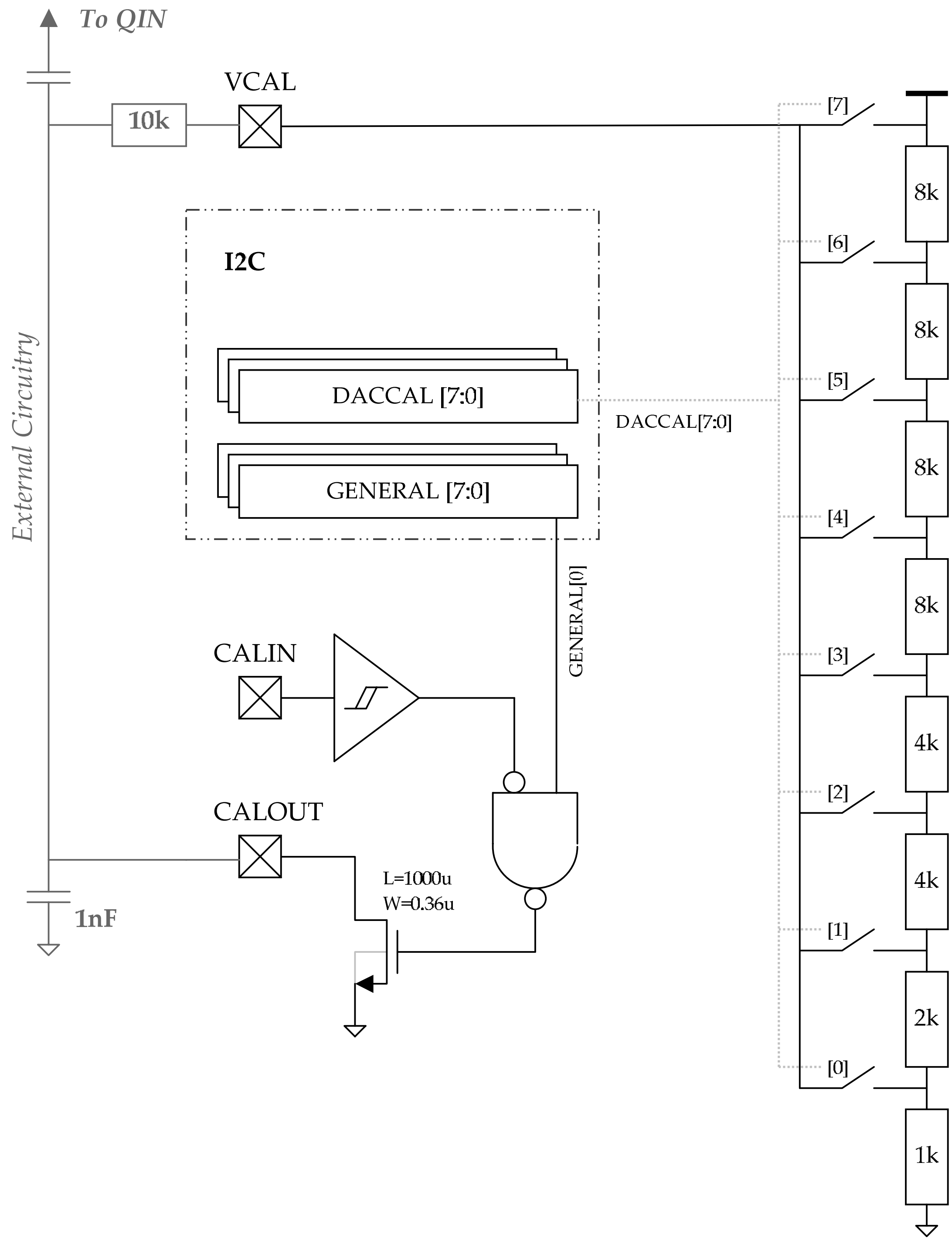
TEST_DS	The test-mode clock signal (“data_source”)
TEST_MODE	The test-mode enable signal (active high)
TEST_SI	The test data input pin
TEST_SO	The test data output pin

By driving TEST_MODE to VDD the data paths and clock tree inside the I2C logic are switched to their test mode configuration. In this configuration all registers are arranged in a chain and clocked by “data_source” to form one large shift register. As such, the internal state of every register may be extracted at any particular moment. Alternatively, “stuck-at” tests may be achieved by passing all zeros into the shift register and then observing a single ‘1’ pass through the entire chain unaltered.

During normal chip operation TEST_MODE should be held low.

6. CALIBRATION PULSE GENERATOR

The default setting for this is off. The I2C registers reset to zero, which will inhibit any signal on CALIN affecting CALOUT. By writing a logic ‘1’ to bit zero of the GENERAL register this allows an input on CALIN to pull CALOUT either to ground or to a potential set with external components and the VCAL pin. This forms the input charge test pulse for calibration measurements. The value held in the DACCAL register closes the corresponding switches in the resistor network as illustrated changing the voltage seen at VCAL.



6.1 Calibration Pulse Lookup Table

Simulation results are presented below in a quick reference lookup table for the calibration pulse DAC. The voltage at VCAL is calculated for a 2.5v power supply. Entries which have been greyed out represent circuit configurations in which the output node is directly connected to 2.5v and also nodes in the resistor stack.

VCAL	Reg Value
0.06	00000001
0.07	00000011
0.08	000001X1
0.09	00001XX1
0.12	0001XXX1
0.17	00000010
0.18	001XXXX1
0.21	00000110
0.23	00001X10
0.30	0001XX10
0.33	01XXXX11
0.34	01XXXX01

0.41	00000100
0.42	001XXX10
0.46	00001100
0.58	0001X100
0.64	00001000
0.72	01XXXX10
0.78	001XX100
0.80	00011000
1.03	001X1000
1.11	00010000
1.17	01XXX100
1.35	00110000
1.43	01XX1000
1.57	00100000

1.74	01X10000
1.9	1XXXXXX1
2.04	01000000
2.20	100XX110
2.21	1XXXX110
2.22	11XXX010
2.36	1XXXX100
2.41	1XXX1000
2.45	1XX10000
2.46	1X100000
2.47	11000000
2.50	10000000

7. OFFSET CURRENT GENERATION

Offset currents for the differential output circuit of each channel are generated on-chip and may be set by writing to the corresponding 8-bit I2C register as detailed below:

I2C Register	I2C Address	Function
OFFSET0	0x01	Low gain channel offset
OFFSET1	0x02	Mid gain channel offset
OFFSET2	0x03	High gain channel offset

The bias generator circuit uses weighted current mirrors and switches to generate an output current between 0 and 1mA dependant on the 8-bit value held in the I2C register. The full range comprises 256 discrete currents within the 1mA range giving approximately 4uA step-size. Register value 0xFF will provide 1mA*, value 0x00 will provide 3.4nA*, value 0x01 will provide 4.06uA*. [* Simulation figures]

The bias generator input BIAS_IIN must be provided with a 128uA reference current for correct operation.

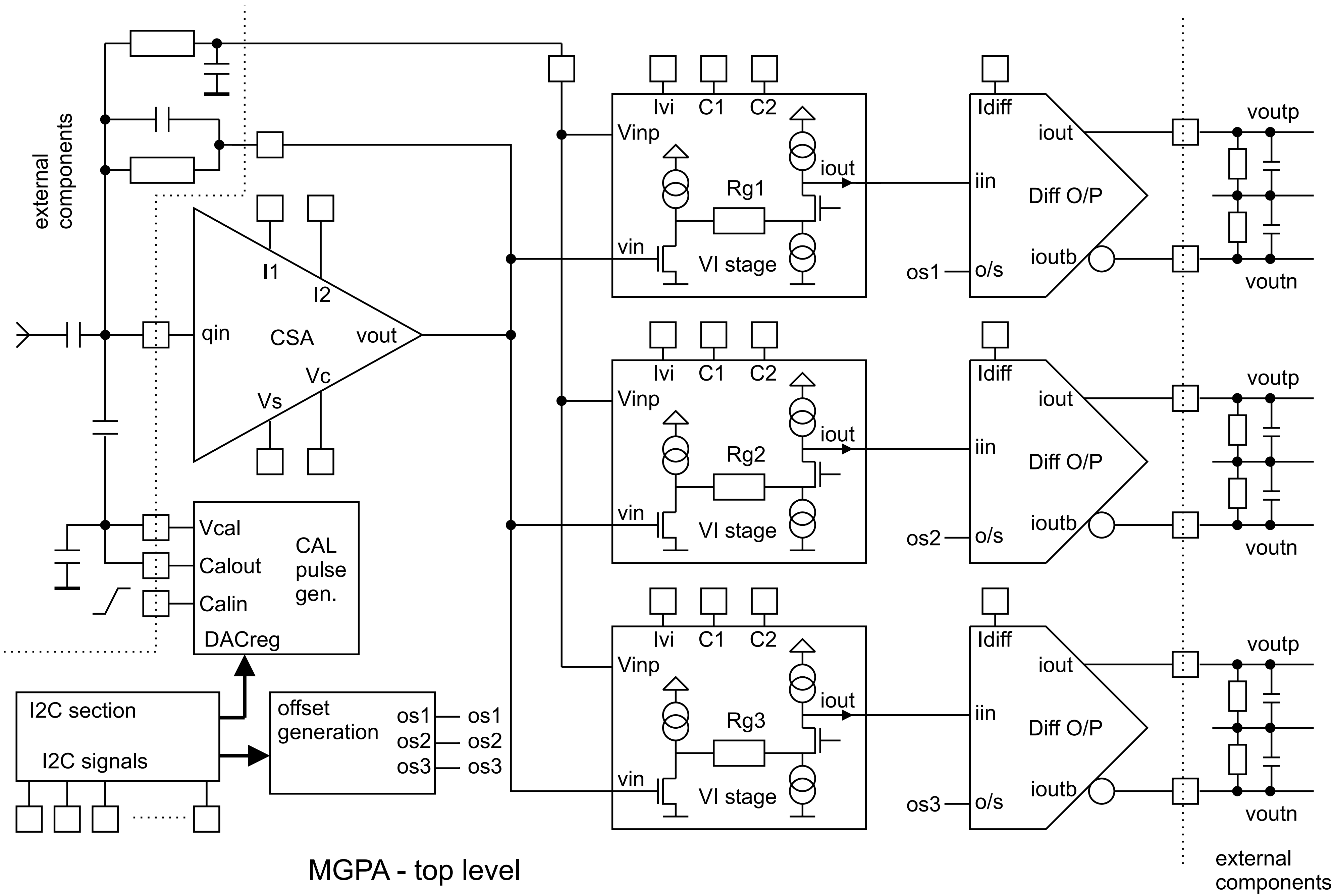
The bias generator circuit also includes a deactivating transistor controlled by the input pin BIAS_ENB. This signal is internally tied to ground with a 50k resistor, and as such may be left unconnected on the PCB. Driving this pin high will switch on the bypassing transistor, deactivating the bias generator circuits.

The bias generator current outputs are wired internally to each differential output stage, but the signals also pass analogue i/o pads (OFFSET0, OFFSET1, OFFSET2). By disabling the bias generator (using the BIAS_ENB signal detailed above) external current references may be fed to each output stage through these pins if required.

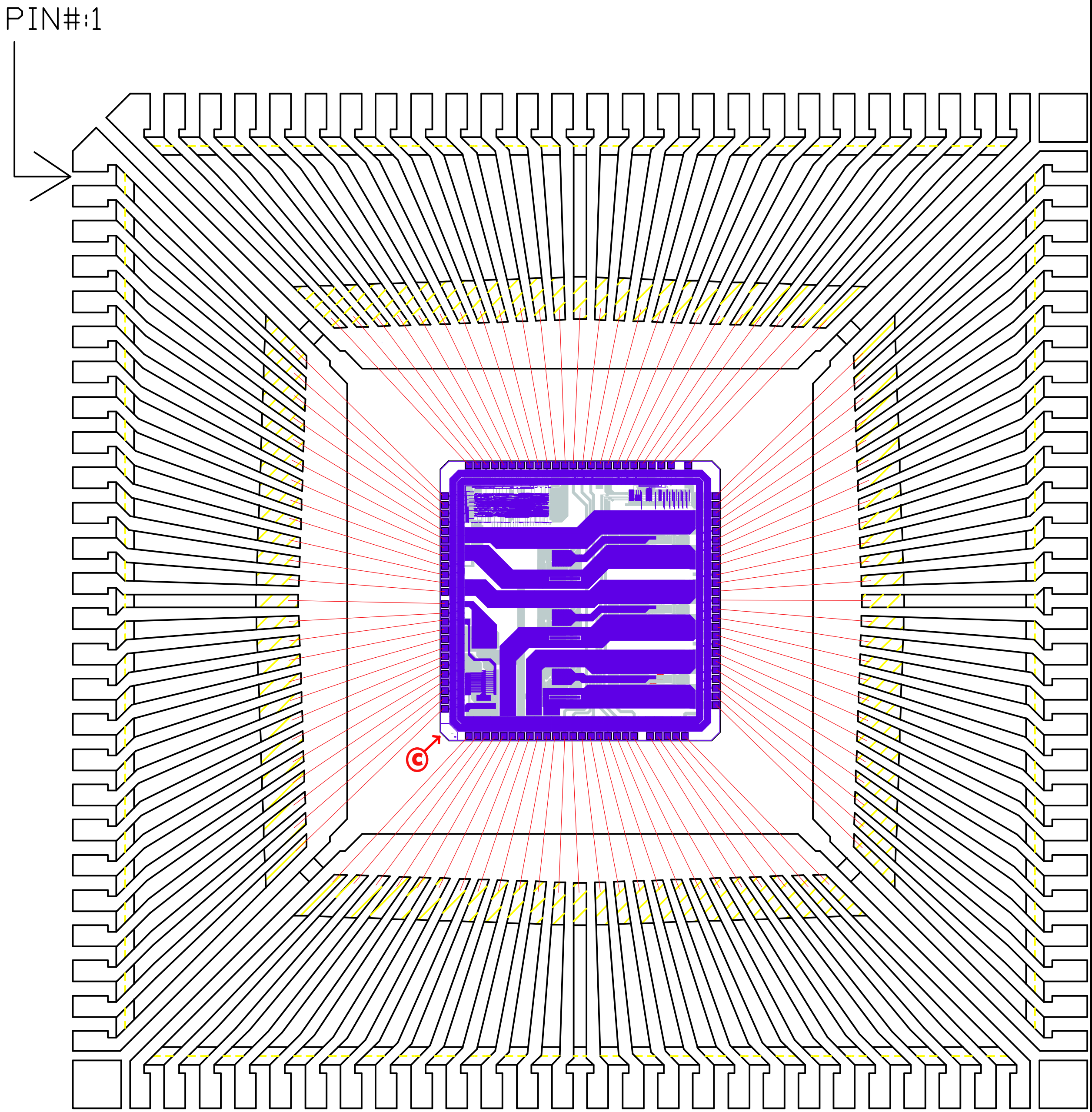
8. APPENDICES

These additional pages should be attached to this document on the pages that follow:

- Functional Block Diagram
- MGPA Version 1 Bonding Diagram.
- External Circuitry schematic. (Mark Raymond)
- Suggested PCB layout. (Mark Raymond)
- Package Technical Drawing: External dimensions. (Atlantic Technology)



MGPA - top level



atlantic technology

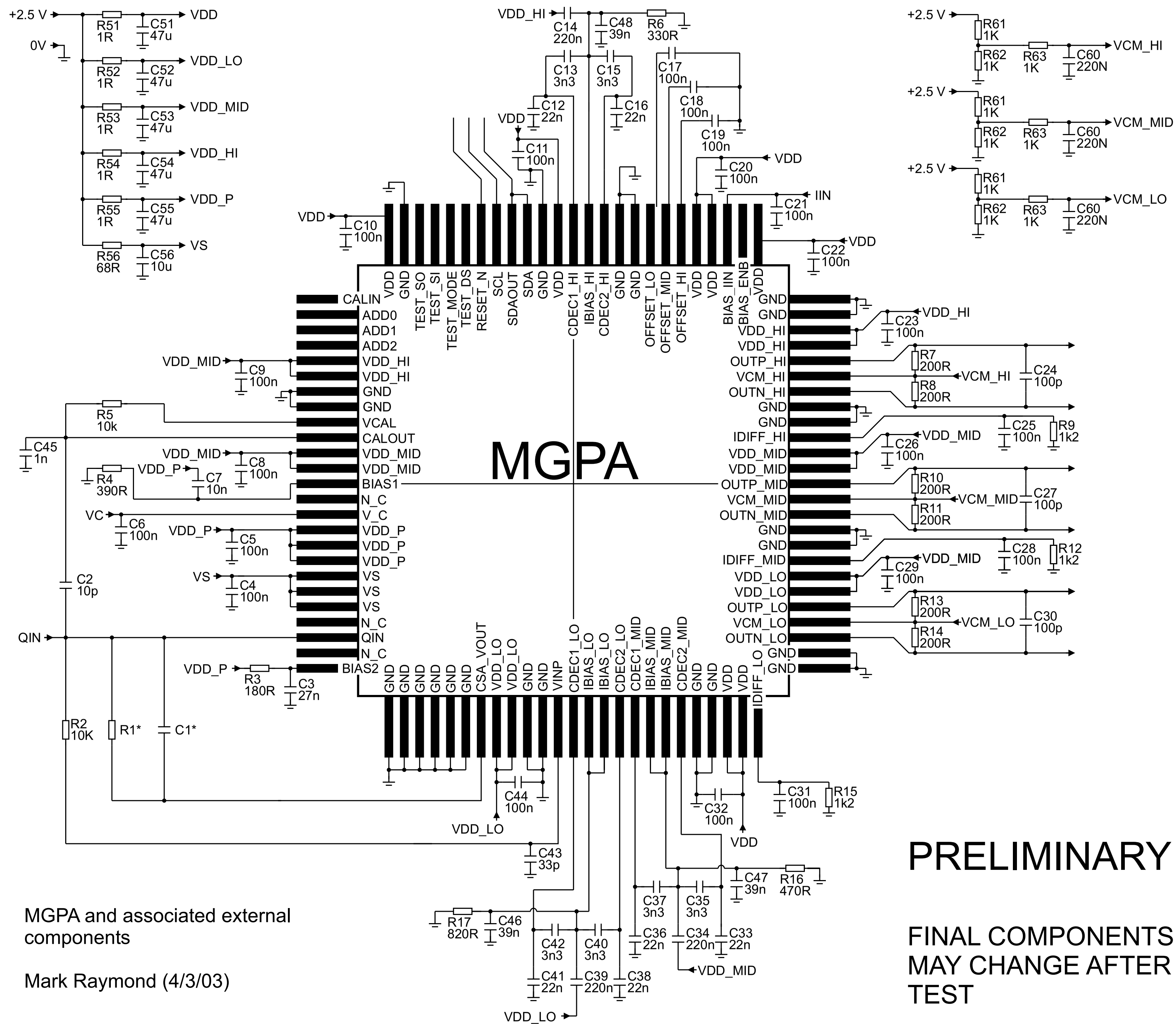
Document # : BBD18100223
Revision : A
Date : June 07 2000
Drawn by : Lewis Hamer

Leadframe

Description : 100LD TQFP 260X260 CU64T
Drawing # : QPL-100-TQFP-0014-R1
Atlantic part # : 18100223

RAL Microelectronics Group

Title	Bonding Diagram
Project	MGPA Version 1
Created	26th February 2003
Updated	6th March 2003
Notes	TQFP 100-pin 0.5mm pitch package Chip placed in centre of die mounting 25 Bond pads each side All 100 pads are bonded to pins Identifying marks: (c) 2003 CLRC *M* indicated with red arrow



PRELIMINARY

FINAL COMPONENTS
MAY CHANGE AFTER
TEST

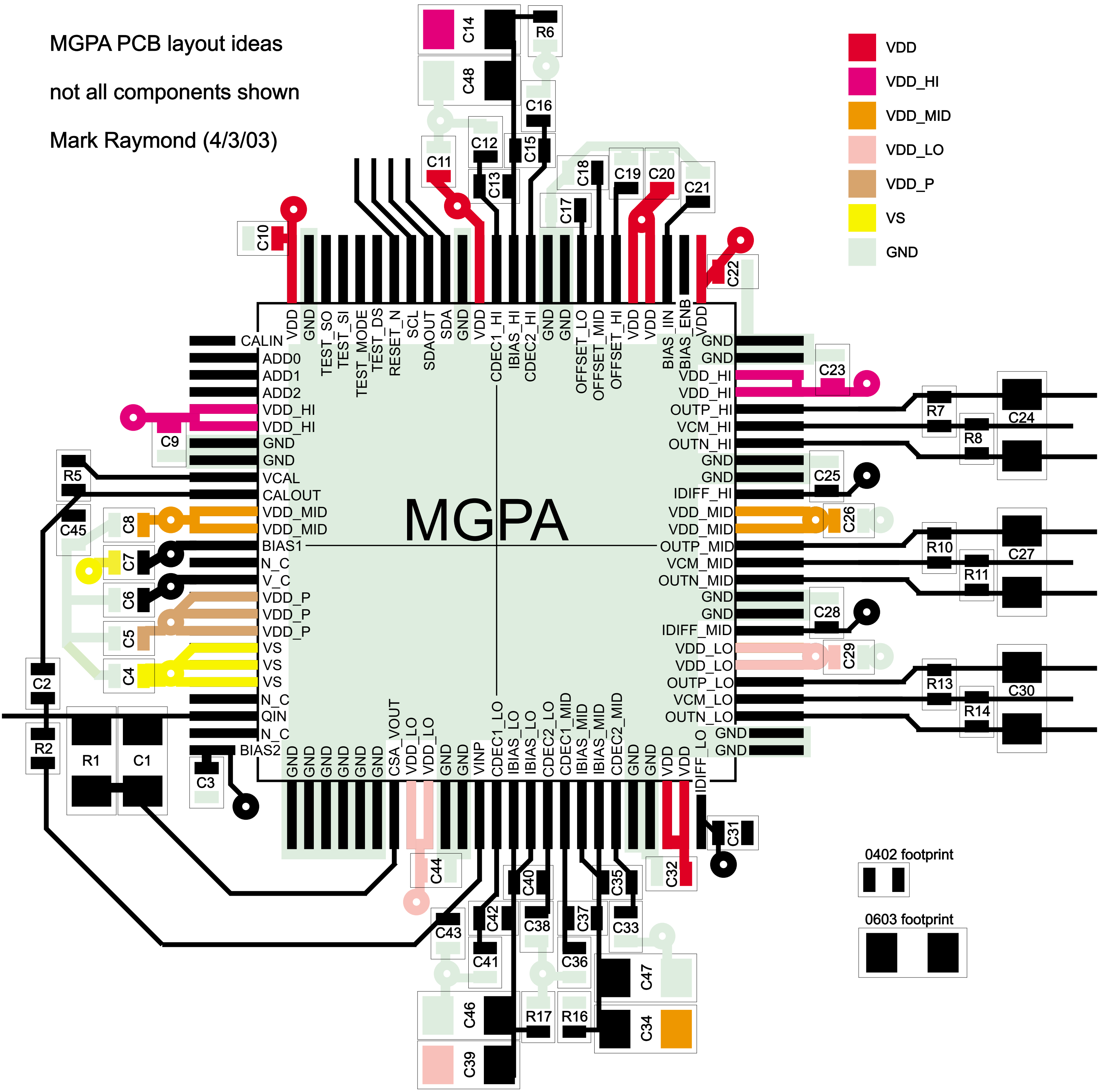
MGPA and associated external components

Mark Raymond (4/3/03)

MGPA PCB layout ideas

not all components shown

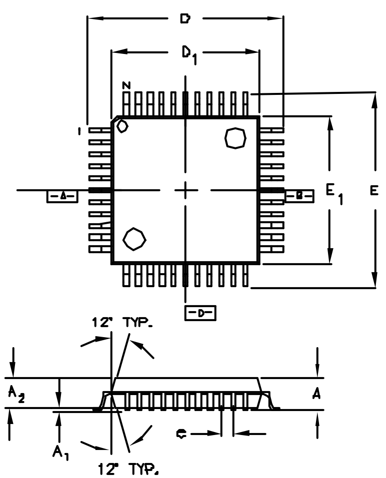
Mark Raymond (4/3/03)



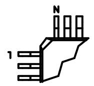
RevNo	Revision note	Date
A1	INITIAL RELEASE	17 09 00
A2	Changed reference to LQFP	04/14/11

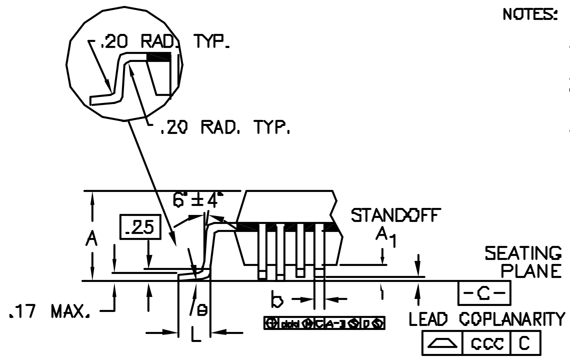
BODY + 2.00 mm FOOTPRINT

DIMS.	LEADS / TOL. \ L/F	44L-1.4 THK. .127	44L-1.4 THK. .152	64L-1.4 THK. .127	64L-1.4 THK. .152	80L-1.4 THK. .127	80L-1.4 THK. .152	100L-1.4 THK. .127	100L-1.4 THK. .152
A	MAX.	1.60		1.60		1.60		1.60	
A_1		.05 MIN./.15 MAX.							
A_2	±.05	1.40		1.40		1.40		1.40	
D	±.20	16.00							
D_1	±.05	14.00							
E	±.20	16.00							
E_1	±.05	14.00							
L	+.15/-.10	.60							
e	BASIC	1.00		.80		.65		.50	
b	±.05	.35		.35		.30		.22	
θ		0°-7°							
ddd	MAX.	.20				.13		.08	
ccc	MAX.	.10						.08	



ANOTHER VARIATION OF PIN 1 VISUAL AID





NOTES:
1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

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Drawn by	Checked by	Approved by - date	Filename	Date	Scale
Lewis Hamer	PP	NB	DGMF14141	Sept 17 00	nts

Marketing Outline Drawing

14x14 mm LQFP

DGMF 14141

Sheet 1 OF 1