MGPA version 2 submission status – Mark Raymond / Jamie Crooks (RAL)

3 changes already proposed:

      1) on-chip current reference
            present VFE card uses external circuit
            simple resistor to VDD -> supply voltage dependence

      2) re-arrange digital signals to help VFE board layout
            allow routing of CALIN line away from chip inputs

      3) Change I2C default settings
            set gain channel pedestals
            set CAL mode to ON and non-zero DAC setting

1 additional change:

      use spare pads either side of present QIN pad to triplicate QIN line
            reduces effective input inductance -> increased stability margin
            trivial layout change, worth having

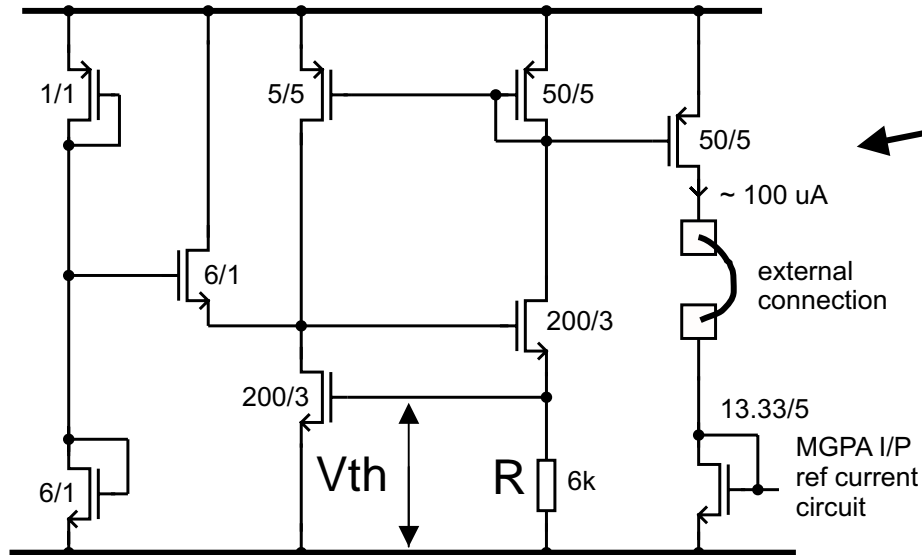# measured pedestal dependence on supply voltage
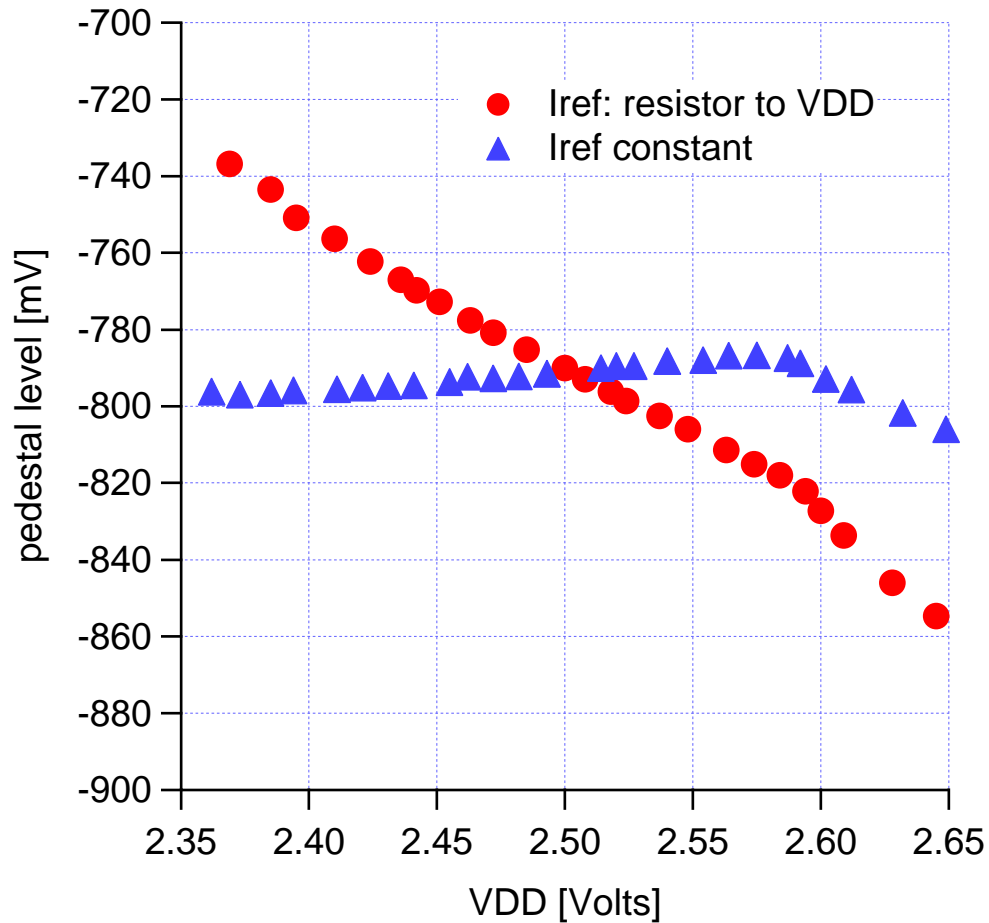
on-chip current reference

improves pedestal stability to supply drift

~ 7.5 mV VDD drift -> 1 lsb pedestal drift (if Iref const.)

(factor ~ 6 improvement on resistor to VDD)

=> worth having
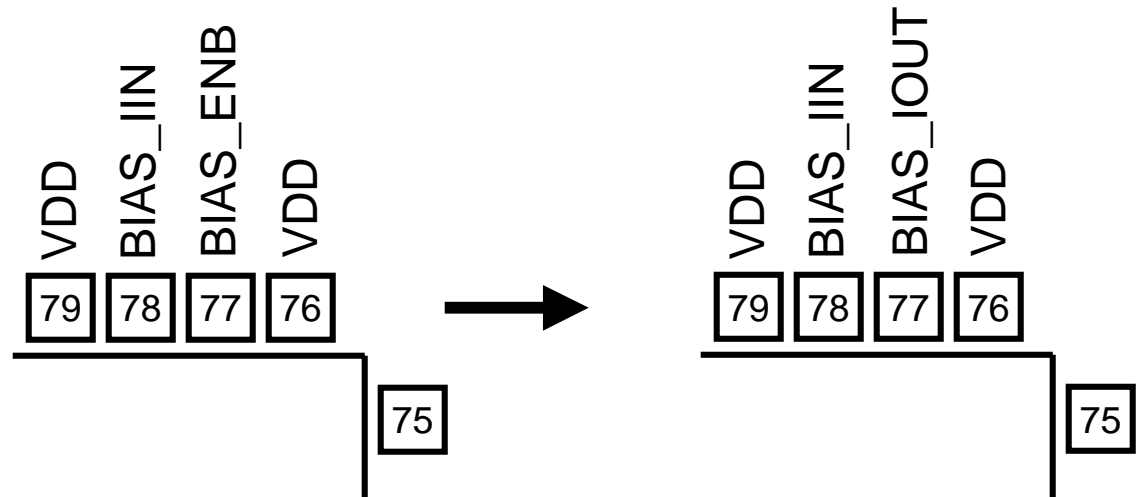
on-chip current reference

standard circuit (used before)

Iref depends on Vth and R
=> process (but **not** supply) dependent
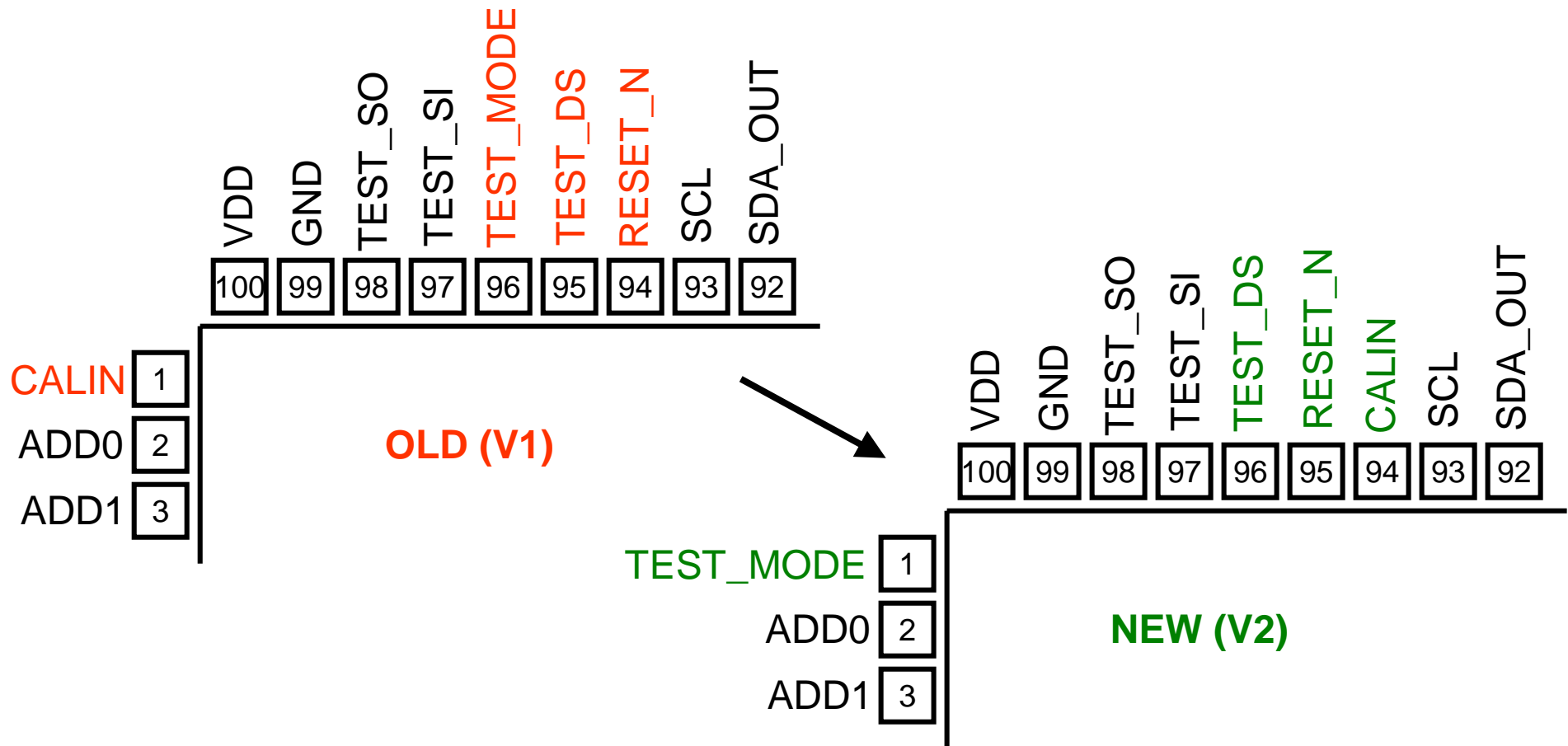
put circuit in corner of chip near BIAS_IIN pad

scrap BIAS_ENB function (not used) and replace by BIAS_IOUT (link on PCB)

Circuit labels: 1/1, 5/5, 50/5, 50/5, ~ 100 uA, external connection, 6/1, 200/3, 200/3, 6/1, Vth, R 6k, 13.33/5, MGPA I/P ref current circuit

VDD	BIAS_IIN	BIAS_ENB	VDD
79	78	77	76

75

→

VDD	BIAS_IIN	BIAS_IOUT	VDD
79	78	77	76

75

re-arrange digital signals

allows CALIN (2.5V transition) to route well away from MGPA I/P on VFE card (1 line for all 5 chips)

=> V1 and V2 pinouts **not** compatible

OLD (V1)

Pins 100–92: VDD (100), GND (99), TEST_SO (98), TEST_SI (97), TEST_MODE (96), TEST_DS (95), RESET_N (94), SCL (93), SDA_OUT (92)

CALIN 1
ADD0 2
ADD1 3

NEW (V2)

Pins 100–92: VDD (100), GND (99), TEST_SO (98), TEST_SI (97), TEST_DS (96), RESET_N (95), CALIN (94), SCL (93), SDA_OUT (92)

TEST_MODE 1
ADD0 2
ADD1 3

change I^{2}C default settings

user request for non-zero default settings for pedestals, cal mode ON and non-zero DAC value
>> chip usable (and testable) wthout I^{2}C control

problem: I^{2}C block synthesized -> don't want to re-synthesize and re-route (risk, time)

solution: can make manual changes to wiring but each bit requires several cuts/straps X 3 (triplicated registers)

=> can be done but bigger job if several bits/register

=> limit changes to one bit/register
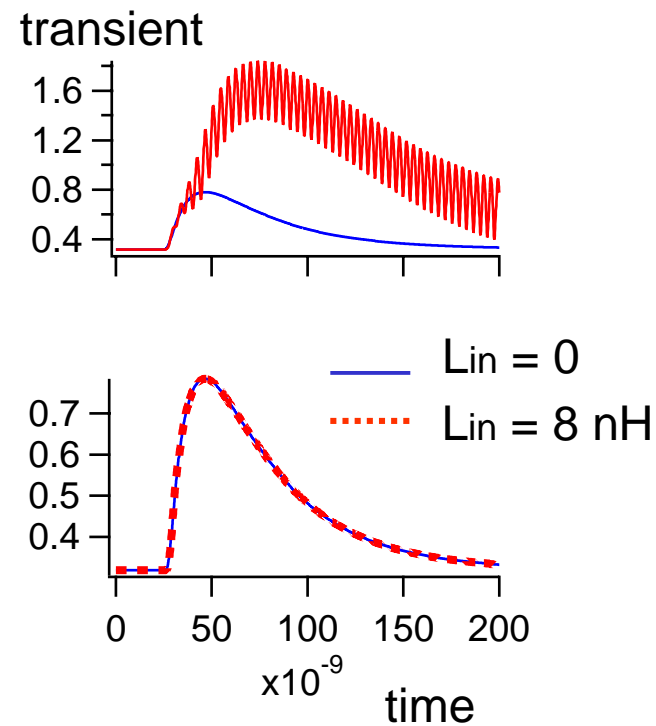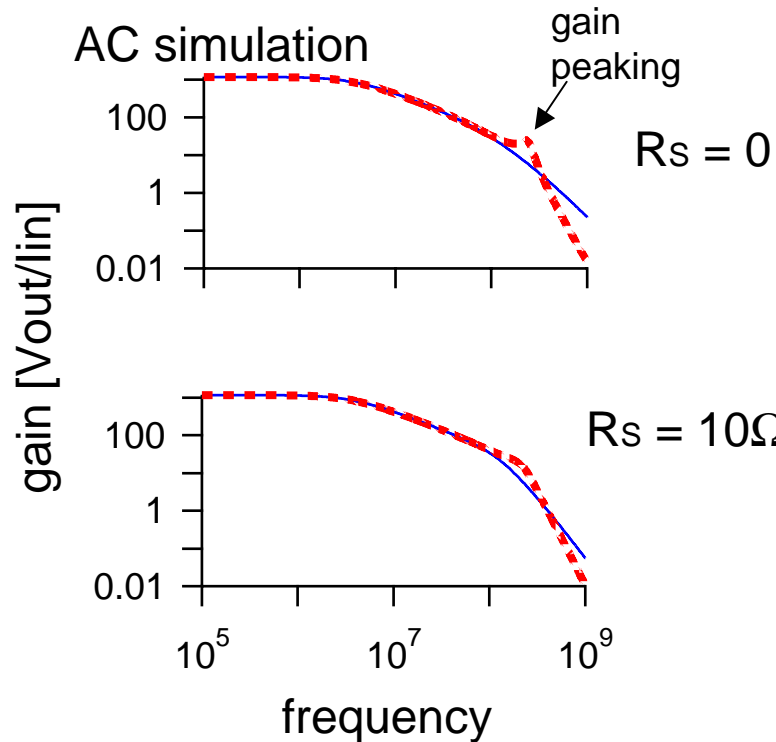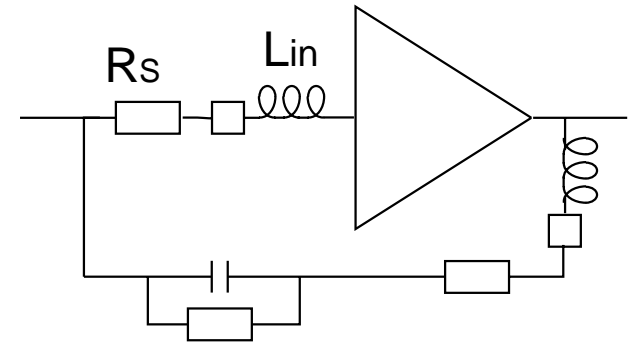
all 3 pedestal registers default to 64
control register defaults to cal ON
DAC defaults to 4 (~ 2/3 fullscale signal on high gain range for Cinj = 10 pF)

NOTE: process/fabrication variations => optimum pedestal setting will still require I^{2}C
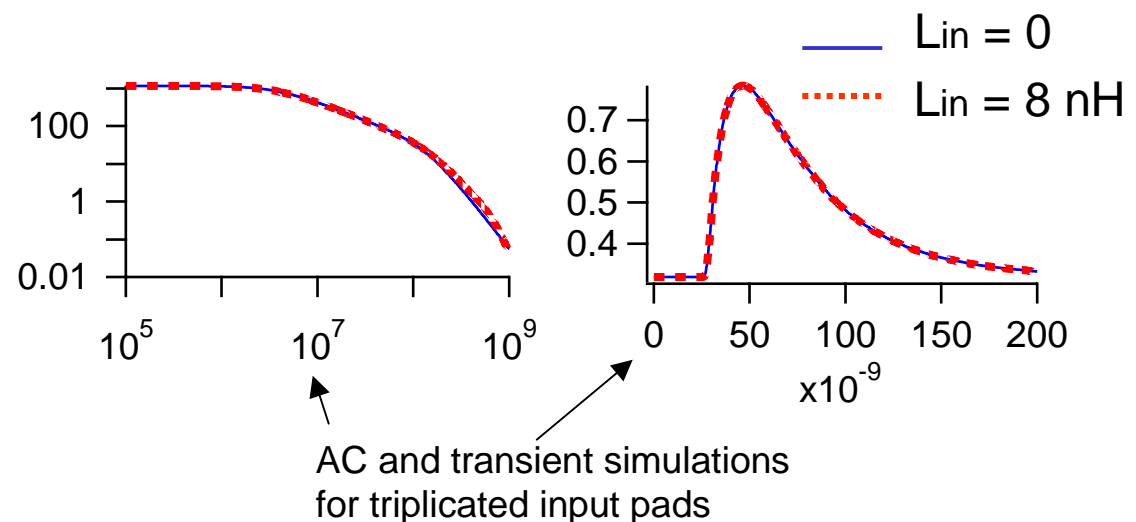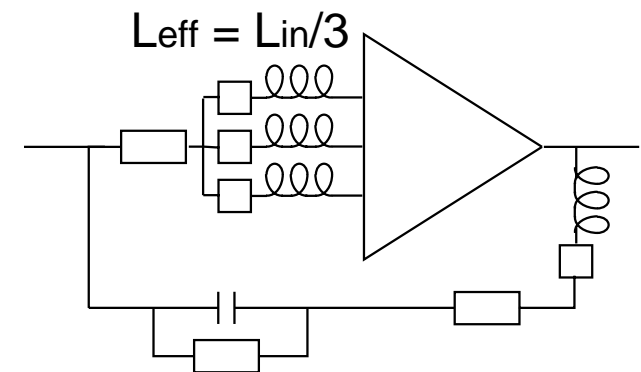
1st stage stability
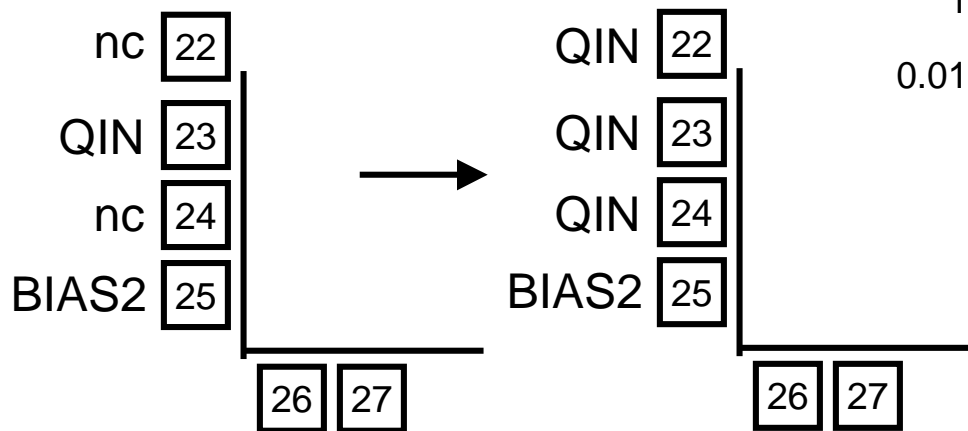
need series resistors to damp effect of parasitic L (bondwire/package)
-> effective fix for current VFE card
observed behaviour can be simulated – gain peaking in AC simulation
-> instability in transient simulation
stable if series resistor inserted

AC simulation

gain peaking

$R_S = 0$

$R_S = 10\Omega$

transient

$L_{in} = 0$

$L_{in} = 8$ nH

gain [Vout/Iin]

frequency

time

1st stage stability – any improvement possible?

yes – if make use of spare pads either side of current Qin pad
    can reduce Lin by factor 3

minor change to wiring, no change to 1st stage layout
    -> improved stability margin -> worth having

$L_{eff} = L_{in}/3$

nc	22
QIN	23
nc	24
BIAS2	25
	26 27

→

QIN	22
QIN	23
QIN	24
BIAS2	25
	26 27

—— $L_{in} = 0$
······ $L_{in} = 8$ nH

100
1
0.01

10^5 10^7 10^9

0.7
0.6
0.5
0.4

0   50   100   150   200
$x10^{-9}$

AC and transient simulations
for triplicated input pads

MGPA version 2 submission status summary

1) on-chip current reference

2) re-arrange digital signals to help VFE board layout

3) Change I2C default settings

4) modify QIN to 3 pads instead of 1

all layout changes completed and full DRC passed
most of simulations complete
some additional routine checks still outstanding (nothing major - won't go into details here)

estimated time required ~ only day or two more

design transmission to CERN expected at end of this week (Friday 14th November)