Possible use of TRIP-T for SiPM readout in ND280 experiment for T2K

Mark Raymond (Imperial College - August, 2005)
(m.raymond@imperial.ac.uk)

Introduction

This note is intended to explore ideas for using the Fermilab TRIP-T chip to instrument the front end SiPM readout of scintillators in the ND280 detector for the T2K experiment. Several aspects of the situation are evolving, including the accelerator bunch structure and details of the ND280 design, which make it difficult to specify the final readout electronics requirements precisely. The main goals of this note are to introduce the ND280 experiment in its current conceptual state, and to present a possible implementation of the front end readout electronics using the TRIP-T. It is hoped that design and test engineers associated with the TRIP-T can then use this as a basis for evaluating the suitability of their chip for the application, make suggestions for alternative or better implementations, and also clarify any issues arising from misunderstandings of the chip functionality or performance.

The ND280 detector for T2K

The Tokai-to-Kamioka experiment [1] will use a neutrino beam derived from the JPARC accelerator in Tokai. The beam will be measured by the Near Detector at 280m from its origin (ND280) and subsequently by the SuperKamiokande detector at 295 km distance. A very conceptual view of the ND280 detector is shown in figure 1. Much of the detail is still under discussion but the following parameters are more or less fixed:

- The experiment will use the CERN UA1 Magnet. This constrains the dimensions of what has to go inside (UA1 magnet dimensions 7.5 x 6.2 x 5.8 m), and also the services (cable volumes, cooling) that can be fed into the internal subdetectors (access apertures are limited).
- Much of the subdetector readout will be plastic scintillator based, with embedded wavelength shifting fibres, and it is planned to use the same photoelectric element (and hence the same front end electronics architecture) throughout. The Silicon Photomultiplier (SiPM) is the preferred choice.
- The number of scintillator based channels will probably be ~ 50 – 100k.
- The entire detector must be finished by April 1, 2010. The Fine Grained detector (scintillator/SiPM based) must be operating by April 1, 2009.

The accelerator beam bunch structure will be something like that shown in figure 2. This figure is already out of date however, and it is now thought likely that the number of bunches/spill at start-up may be 15, with the gap between buckets at roughly half that shown (i.e. ~ 290 ns). The gap between spills is long, allowing plenty of readout time. The physics occupancy will be low with only ~ few ν events/spill, and the event rate/channel will be dominated by the dark rate in the SiPMs, which will depend on the electronics detection threshold (e.g. the discriminator threshold setting in the TRIP-T).

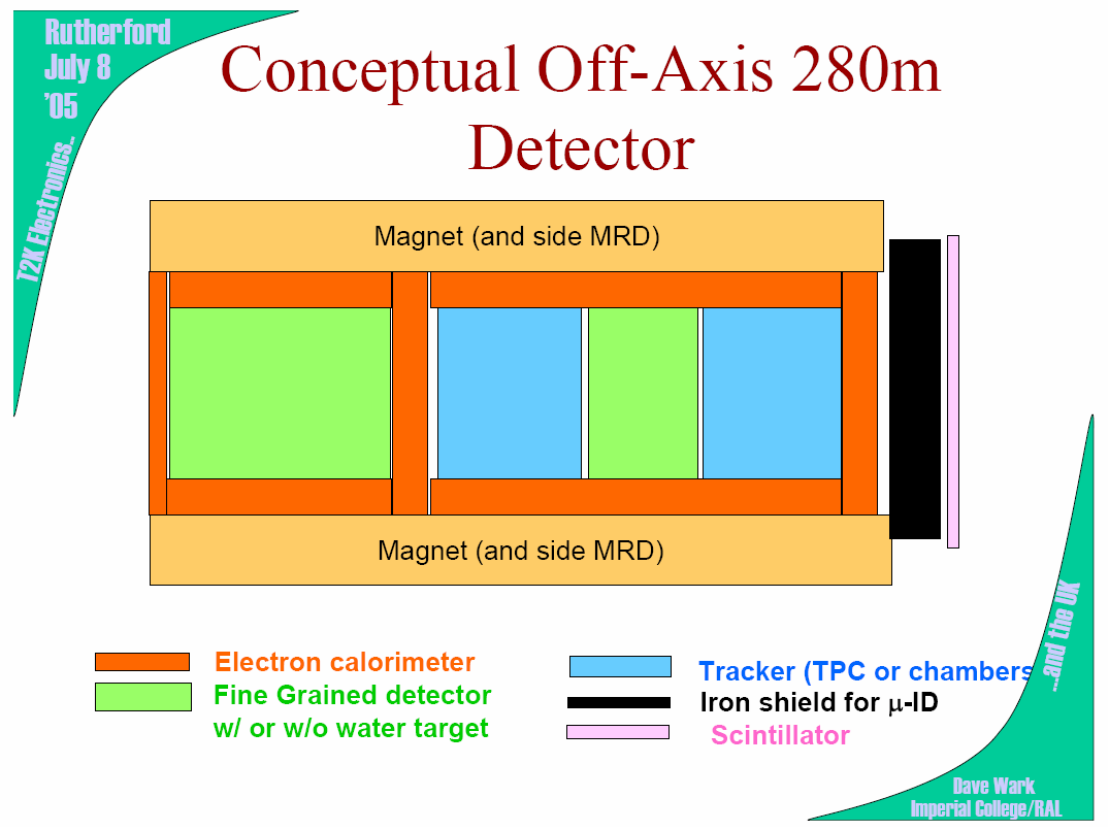

Figure 1. ND280 conceptual view

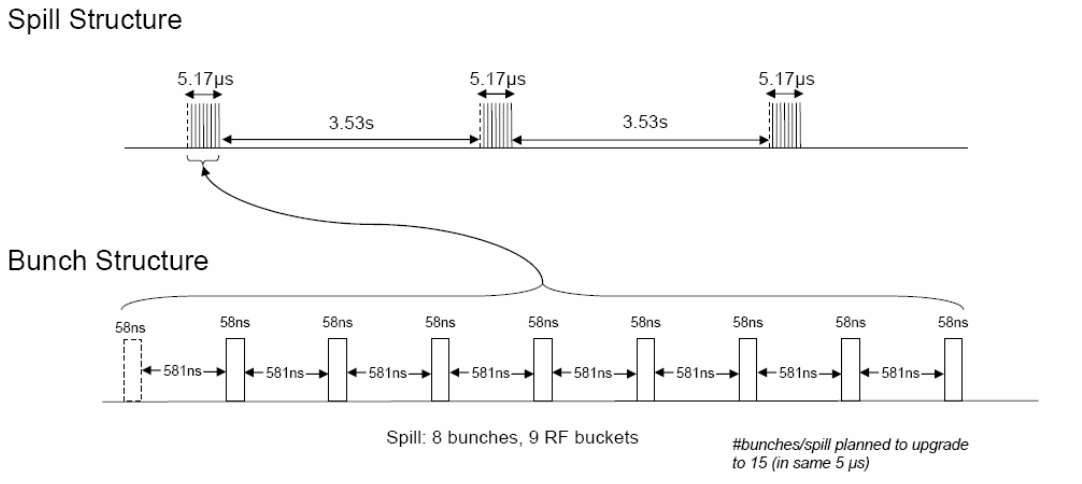

Figure 2. Accelerator beam spill and bunch structure. Note this structure will change and it is already expected that the number of bunches/spill will increase to 15, and the inter-bunch spacing will reduce to ~ 290 ns. There will still be a long gap between spills.

Silicon Photomultipliers

The SiPM has been around for a number of years, and is based on the principle of a pixellated array of APDs operated in Geiger mode, the signals from all pixels being summed together on one output. Arrays of several thousand pixels, with total areas of a few mm^2 are possible. The resulting detector has single photon resolution, and sub nsec. time response. The output signal is given by the number of photo-electrons generated by the incident light (the number of pixels firing), multiplied by an avalanche gain factor of $\sim 10^5 - 10^6$. Figure 3 shows a pulse height spectrum where the single photoelectron peaks arising from an LED light pulse are clearly observed, and they can also be observed in the spectrum for charged particles traversing a scintillator tile with SiPM readout.

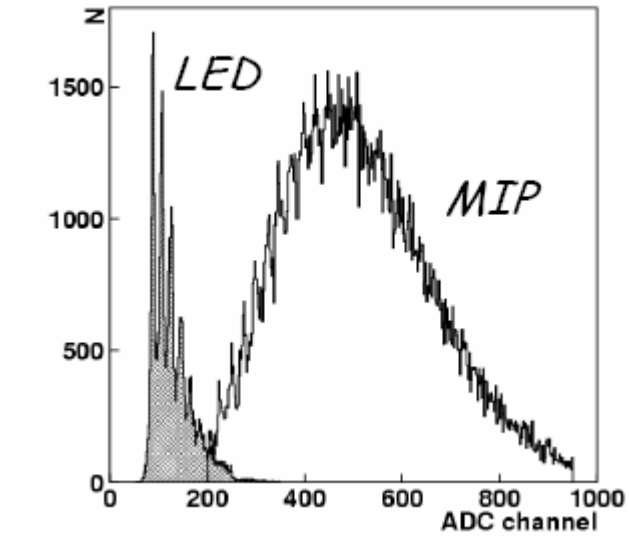

Figure 3. Pulse height spectra of SiPM response to LED light pulses, and charged particles traversing a scintillator tile read out by a SiPM [2].

Two attractive features of SiPMs are room temperature operation and magnetic field insensitivity. There is a significant single photoelectron (p.e.) dark rate, however, of ~ 1MHz at room temperature, but this can be suppressed by setting a detection threshold of greater than 1 p.e..

SiPMs are not yet commercialised but we have good grounds to believe that high quality devices will be available, in quantity, within the T2K time-scale.

ND280 SiPM readout electronics requirements

signal

A summary of some of the requirements for the ND280 SiPM front end electronics is given in table 1. A range of signal sizes is given in all cases for SiPM gains of between 10^5 and 10^6. SiPM gain cannot be defined more precisely at this stage.

The typical physics event signal size will be ~ 10 p.e., but other signal sizes may occur up to 300 p.e.. We would like to resolve single p.e. signals as this can be used for SiPM gain calibration. This then defines the overall resolution requirement at ~ 10 bits, assuming that a single channel has to cope with the full dynamic range with single p.e. resolution. This assumption may not be necessary – see later.

The rms noise should be better than the single p.e. signal size if this is to be resolved, and I have arbitrarily suggested a factor of 5. It is not clear what linearity is required but this spec. should not be too demanding since there will be significant inherent signal size fluctuations (e.g. variations in number of photoelectrons produced).

deadtime, timing and triggering

The detector should be dead-time less during the spill or, in other words, the system should be sensitive to signals at all times when there is a possibility of their occurrence. I don't think this prohibits resetting the preamp between bunches (as would likely be required for the TRIP-T), although it would be desirable to keep the reset period as short as possible. There is also a requirement to be sensitive to cosmics for some of the time for calibration purposes, but this can be outside the spill period.

A time resolution of ~ 1nsec is required to obtain position resolution of the scintillation along the scintillator length.

The scintillator/SiPM based detector system does not have to provide a trigger during the spill. There is a requirement for a trigger on cosmics to the TPC based tracker, which could (and probably should) be provided by one of the scintillator/SiPM systems, but this does not seem difficult if the ~ 1 nsec timing resolution requirement has been met.

Table 1. ND280 electronics requirements.

parameter	**value/comment**	**additional comments**
full-scale signal range	5 - 50 pC	value for 300 p.e. depending on SiPM gain of 10^5 - 10^6
resolution	single p.e., 16 – 160 fC	needed for gain calibration
typical signal size	~ 10 p.e., 0.16 – 1.6 pC	
digitization resolution	~ 10 bits (single p.e. res'n, 300 p.e. full-scale)	assumes single gain channel per SiPM
linearity	not yet clear what is required	probably not demanding
noise	< (single p.e. signal size)/5	S/N for single p.e. > 5
time resolution	~ 1ns time stamping of hits desirable	

TRIP-T for ND280 at T2K

The TRIP-T chip, figure 4, was developed for VLPC readout of scintillating fibres in the D-zero tracker. It is a 32 channel 0.25 μm CMOS chip available in a QFP type package, and operates with a single 2.5 V rail. Each channel has an integrating preamplifier with a programmable choice of two gain ranges. The preamplifier output is buffered and fed, via another programmable gain stage, to a 48 cell deep analogue pipeline, and a discriminator with a programmable threshold. An analogue level representing the time between the discriminator firing, and the end of the preamplifier integration period is stored in a second 48 cell pipeline. The signal and timing pulse amplitudes are referred to as the *A* and *t* pulses respectively.

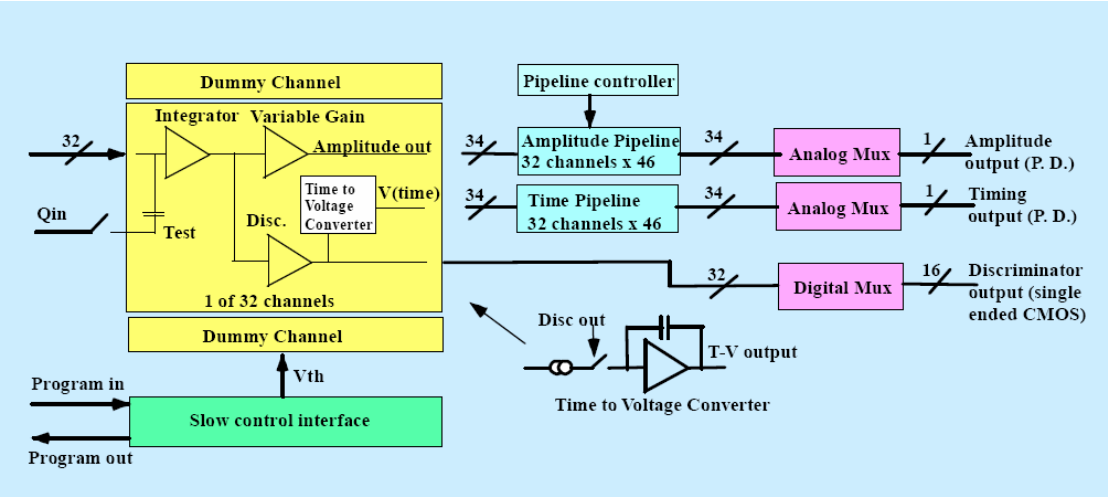

Figure 4. TRIP-T block diagram [3].

The state of the 32 discriminators can be read in a two stage process during the preamp reset period. If a hit has occurred a trigger pulse should be returned to the TRIP-T (with the appropriate timing to take account of programmed latency) to mark the required time-slice for subsequent readout.

My understanding of some of the TRIP-T specifications and performances is summarized in table 2.

Table 2. TRIP-T specifications and performance. Data taken from [3,4,5].

parameter	value/comment	additional comments
full-scale signal range	150 fC – 2 pC	programmable gain (2 preamp settings, 8 for *A*-pulse stage)
preamp reset time	variable: 245 ns used for D0	would like to use minimum possible value
preamp integration time, T_{INT}	variable: 155 ns used for D0	noise increases with T_{INT}
A-pulse noise	< 1fC	for C_{DET} = 35pF will also depend on T_{INT}
discriminator threshold	> 30-40 fC required to keep t-pulse amp. ~ independent of signal size	ref [4]
t- pulse time resolution	~ 2 ns	
power	265 mW / 32 channel chip	
digitization	external ADC required	e.g. AD9201, dual channel, for *A* and *t* pulses, 215 mW

Operating TRIP-T in ND280

Like the AFE system for D-zero, each TRIP-T in the ND280 system will be associated with a Front End FPGA (as many TRIPs / FE FPGA as possible) which would provide the following functionality:

- programming analog bias level and control registers: There are a number of control and bias registers which have to be programmed for correct chip operation, including analog bias currents and voltages, discriminator threshold, pipeline depth, gain, and internal test pulse circuitry.
- fast digital control signals: These include the preamplifier reset/integrate control line, the pipeline clock and readout lines, the discriminator output control lines, the slow control interface lines, …
- control lines to the external ADC
- formatting the front end data, and transmission to higher levels of the DAQ

Figure 5 shows the same picture as figure 2 but includes some detail of how the TRIP-T chip might be operated. The preamp is reset during the gaps between bunches. The pipeline clock follows a similar cycle, controlling the *A* and *t* pulse storage to their respective pipelines If a signal above threshold occurs during the preamp integration period, in any channel, the relevant discriminator fires and the *t* pulse is generated. The *A* and *t* pulses are transferred to their pipelines at the end of each integration period and then the preamps are reset. In the absence of hits just the *A* and *t* pulse pedestals are written to the pipelines. The state of the discriminators is accessed by the FE FPGA during every preamp reset period. If a hit is present the FE FPGA generates a trigger back to the TRIP-T to mark the appropriate pipeline column for subsequent readout.

Readout and digitization, if one or more hits has been registered, will occur at the end of the bunch train, within the long spill gap. Acquisition sequences can also be generated during the spill gap to provide sensitivity to cosmics.

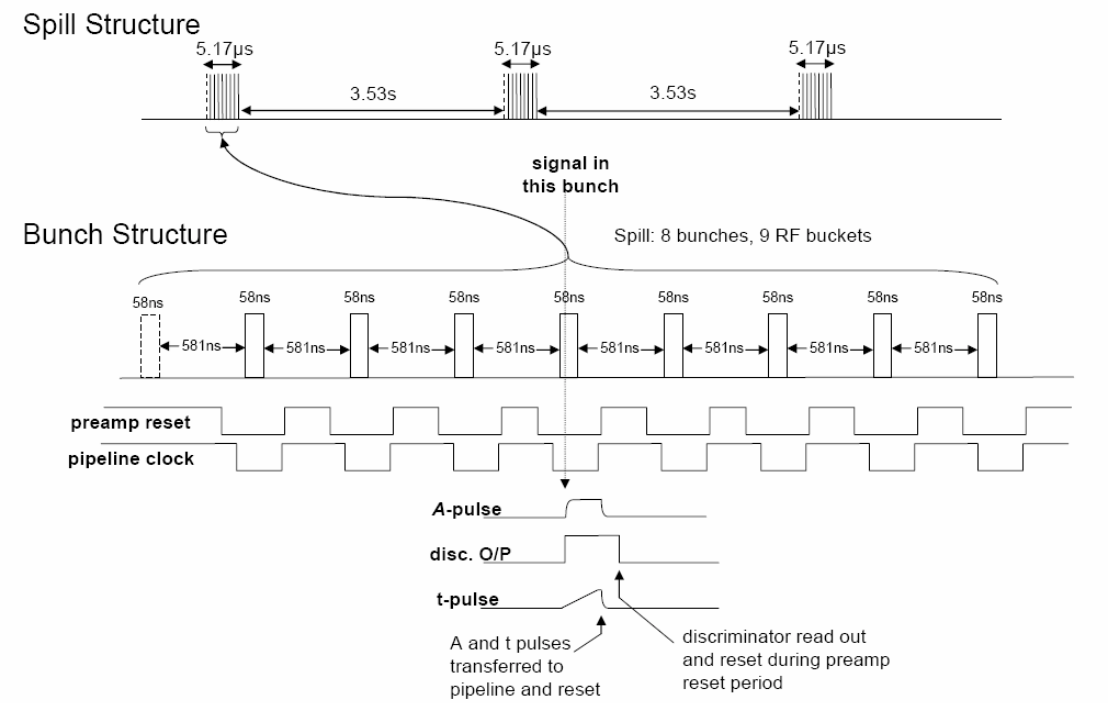

Figure 5. Beam structure with added TRIP-T signals.

Analog front end issues

It is clear that there is an incompatibility between the TRIP-T input range and the expected SiPM output. Some method of external attenuation will be required, but this does not solve all the issues. For example, if the TRIP-T is used on a gain setting to give a full-scale range of 500 fC, and the external attenuation is adjusted such that the SiPM 300 p.e. signal delivers this amount of charge, then a single p.e. will only give 1.7 fC which is similar to the TRIP-T rms noise and a long way from the 30 – 40 fC required to reliably trigger the discriminator [4]. I believe it is not possible to program different gains for different TRIP-T channels. A possible approach might be to assign two TRIP-T channels to each SiPM and adjust the external attenuation components such that one channel receives more signal than the other. In other words, each SiPM is read out by two channels with different gains. Consider the following scenario:

- Program the TRIP-T gain for ~500 fC full-scale range (max. preamp gain, minimum 2nd stage *A*-pulse gain).
- Set **high** gain channel external attenuation such that **20 p.e.** from SiPM delivers full-scale (500 fC) to TRIP-T.
- Set **low** gain channel external attenuation such that **300 p.e.** from SiPM delivers full-scale (500 fC) to TRIP-T.

In this situation the high gain channel gets 25 fC / p.e. and a reliable discriminator threshold can be set at ~ 1.5 p.e.. Once the high gain channel saturates (at signals greater than 20 p.e.) the signal can still be retrieved from the low gain channel, where a 20 p.e. signal would correspond to 33 fC, well in excess of the noise.

Chip count and power

If the two TRIP channels/SiPM idea was to be adopted, and using 50k SiPM channels as an example, this would translate to 3125 TRIP-T chips and AD9201 ADCs. The power consumption for these two chips alone is 30 mW / SiPM channel leading to a total power of 1.5 kW for 50k channels. In addition to this there will be the power in the FE FPGAs, which will be speed and functionality dependent. For comparison the D-zero AFEII board consumes 48 Watts for 16 TRIP-T front end chips [6], which would translate to 187 mW / SiPM channel, or 9.35 kW total in our scenario. It is to be hoped that the substantial difference between total power and TRIP-T/ADC power alone in the AFE system would not be the same in ours, as we will be constrained in terms of power and cooling provision by the UA1 magnet design. Hopefully there is more power hungry functionality in the AFE system than we would have. I think it is also true that our system would (on average) run much slower.

Conclusion

An outline of the ND280 experiment for T2K and its front end electronics requirements has been presented, together with some ideas for an implementation of this using the Fermilab TRIP-T chip. I hope this is sufficient to allow the TRIP-T experts to comment and/or provide alternative ideas, and to correct any misunderstandings of TRIP-T functionality or performance.

References

[1] http://neutrino.kek.jp/jhfnu/

[2] “The scintillator HCAL testbeam prototype”, Felix Sefkow, March 2005, talk given at the 2005 International Linear Collider Workshop.

[3] “ASIC Research and Development”, Ray Yarema, April 20th 2005, talk given at Super B Factory Workshop in Hawaii.

[4] Bench test of Trip-t, Leo Bellantoni and Paul Rubinov, Draft D0 note.

[5] “TRIP-t bench measurements”, Leo Bellantoni, April 2005, D0 AFEII Directors Review (talk).

[6] D-Zero Central Fiber Tracker AFEII Analog Front End Board Design Specification, Paul Rubinov.
http://d0server1.fnal.gov/projects/run2b/Meetings/DirectorsReviews/AFEII_April_2005/D0Notes/AFEII%20design%20specifications.doc