Preliminary results of hybrid simulations M.Raymond (30/11/00)

After discussions with Jean-Daniel I have made some SPICE simulations to investigate the instability he has observed when powering up more than ~2 chips on the hybrid. The results here are preliminary to say the least, but I think some conclusions can be drawn which I believe indicate a way forward.

Background

During the APV25 design it was found necessary to include a unity gain inverting stage between the preamp and shaper which can be switched in or out, depending on the detector signal polarity. This maintains the same polarity of signal swing at the shaper output, maximising the use of the linear dynamic range at that point, without having to compromise on gain which would leave the design vulnerable to noise contributions from subsequent stages. The inverting stage has to be switched <u>in</u> for operation with p-strip Silicon detector readout.

The schematic of one channel of the preamplifier and inverter is shown in figure 1. The inverter implementation is very simple, its operating point being determined by the operating point of the preamp input device, since the sources of both devices are taken to V125. (I will try and stick to the convention VSS, V125, V250 here).

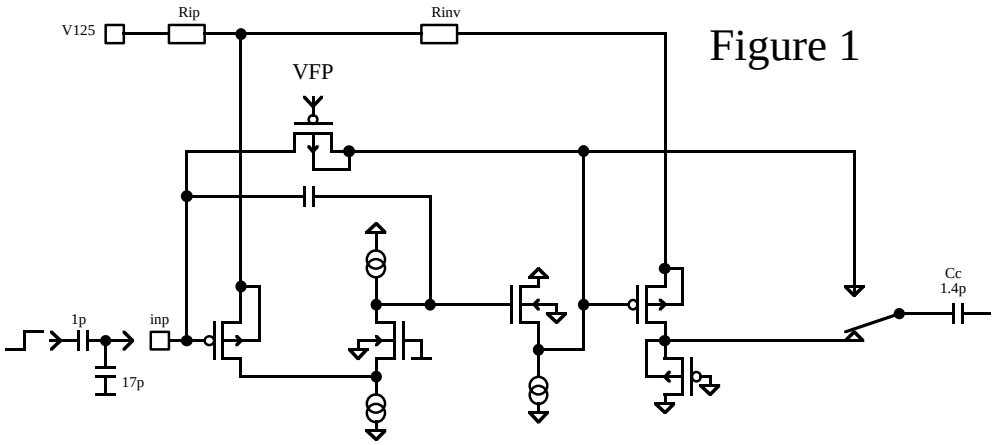

Figure 1

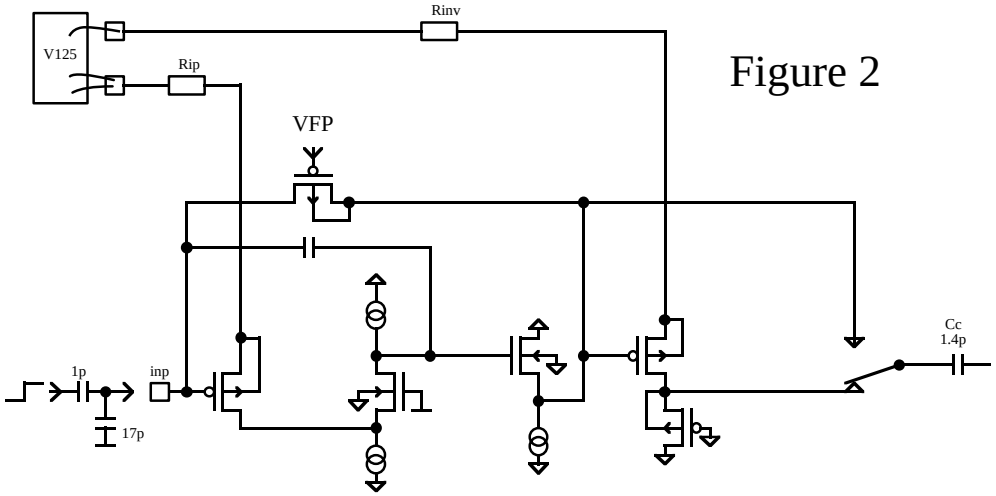

Figure 2

During simulation of the design it became clear that a common V125 line with associated resistances Rip and Rinv in figure 1 (note that these resistances are common to all 128 channels) would provide a mechanism for positive feedback around the preamplifier, resulting in instability. The solution was to split the V125 on the chip, right back to two separate V125 pads, thereby cutting the feedback loop entirely, see figure 2. This solution should be safe provided the external V125 impedance is low enough, and it was assumed that this would be the case. It now appears that this was too simplistic an assumption.

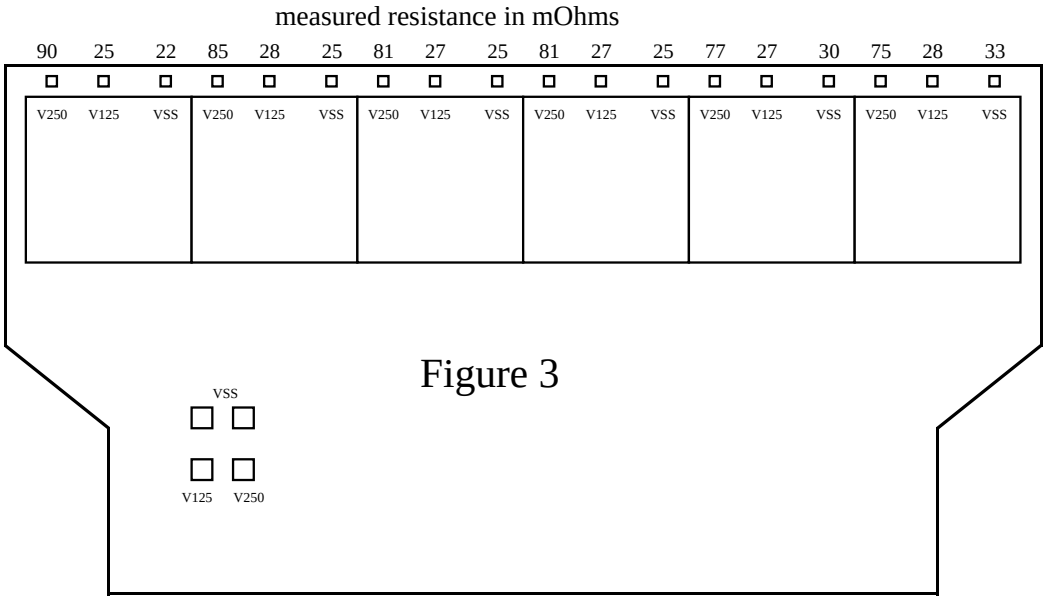

Figure 3

Measured hybrid resistances

The resistances I have measured on the hybrid are included in figure 3. The measurements were made using a four point method, from the pads where the large value capacitors are mounted to the pads at the front edges of the APVs where the analogue power is bonded. Concentrating on the V125 values it can be seen that the values are in the range 25 - 28 mOhms. For reference a 5 μm layer of Cu would have a resistance of ~ 3 mΩ/square (roughly the same for an 8 μm Au layer). The relatively large values on the hybrid arise because the power planes have significant discontinuities between the APVs and the back (power connector) edge. Maybe this could be improved in a subsequent design, although I appreciate the considerable difficulty that was encountered in getting the design into the small footprint it presently occupies.

Simulations

One way to simulate the effects of common resistance in power lines for a multi-channel chip is to simulate one channel, but insert resistor values which are the true (or best estimate) values multiplied by the total number of channels. This is the method which was used when simulating the chip. I have used a similar approach here for the hybrid, multiplying again by the number of chips. In this approach, if

capacitors are included (e.g. decoupling components) then their values must be divided by the total number of channels.

Figure 4

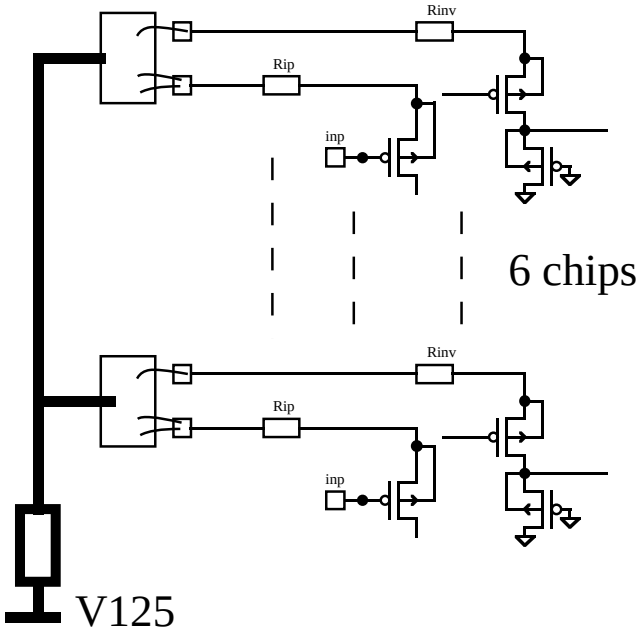

Figure 4 shows a representation of the hybrid with a common resistance from the bond pads to V125. Figures 5 and 6 show the results of a transient simulation of this network, for values of the common resistance between 0 and 35 mΩ. The simulations show the output of the preamplifier with a signal injected just after time zero (in figure 5 the time origins of the traces have been offset for clarity). This will ideally be a fast step with a slow decay time. For common resistor values up to 10 mΩ (equivalent) there is stability (figure 5), although some increase in gain is evident. Instability sets in at 30 mΩ, and at 35 there is oscillation at a frequency of about 30 kHz. This frequency (and the resistance value) are not too dissimilar to the values observed on the hybrid. It seems that stability can be achieved if the power line resistances are low enough and I think Jean-Daniel has demonstrated this with his external copper plane.

Figure 7 shows an alternative possible layout with the V125 layer segmented such that the inverter V125 connection is separated from that for the preamplifier input device. Figure 8 shows the simulation results for this layout with quite large values used for the common resistances (once again the time origins have been offset for clarity). This result shows that stability is achieved here, perhaps not surprisingly since the technique is identical to that used on the chip itself.

Preliminary conclusions

I think the simulations are reasonably consistent with Jean-Daniel's observations. The results in figure 8 indicate that it is probably better to adopt a segmentation approach than to try and achieve stability with solid power planes. If this were the approach adopted then I think it would be wise to segment the V125 supply through the connector as well (this should be possible without changing pinout). There is more

simulation work which can be done here, for example it would be good to include a realistic representation of the power cabling to the hybrid as well. No decoupling capacitance has been included in the simulation but (as J-D has pointed out) at these frequencies the capacitance values would have to be very big. I would like to mention that ceramic (at least this is what they are called in the RS catalogue) capacitors **are** available up to 10 µF in 1206 format, and 22 µF in 1210.

Figure 5

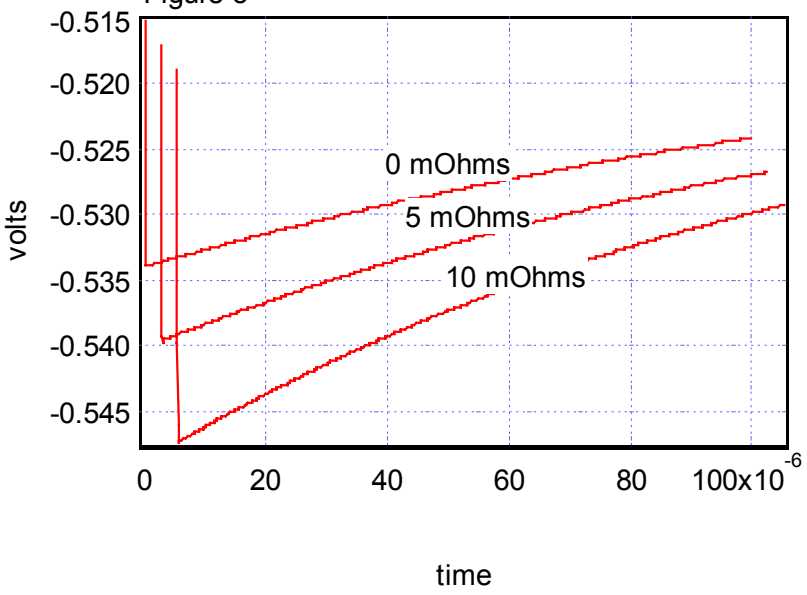

Figure 6

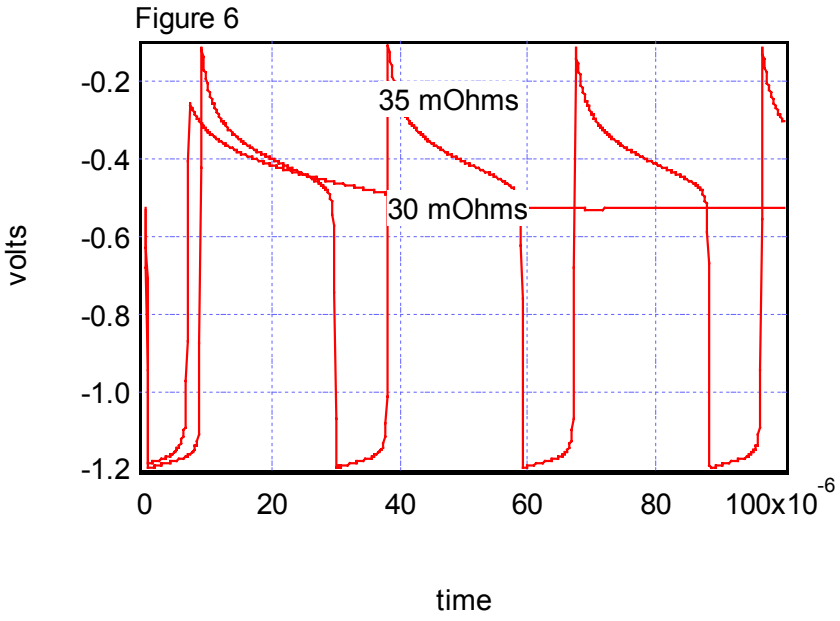

Figure 7

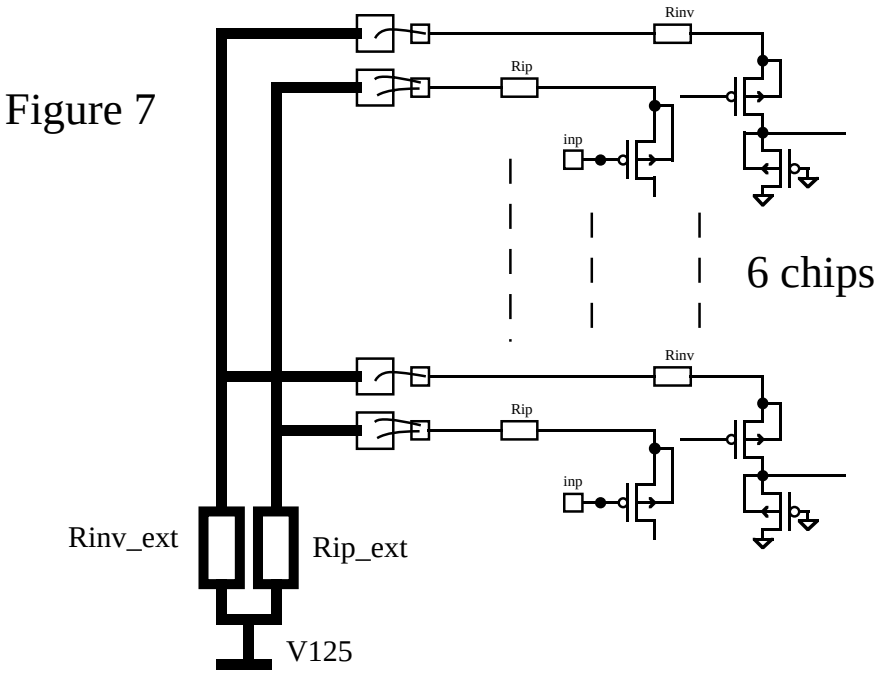

Figure 8