CBC2 update and test plans

not that much to say (test beam effort has dominated activities over recent weeks)

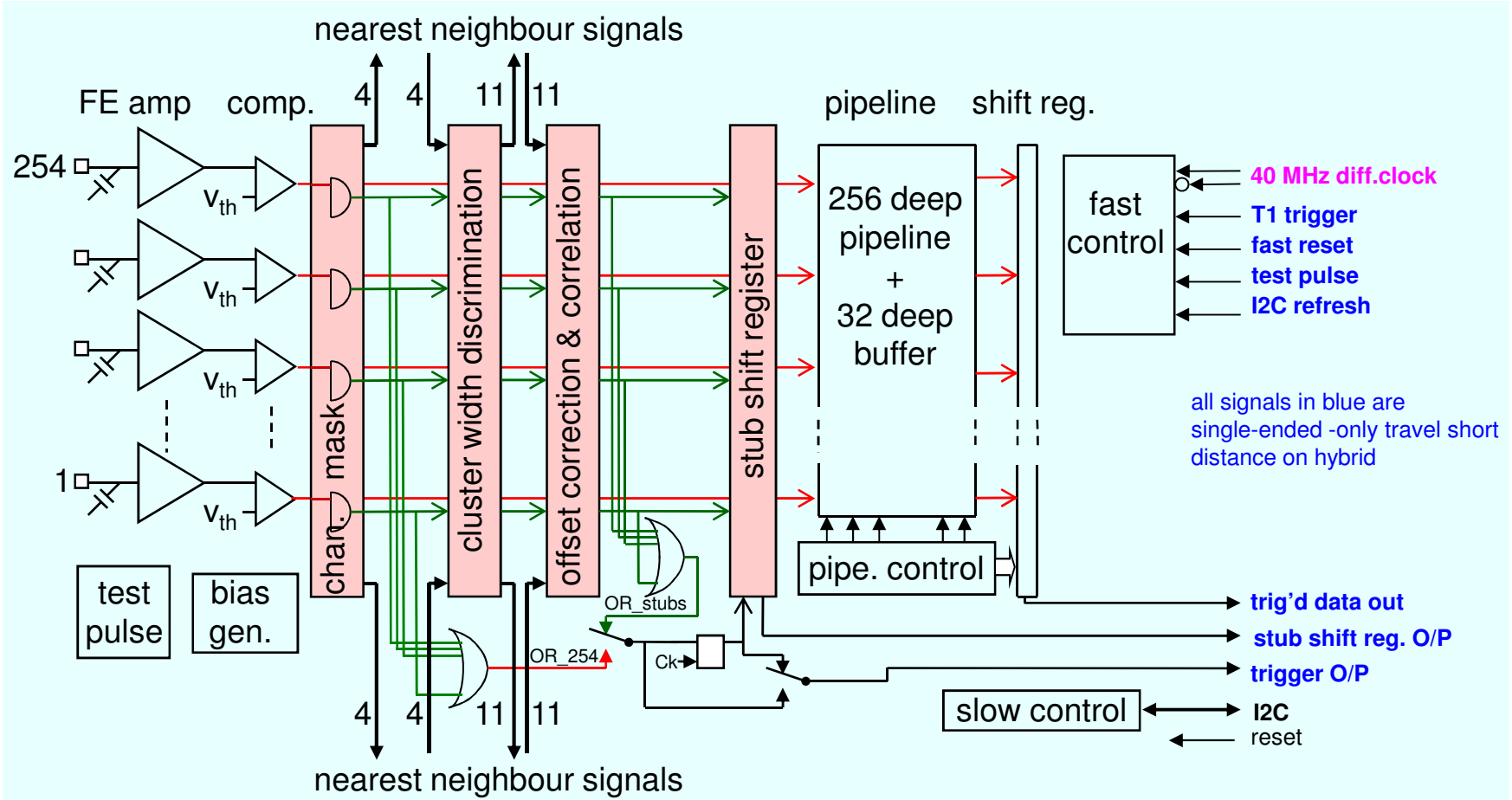
CBC2

- update on delivery
- some progress with test hardware
- update on test plans

CBC3

- some clarification of ½ strip resolution specifications

CBC2 architecture reminder



blocks associated with Pt stub generation

channel mask: block problem channels (but not from L1 pipeline)

cluster width discrimination: exclude wide clusters > 3

offset correction and correlation: correct for phi offset across module and correlate between layers

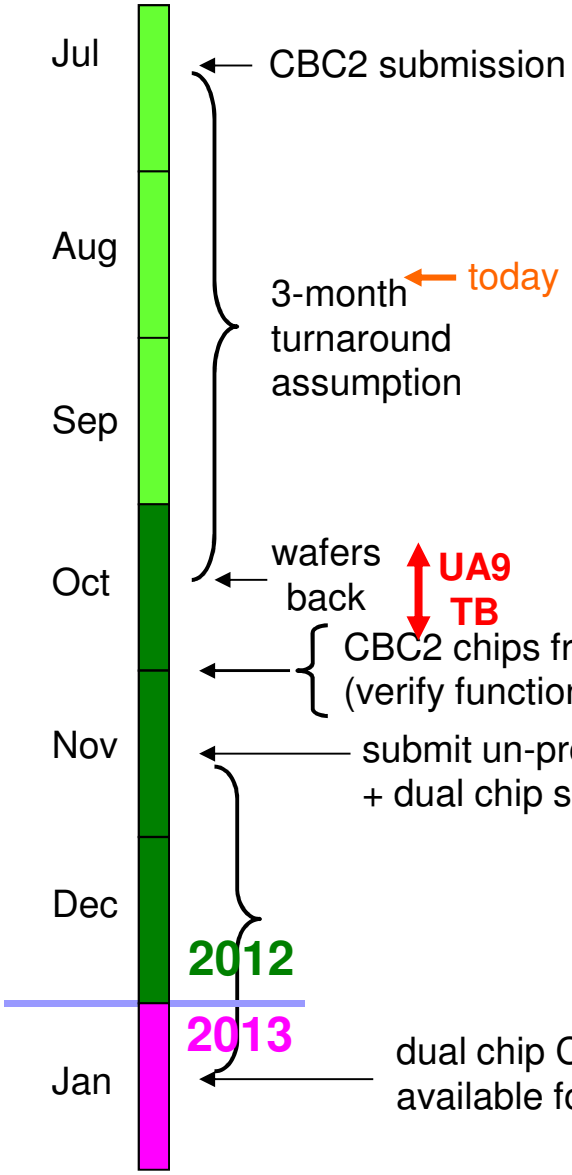
stub shift register: test feature - shift out result of correlation operation at 40 MHz

OR_254 at comp. O/P and OR_stubs at correlation O/P: - can select either to transmit off-chip, latched or un-latched

allows to study signal propagation times

timeline for next ~ 6 months

THIS ONE OUT OF DATE (from last time)



CBC2 submission

3-month turnaround assumption ← today

wafers back — **UA9 TB**

CBC2 chips from diced wire-bond (XFEL) wafer available for test (verify functionality before committing to bump-bonding assembly)

submit un-probed CBC2 C4 wafer + dual chip substrate for assembly

dual chip CBC2 substrates available for test

in this ~ 3 month period:

- prepare wire-bond board for basic functionality test (using wire-bond backend pads) — **DONE**
- prepare peripheral boards for 2xCBC2 substrate — **almost done**
- start thinking about wafer probe test — **some thinking -not much done**
- CBC1 + Infineon sensor test parasitic to UA9 test beam in Oct. (some hardware to prepare) — **DONE**

wire-bonded CBC2 first tests

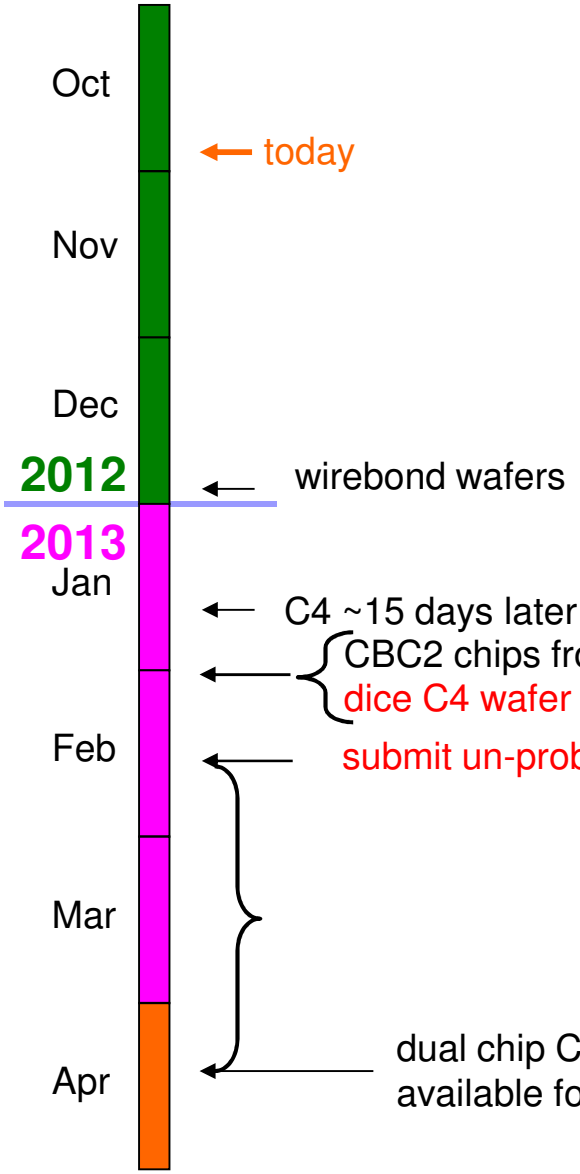
in this ~ 2 month period:

- complete wafer probe test preparations (procure probe card, prepare any other hardware, test software, ...)
- probe the wafers

2xCBC2 substrates detailed tests begin

... 8 chip substrates and prototype SS-Pt module studies follow on later in 2013

revised timeline for next ~ 6 months



latest info – wirebond wafers will leave foundry Dec. 17th
C4 wafers ~15 days later
=> schedule slips by ~ 2½ - 3 months

today

wirebond wafers

in this ~ 2.5 month period:

produce peripheral boards for 2xCBC2 substrate

use extra time to
make more thorough wafer probe test preparations
(replace old DAQ)
anticipate other test requirements (ionizing, SEU, …)

C4 ~15 days later

CBC2 chips from diced wire-bond (XFEL) wafer available for test
dice C4 wafer CBC2 chips - required for Endicott

submit un-probed CBC2 C4 chips + 2xCBC2 substrate for assembly

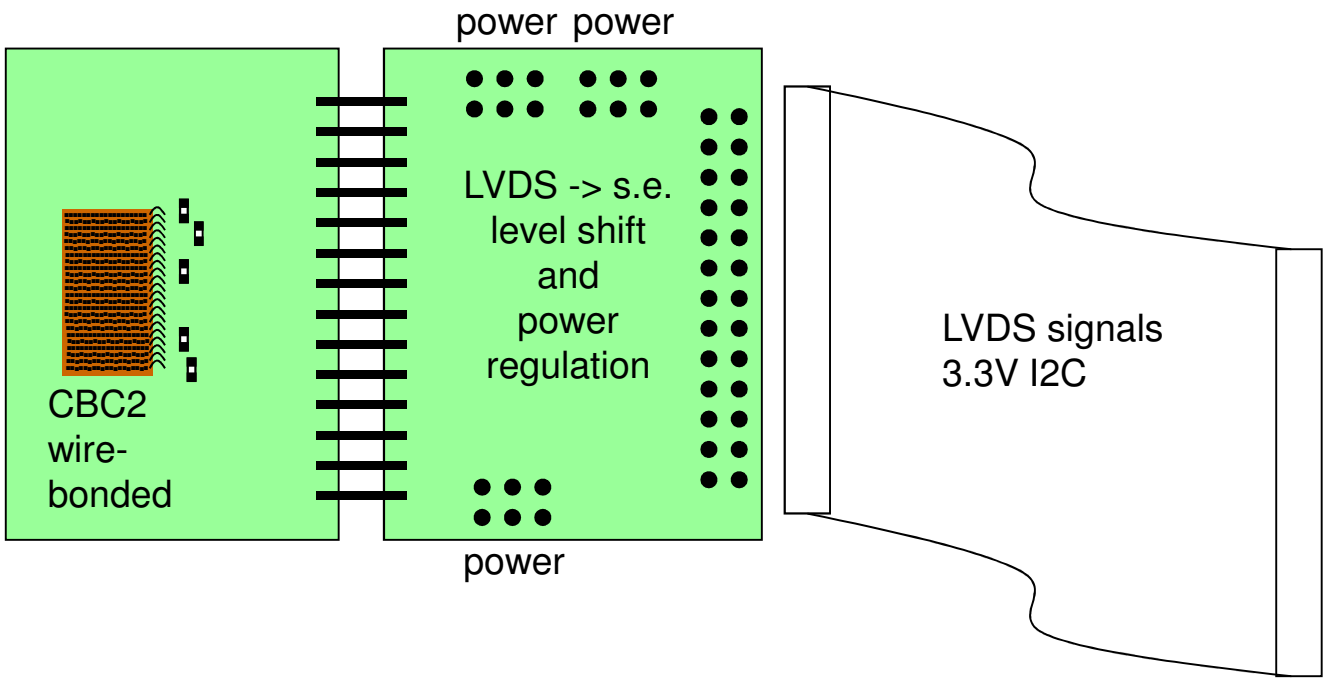
in this ~ 2 month period:

- wire-bonded CBC2 first tests
- complete wafer probe test preparations and probe the wafers

dual chip CBC2 substrates available for test

... 8 chip substrates and prototype SS-Pt module studies follow on later in 2013

wirebond CBC2 test setup

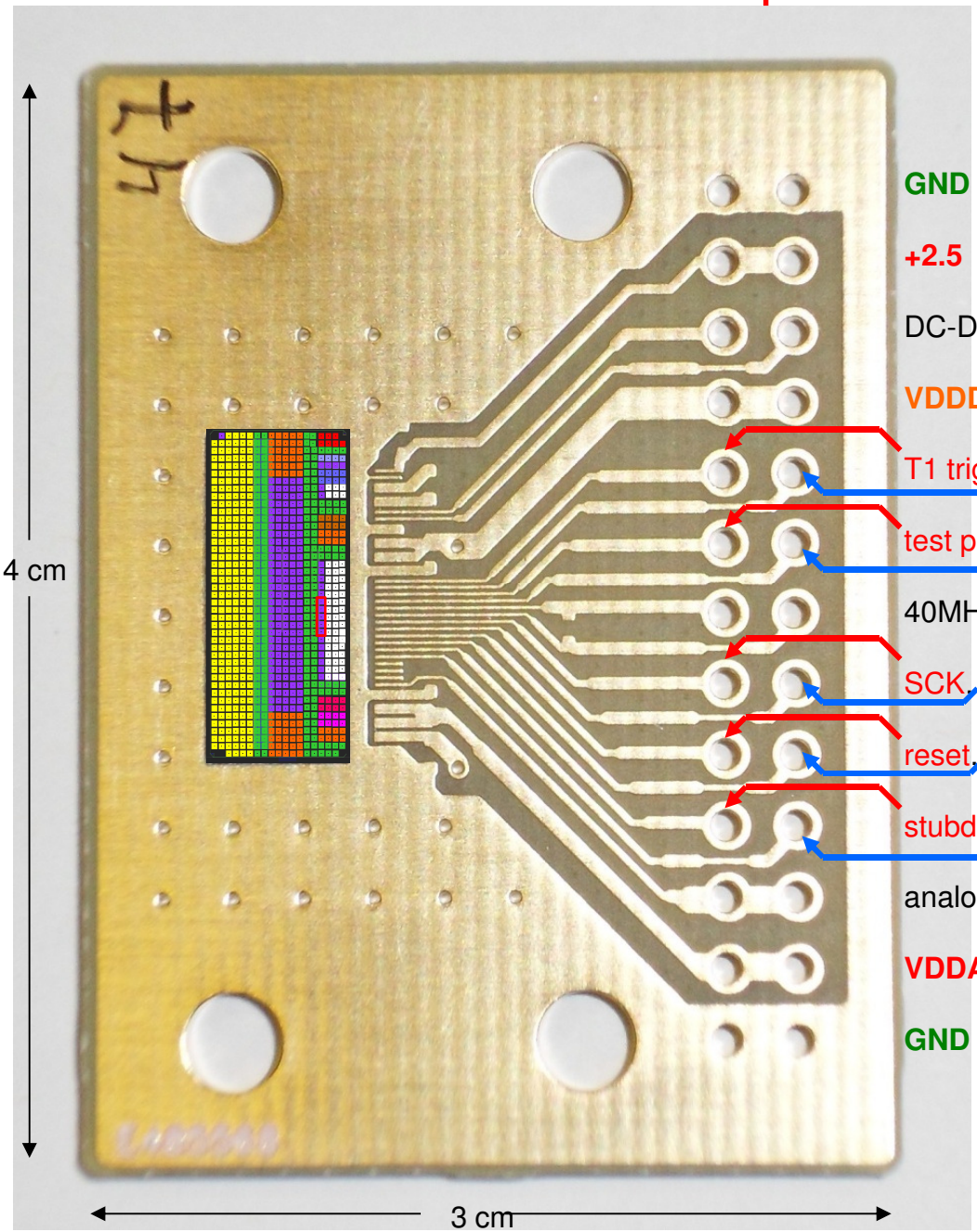


use wafer probe pads to wirebond single CBC2 die to carrier
(CBC2 chips from diced wire-bond (XFEL) wafer)

allows to verify CBC2 functionality before committing to bump-bond

can also use to develop wafer probe procedures

CBC2 wirebond carrier PCB produced



double-sided PCB (other side ground)

GND

+2.5

DC-DC ck (1M diff)

VDDD

T1 trigger, fast reset

test pulse, I2C refresh

40MHz diff

SCK, SDA

reset, trigdata

stubdata, trigger

analog

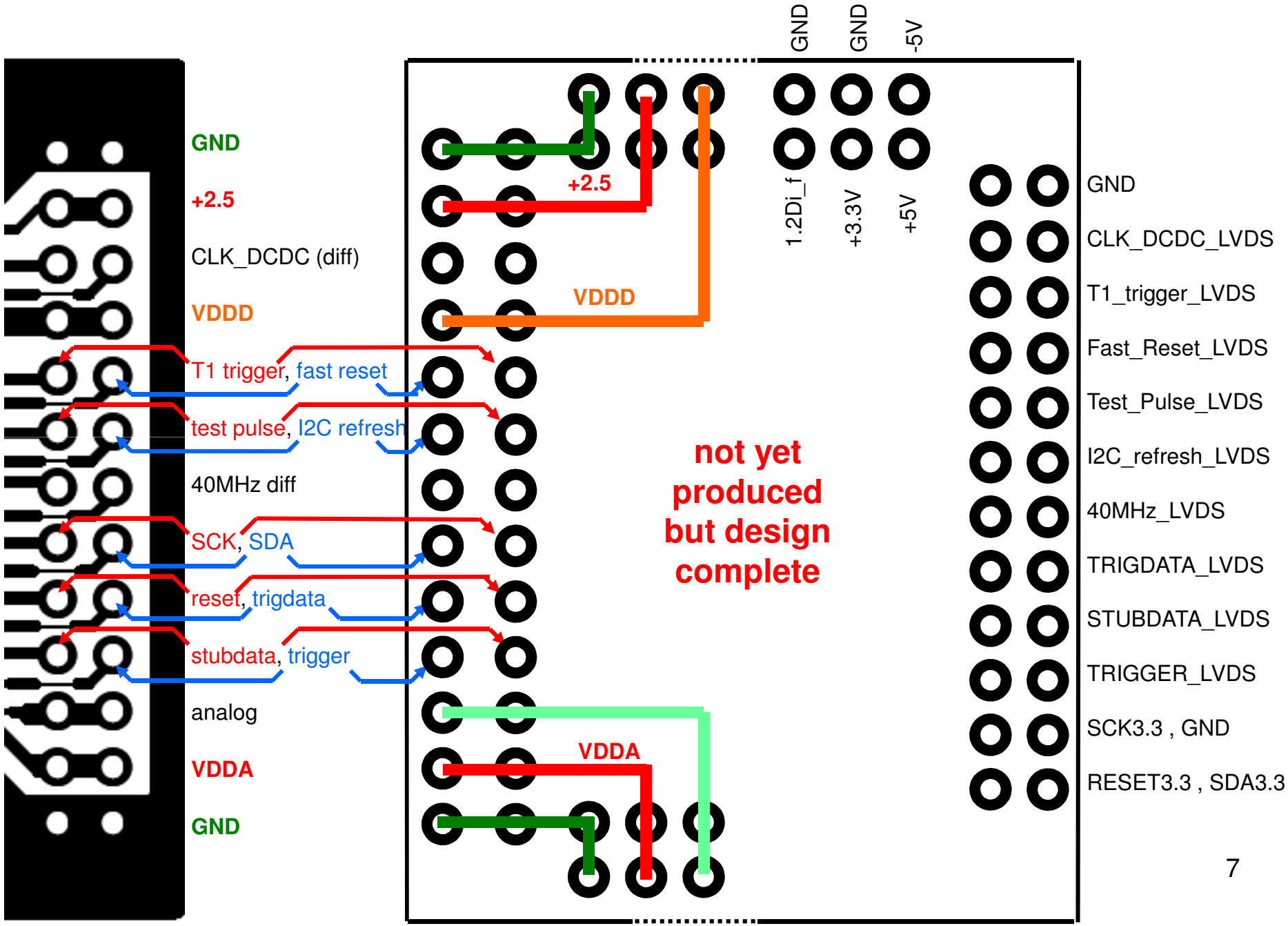
VDDA

GND

pads on chip

GND
+2.5
GND
1M diff
1M diff
GND
VDDD
GND
T1 trigger
fast reset
test pulse
I2C refresh
40M diff
SCK
SDA
reset
trigdata
stubdata
trigger
analog
GND
VDDA
VLDOO
GND

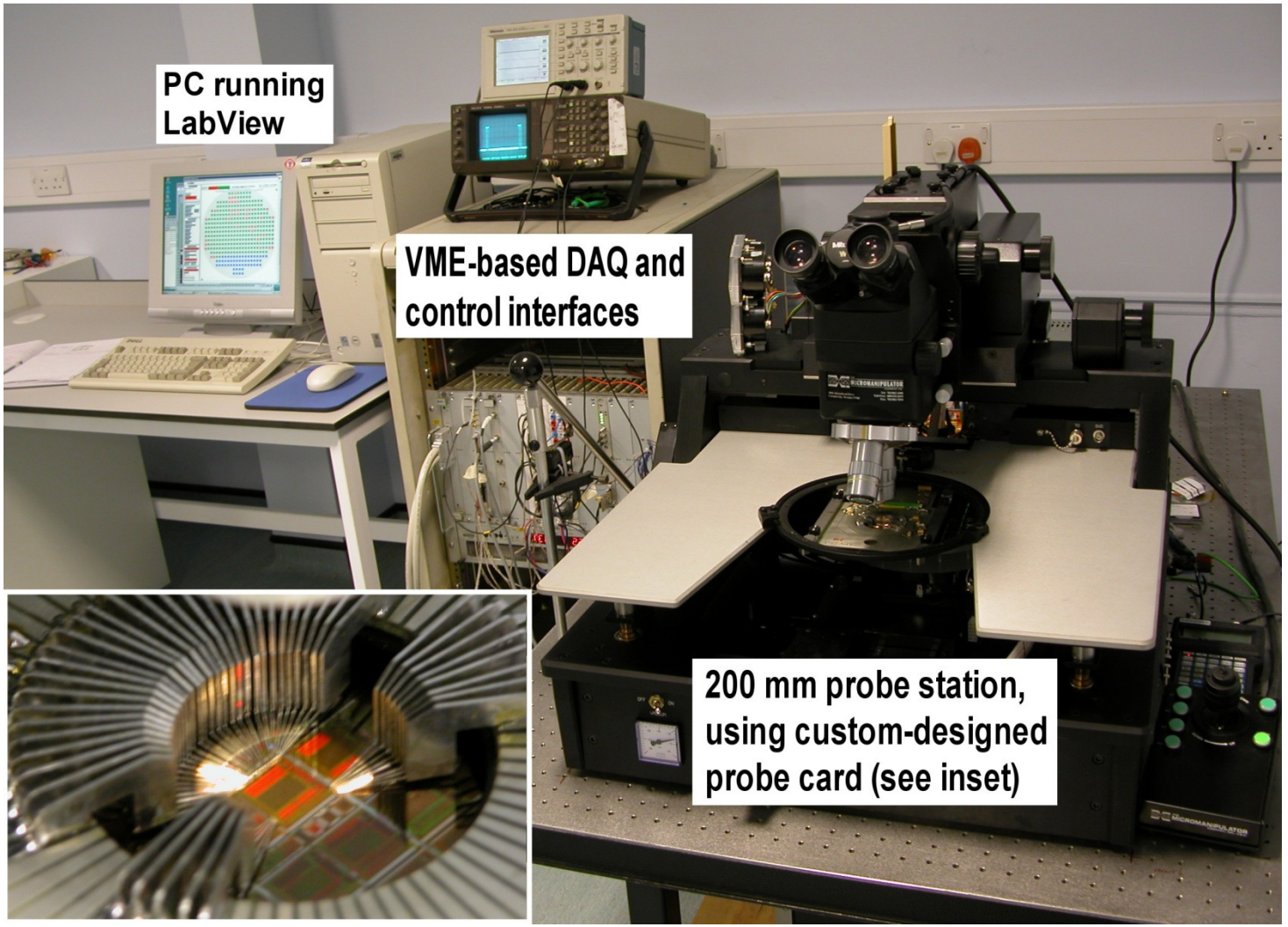
CBC2 wirebond carrier interface PCB



Wafer Test Hardware

re-use APV screening system (would like to update but time is short) ← **should now be able to find time**

need to get probe card manufactured (re-establish links with manufacturers) ← **no progress here yet**



Micromanipulator
8 inch semi–automatic
probe station

VME based
- ADC (8 bits)
- RAL SeqSi
  - 40 MHz CK/T1
- CERN VI2C I/F

PC controls both
DAQ (VME)
& probe-station (RS232)

2xCBC2 substrate test setup

(following two slides repeated from last time)

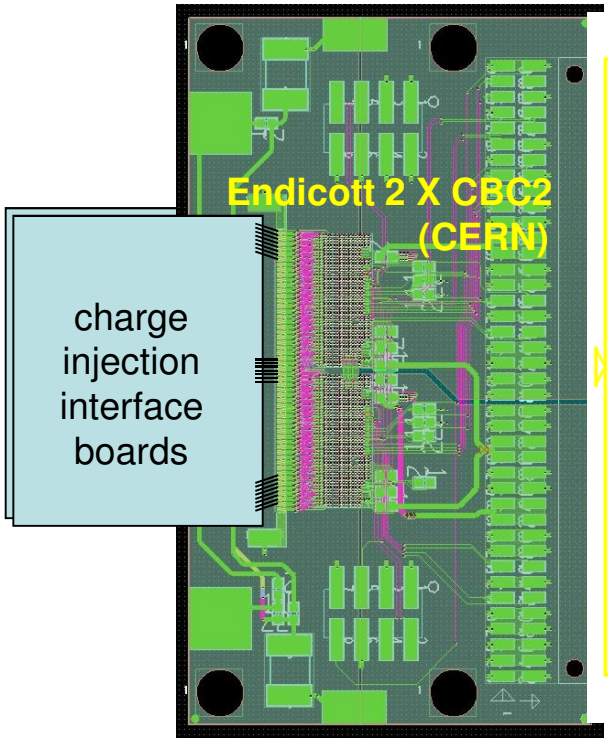
2xCBC2 substrate test setup

this will be the platform for detailed performance measurements

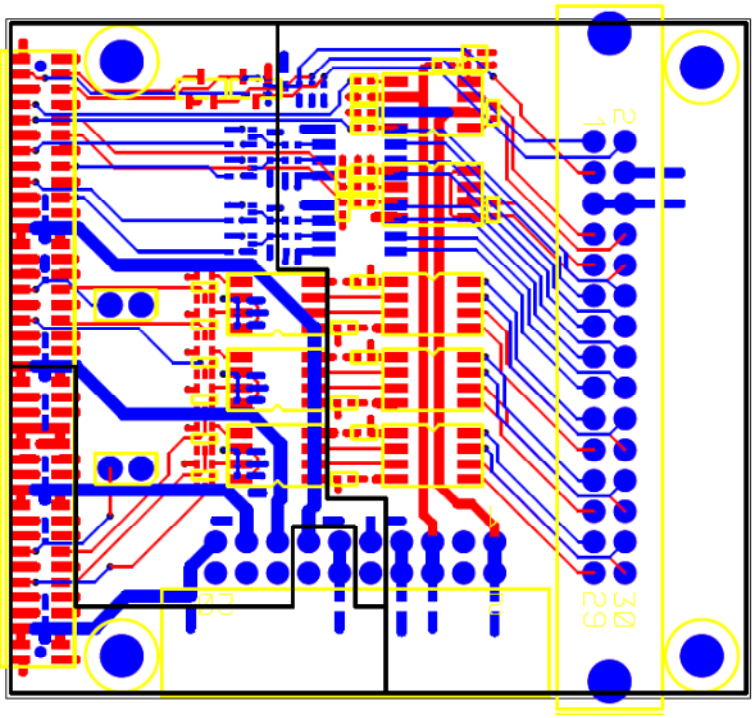
4 layer interface PCB

Imperial will produce charge injection and interface

Bristol (D.Cussans) will produce FMC



charge injection interface boards



LVDS signals
3.3V I2C

custom test setup

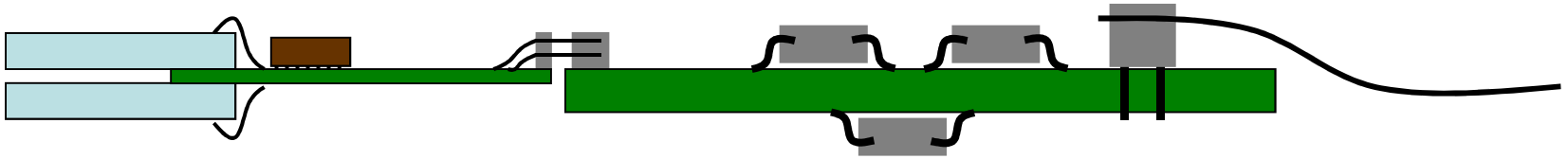
or

FMC

power
+/- 5, +3.3, +2.5, +1.2

these boards needed by ~ end of year

Infineon sensors can be used to produce mini 2S-Pt module



charge injection

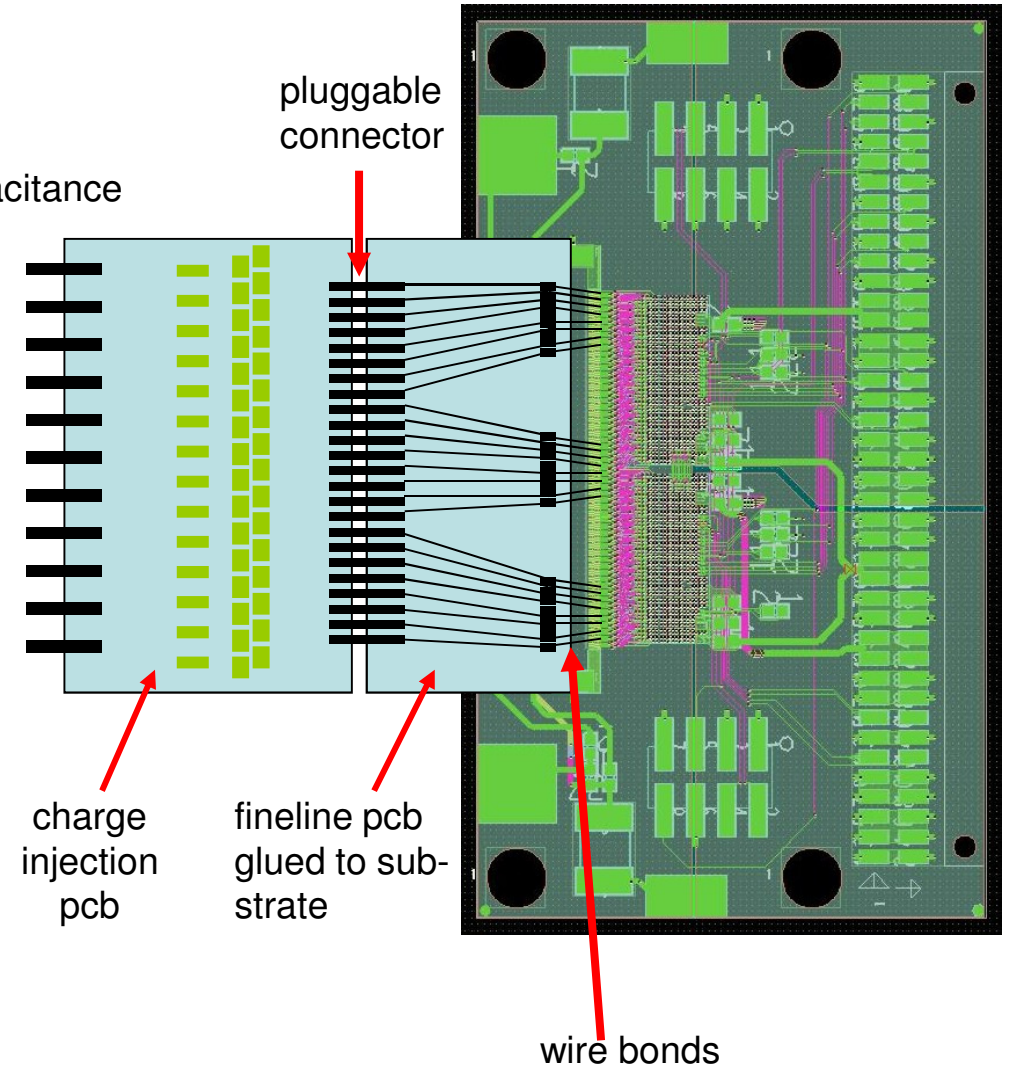
can only wirebond to 2xCBC substrate inputs

will want to study effects of varying external capacitance

don't want to waste substrates so propose a 2 stage approach

1) glue fineline pcb to substrate and wire-bond to CBC2 inputs. fineline pcb adapts to pluggable connector

2) can then have different variants of charge injection board that plug onto this to provide electrical interface



summary – up to here

CBC2 wafers arriving later than previously expected – late Dec

probably not in our hands till new year

expect wire-bond wafers first, C4 following few weeks later

first draft of CBC2 user manual ready (Davide)

test plans

wire-bond substrate ready, level shift interface PCB soon

Endicott require diced C4 chips for 2xCBC2 substrate manufacture
$\Rightarrow$ dice one C4 wafer as soon as possible

2xCBC2 substrate interface PCB designed, will be produced soon

FMC for DAQ interface in preparation (David Cussans, Bristol)

populated 2xCBC2 substrates unlikely to be available before April 2013

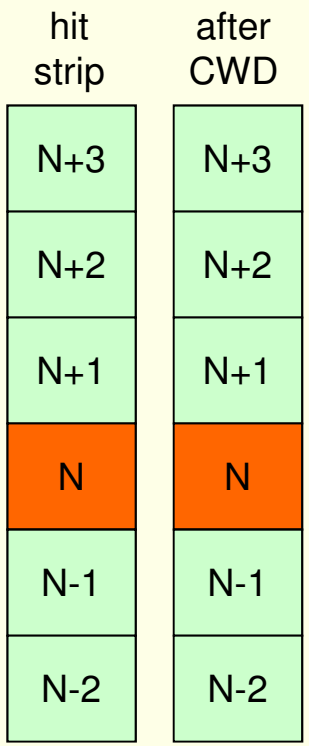
CBC3 architecture definition progress

will summarise understanding of requirements for:

Cluster Width Discrimination resolution
Correlation Window width and offset definition
Bend information requirements

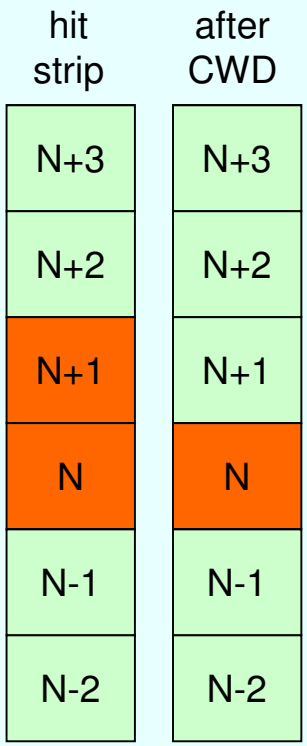
as discussed in August meeting and other discussions since

cluster finding - how it works on CBC2



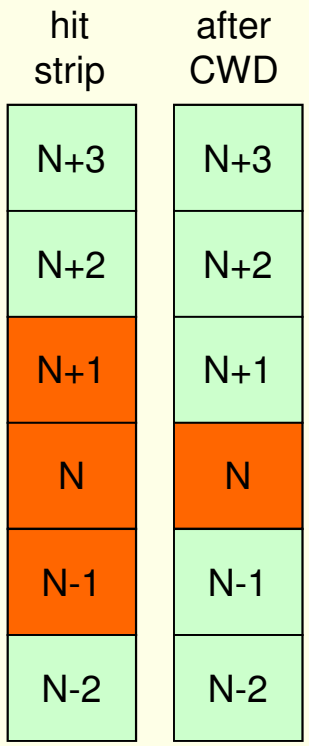
can choose to accept only 1 strip clusters

hit on strip N
=> cluster on strip N



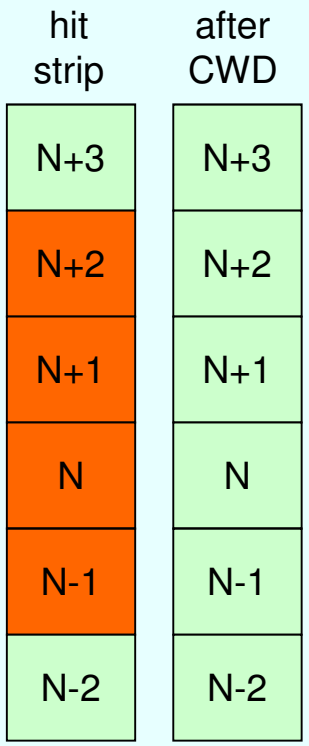
or 1 and 2 strip clusters

hit on strip N and N+1
=> cluster on strip N



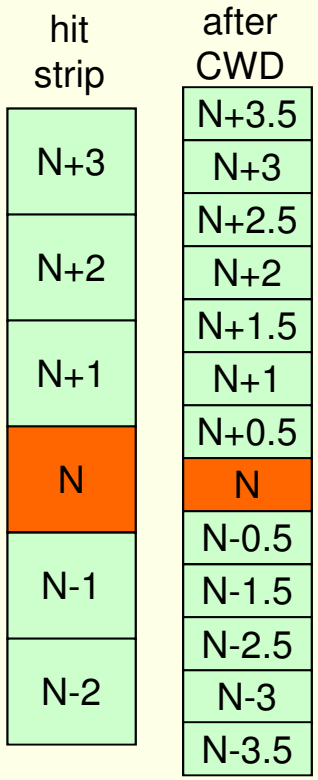
or 1, 2 and 3 strip clusters

hit on strip N-1, N and N+1
=> cluster on strip N



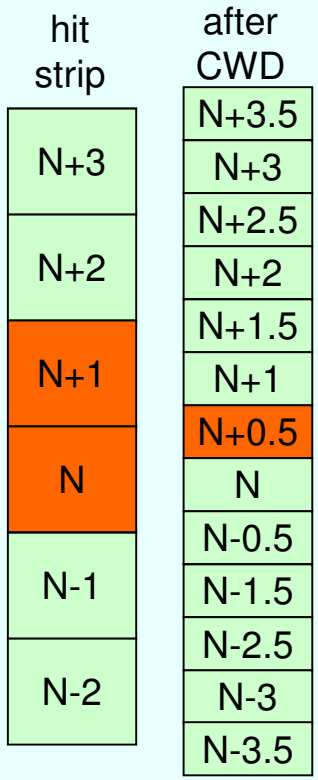
> 3 strip clusters rejected

cluster finding - proposed for **CBC3**



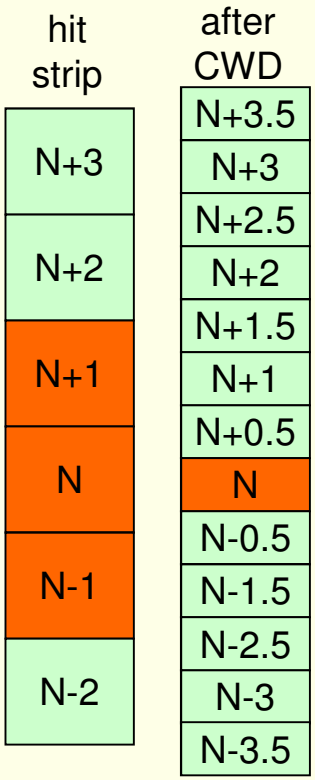
can choose to accept only 1 strip clusters

hit on strip N
=> cluster on strip N



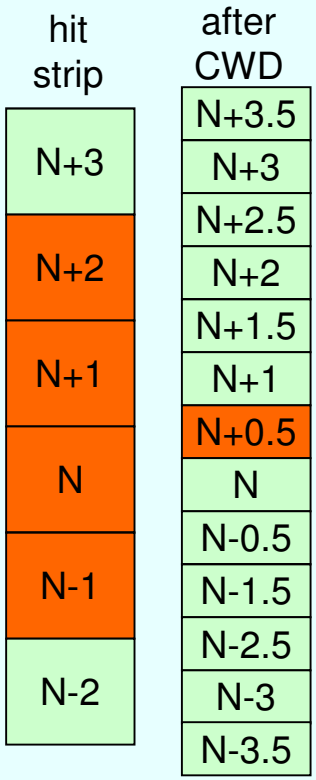
or 1 and 2 strip clusters

hit on strip N and N+1
=> cluster on strip N+0.5



or 1, 2 and 3 strip clusters

hit on strip N-1, N and N+1
=> cluster on strip N



or 1,2,3 and 4 strip clusters

hit on strip N-1, N, N+1 and N+2
=> cluster on strip N+0.5

for 127 strips (7 bits) - half strip resolution requires extra bit
=> 8 bit address required for cluster position

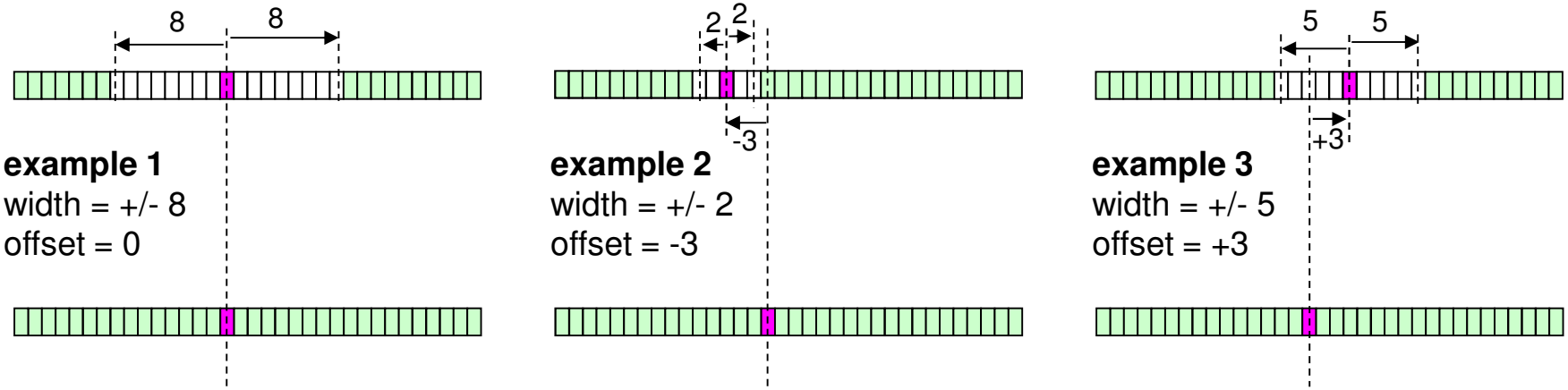
> 4 strip clusters rejected

window width and offset - CBC2

correlate cluster in inner layer with cluster occurring within window in upper layer

window width defines Pt cut
width programmable up to **+/- 8** strips

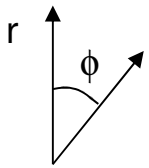
offset defines lateral displacement of window across chip
programmable up to **+/- 3** strips
can choose 2 different values in 2 halves of chip (=> 16 offset regions across SS-Pt module)



example 1
width = +/- 8
offset = 0

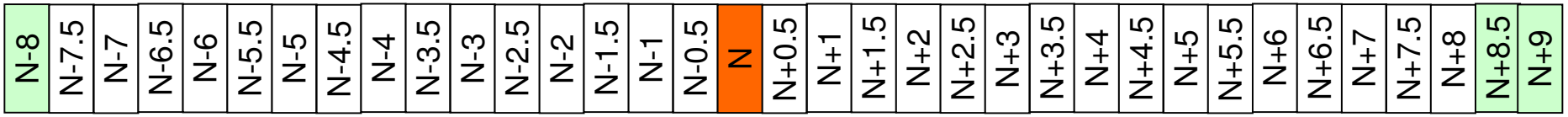
example 2
width = +/- 2
offset = -3

example 3
width = +/- 5
offset = +3

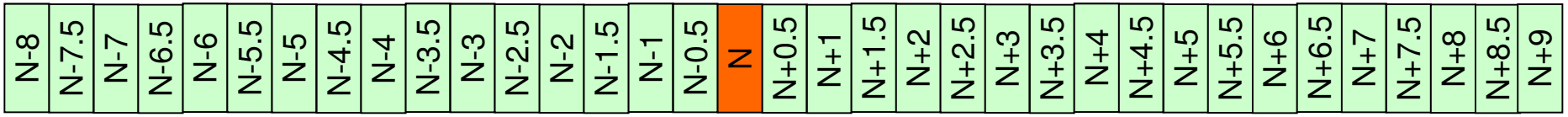


window width - CBC3

half strip cluster resolution in upper layer



half strip cluster resolution in lower layer



for each cluster in lower layer, want address of correlating cluster in upper layer window => bend info

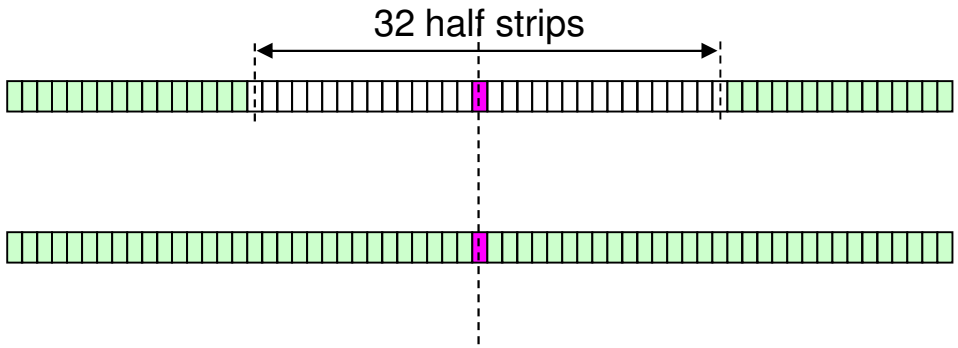
for 5 bits bend info => maximum 32 cluster locations in upper layer

=> -7.5 / +8 strips around central strip

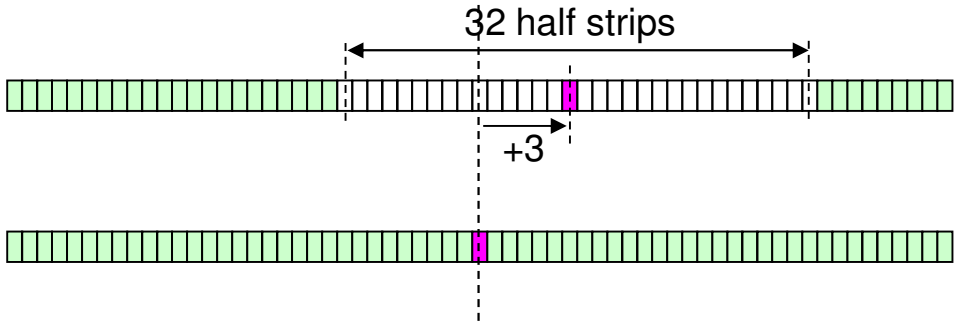
stub described by **8-bit** cluster position in lower layer + **5 bit** bend info = **13 bits**

window offset - CBC3

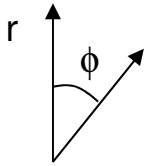
retain programmability of correlation window width and offset - but with ½ strip resolution
(window and offset?)

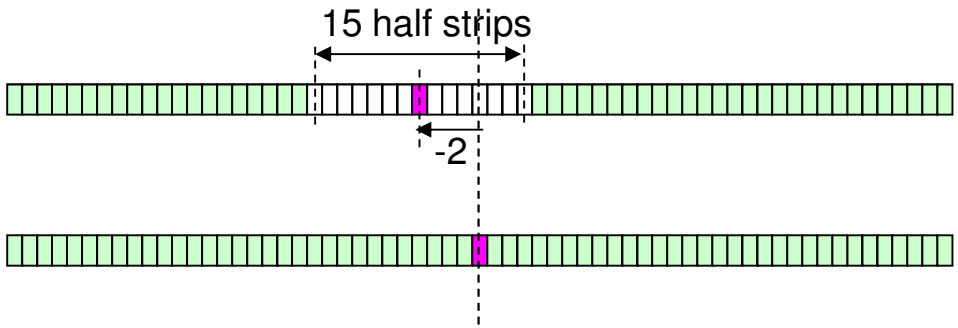


example 1
width = 32 half strips (+8 / -7.5 strips)
offset = 0



example 2
width = 32 half strips (+8 / -7.5 strips)
offset = +3 (strips)





example 3
width = 15 half strips (+3.5 / -3.5 strips)
offset = -2 (strips)

summary

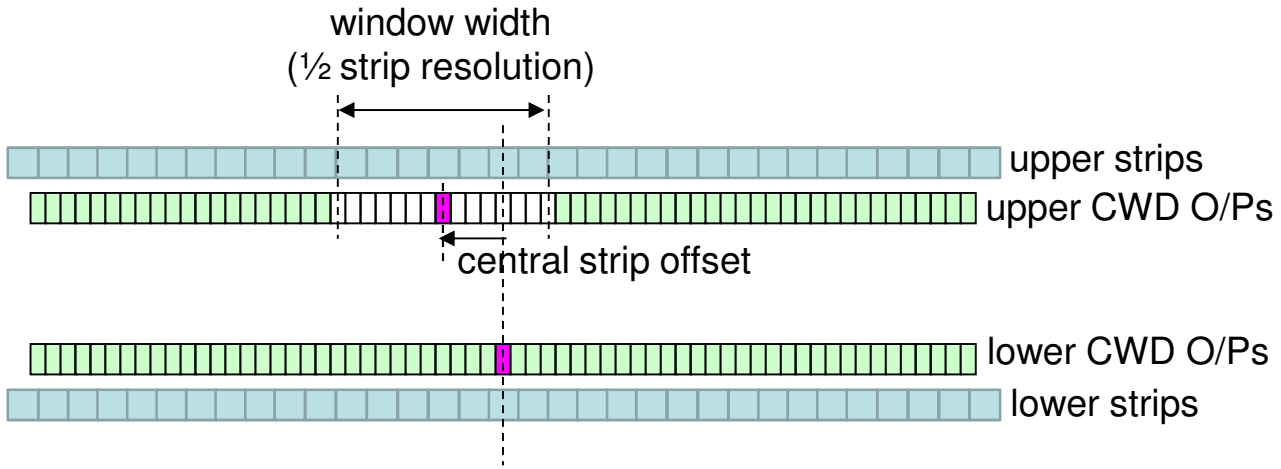
CBC2

up to **3** strip cluster width discrimination
single strip resolution at output of CWD block
correlation window width programmable up to **+/- 8 strips** around central strip
central strip offset programmable up to **+/- 3 strips** (2 values: one for each chip half)

proposed for CBC3

up to **4** strip cluster width discrimination
half strip resolution at output of CWD block
correlation window width programmable up to **+8 /- 7.5 half strips** around central strip
central strip offset programmable up to **+/- 3 strips** (2 values: one for each chip half)
(is ½ strip resolution of central strip offset position necessary??)

a stub will be defined by 13 bits (8 address, 5 bend)



extra

bend table

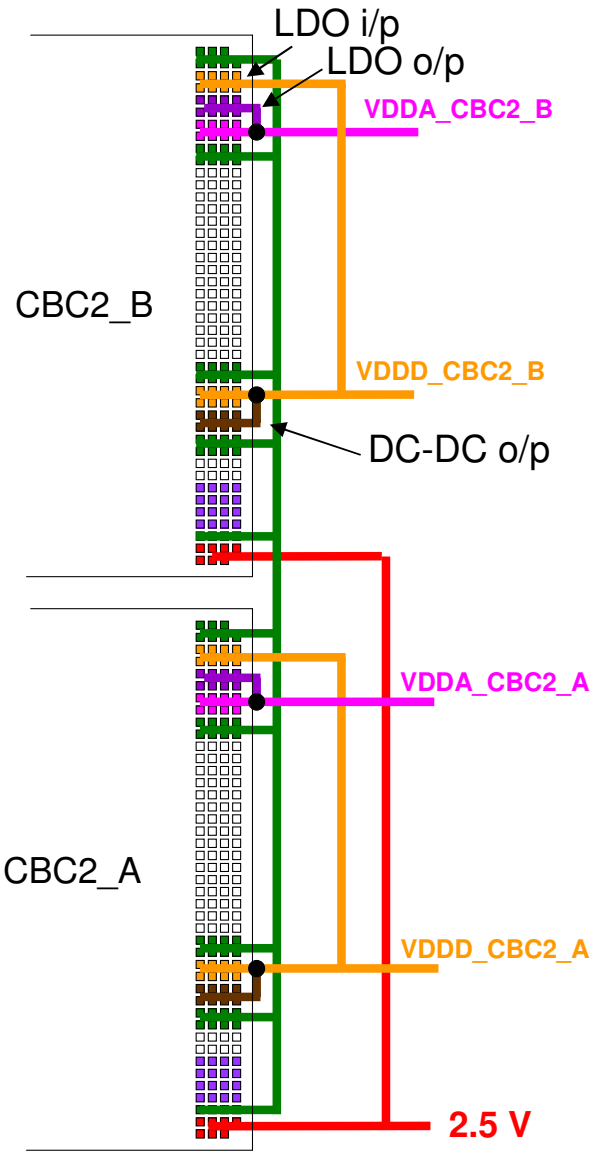
suggest use same code for central strip in window

(even if window is offset)

e.g. b10000 in this example

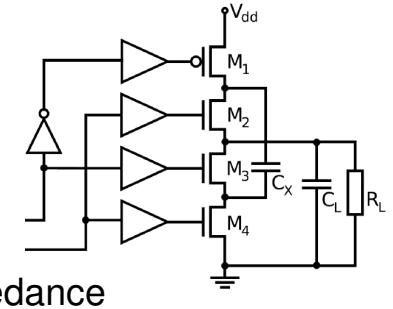
half strip cluster pos'n	binary code
N+8	01111
N+7.5	01110
N+7	01101
N+6.5	01100
N+6	01011
N+5.5	01010
N+5	01001
N+4.5	01000
N+4	00111
N+3.5	00110
N+3	00101
N+2.5	00100
N+2	00011
N+1.5	00010
N+1	00001
N+0.5	00000
N	10000
N-0.5	10001
N-1	10010
N-1.5	10011
N-2	10100
N-2.5	10101
N-3	10110
N-3.5	10111
N-4	11000
N-4.5	11001
N-5	11010
N-5.5	11011
N-6	11100
N-6.5	11101
N-7	11110
N-7.5	11111

CBC2 powering scheme on 2-chip substrate



backend pads as viewed through CBC2 substrate

after some thinking and discussion with Georges we have arrived at this scheme



2.5 V common to both chips

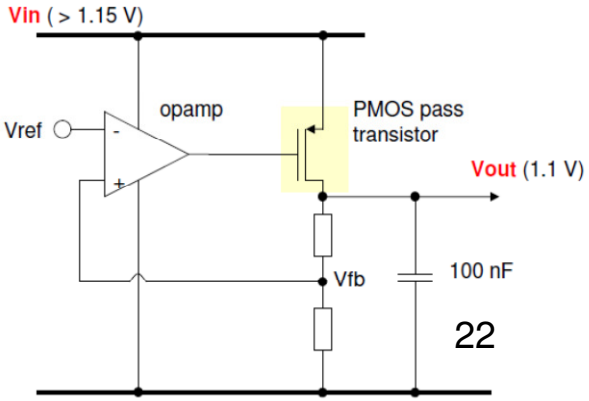
if DC-DC not clocked then output -> high impedance
=> DC-DC o/p can be shorted to VDDD
VDDD can be provided externally if not using DC-DC

connect VDDD directly to LDO i/p
keeping separate would allow to run VDDD at low voltage
but no significant power advantage to doing this

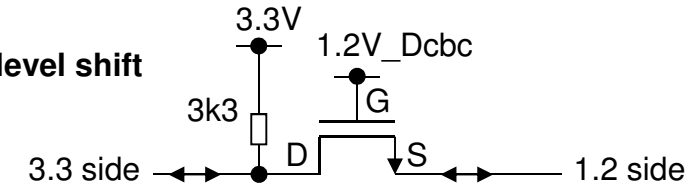
connect LDO o/p directly to VDDA
if want to supply VDDA externally then provide at slightly higher voltage than normal LDO o/p level

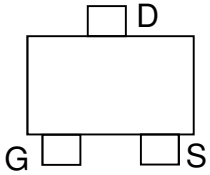
=> LDO shuts down (pass transistor turns off)
verified on CBC prototype

=> no jumpers required at all on substrate



3.3 -> 1.2 level shift

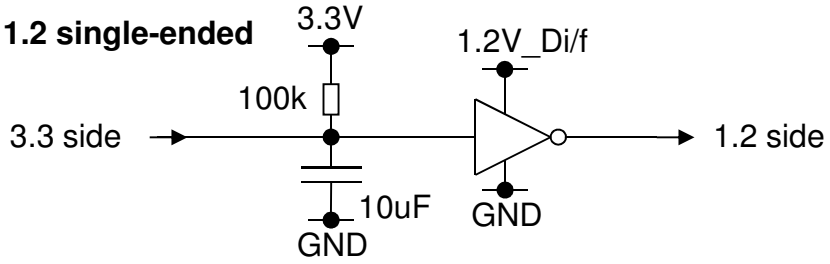


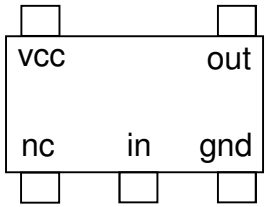


FDV303N
or
BSH103

3.3 -> 1.2 single-ended

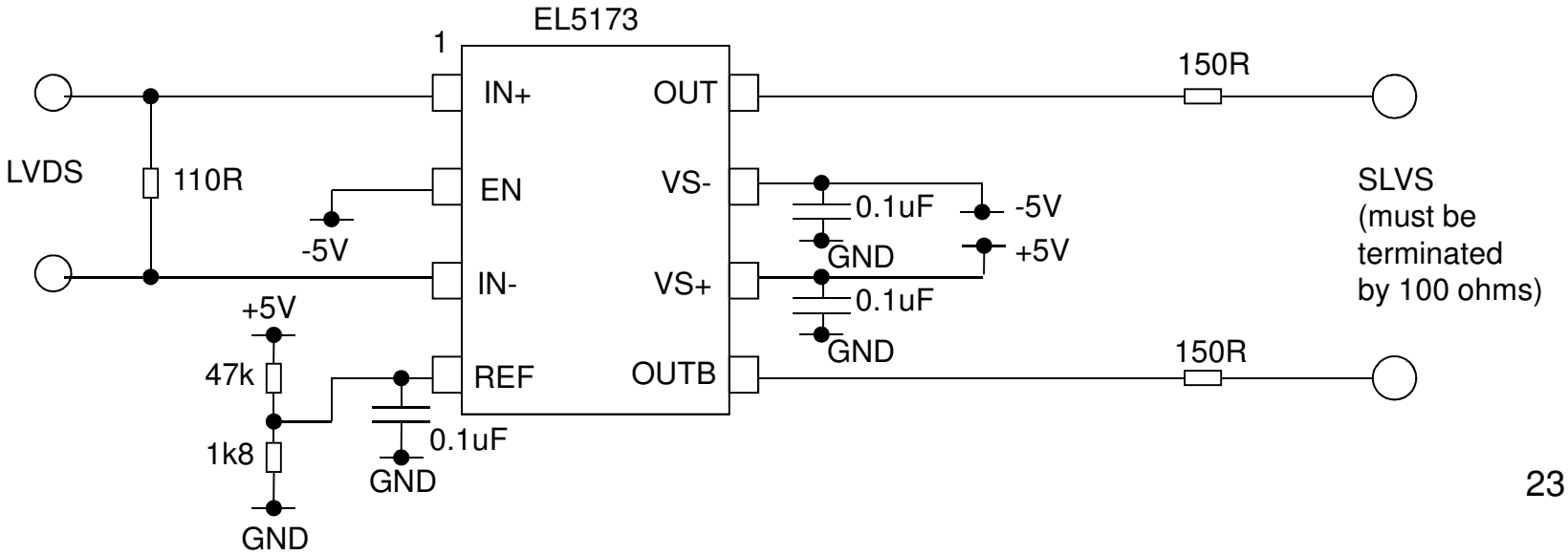
SN74AUC1G04



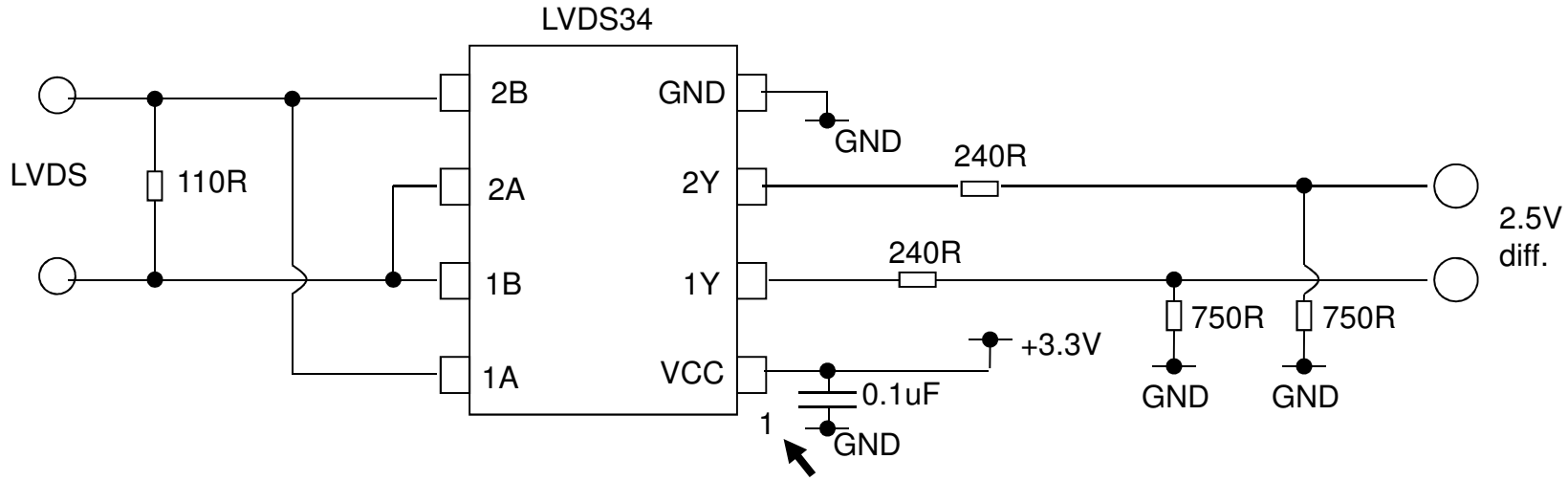


SN74AUC1G04

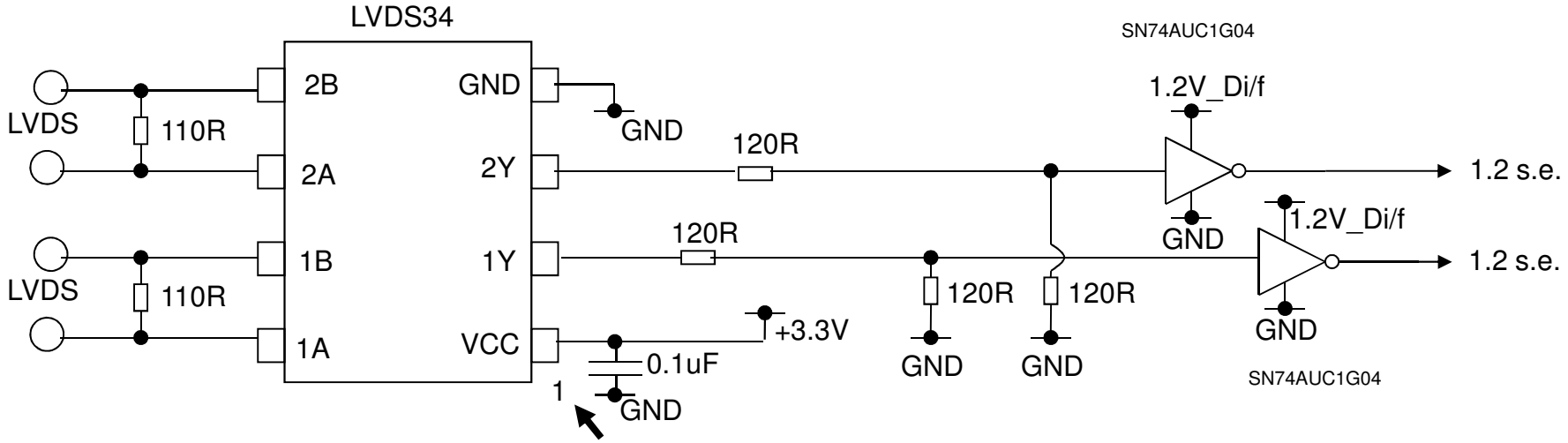
LVDS -> SLVS



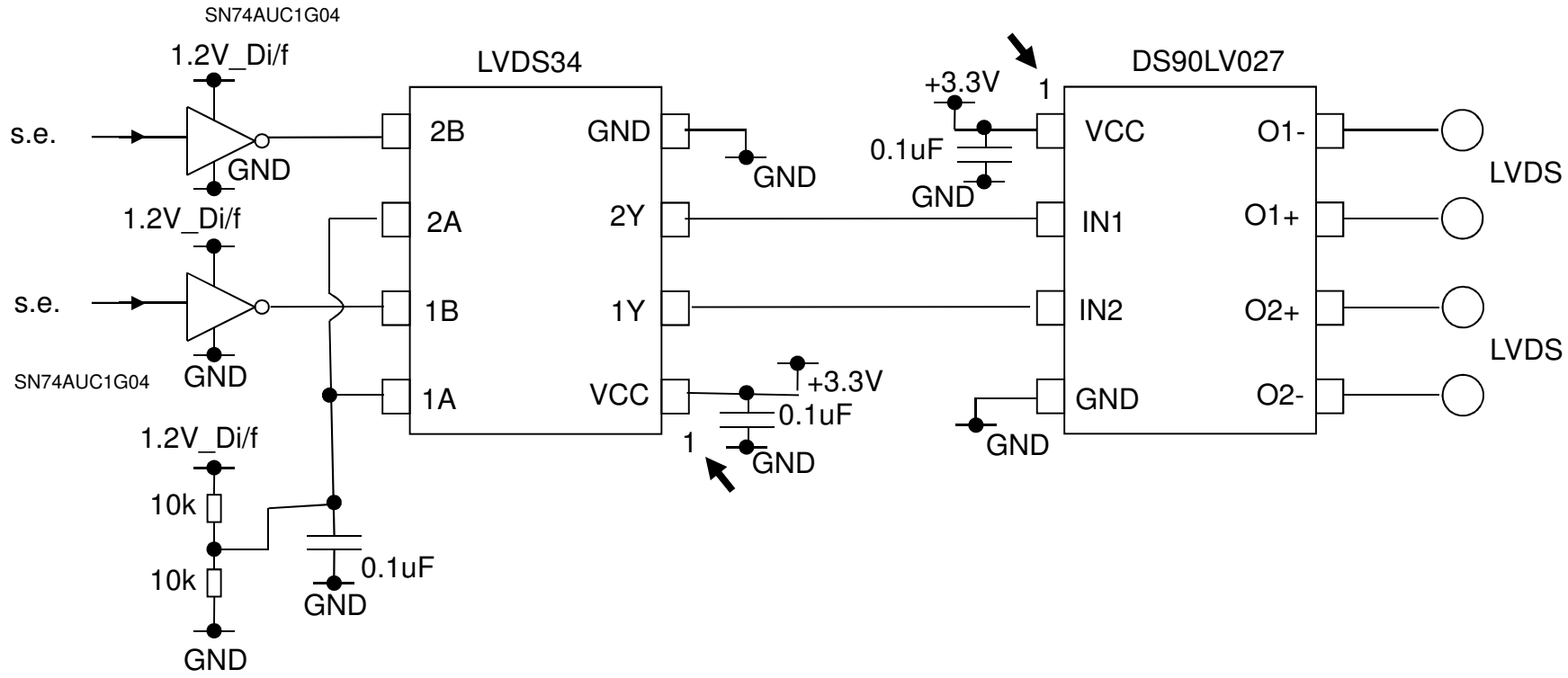
LVDS -> 2.5V diff.



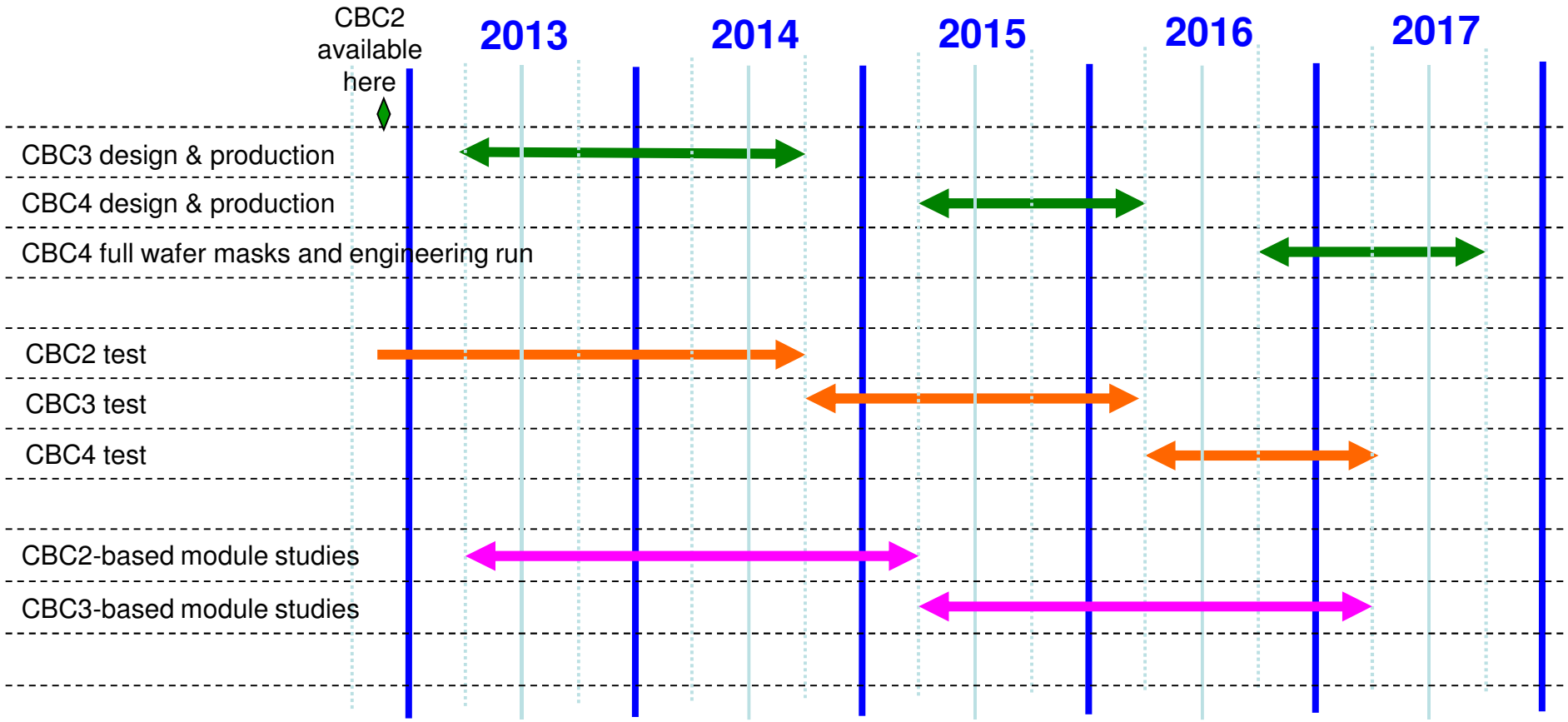
LVDS -> single-ended



single-ended -> LVDS



UK Phase II programme



CBC3 should be very close to final chip – available late 2014
- incorporate architecture to transmit stub addresses
- slow ADC for on-chip monitoring
- …

CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017