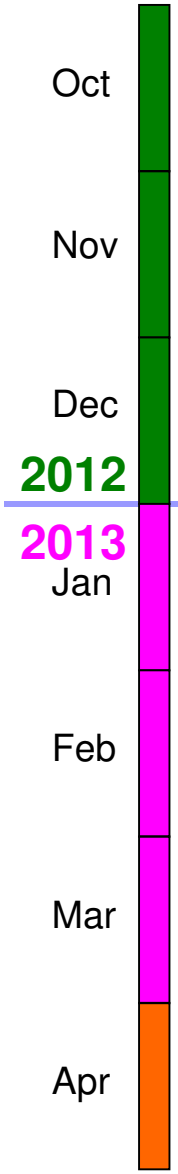
CBC2 update

update on test plans and status of test setups

plans for CBC2 wafers

what to do for future productions

timeline for next ~ 6 months



wirebond wafers will leave foundry Dec. 17th
C4 wafers ~15 days later

some further delay now due to need for re-design of the C4 mask
- not clear to me why
- not yet clear how long

in this ~ 2.5 month period:

produce peripheral boards for 2xCBC2 substrate

make more thorough wafer probe test preparations
- replace old DAQ (PC on order)
- obtain basic probe card (on order)
- prepare basic probe test
  - power consumption, maybe basic functionality

anticipate other test requirements (ionizing, SEU, …)

← today

← wirebond wafers

← C4 ~15 days later

← CBC2 chips from diced wire-bond (XFEL) wafer available for test

← dice C4 wafer CBC2 chips - required for Endicott

can either probe wafers or chips

submit **probed** CBC2 C4 chips + 2xCBC2 substrate for assembly

in this ~ 2 month period:

- wire-bonded CBC2 first tests
- complete wafer probe test preparations and probe remaining wafers

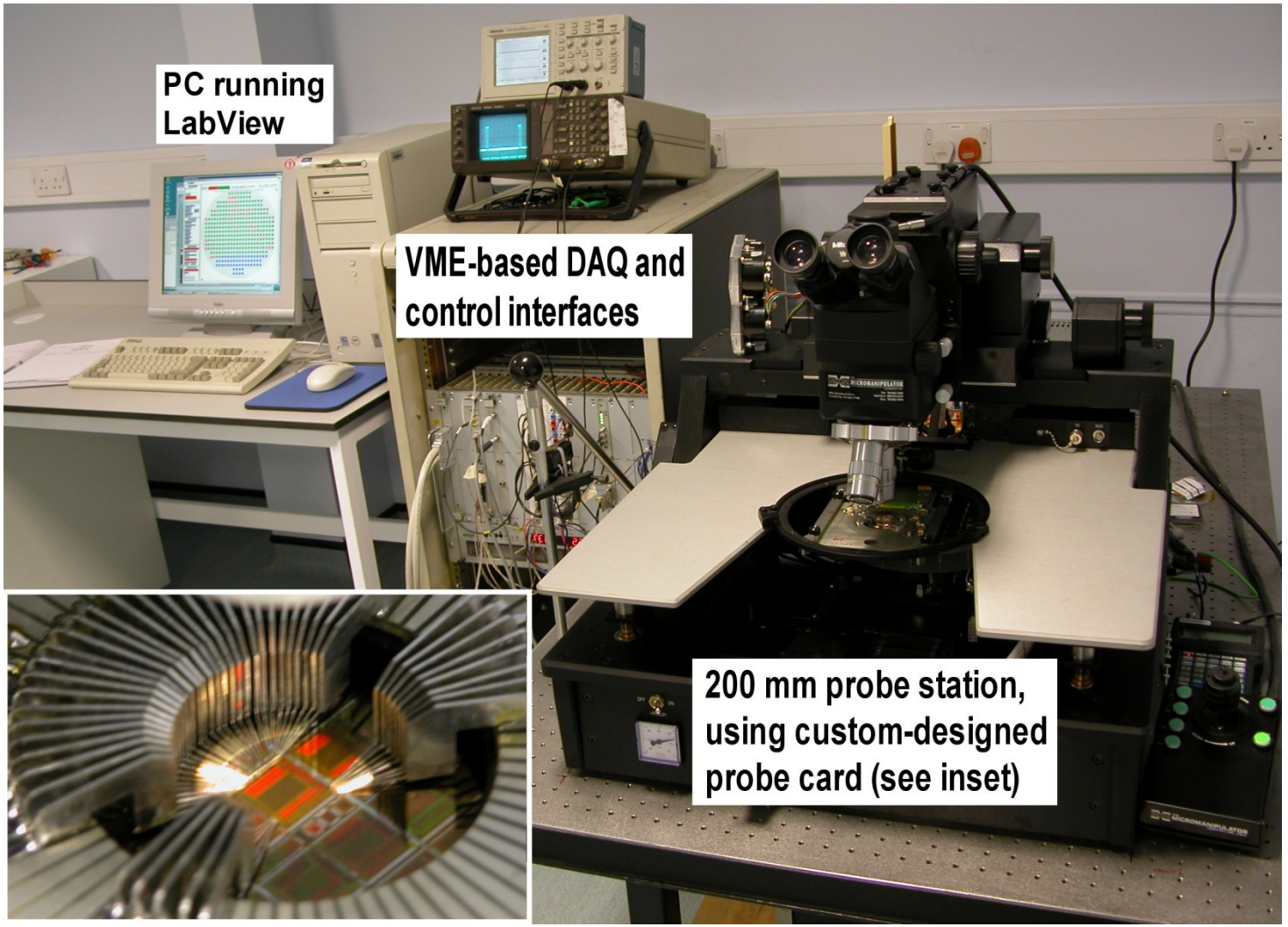
← dual chip CBC2 substrates available for test

... 8 chip substrates and prototype SS-Pt module studies follow on later in 2013

Wafer Test Hardware

re-use APV screening system (would like to update) ← **new PC on order**

need to get probe card manufactured ← **2 basic probe cards on order**

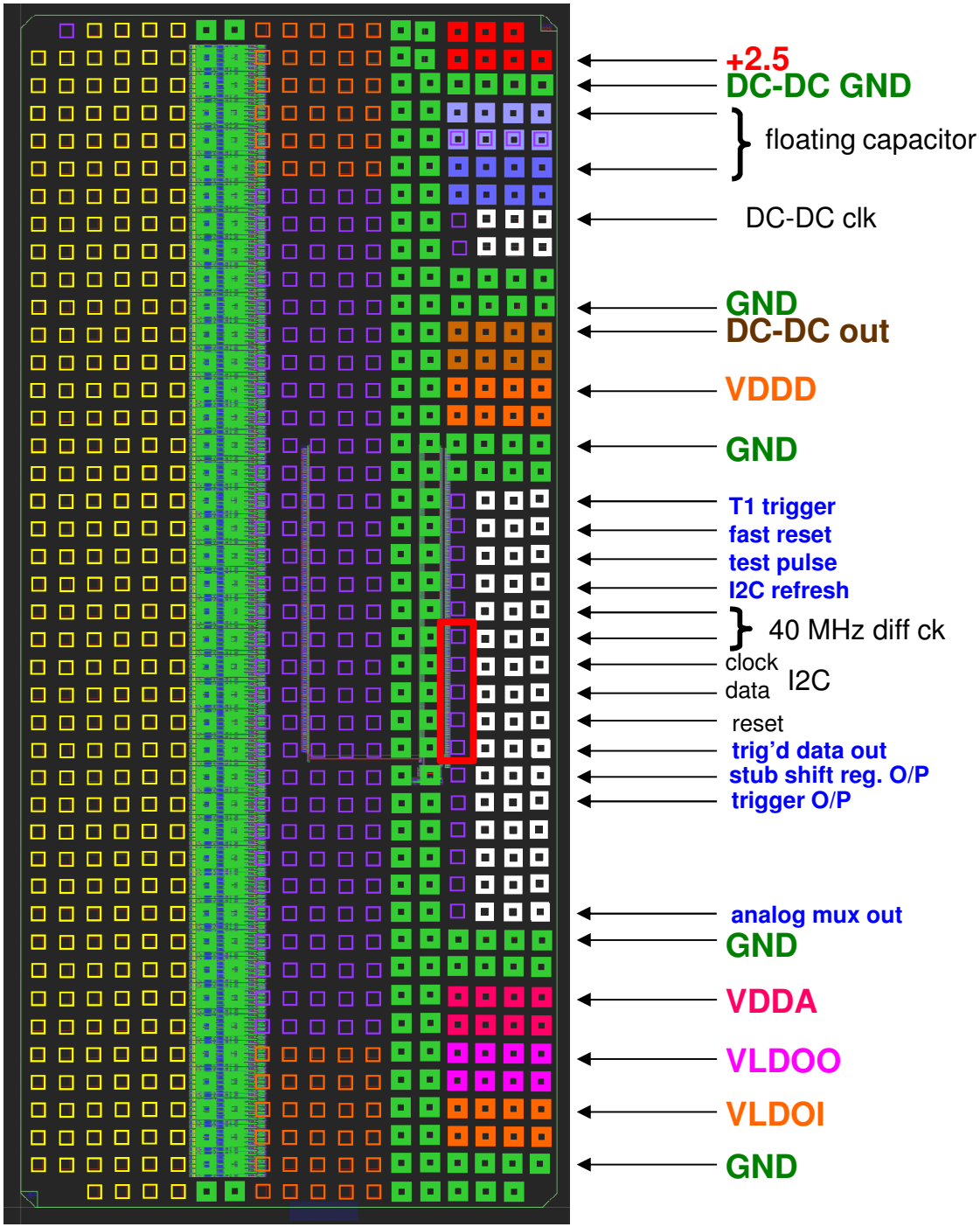


Micromanipulator
8 inch semi–automatic
probe station

VME based
- ADC (8 bits)
- RAL SeqSi
  - 40 MHz CK/T1
- CERN VI2C I/F

PC controls both
DAQ (VME)
& probe-station (RS232)

probe card signals

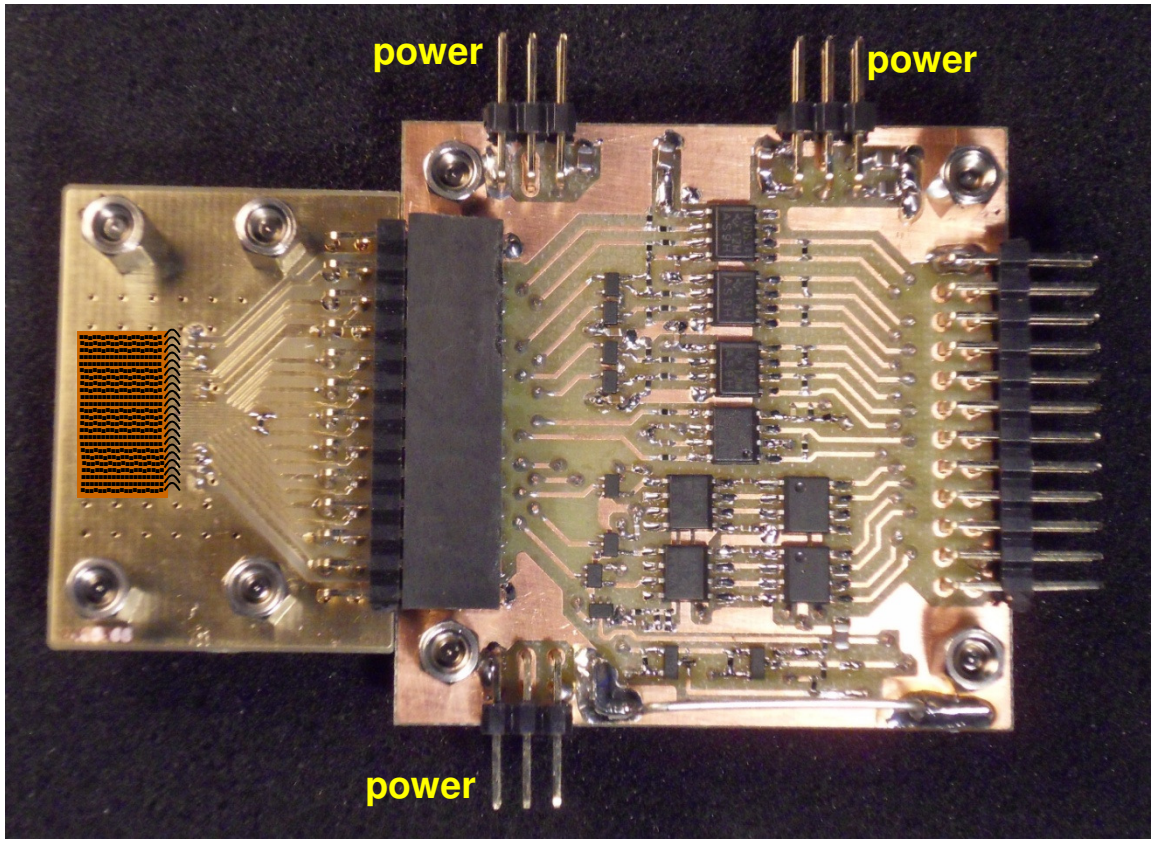


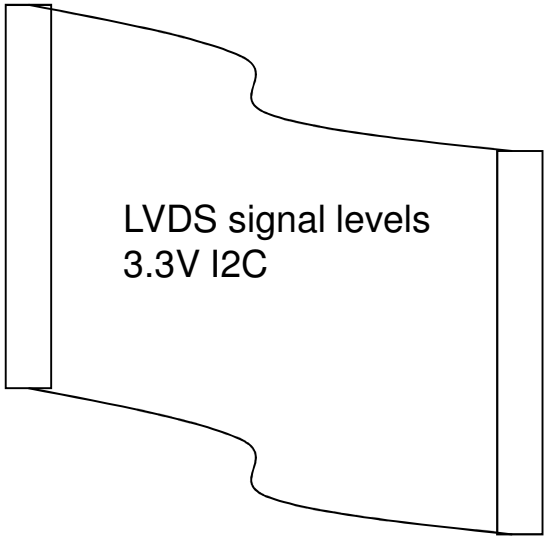
27 altogether

160 MHz signals left out

can try and use DC-DC and LDO
but unlikely to work well
necessary associated capacitors
a long way away from pads

wirebond CBC2 test setup





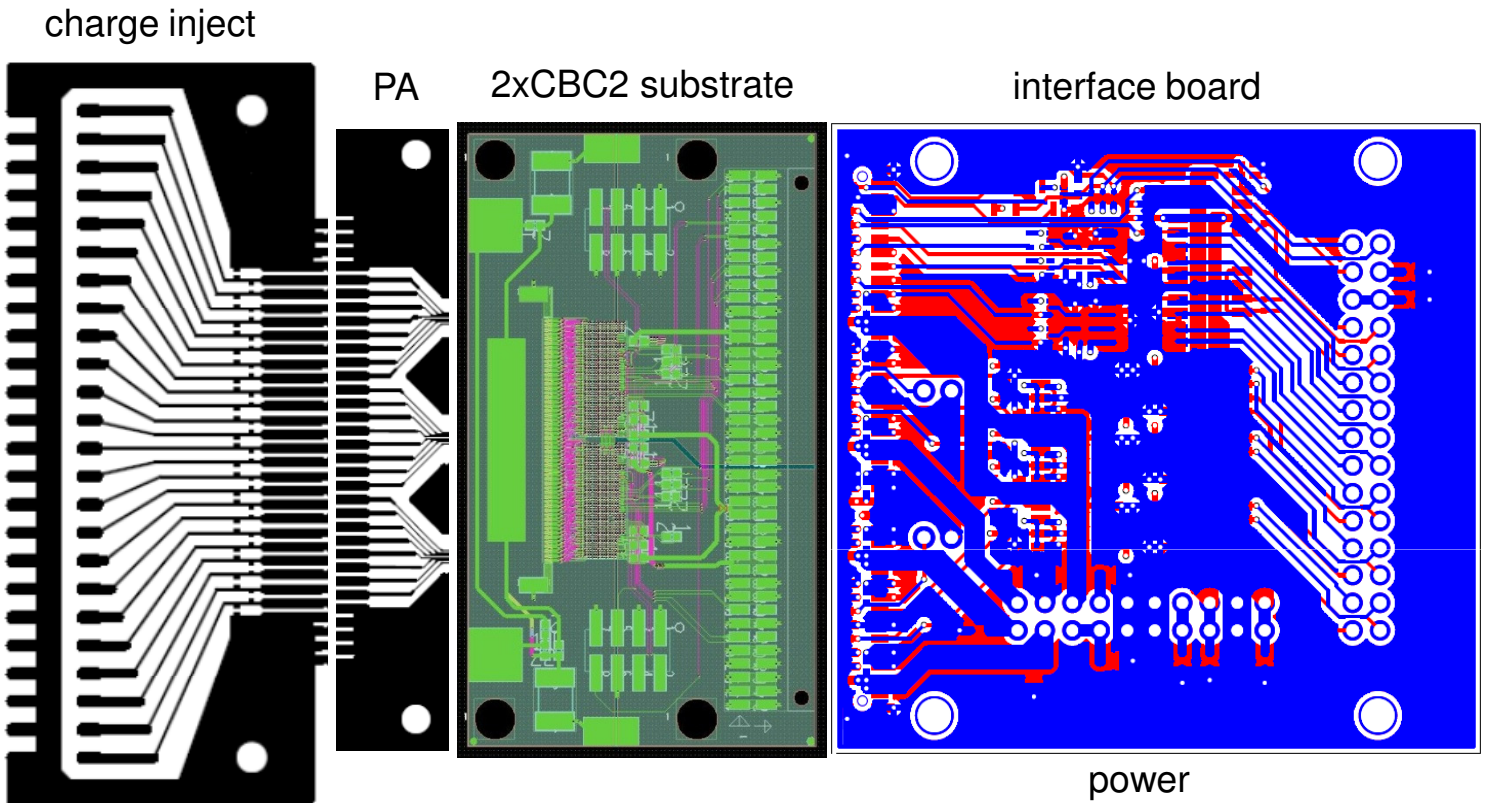
use wafer probe pads to wirebond single CBC2 die to carrier
(CBC2 chips from diced wire-bond (XFEL) wafer)

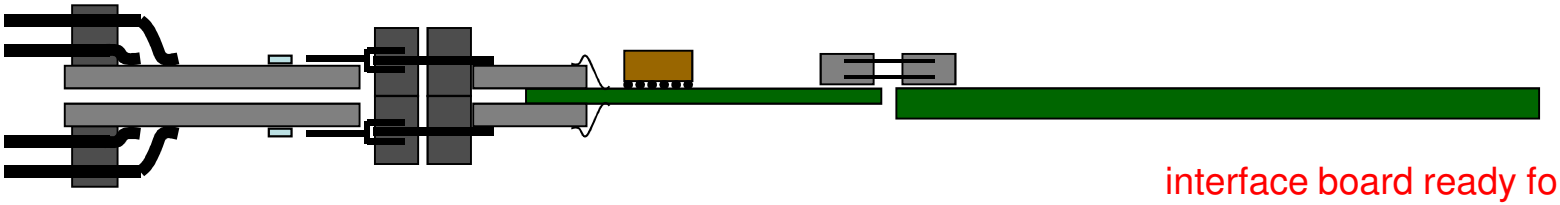
convenient setup for developing detailed wafer probe procedures

can also be used for irradiation studies

interface board tested and working

2xCBC2 substrate test setup





2xCBC substrate + PA (both sides) becomes device under test
pluggable charge inject board allows different external capacitance

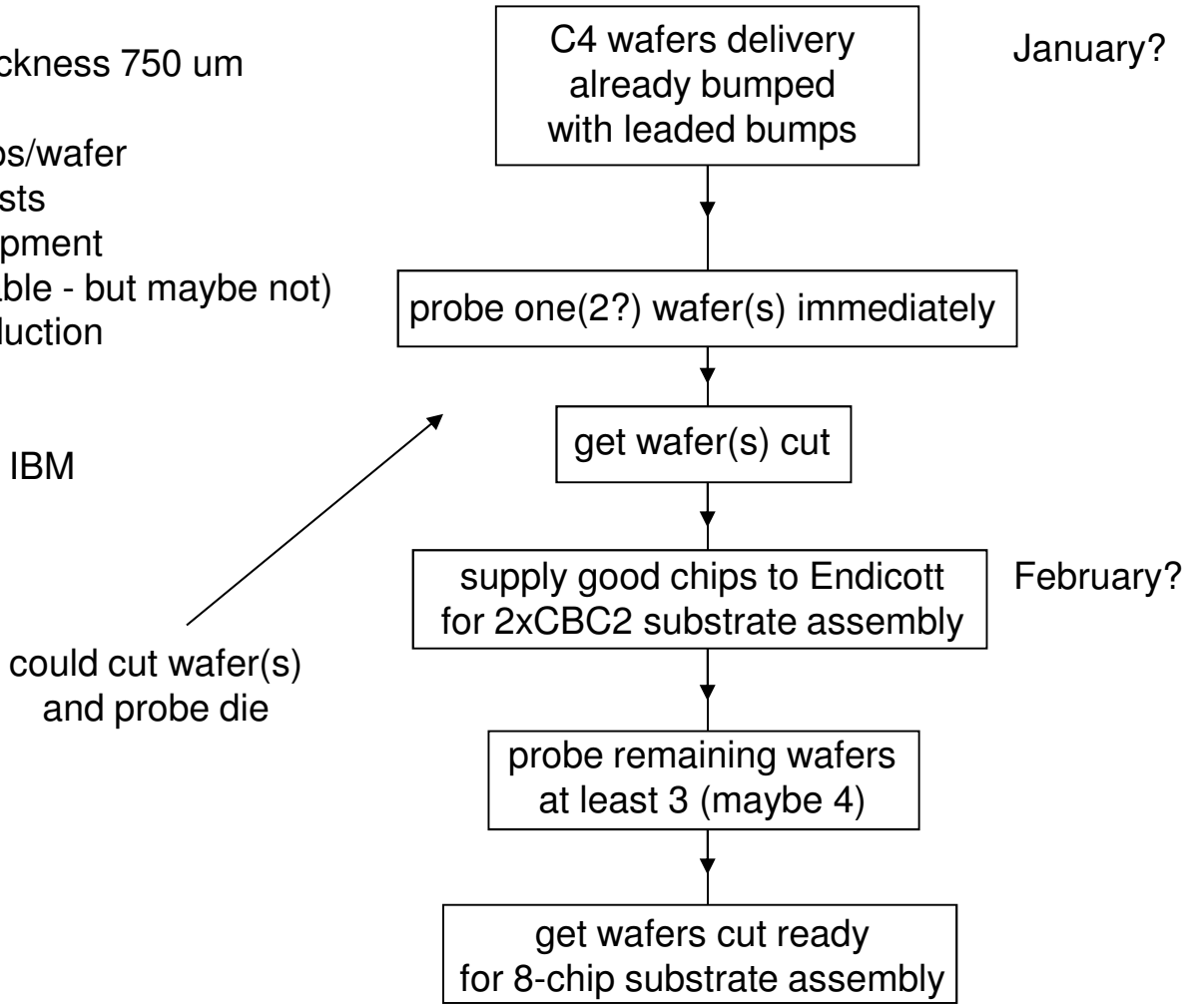
interface board ready for submission
PA and charge inject boards will be made in-house

CBC2 wafer plans summary

CBC2 standard IBM 130 nm wafer thickness 750 um

6 C4 wafers requested, 110 chips/wafer
- 1 for 2xCBC2 substrate tests
- 1 for wafer probing development
  - (may become unusable - but maybe not)
- 3 for 8-chip substrate production
- 1 contingency

CBC2 C4 wafers supplied bumped by IBM
- leaded bumps (97Pb/3Sn)



future productions - some questions

want thinned wafers (how thin? - don't want excessive fragility)

wafers must be thinned before processing to add bumps

where do we go for thinning? (not IBM - I think)

where do we go for subsequent bumping?

- bump metallurgy - move to Pb-free?
  - what are implications of ball composition for us?
  - note: e.g. Endicott don't propose to melt bumps

wafer probing - who will look after?

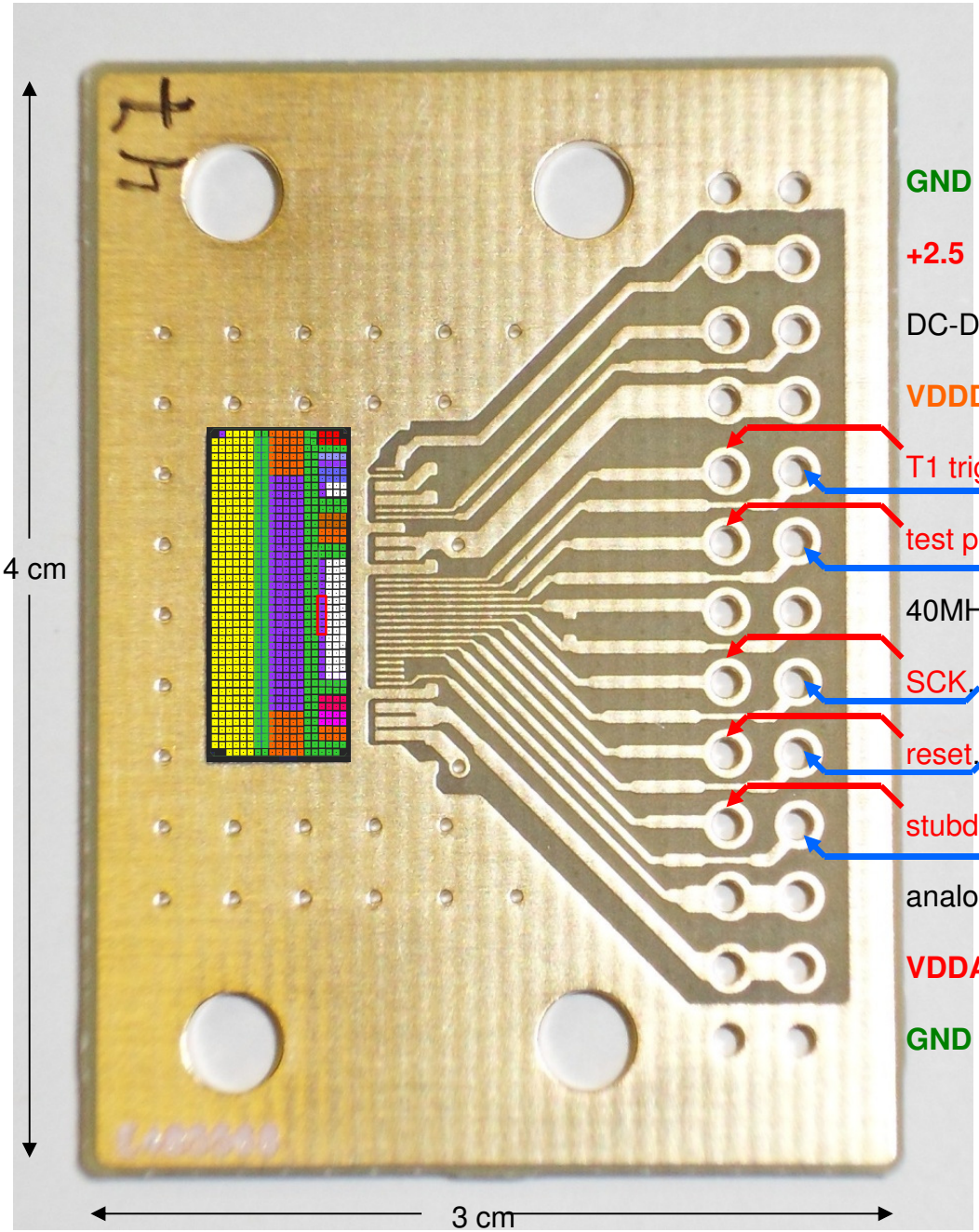
- do we continue to do this in-house? (I don't see why not)

would be preferable to supply assembly company with probed wafers and wafer maps

- they look after cutting,
- pick and place good die
- return backing foils to us (can then very only good die picked)
- (this was the way it worked for the APV production testing and hybrid assembly)

extra

CBC2 wirebond carrier PCB detail



double-sided PCB (other side ground)

GND

+2.5

DC-DC ck (1M diff)

VDDD

T1 trigger, fast reset

test pulse, I2C refresh

40MHz diff

SCK, SDA

reset, trigdata

stubdata, trigger

analog

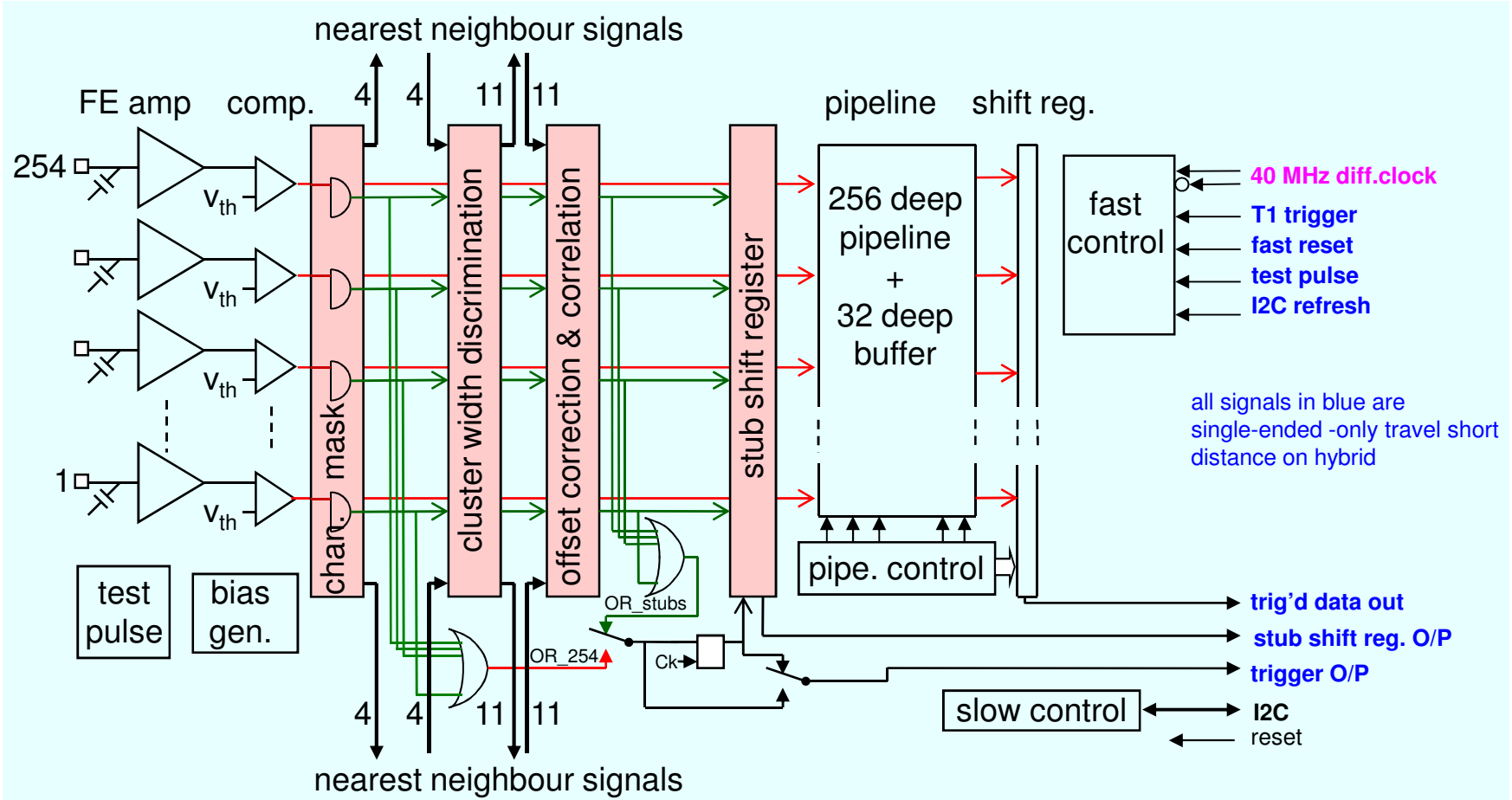
VDDA

GND

pads on chip

- **GND**
- **+2.5**
- **GND**
- 1M diff
- 1M diff
- **GND**
- **VDDD**
- **GND**
- T1 trigger
- fast reset
- test pulse
- I2C refresh
- 40M diff
- SCK
- SDA
- reset
- trigdata
- stubdata
- trigger
- analog
- **GND**
- **VDDA**
- **VLDOO**
- **GND**

CBC2 architecture reminder



blocks associated with Pt stub generation

channel mask: block problem channels (but not from L1 pipeline)

cluster width discrimination: exclude wide clusters > 3

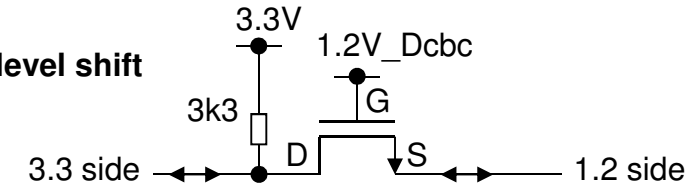
offset correction and correlation: correct for phi offset across module and correlate between layers

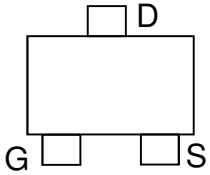
stub shift register: test feature - shift out result of correlation operation at 40 MHz

OR_254 at comp. O/P and OR_stubs at correlation O/P: - can select either to transmit off-chip, latched or un-latched

allows to study signal propagation times

3.3 -> 1.2 level shift

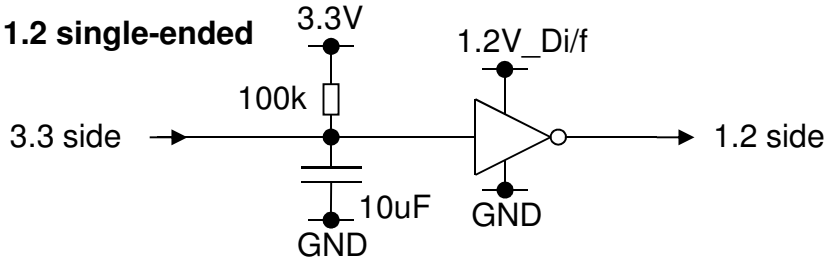


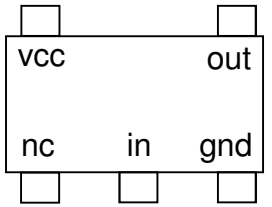


FDV303N
or
BSH103

3.3 -> 1.2 single-ended

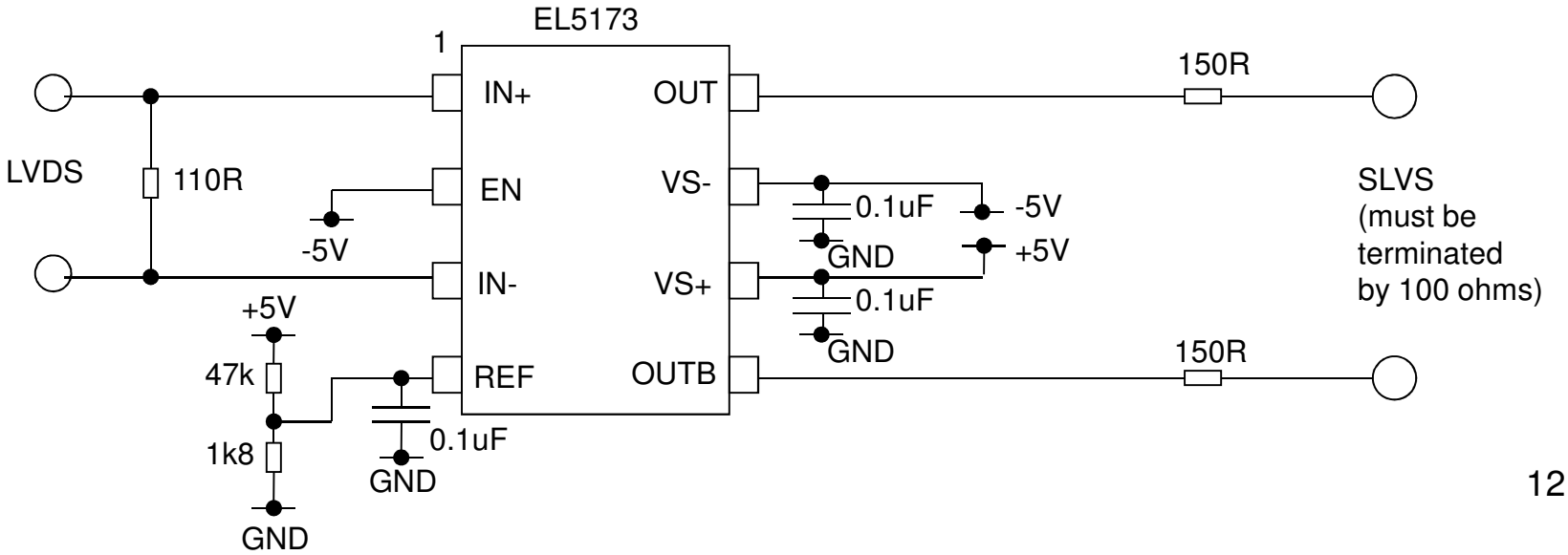
SN74AUC1G04



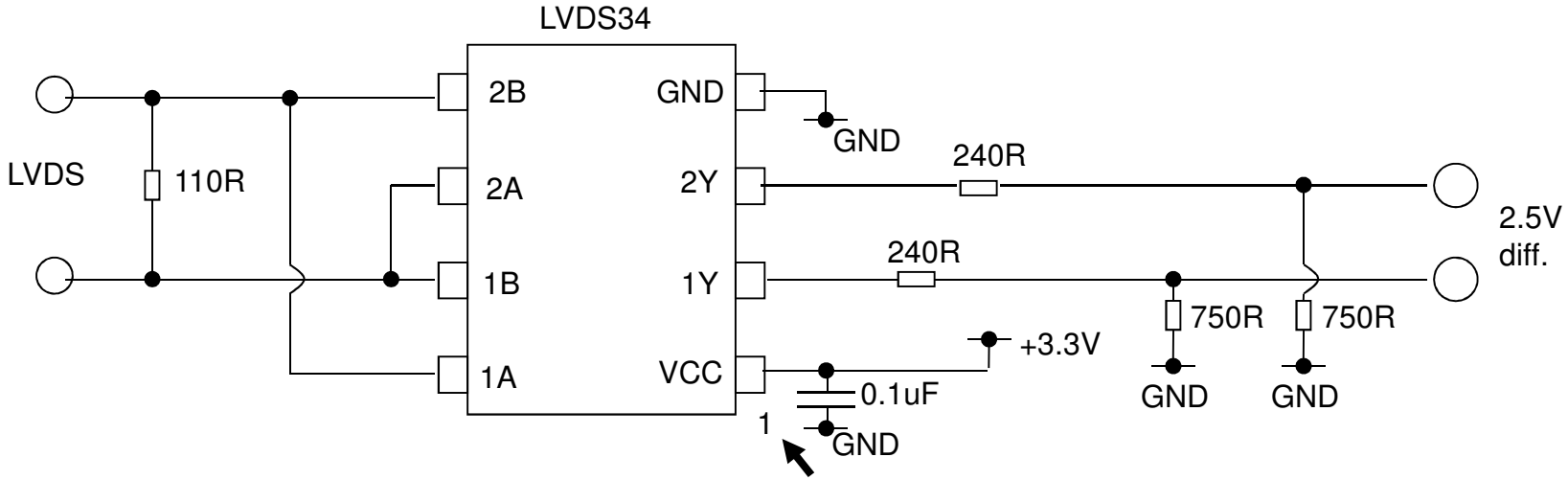


SN74AUC1G04

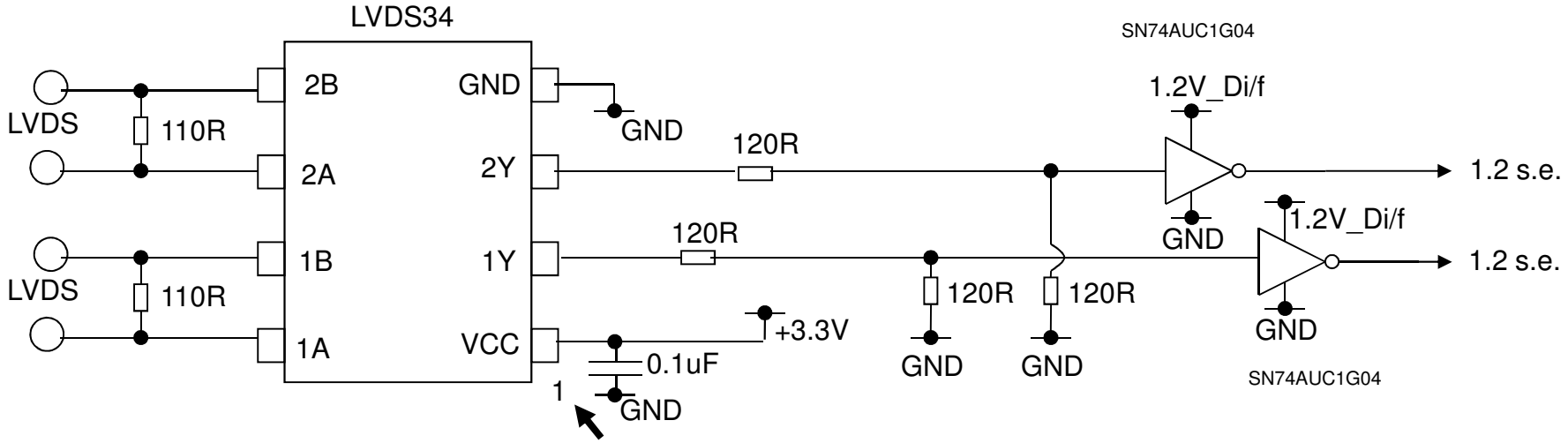
LVDS -> SLVS



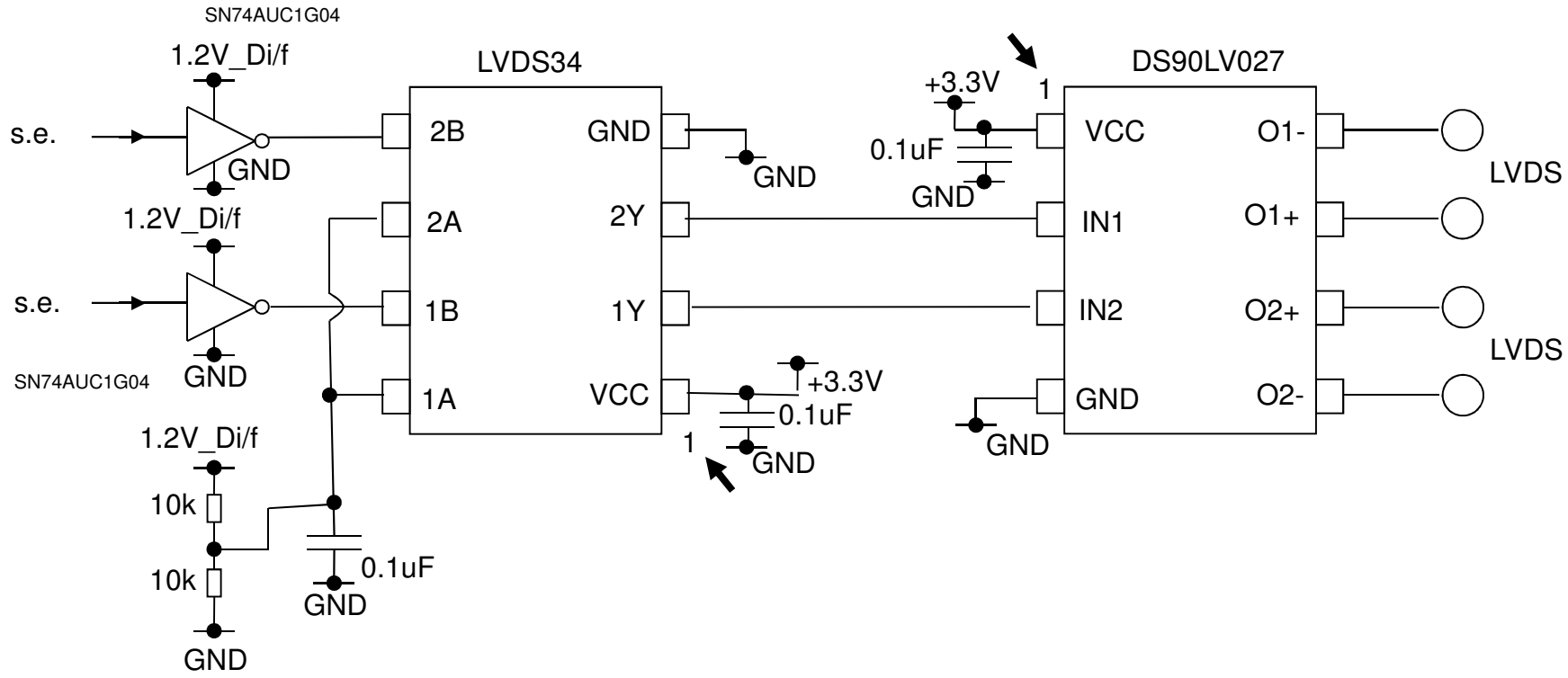
LVDS -> 2.5V diff.



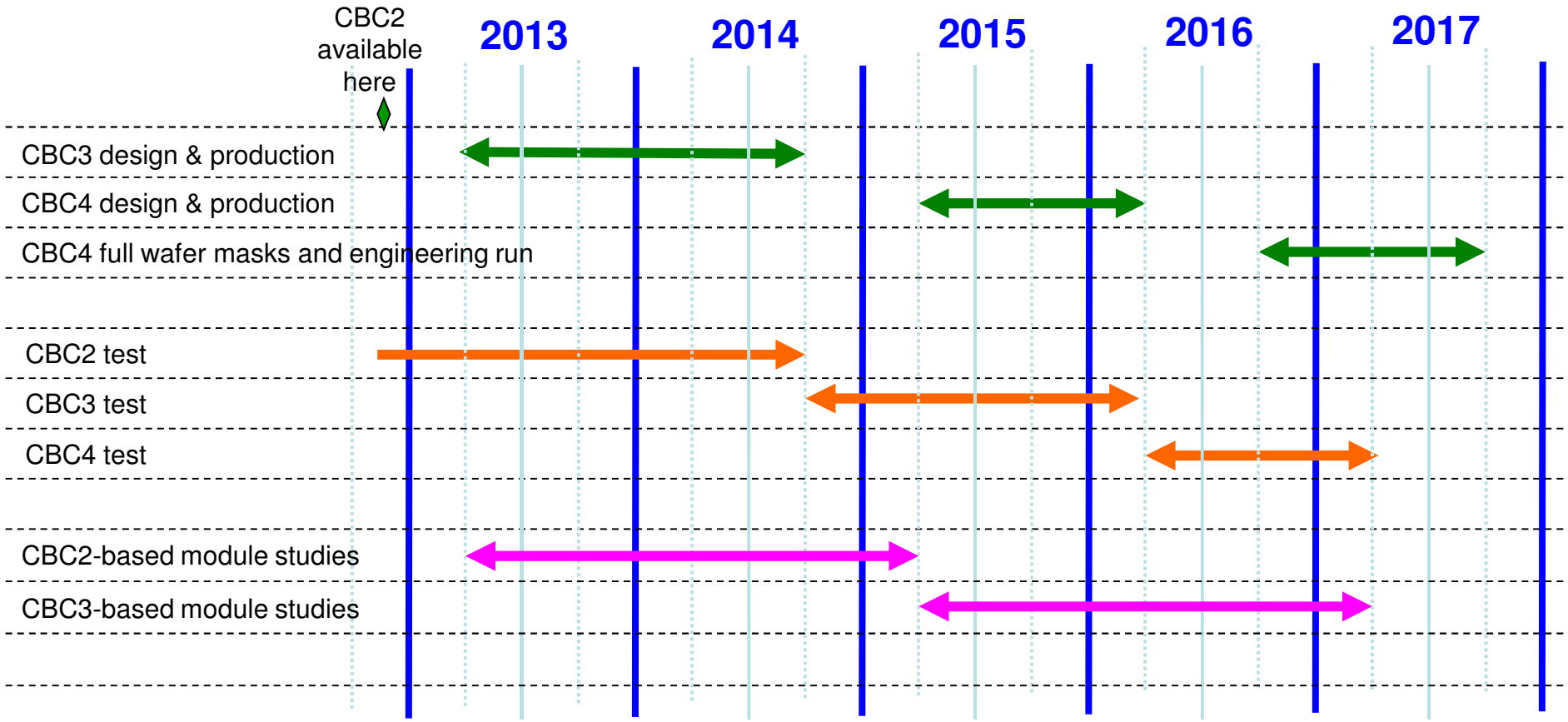
LVDS -> single-ended



single-ended -> LVDS



UK Phase II programme



CBC3 should be very close to final chip – available late 2014
- incorporate architecture to transmit stub addresses
- slow ADC for on-chip monitoring
- …

CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017