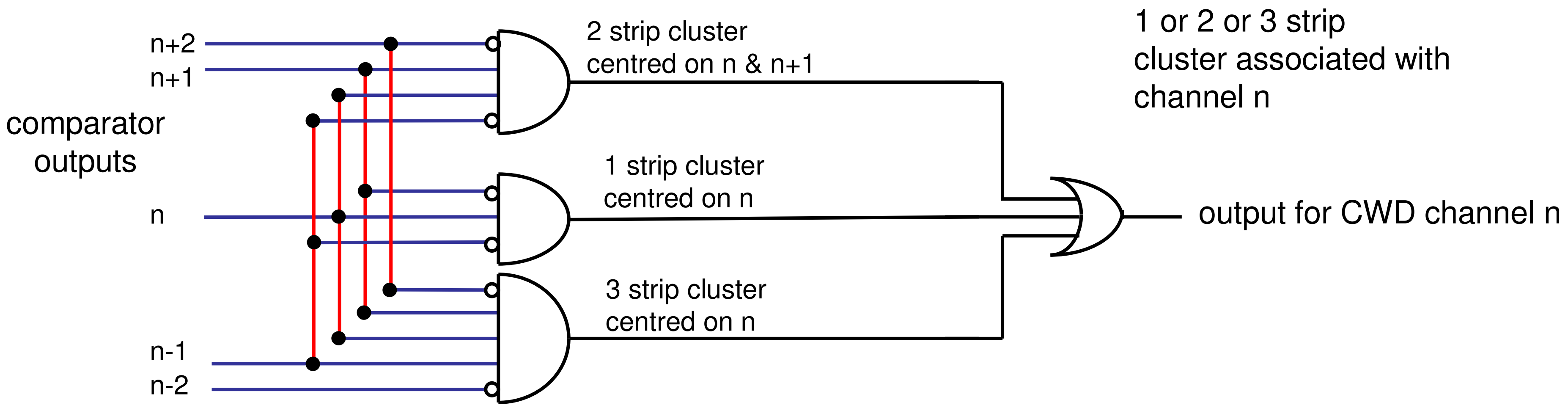
how to reach ½ strip resolution in CBC3?

a few slides to aid discussion and maybe clear up any possible misunderstandings

CWD logic on CBC2



comparator outputs

n+2

n+1

n

n-1

n-2

2 strip cluster centred on n & n+1

1 strip cluster centred on n

3 strip cluster centred on n

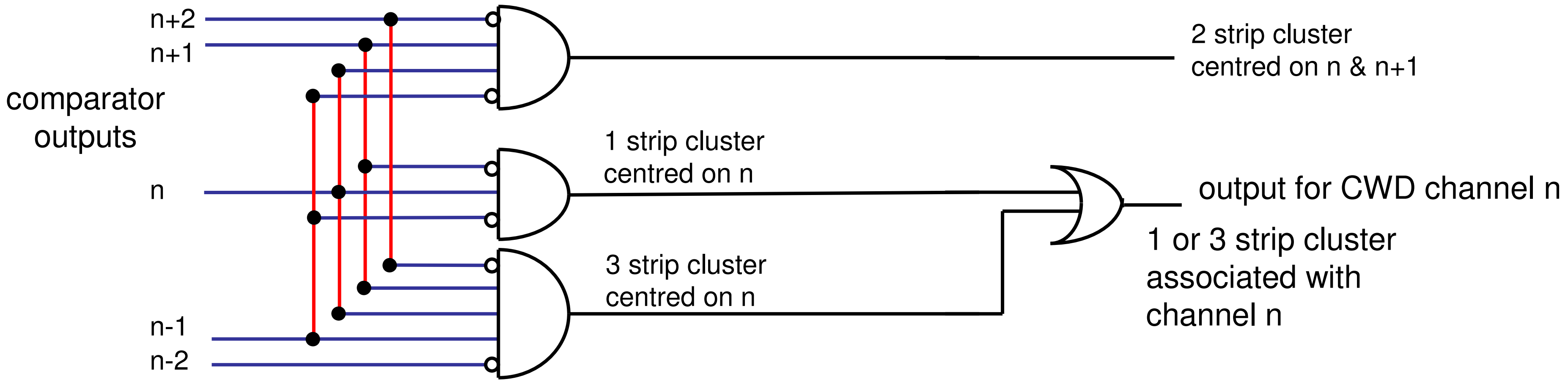
1 or 2 or 3 strip cluster associated with channel n

output for CWD channel n

this is the current approach in CBC2
programmability not shown but can choose one of 4 options:

CWD switched off	**: output = n**
1 strip cluster	**: output =** $(\overline{n-1}).n.(\overline{n+1})$
1 or 2 strip cluster	**: output =** $(\overline{n-1}).[n+(n+1)].(\overline{n+2})$
1 or 2 or 3 strip cluster	**: output =** $(\overline{n-2}).[(n-1)+n+(n+1)].(\overline{n+2})$

CWD logic with separate output for 2 strip clusters



comparator outputs

2 strip cluster centred on n & n+1

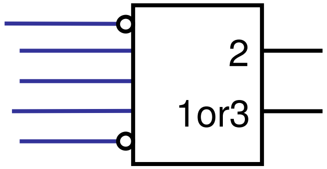
1 strip cluster centred on n

3 strip cluster centred on n

output for CWD channel n

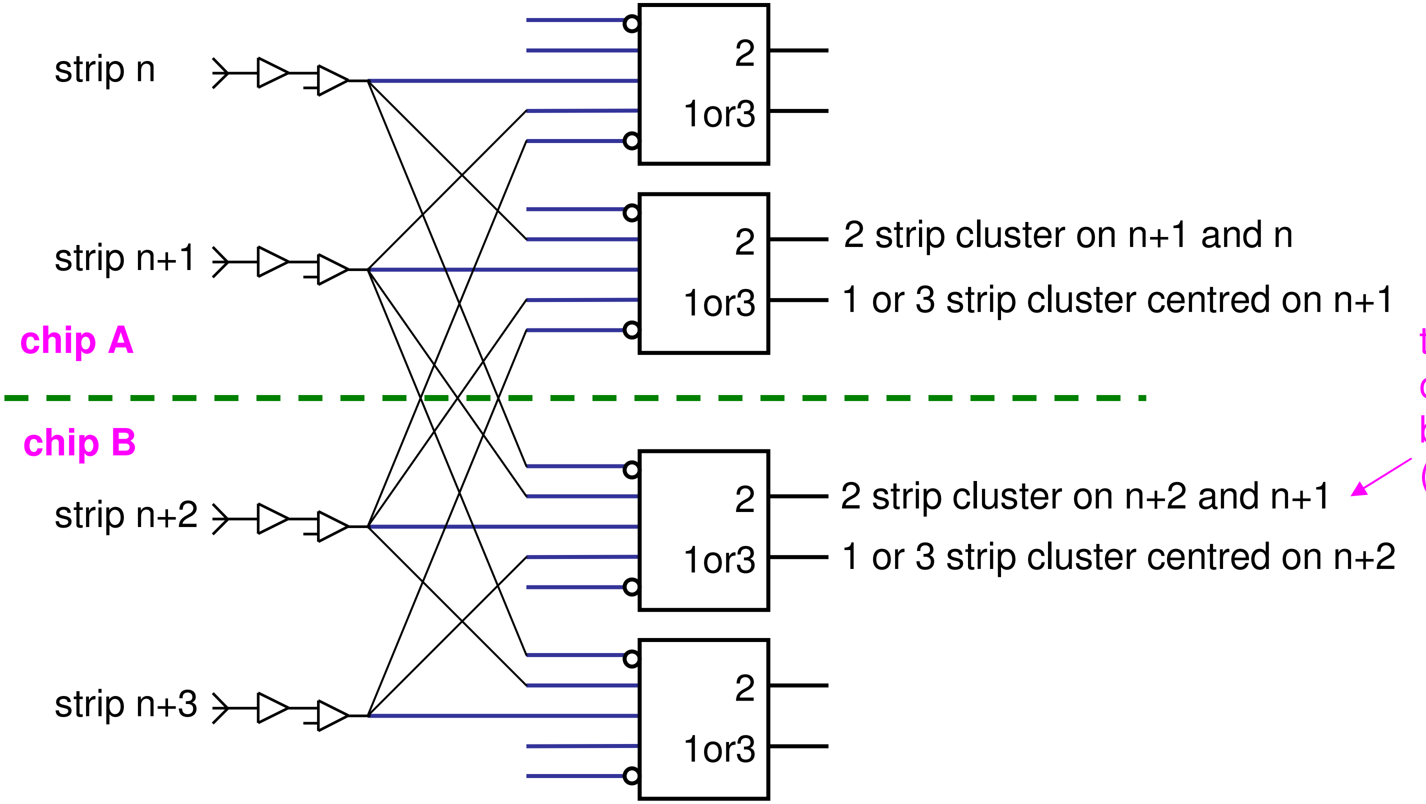
1 or 3 strip cluster associated with channel n

represent above as



any consequences at chip boundaries?

I don't think so



2 strip cluster on n+1 and n

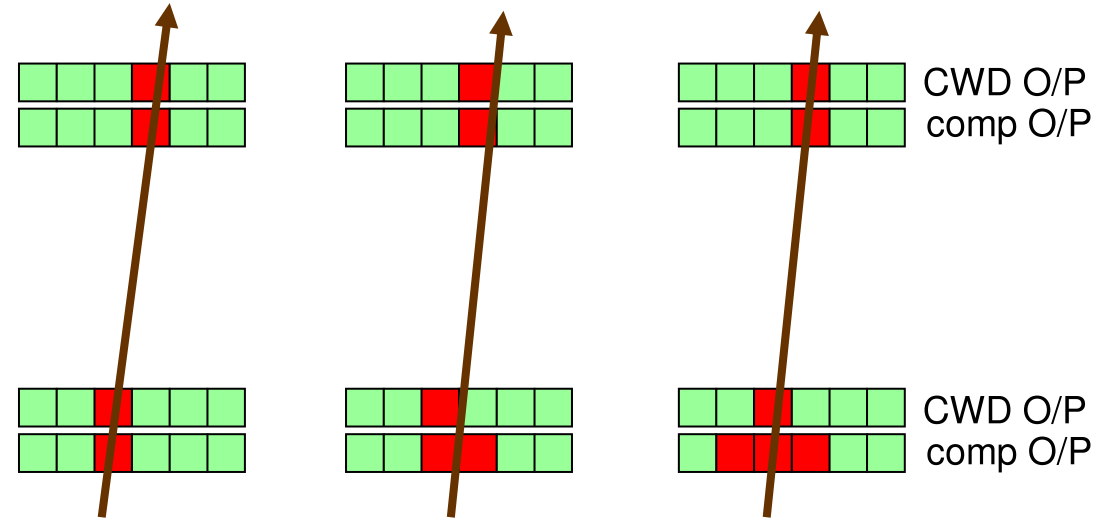
1 or 3 strip cluster centred on n+1

2 strip cluster on n+2 and n+1

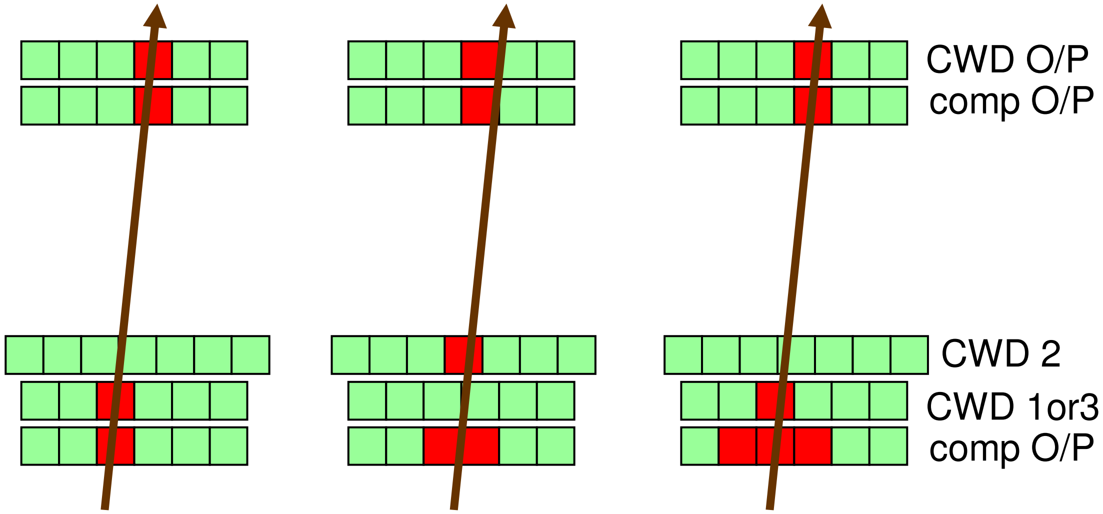
1 or 3 strip cluster centred on n+2

this cluster crosses chip boundary - will be detected on chip B (not chip A)

what about correlation



existing logic



future system - some assumptions and questions

½ strip precision only required in inner (lower) layer?

can OR 1or3 output with 2 for correlation purposes?

final comments

if assumptions on previous slide correct then ½ strip resolution (for hit in inner layer)
only has implications for transmission data volume off-chip

½ strip resolution for *correlation* and/or *outer layer window definition* means more inter-chip signals
(I think) so that probably rules it out

off-chip data volume issues need further study (how to do it)

would like requirements for CBC3 to be firm by ~ March 2013 if possible (design phase should begin)

neighbour chip signals - CWD O/Ps

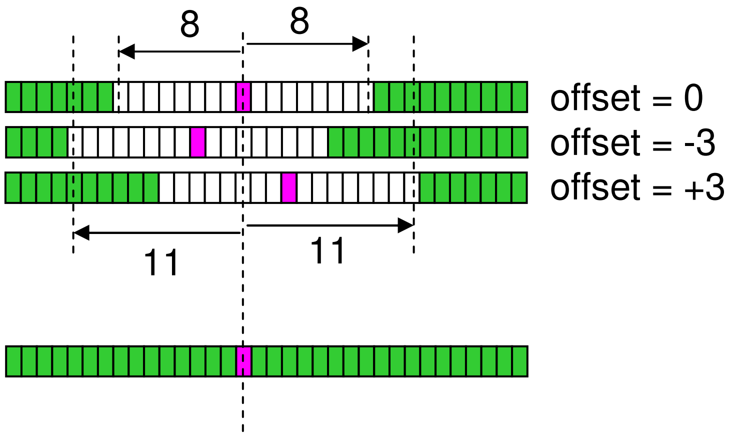
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

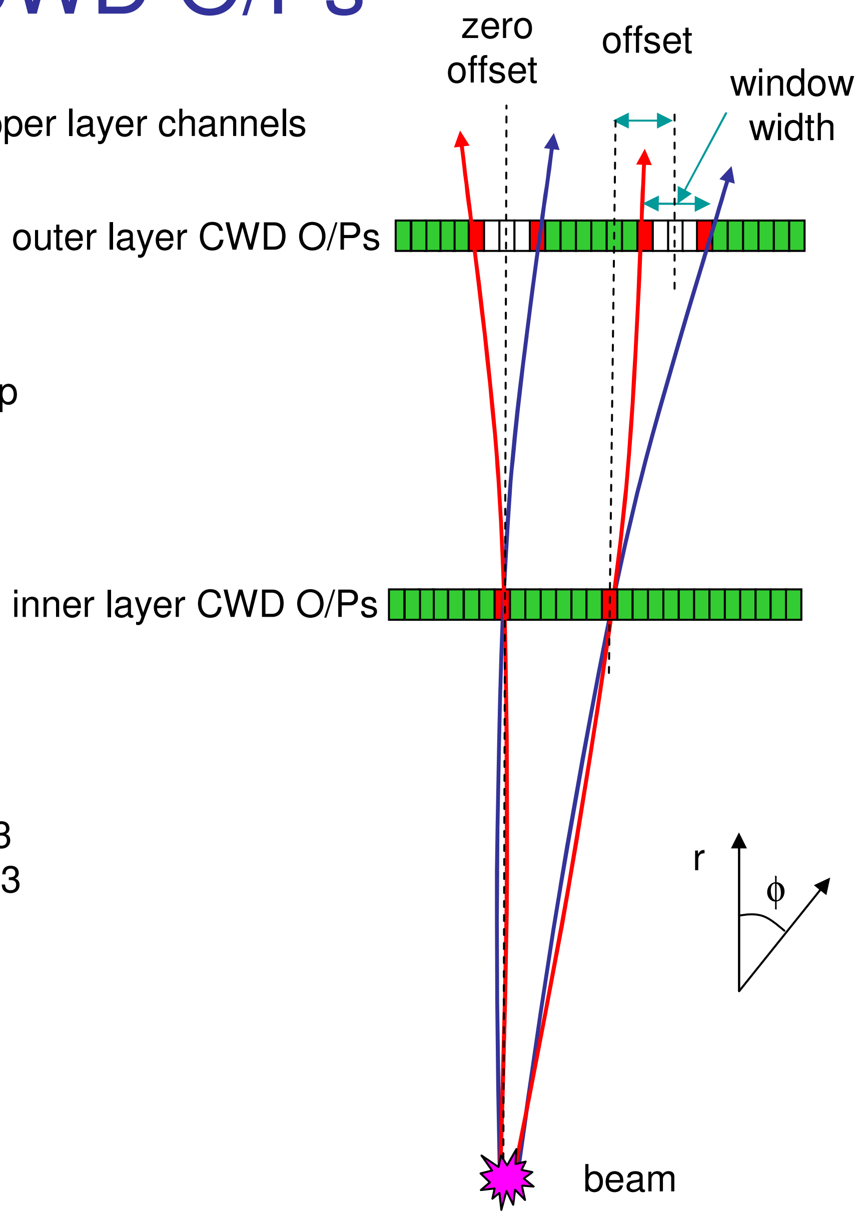
window defines Pt cut
        width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
        programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
    11 to receive from neighbouring chip

  = 22 signals





adding comp O/Ps -> 30 signals altogether, top and bottom of chip