CBC2 test plans

short term
- CBC1 test beam
- wirebond CBC2 test setup
- CBC2 wafer test
- 2xCBC2 substrate test setup

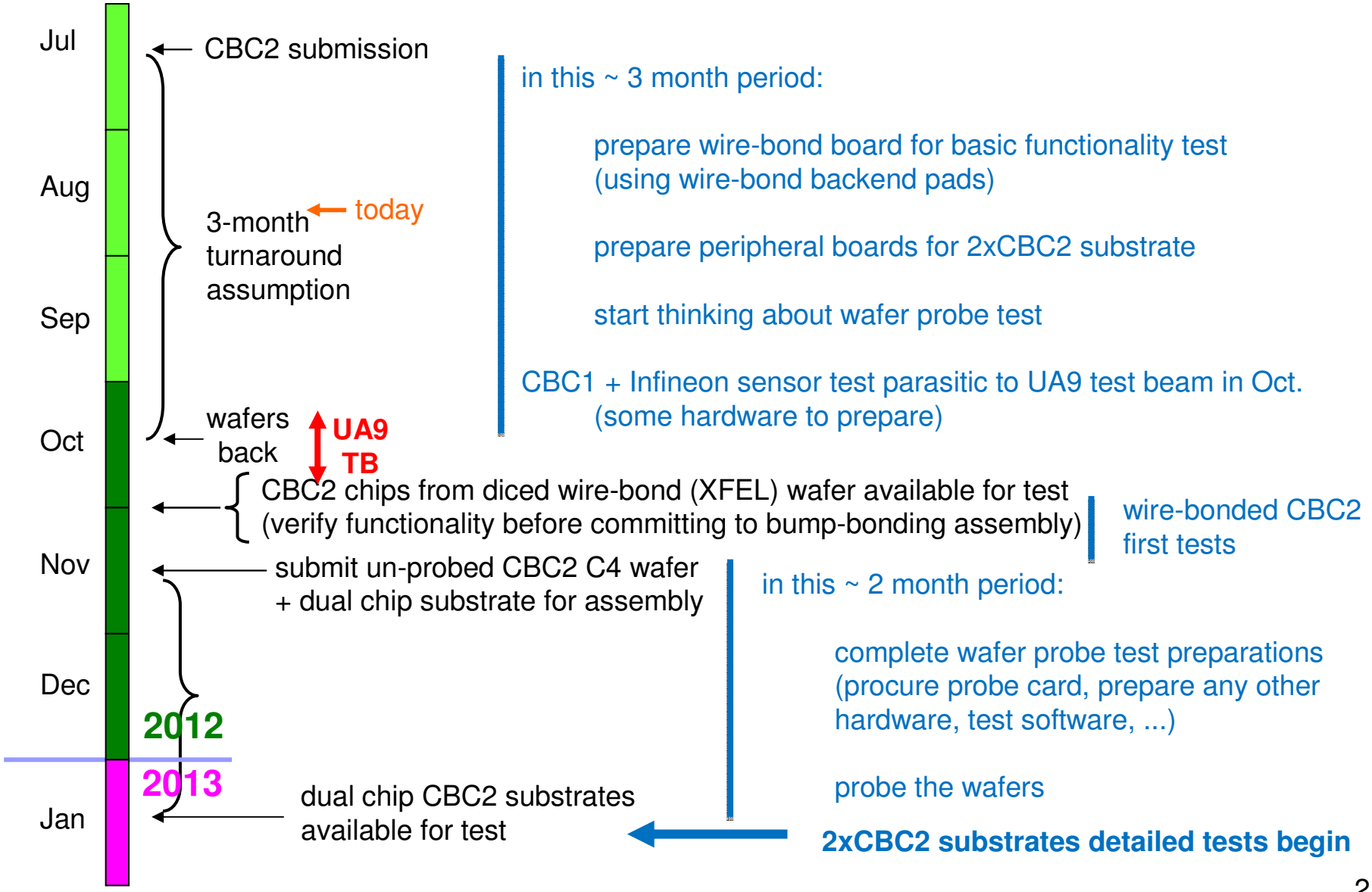
} will say something today

longer term
- 8xCBC2 substate
- full-size 2S-Pt module prototype

will not cover

M.Raymond

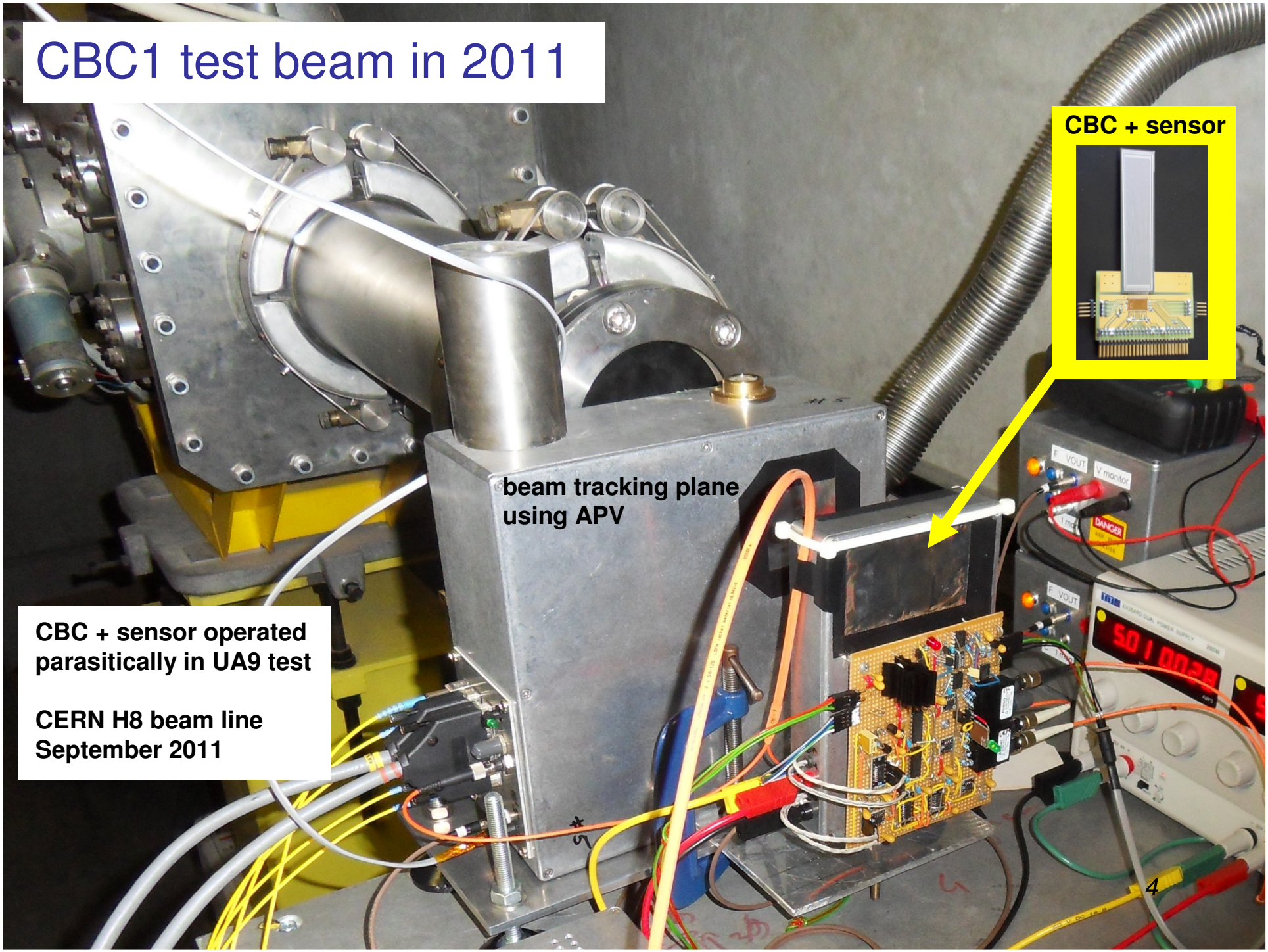
timeline for next ~ 6 months



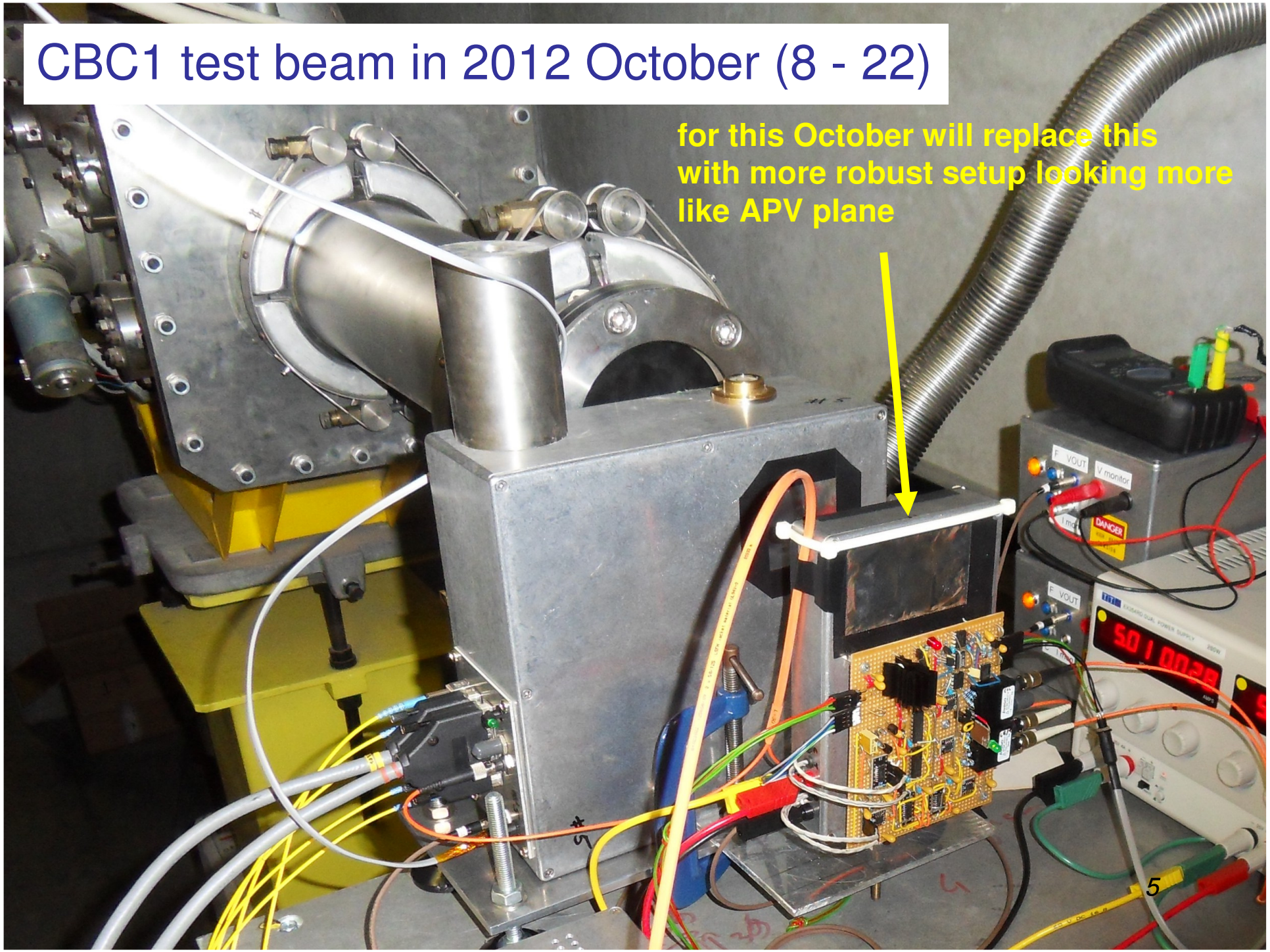
... 8 chip substrates and prototype SS-Pt module studies follow on later in 2013

CBC1 test beam this year

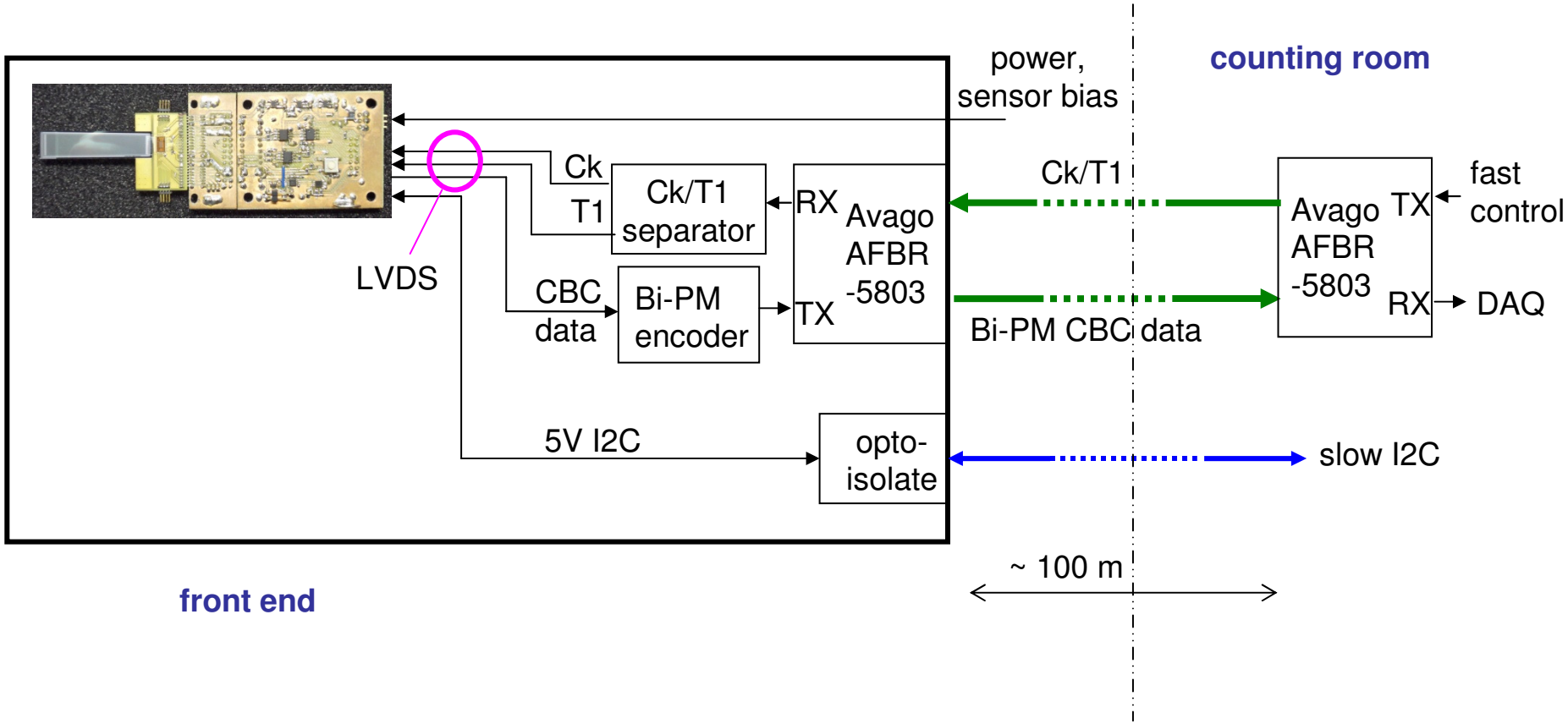
CBC1 test beam in 2011



CBC1 test beam in 2012 October (8 - 22)



CBC1 test beam system Oct. 2012



hardware under construction

will use Infineon 256 channel sensors from Vienna (4 received - will bond 2)
reading out ~ 128 good strips (avoid bad strips region)

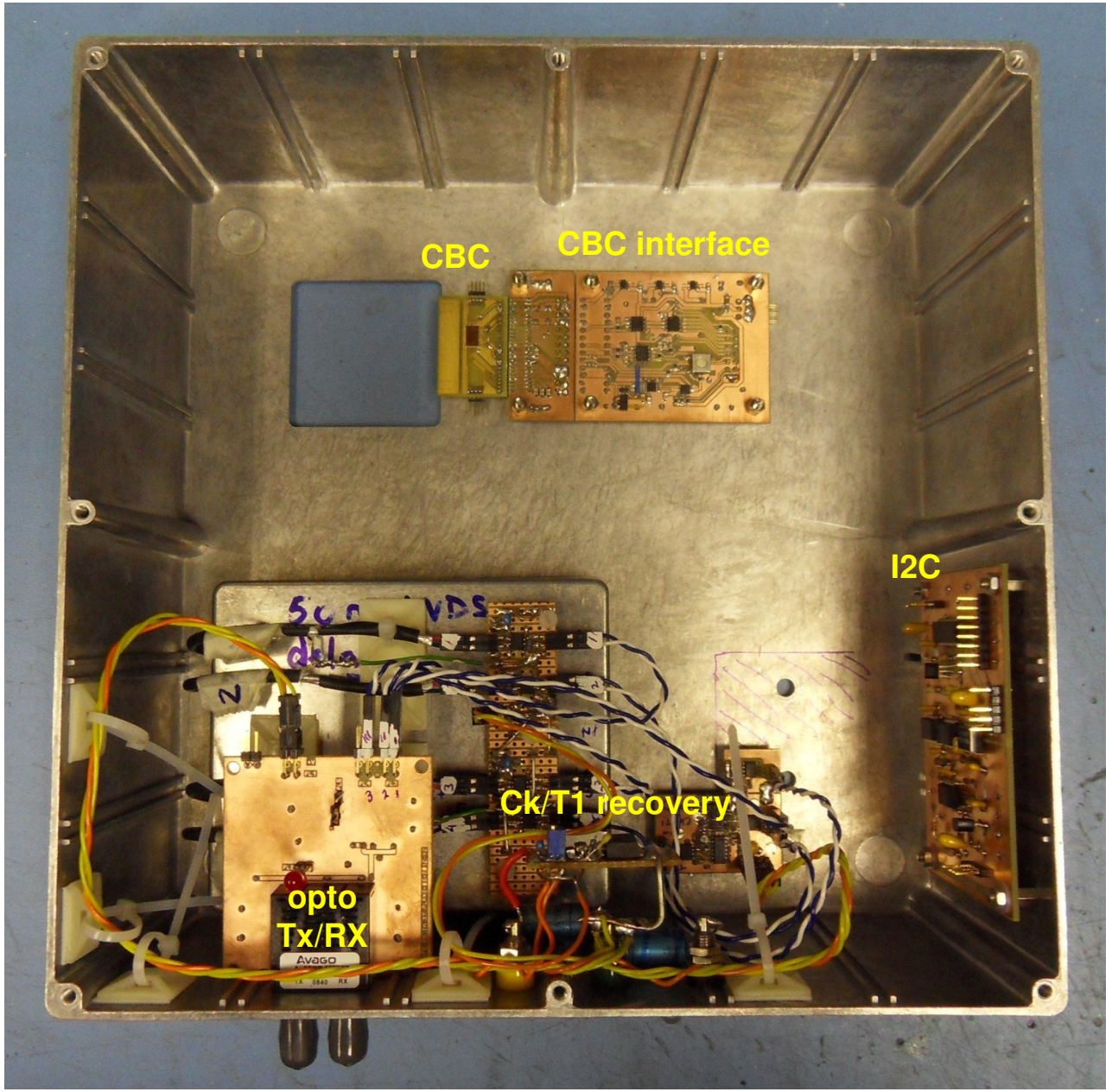
will give point of comparison with 2xCBC substrates using same sensors

current hardware status

few bits left to put in

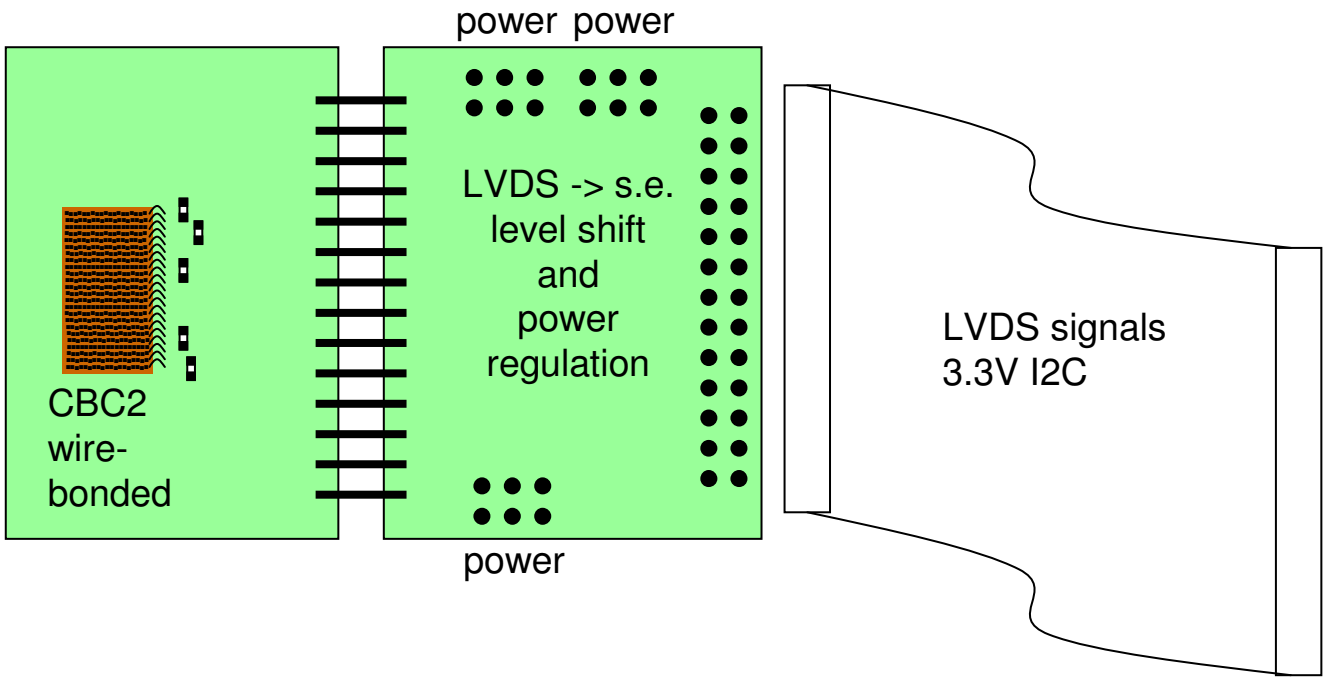
sensor to be glued and bonded this/next week

some testing required



wirebond CBC2 test setup

wirebond CBC2 test setup

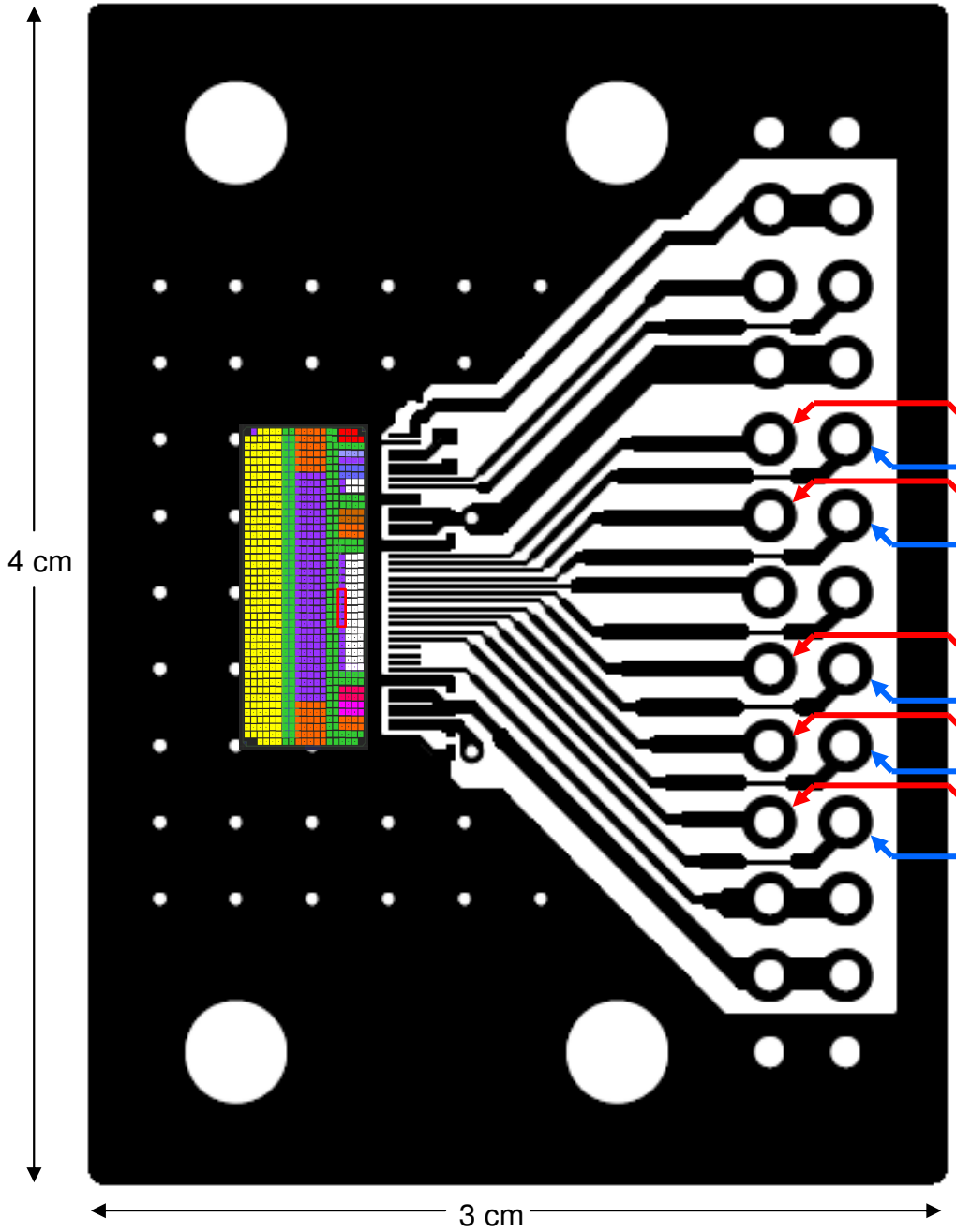


use wafer probe pads to wirebond single CBC2 die to carrier
(CBC2 chips from diced wire-bond (XFEL) wafer)

allows to verify CBC2 functionality before committing to bump-bond

can also use to develop wafer probe procedures

CBC2 wirebond carrier PCB

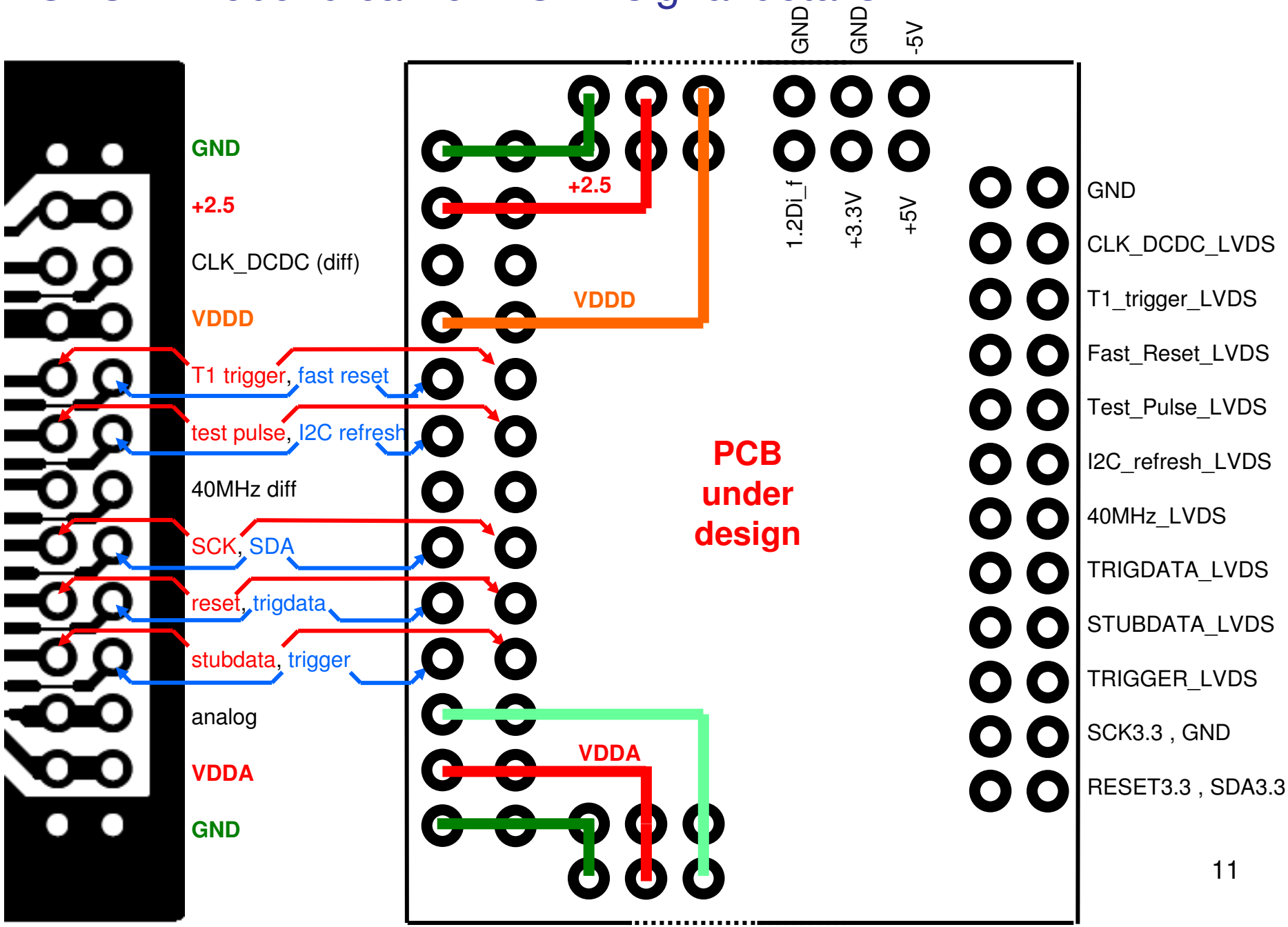


double-sided PCB (other side ground)

	pads on chip
GND	**GND**
+2.5	**+2.5**
GND	**GND**
DC-DC ck (1M diff)	1M diff
	1M diff
VDDD	**GND**
	VDDD
	GND
T1 trigger, fast reset	T1 trigger
	fast reset
test pulse, I2C refresh	test pulse
	I2C refresh
40MHz diff	40M diff
	SCK
SCK, SDA	SDA
	reset
reset, trigdata	trigdata
	stubdata
stubdata, trigger	trigger
	analog
analog	**GND**
VDDA	**VDDA**
	VLDOO
GND	**GND**

will be submitted for manufacture soon

CBC2 wirebond carrier PCB - signal details

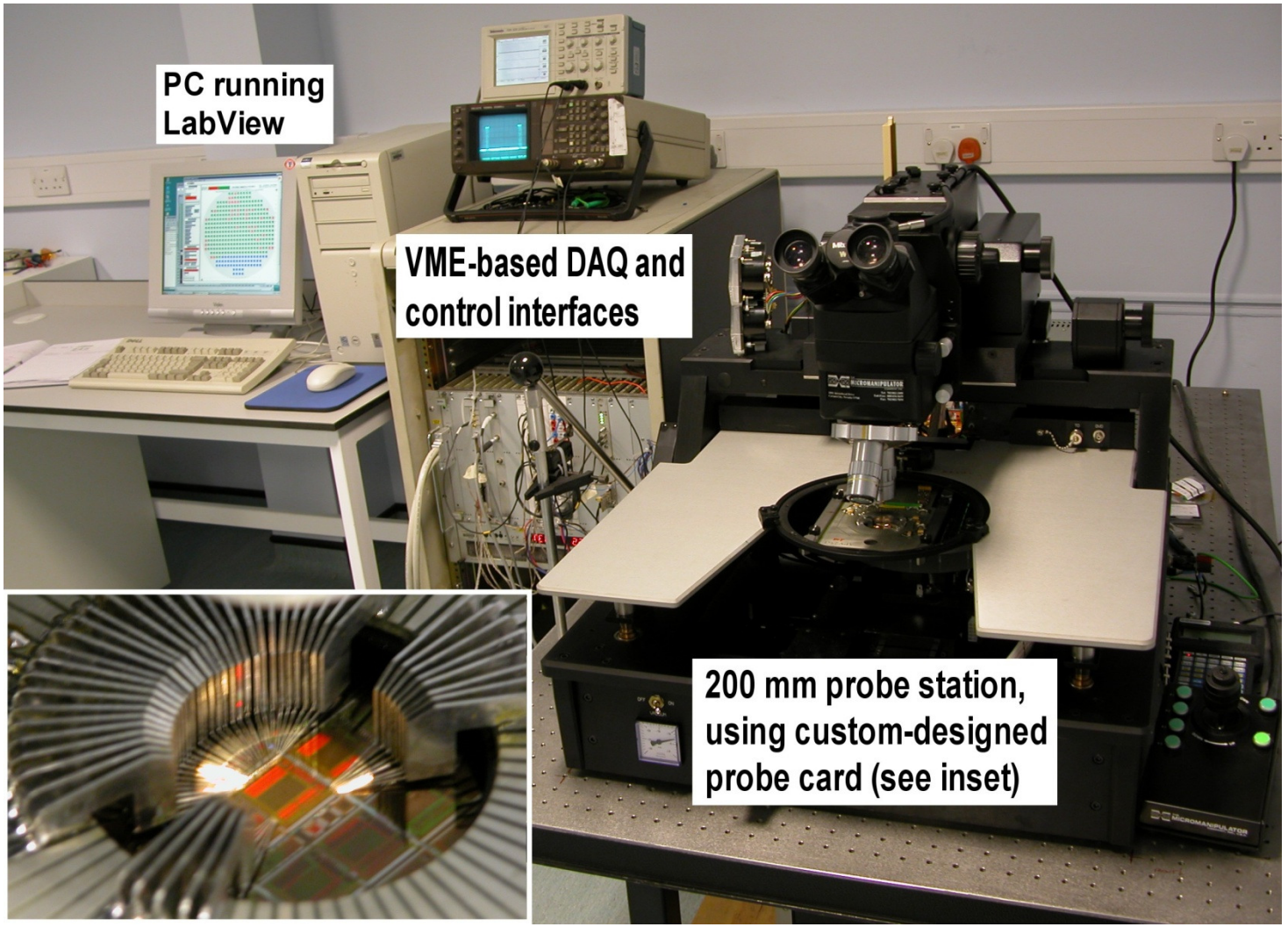


CBC2 wafer probing

Wafer Test Hardware

re-use APV screening system (would like to update but time is short)

need to get probe card manufactured (re-establish links with manufacturers)



Micromanipulator
8 inch semi–automatic
probe station

VME based
- ADC (8 bits)
- RAL SeqSi
  - 40 MHz CK/T1
- CERN VI2C I/F

PC controls both
DAQ (VME)
& probe-station (RS232)

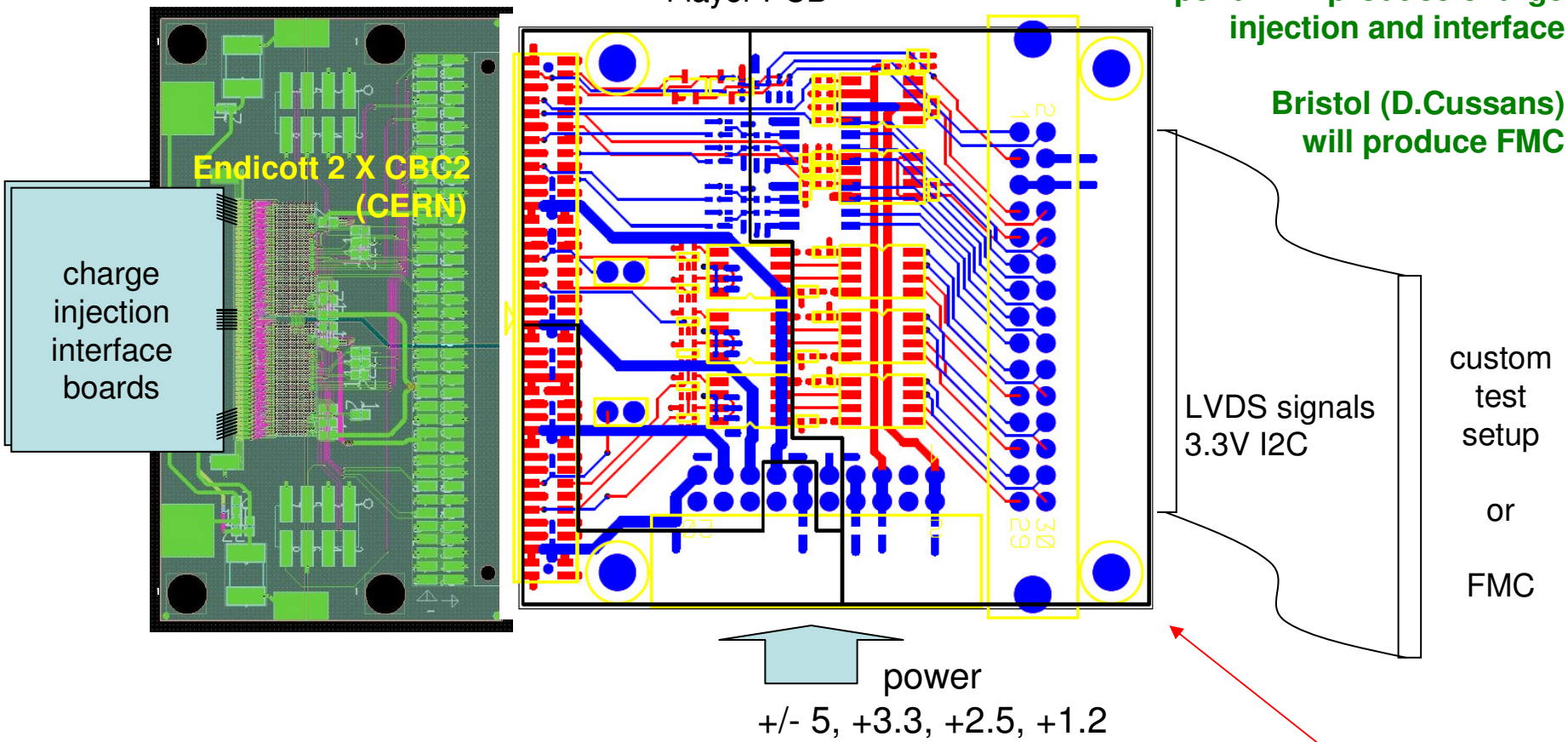
2xCBC2 substrate test setup

2xCBC2 substrate test setup

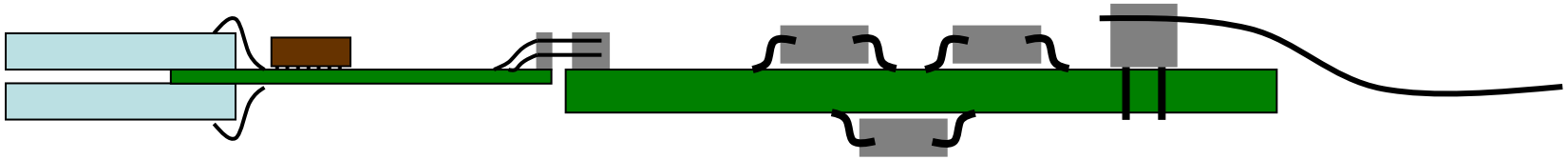
this will be the platform for detailed performance measurements

Imperial will produce charge injection and interface

Bristol (D.Cussans) will produce FMC



Infineon sensors can be used to produce mini 2S-Pt module



charge injection

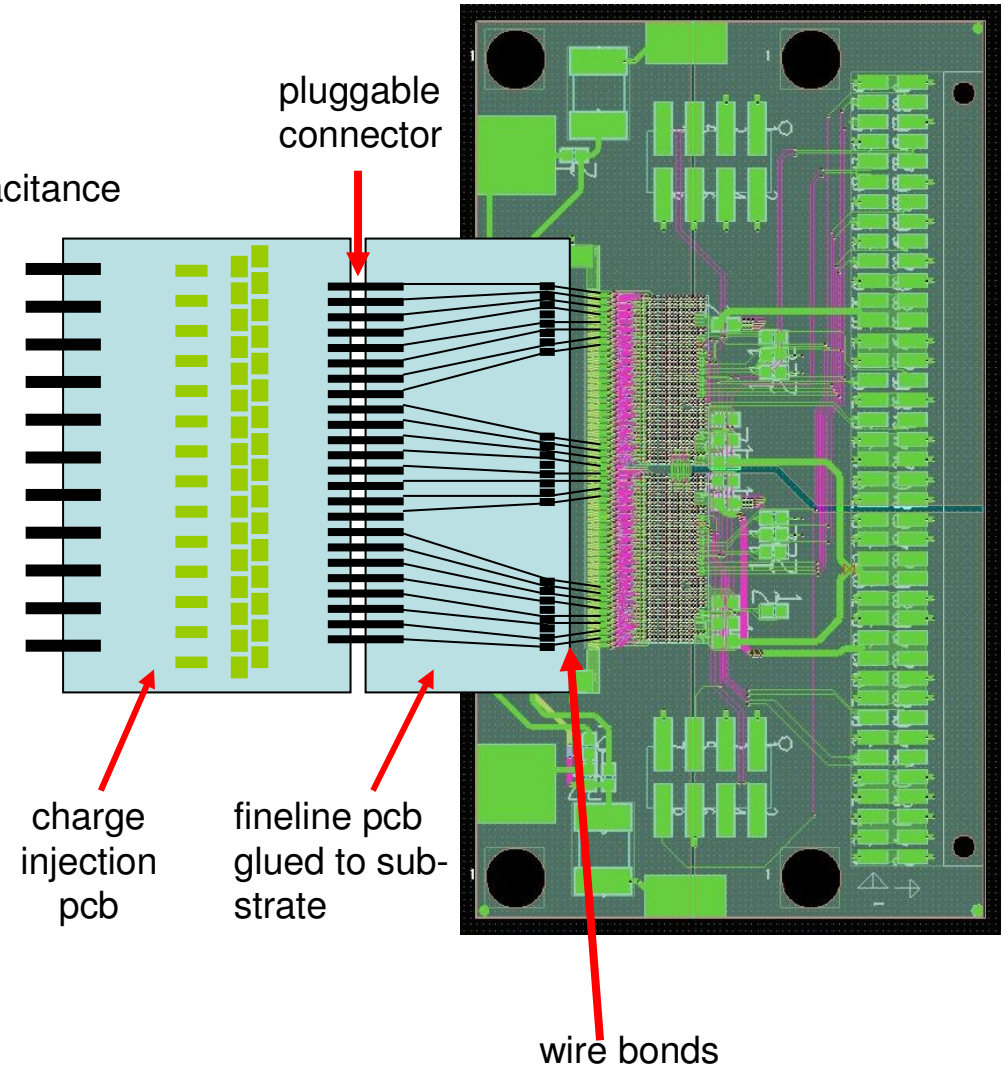
can only wirebond to 2xCBC substrate inputs

will want to study effects of varying external capacitance

don't want to waste substrates so propose a 2 stage approach

1) glue fineline pcb to substrate and wire-bond to CBC2 inputs. fineline pcb adapts to pluggable connector

2) can then have different variants of charge injection board that plug onto this to provide electrical interface



summary

short term (up to ~ end 2012 / beginning 2013)

CBC1 test beam
- October - hardware in preparation

wirebond CBC2
- ~ October/November - depending on wafer delivery
- should submit chip carrier boards for manufacture soon

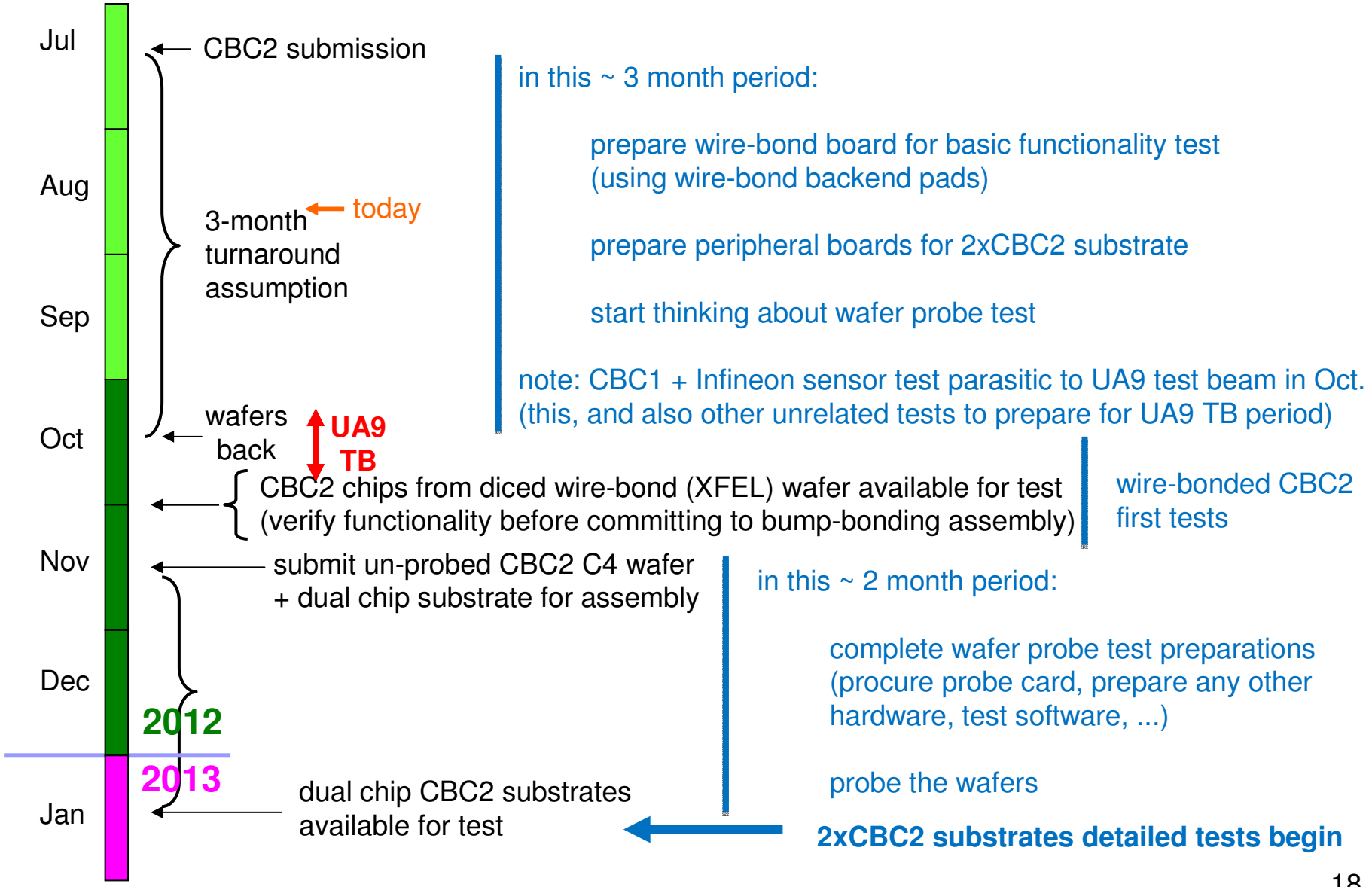
CBC2 wafer probe
- ~ end 2012 - needed for 8-chip substrate production next year
- get probe card manufactured ~ November

2xCBC2 substrate
- early 2013
- interface board already close to finished, simple charge injection boards need bit more thought
- FMCs to be produced by Bristol

division of labour

plan to concentrate test activity at Imperial (Davide will travel)
- avoids duplication of effort and extra hardware

timeline for next ~ 6 months - repeated slide



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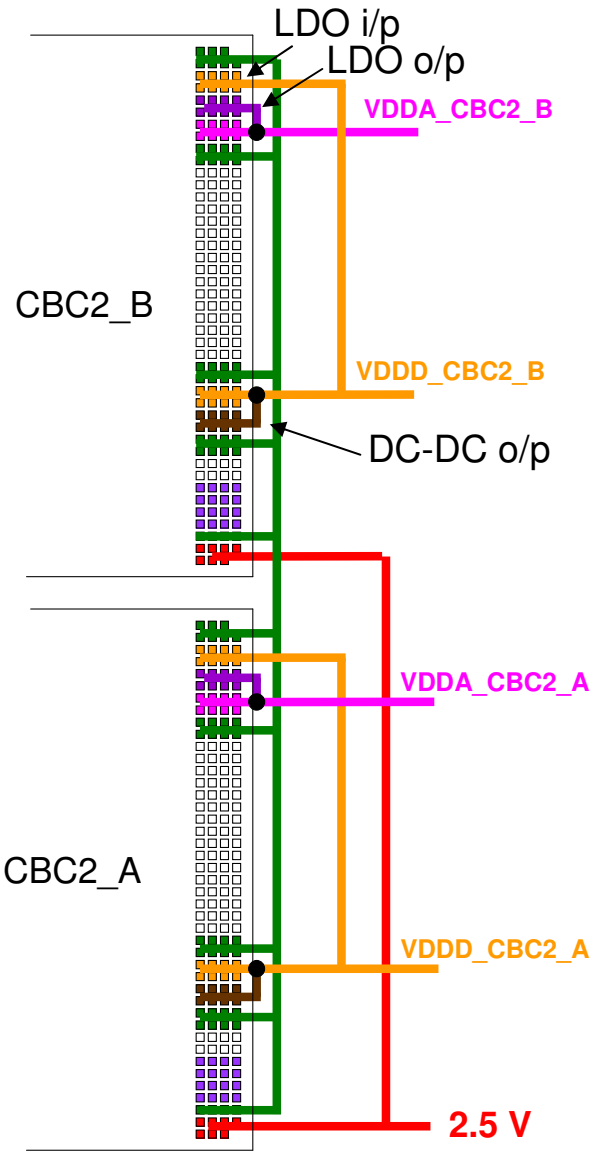
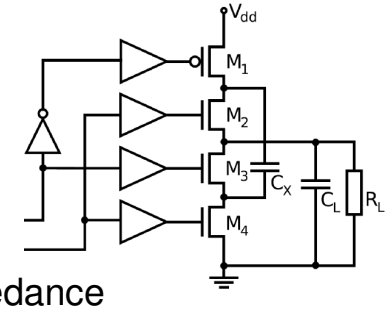
extra

CBC2 powering scheme on 2-chip substrate



backend pads as viewed through CBC2 substrate

after some thinking and discussion with Georges we have arrived at this scheme



2.5 V common to both chips

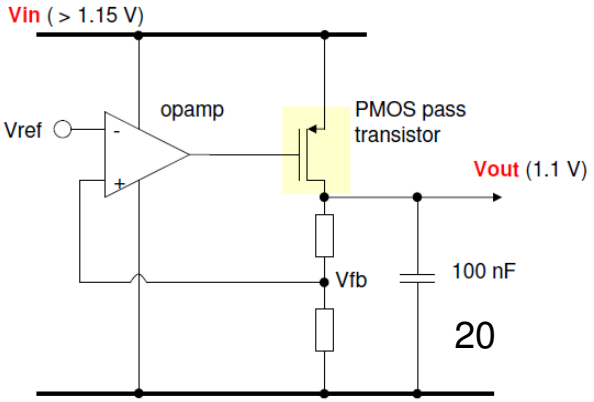
if DC-DC not clocked then output -> high impedance
=> DC-DC o/p can be shorted to VDDD
VDDD can be provided externally if not using DC-DC

connect VDDD directly to LDO i/p
keeping separate would allow to run VDDD at low voltage
but no significant power advantage to doing this

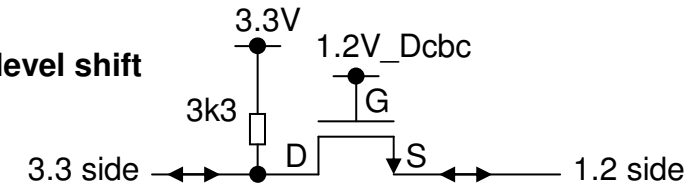
connect LDO o/p directly to VDDA
if want to supply VDDA externally then provide at slightly higher voltage than normal LDO o/p level

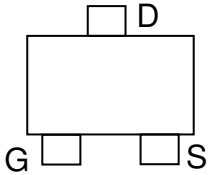
=> LDO shuts down (pass transistor turns off)
verified on CBC prototype

=> no jumpers required at all on substrate



3.3 -> 1.2 level shift

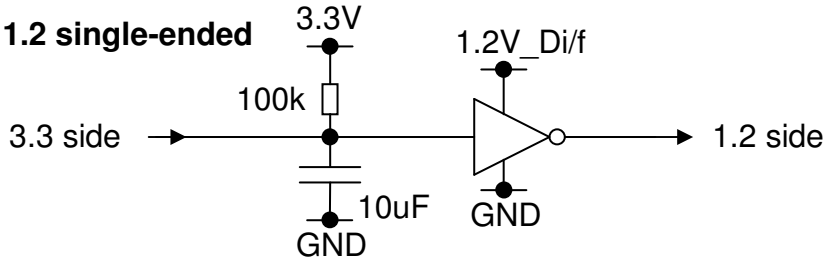


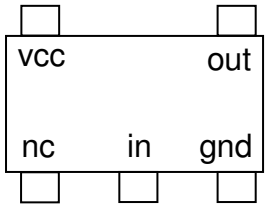


FDV303N
or
BSH103

3.3 -> 1.2 single-ended

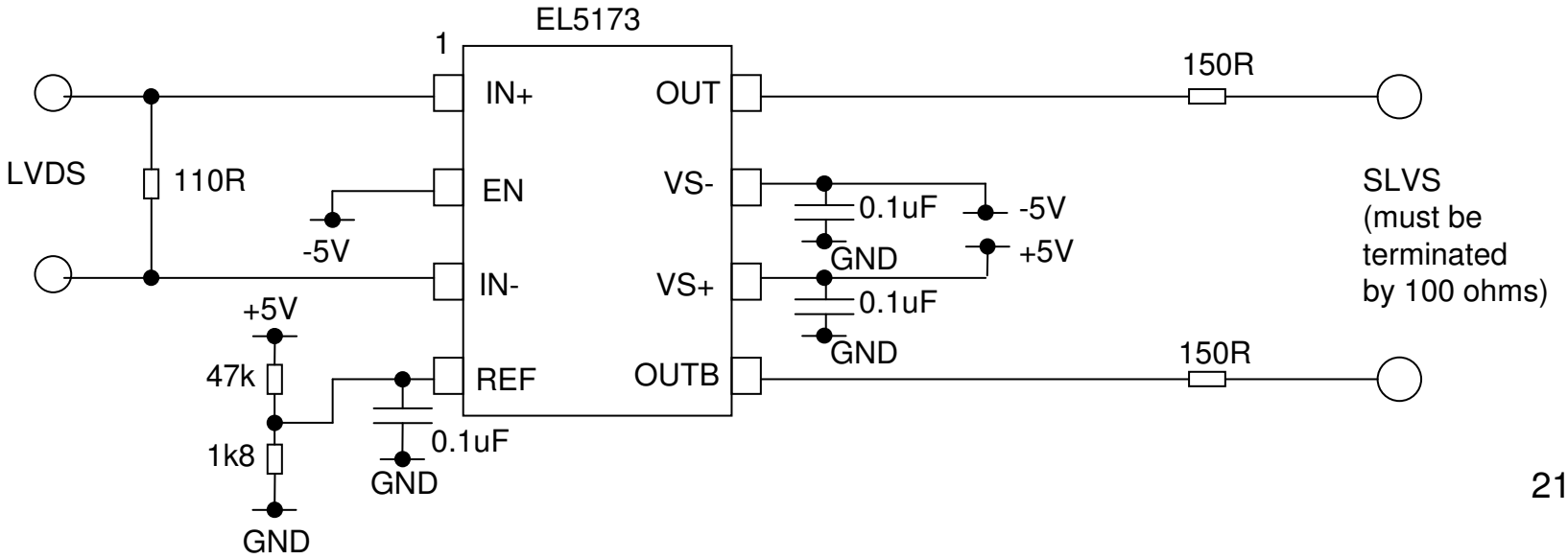
SN74AUC1G04



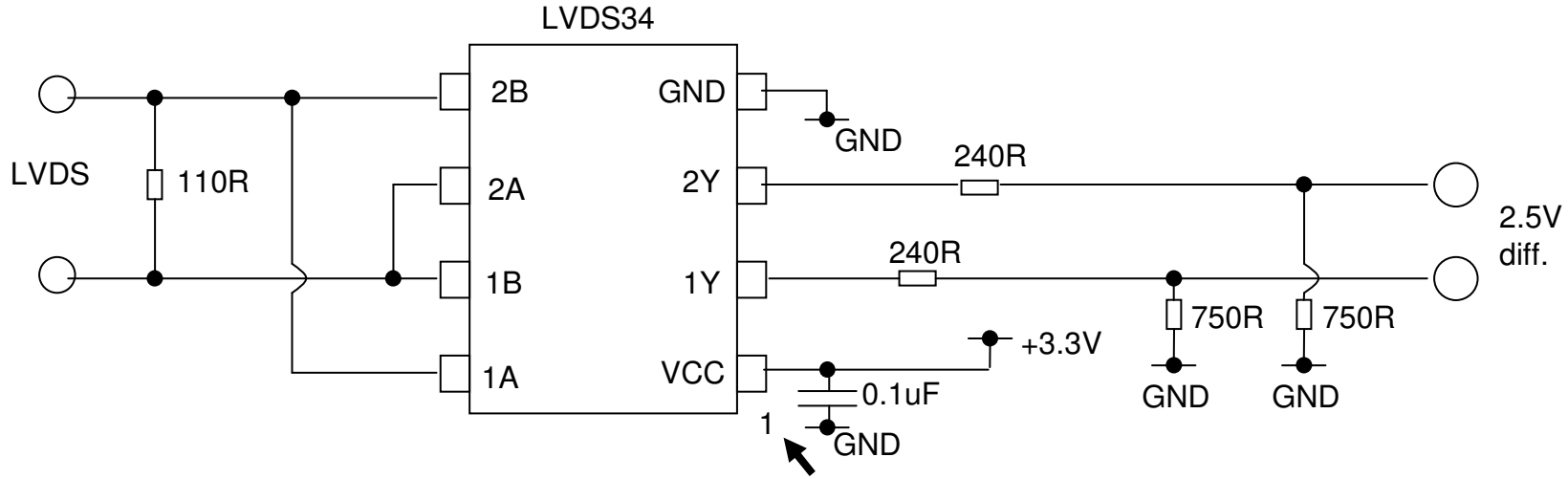


SN74AUC1G04

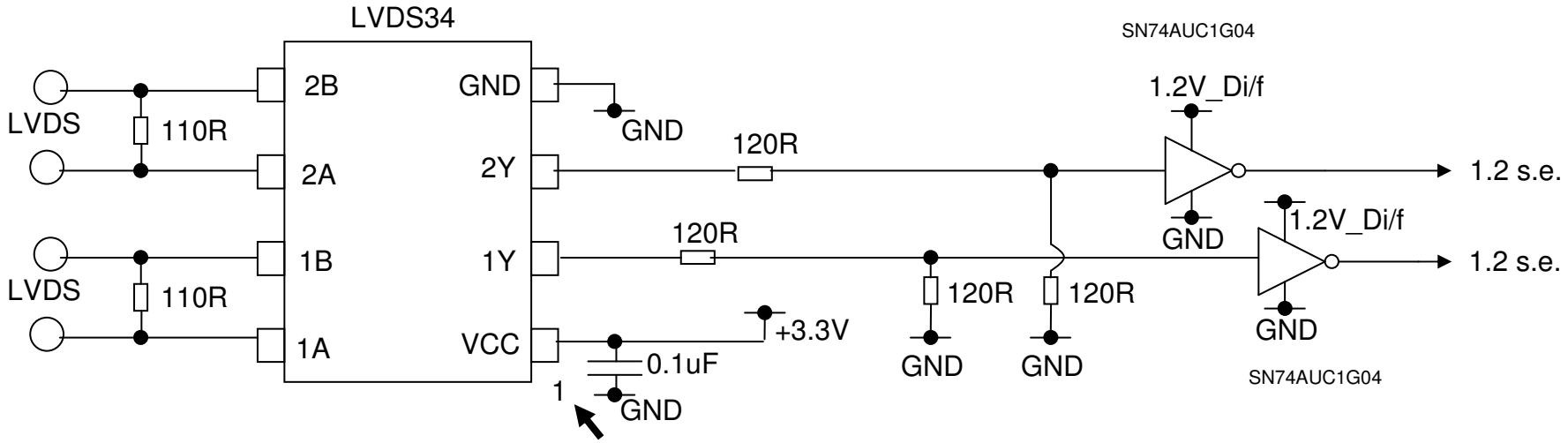
LVDS -> SLVS



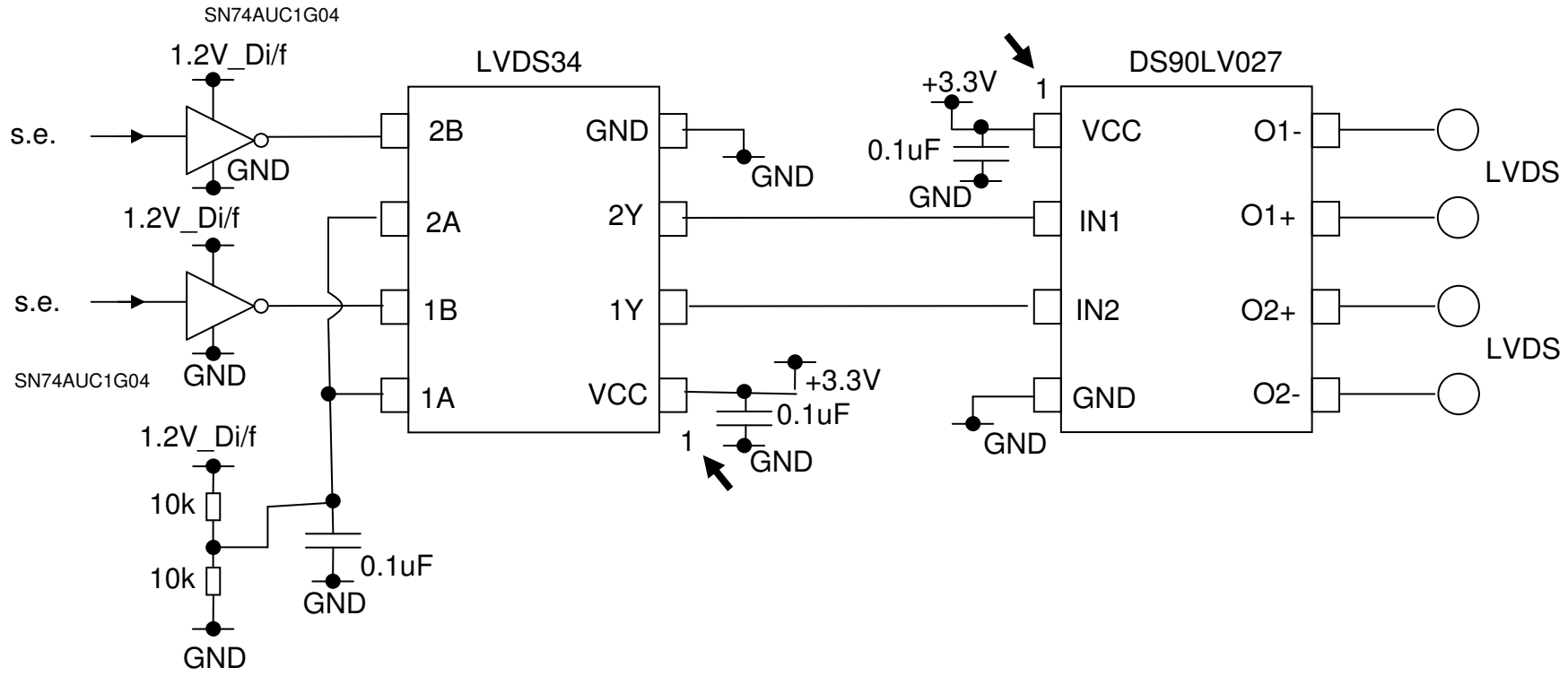
LVDS -> 2.5V diff.



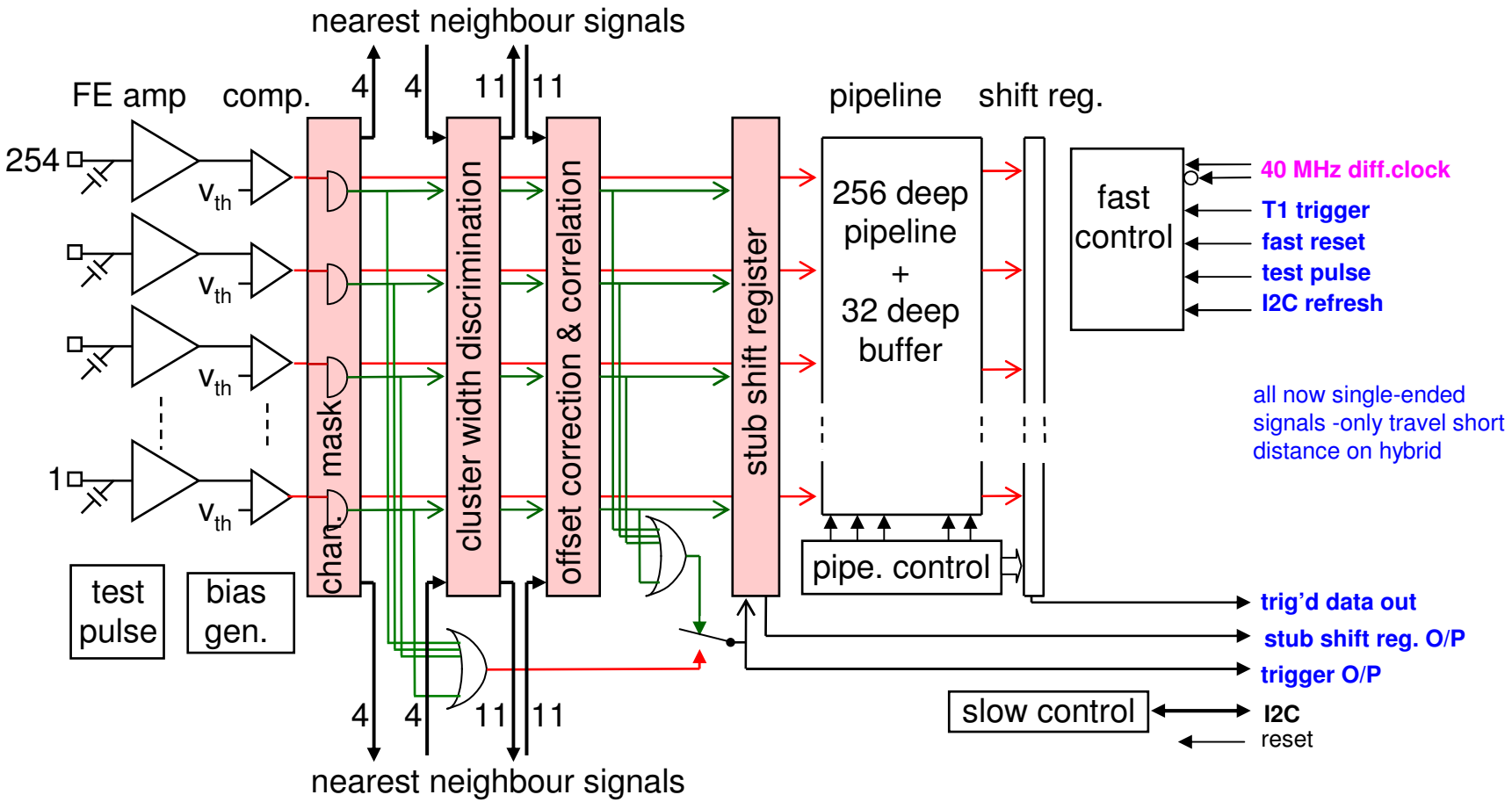
LVDS -> single-ended



single-ended -> LVDS



CBC2 architecture



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)

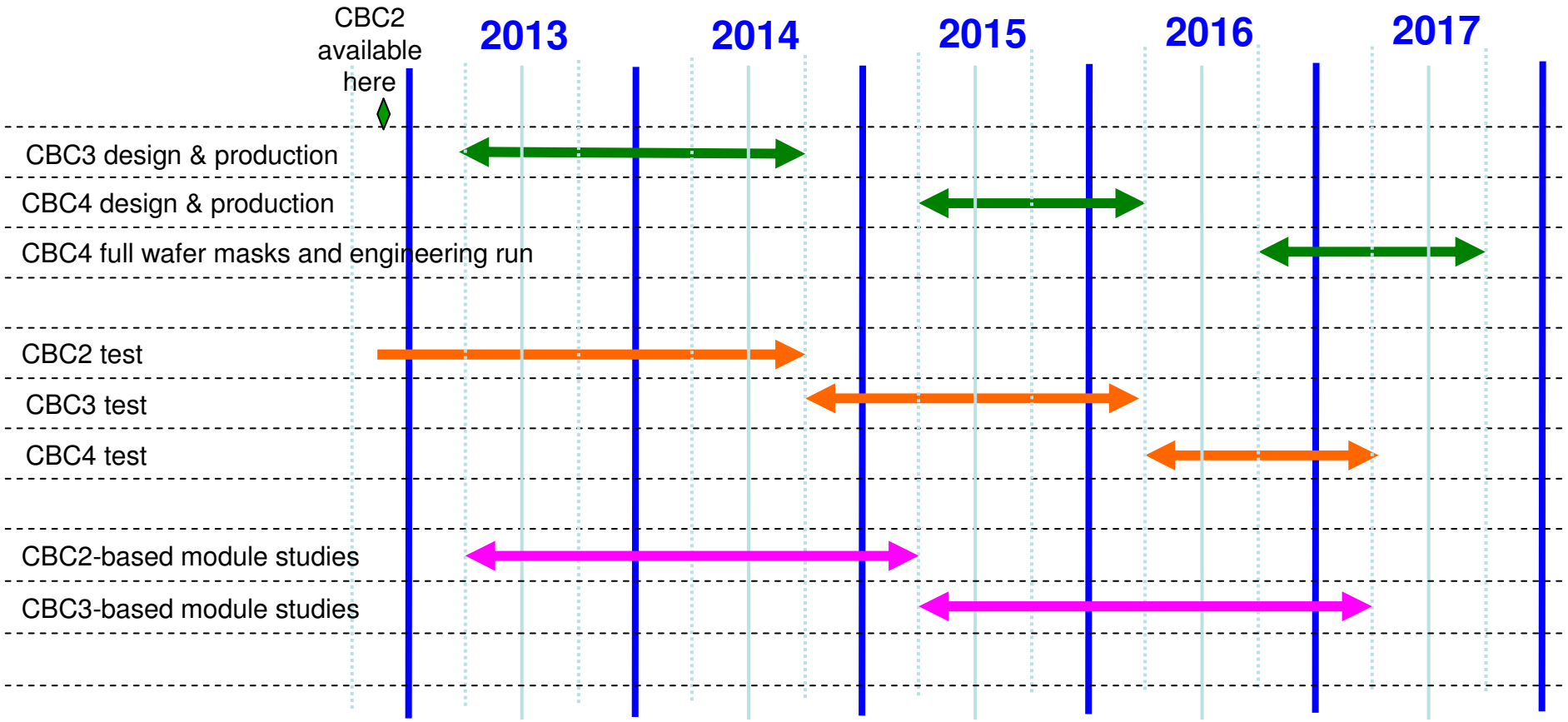
cluster width discrimination: exclude wide clusters > 3

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip for normal operation choose correlation O/P

UK Phase II programme



CBC3 should be very close to final chip – available late 2014
- incorporate architecture to transmit stub addresses
- slow ADC for on-chip monitoring
- …

CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017