# 2S-Pt module systems meeting, CERN, 26th January, 2012.

extract from Francois' agenda

1. CBC update (Mark)
   a. Do we have additional test results? Irradiation test plans?
      **DC-DC circuit measurements**
   b. Dead time issue due to pileup:
      i. have we made progress in estimating impact on physics?
         **not to my knowledge**
      ii. have other shaper designs been evaluated (incl. impact on power consumption)?
         **not in detail but can give a few preliminary thoughts and numbers**
   c. I2C: what variant has been implemented in CBC, what termination is required on hybrid?
      **Davide will cover**
   d. Enclosed transistors in analog front-end: What is the decision, do we keep them or not?
      **Davide will cover**

2. CBC-C4 (Davide)
   a. Design status **- Davide**
   b. CBC bug fixes **- I will cover**
   c. Pad layout and numbering **- Davide**
   d. Single-ended vs differential trigger output lines: what is the decision? **- Davide**
   e. Plans and schedule to submission **- Davide**

M.Raymond

# DC-DC circuit measurements

# CBC power features reminder

### DC-DC switched capacitor converter

converts 2.5 -> ~ 1.2

clearly functioning, high efficiency ~ 90%

**study of DC-DC switching effects on noise follows in next slides**

### LDO linear regulator

provides clean,regulated rail to analog FE

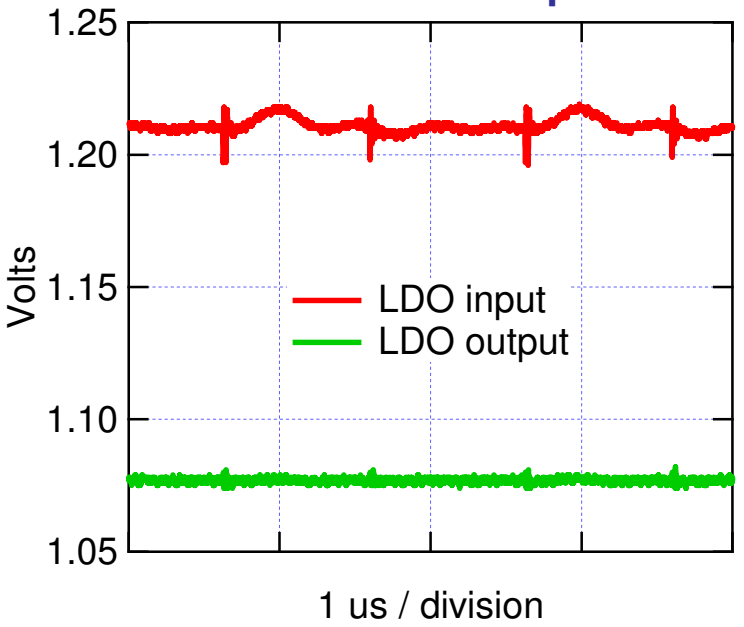
~ 1.2 Vin, 1.1 Vout

dropout ~ 40 mV for 60 mA load

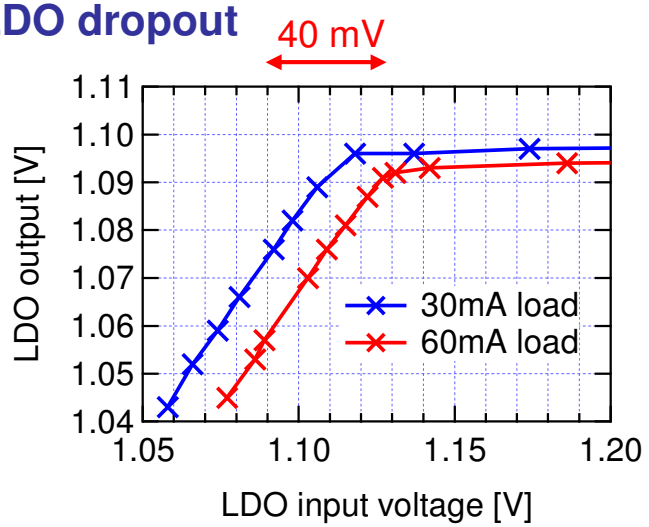
provides > 30dB supply rejection up to 10 MHz

for further details see:
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_Tracker_Electronics_May_11.pdf

### DC-DC & LDO outputs

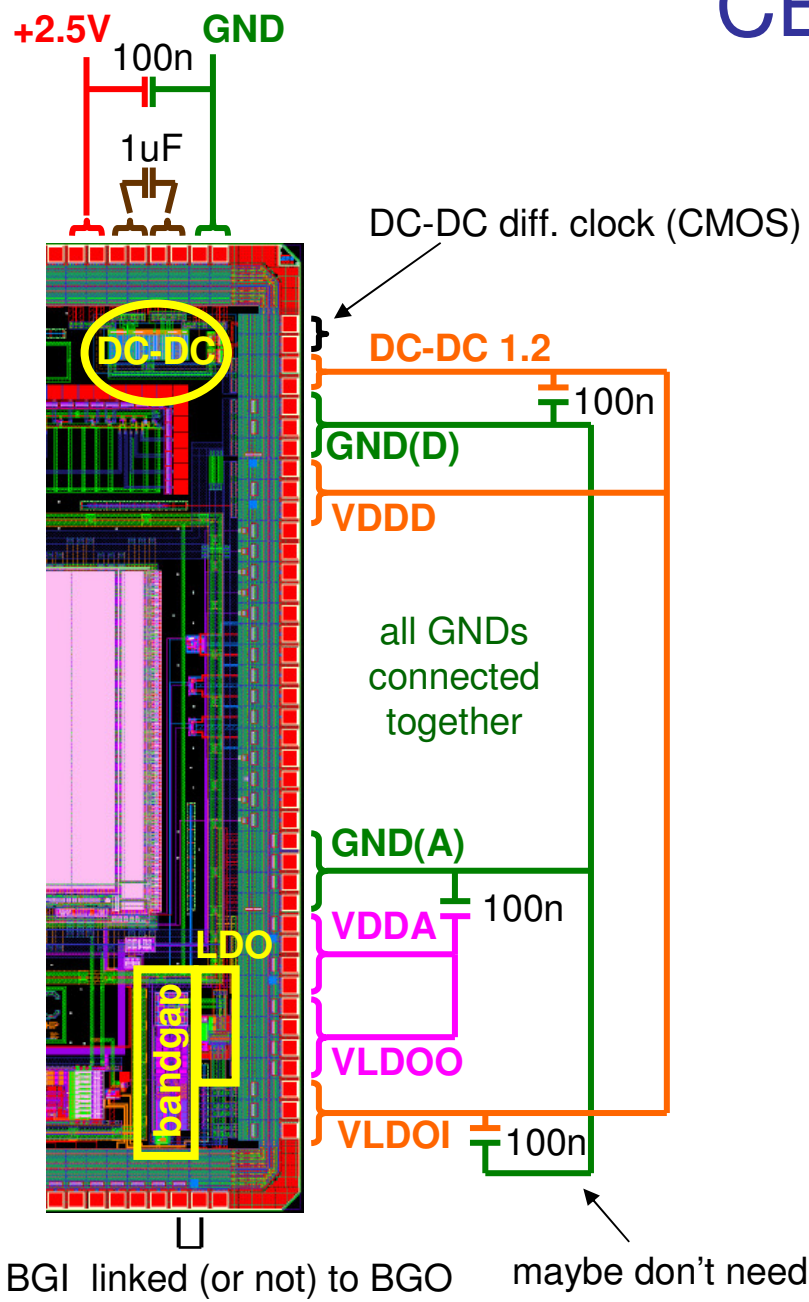



### LDO dropout

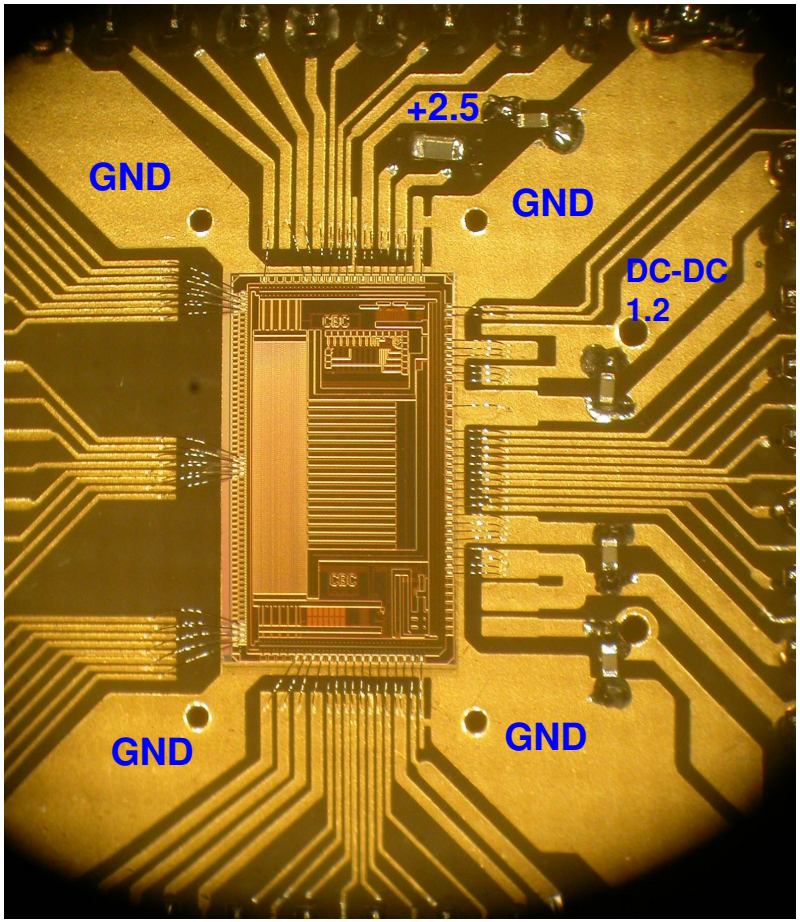


# CBC DC-DC powering option

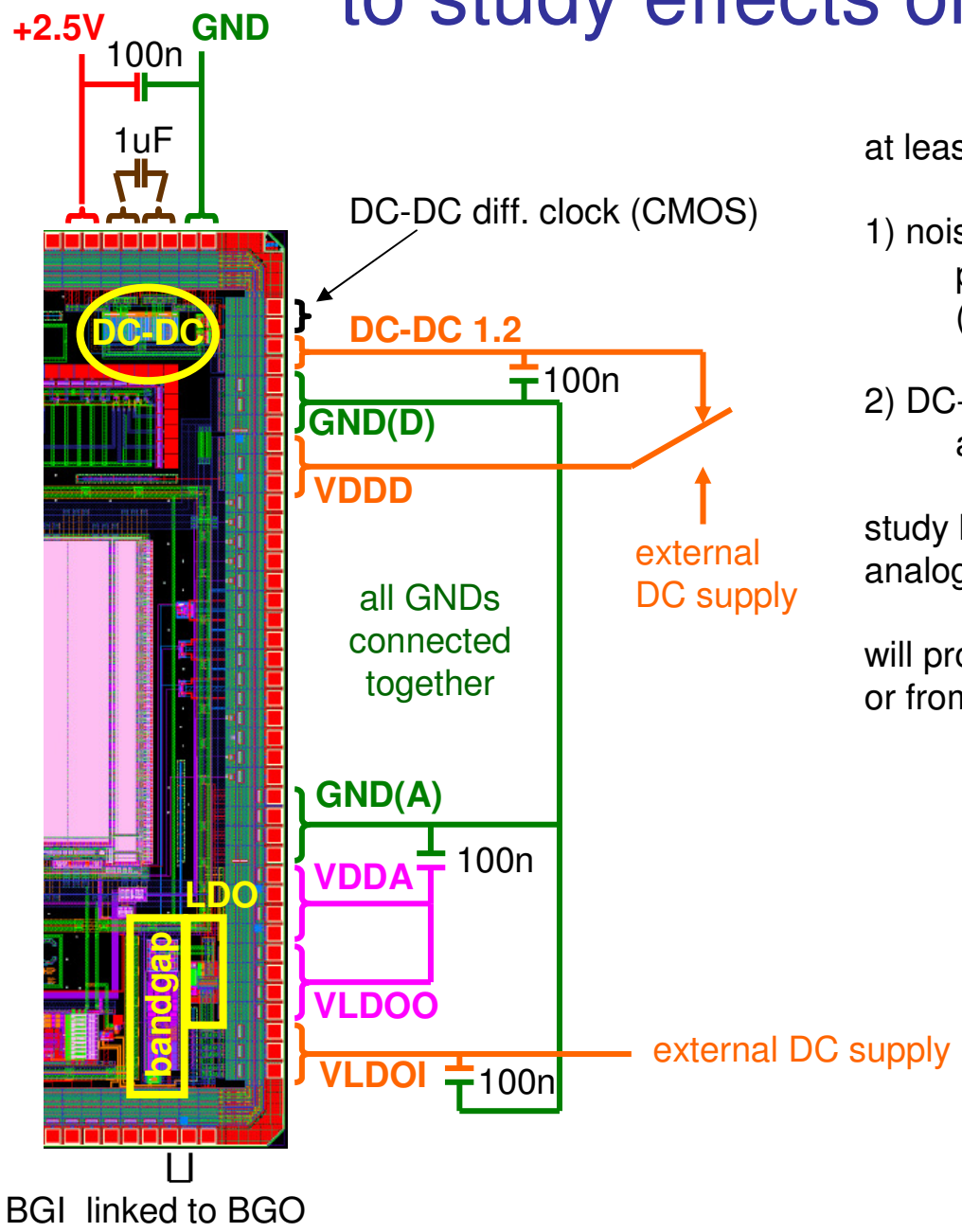
in principle can power CBC from single **+2.5V** supply
1 MHz diff. clock to DC-DC circuit
**DC-DC 1.2V** feeds **VDDD** (dig. supply) and **VLDOI** (LDO I/P)
4 external capacitors minimum
(actually 5 in this picture)




CBC on test board



# to study effects on analog performance




at least 2 possibilities for adverse effects

1) noise on DC-DC O/P rail could affect analogue performance via VDDA rail (though LDO should reject)

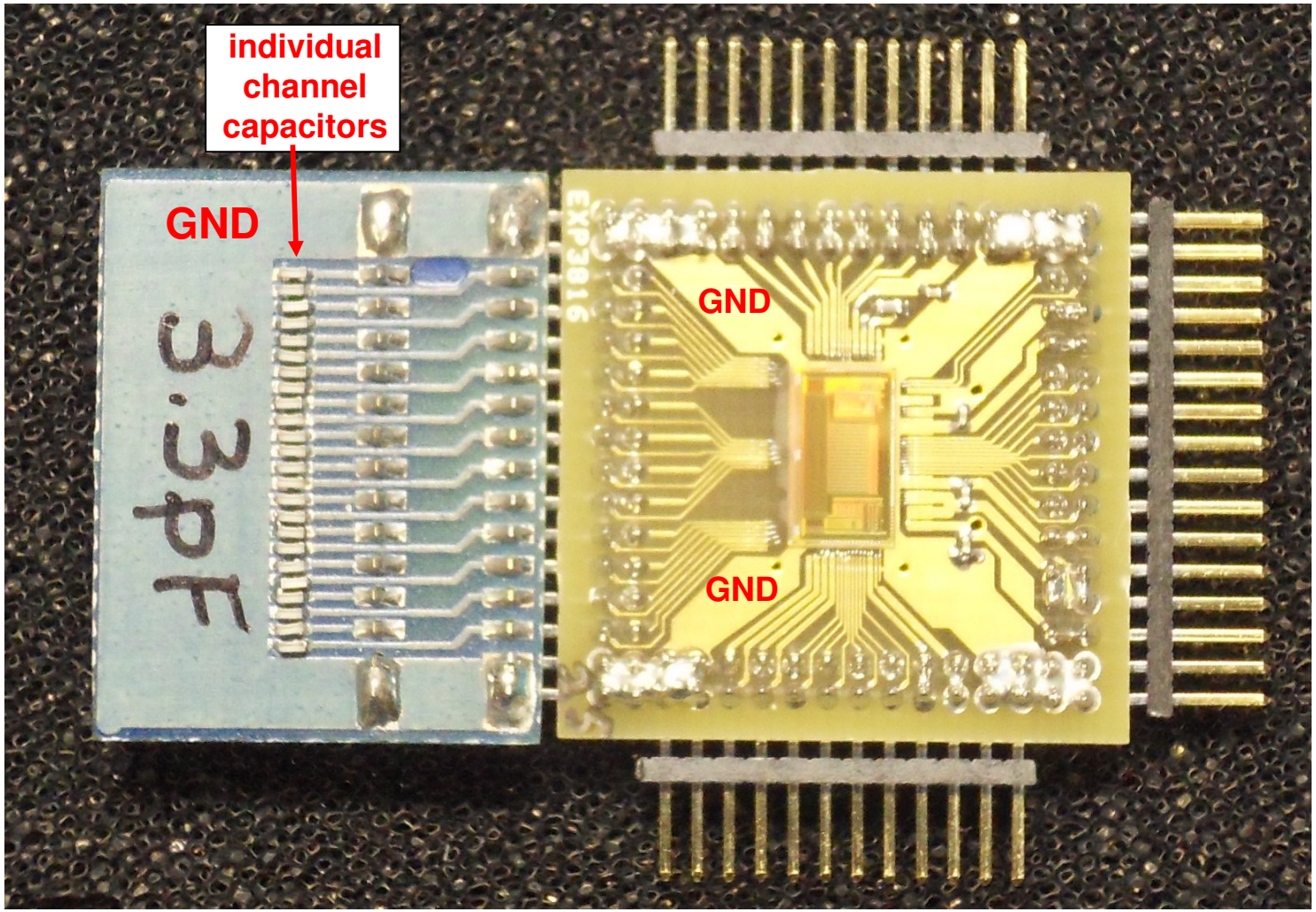
2) DC-DC circuit noise could couple to front end via another path (substrate, GND, ..)

study here concentrates on 2nd path by providing analogue rail from external clean supply

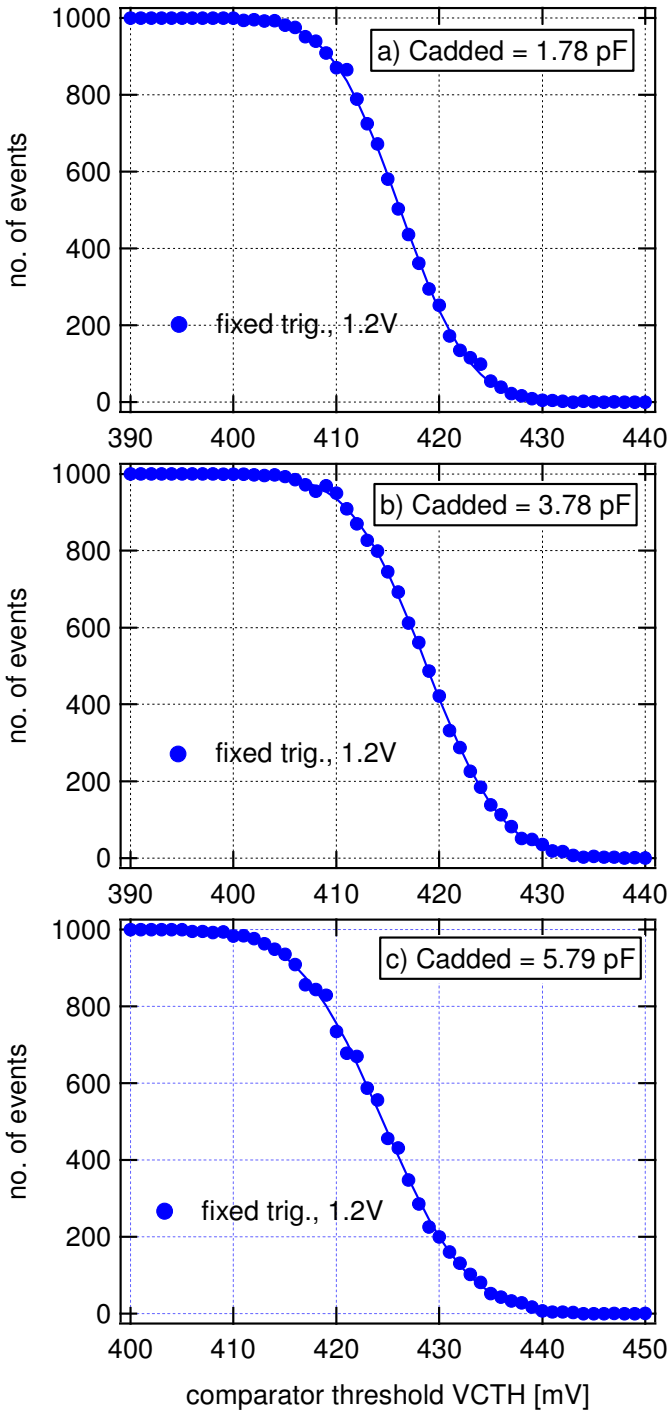
will provide digital rail either from external supply or from DC-DC output

# adding external capacitance

want to measure noise (from s-curves) dependence on external capacitance
plug-on boards containing arrays of capacitors connect to bonded out channels
acquire s-curve for one of the bonded out channels



# s-curves:reference measurement




measure s-curves for single channel for different external capacitances

**conditions for measurements on <u>this</u> slide**

digital circuitry supplied with external 1.2 V supply

**DC-DC not running**

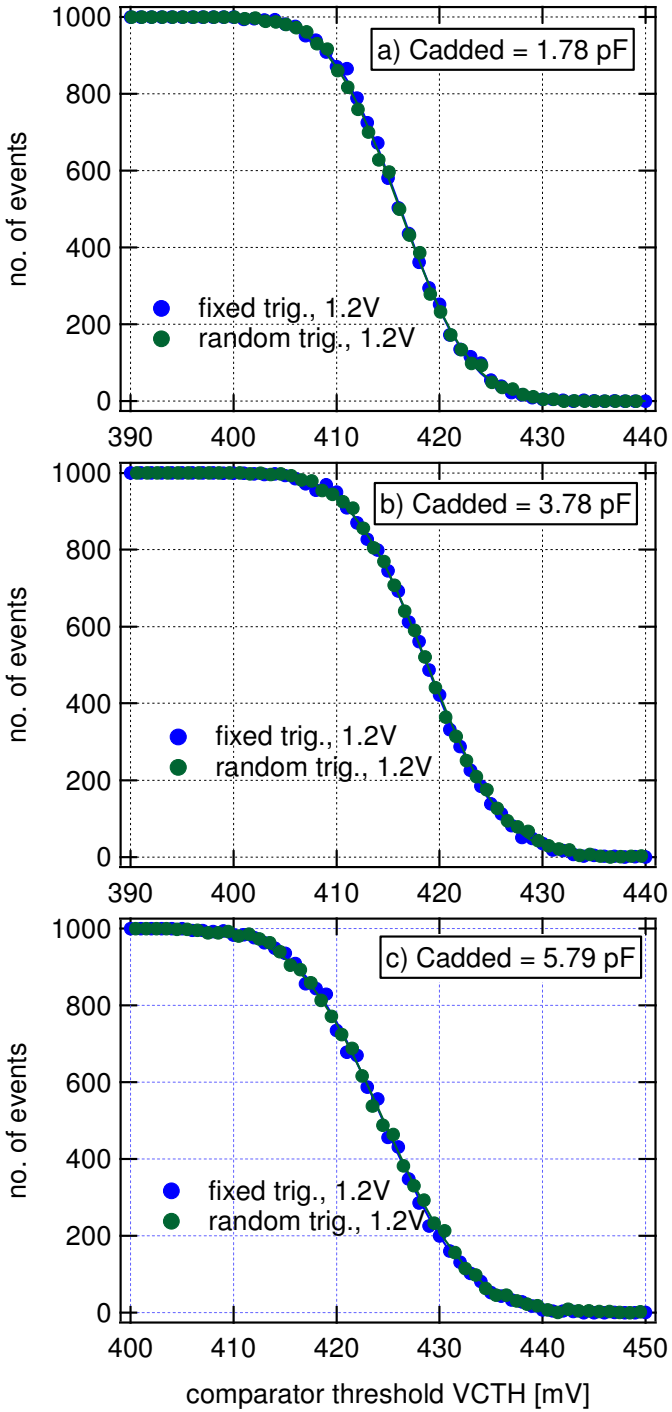
CBC triggered at fixed time following a fast reset

=> always triggering same pipeline location

gives cleanest possible measurement as reference

(no reason to expect any effect from random triggering, but just to check)

# s-curves: DC supply (random trigger)




now repeat for random triggering

digital circuitry still supplied with external 1.2V supply

**DC-DC still not running**

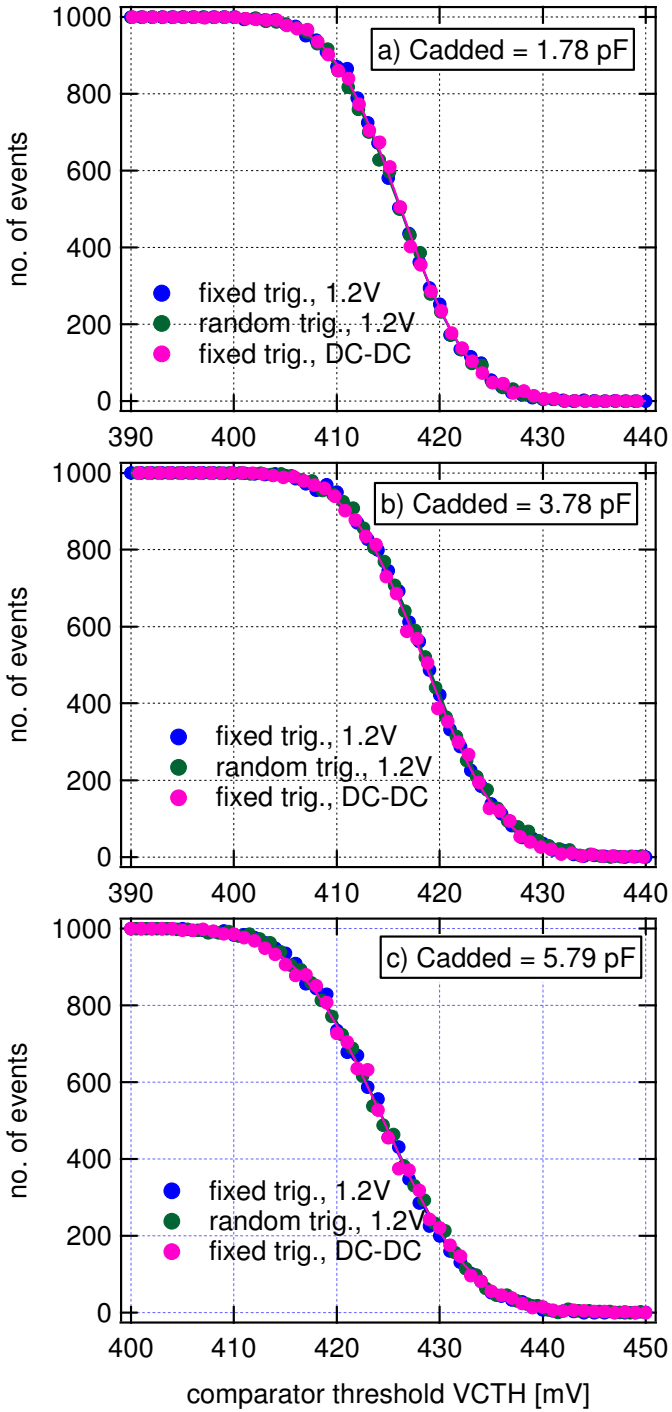
**but fast reset removed**

pseudo-random trigger, so now triggering locations throughout pipeline

no effect on s-curves visible (i.e. no effect on noise)

(as expected)

# s-curves: DC-DC running (fixed trigger time)




now feed digital circuitry with DC-DC 1.2 V

**DC-DC now running**

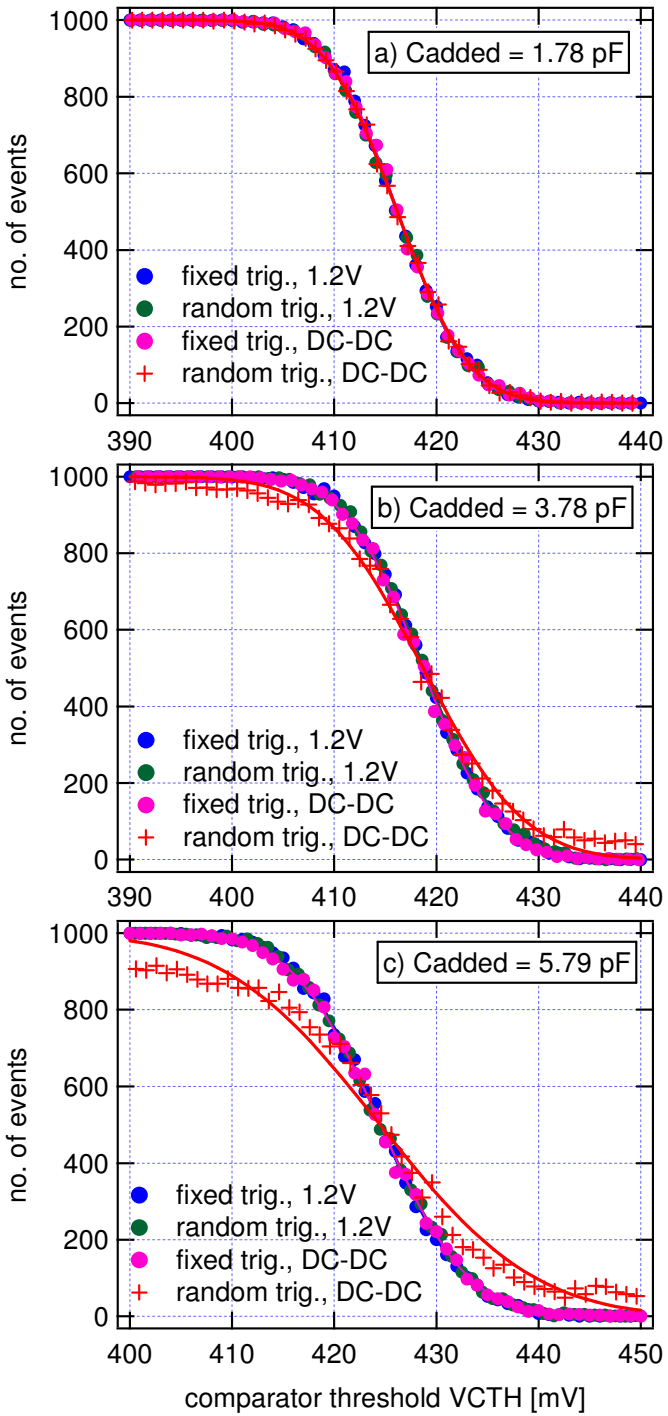
return to triggering at fixed time following a fast reset

DC-DC clocked at 1 MHz
with fixed phase relationship to fast reset

once again - no significant effect on s-curves

=> **DC-DC circuit doesn't affect intrinsic noise**

# s-curves: DC-DC running (random trigger)




now try pseudo-random triggering again

**DC-DC still running**

s-curves now distorted for larger capacitance

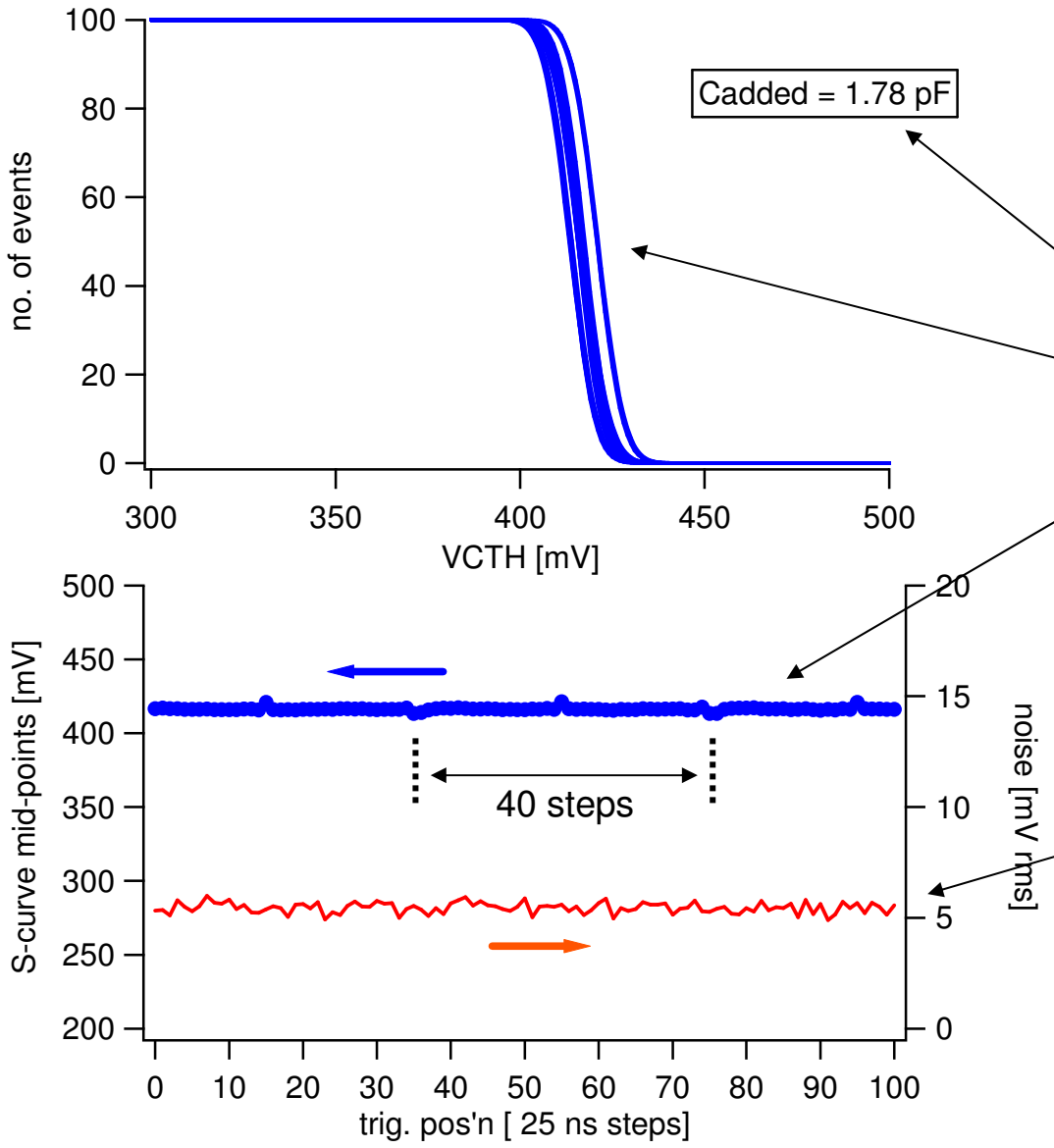
=> something to do with random triggering when DC-DC circuit operating

an effect associated with specific pipeline locations?

try to understand what's going on with a more systematic study

=> look at s-curve dependence on triggered pipeline location

# s-curve dependence on triggered pipeline loc'n




acquire s-curves with increasing separation between fast reset time and trigger position (25 nsec steps)

DC-DC circuit operating

results here for smallest capacitance:

not all s-curves in same position

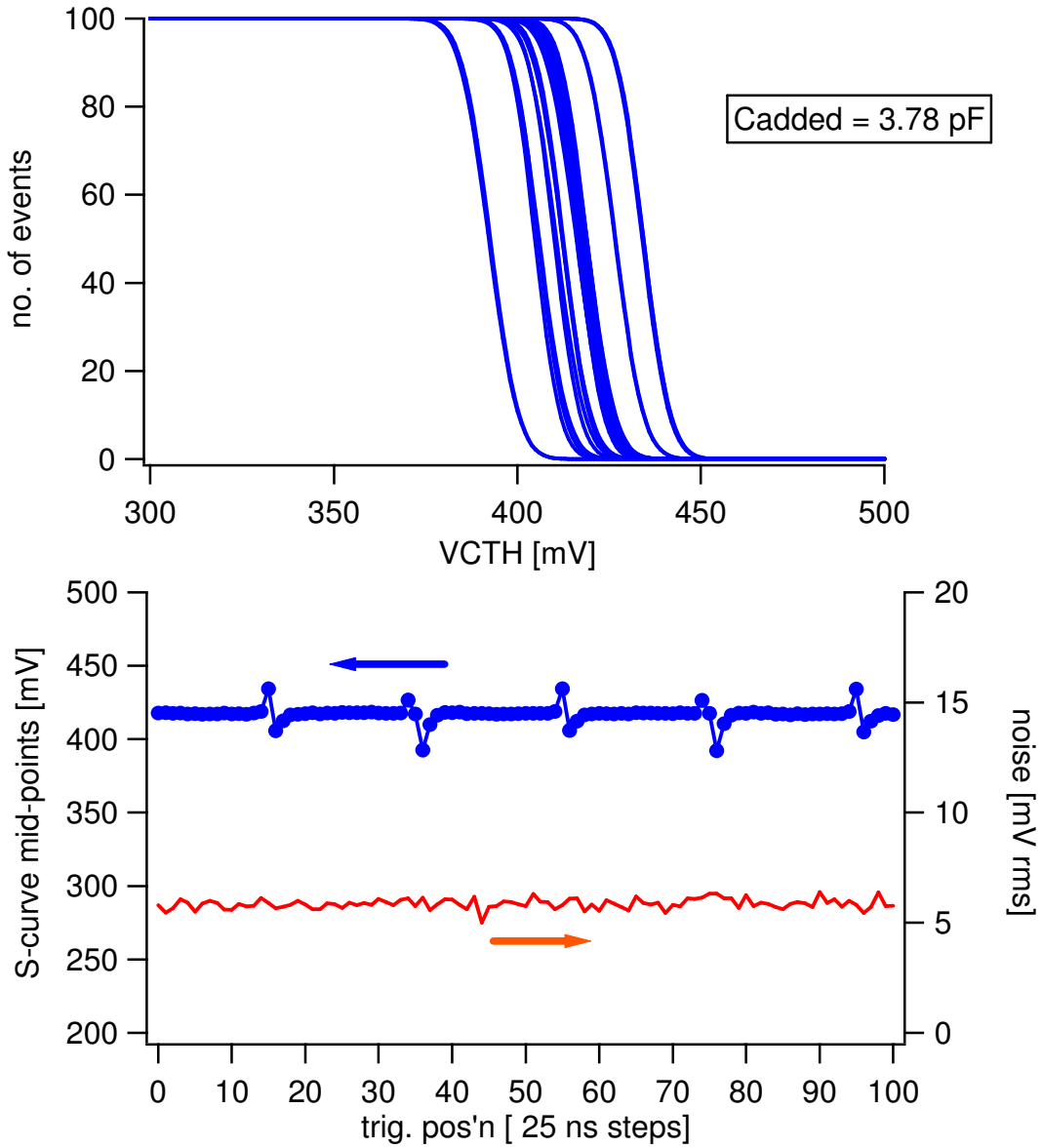
plotting s-curve mid-point vs vs. trigger position shows repetitive structure

separation between positive (or negative) shifts = 40 steps = 1 μsec = DC-DC period

pedestal shift only, no change in shape

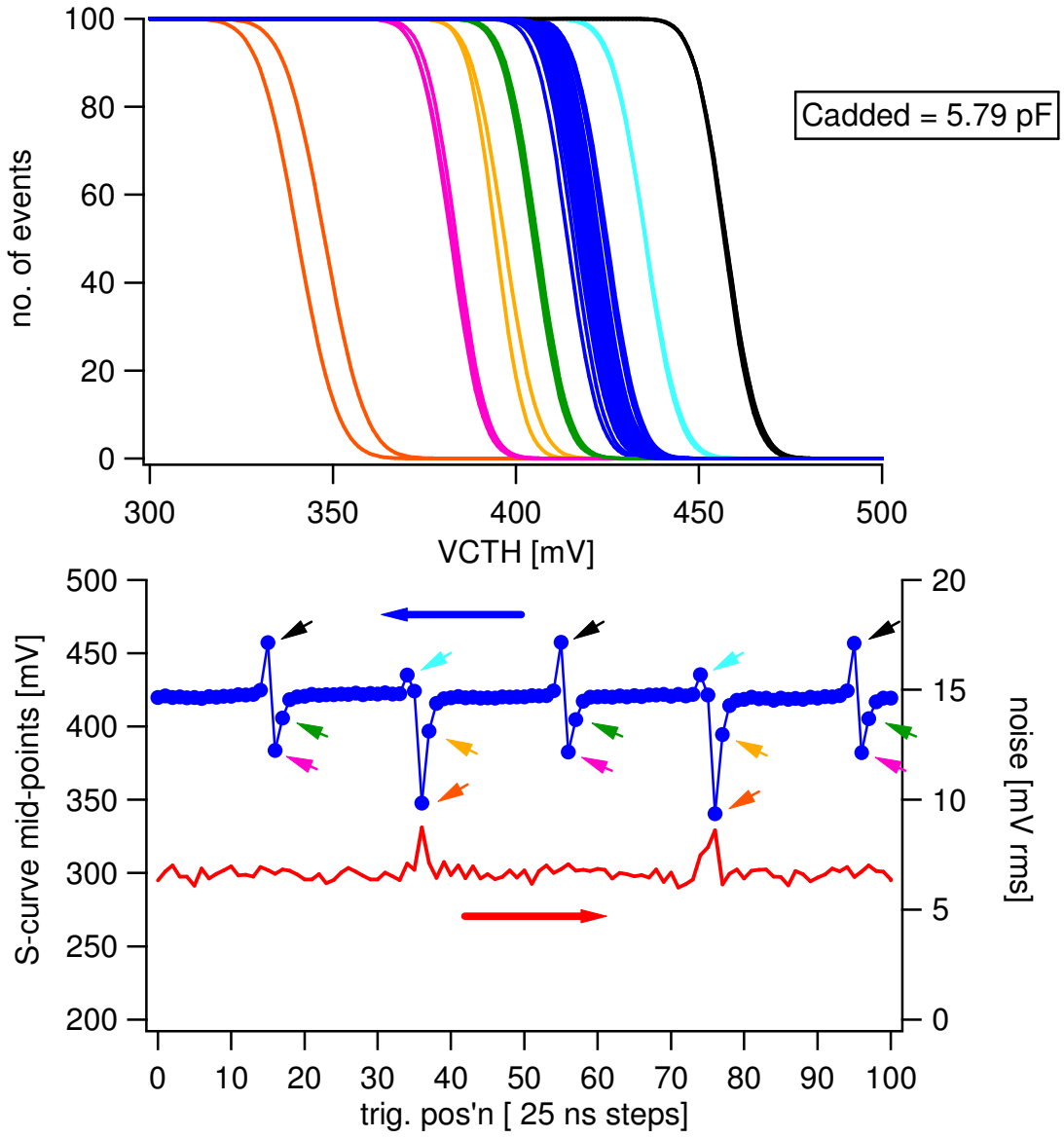
=> intrinsic noise unaffected

# increasing external capacitance




effect becomes much more noticeable

# for largest external capacitance



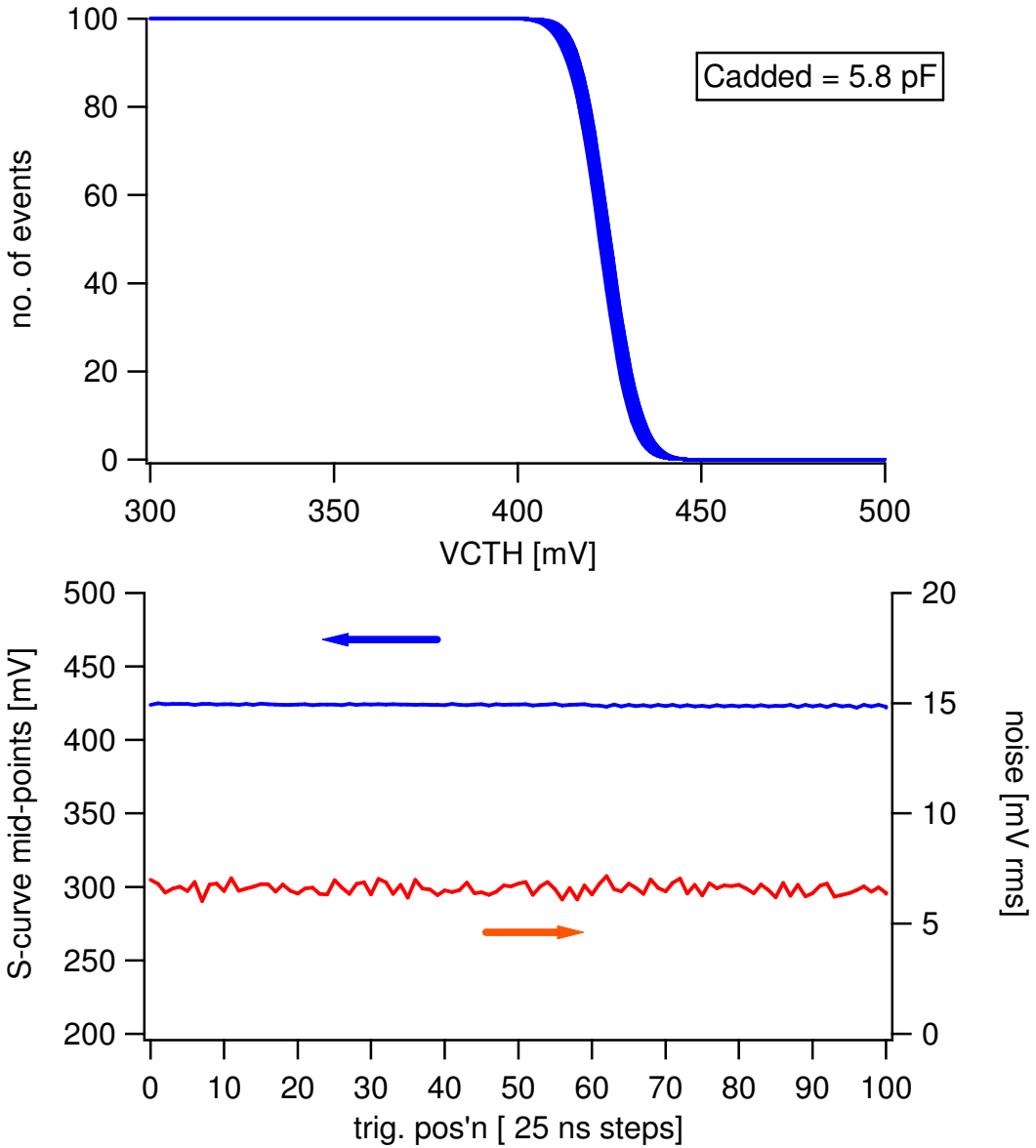

s-curves in top plot colour coded to show which ones correspond to which point in bottom plot

some distortion visible for most negatively shifted curves (out of amplifier linear range)

so DC-DC circuit operation somehow affects channel pedestal

magnitude of effect proportional to external capacitance to ground

# repeat for external DC supplies



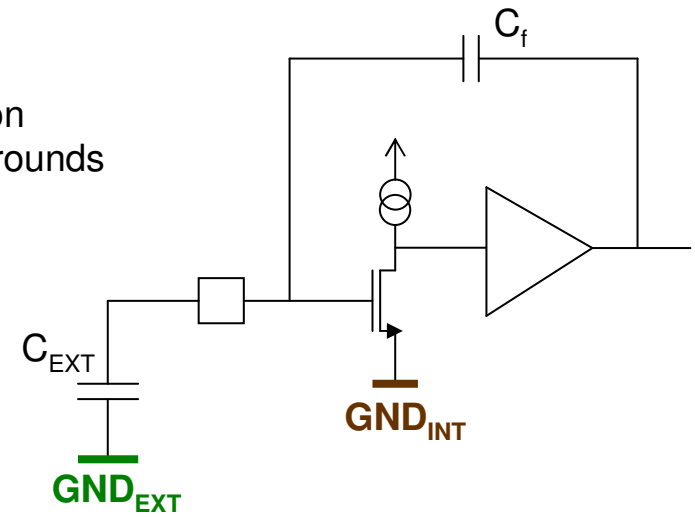

just to check

effect goes away completely if DC-DC circuit not operational

# what's going on?

behaviour most likely due to DC-DC circuit operation
causing difference between internal and external grounds

would result in spurious charge injection
proportional to $C_{EXT}$




**can anything be done to improve situation?**

better connection between $GND_{INT}$ and $GND_{EXT}$ ?

ultimately limited by bond wires

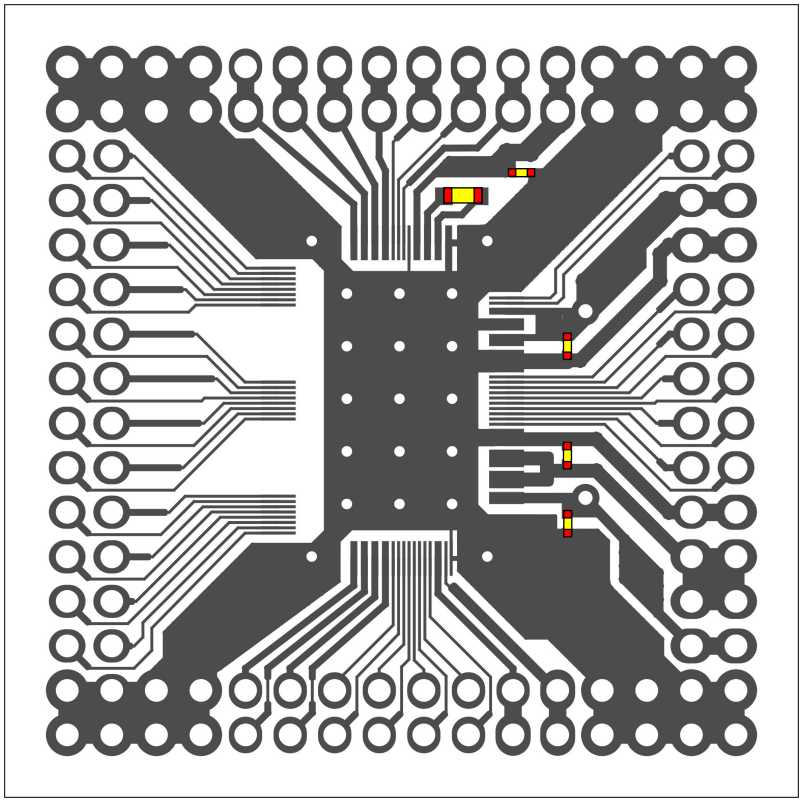
**is present test setup optimal?**

have tried to improve following discussions with CERN engineers

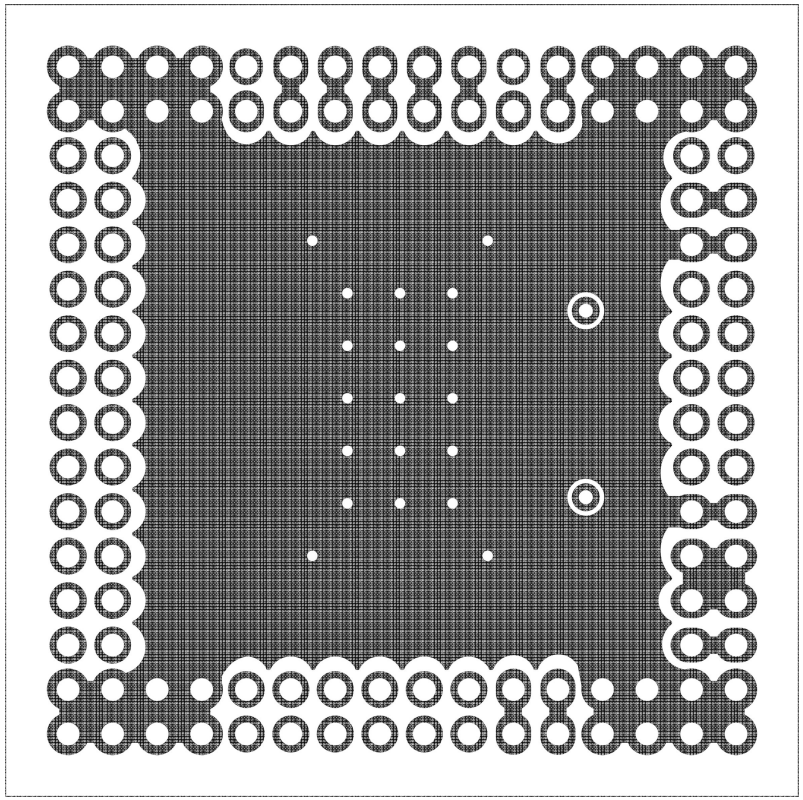
start by taking a critical look at CBC test board

# CBC test board copper layout

top

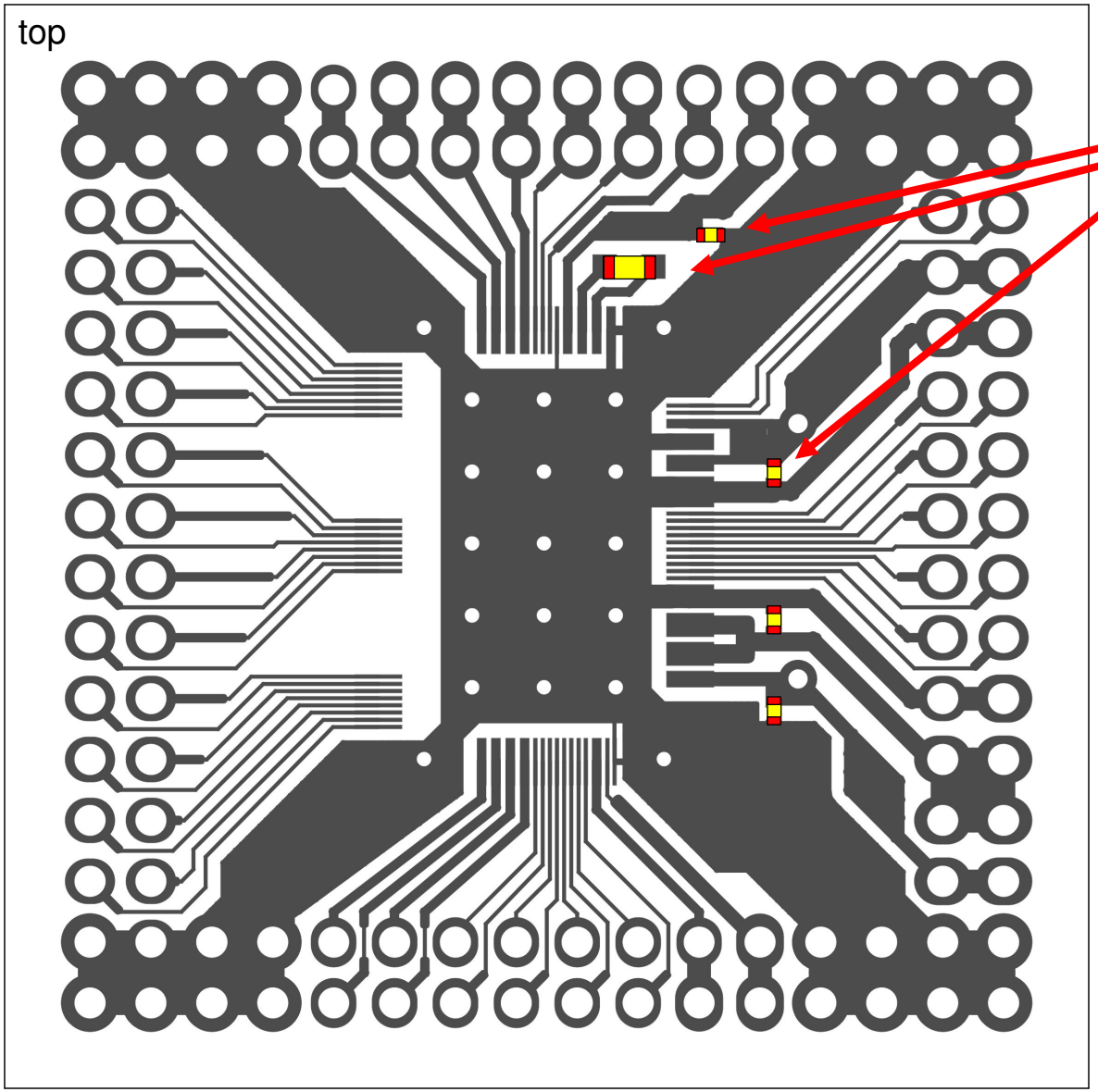


bottom



double-sided pcb
~ solid ground on bottom surface connected (PTH) to ground on top surface
CBC glued on the centre ground area
ground brought out from under chip to bond pads

# possible deficiencies



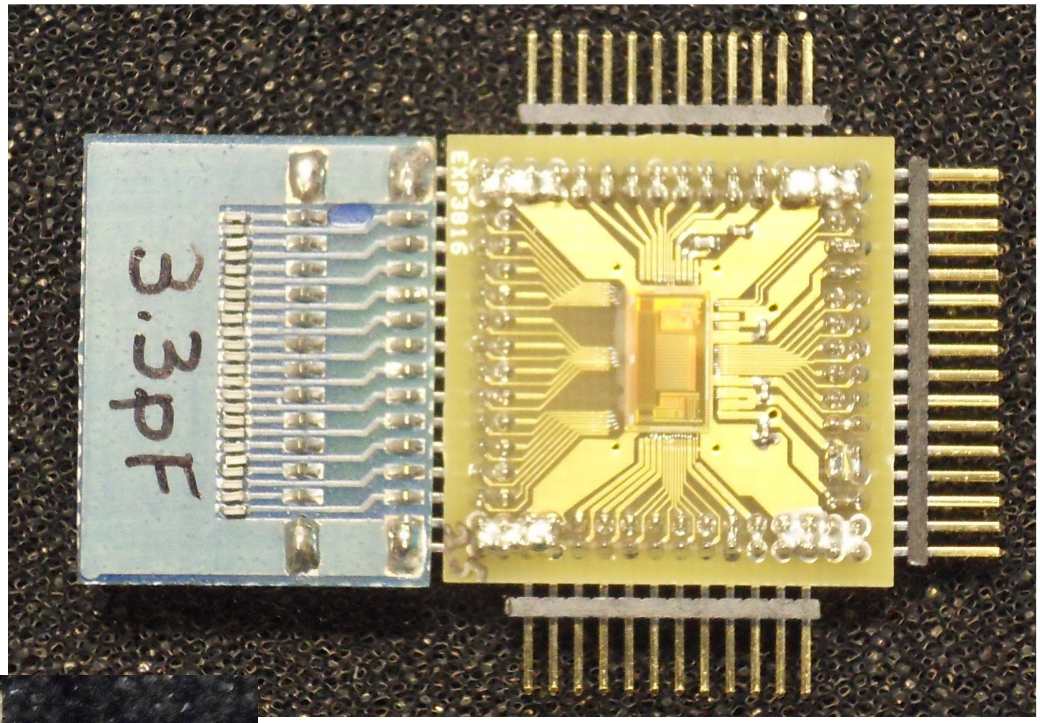

too cautious about keeping bonding area clear - capacitors could have been positioned closer to chip

could have put more plated through holes in

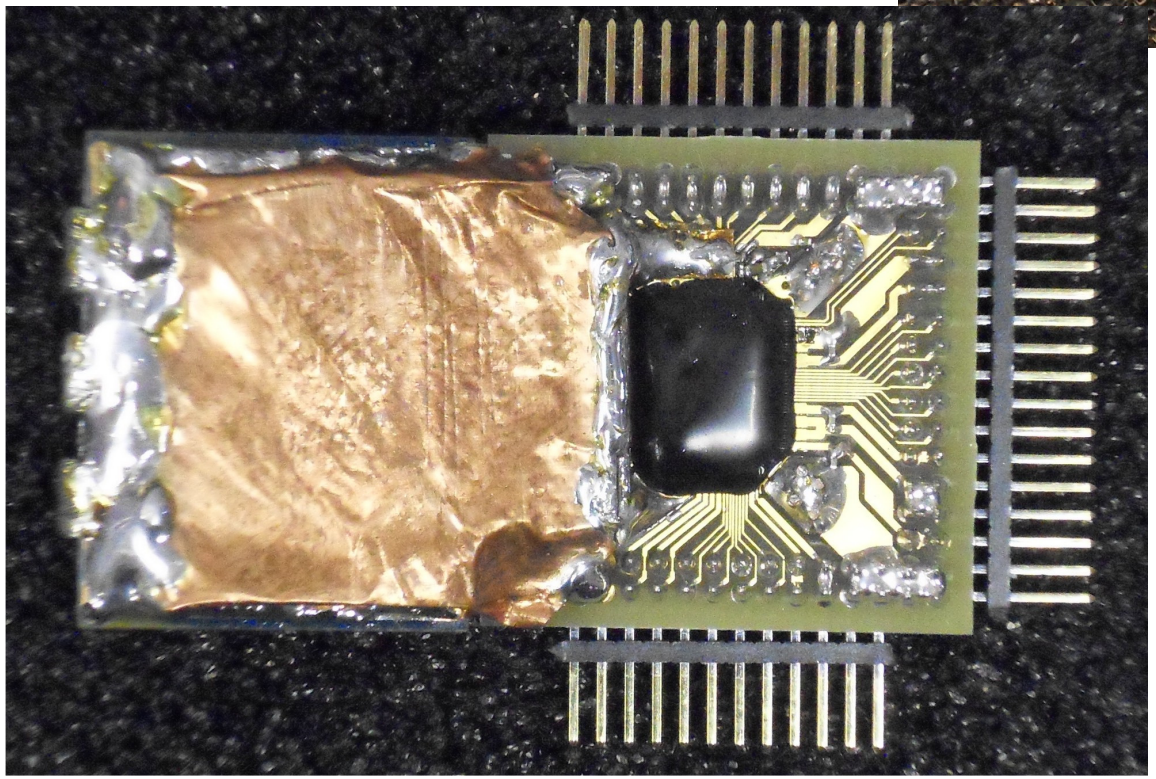
have tried to “make improvements” to existing board to see whether performance is affected

# “improvements”

have tried to improve grounding and decoupling by turning this →



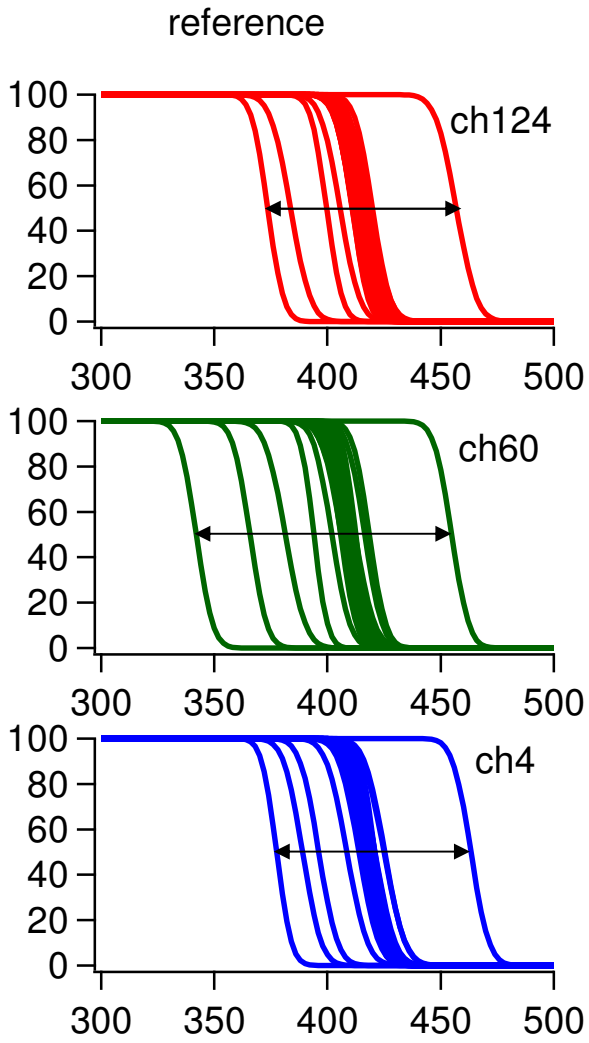

into this ↓



← this is the final version of the test board after all modifications

will go through modifications step-by-step for clarity - describing changes and showing resulting effects on s-curves

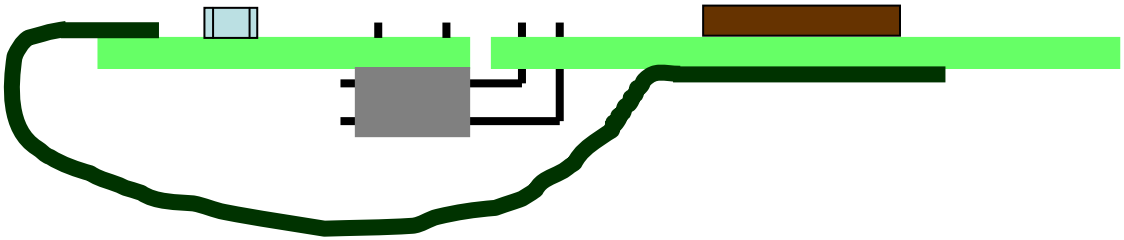
# first take reference measurement




measure s-curves as before for 3.8 pF added external cap.

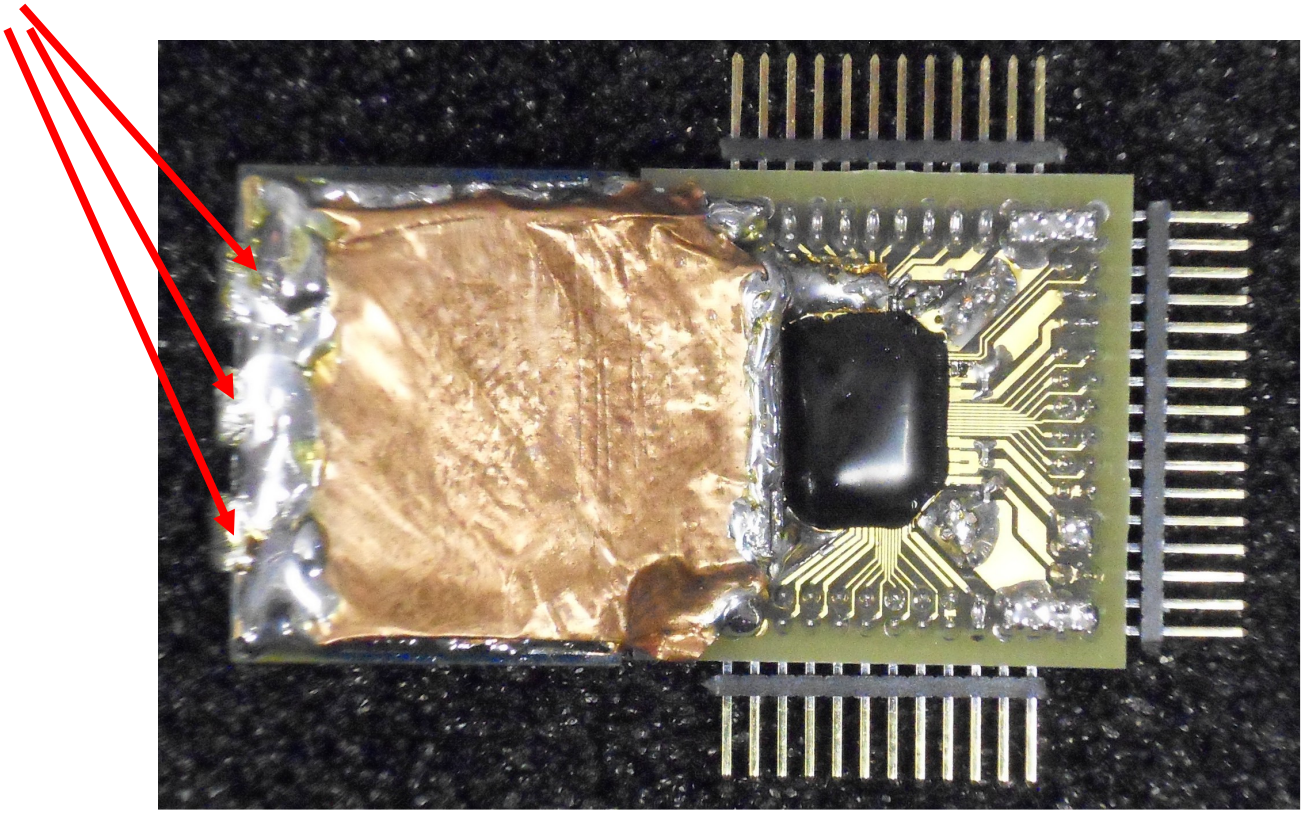
look at 3 channels at top, middle and bottom of chip

# improved ground coupling between CBC and external capacitor board

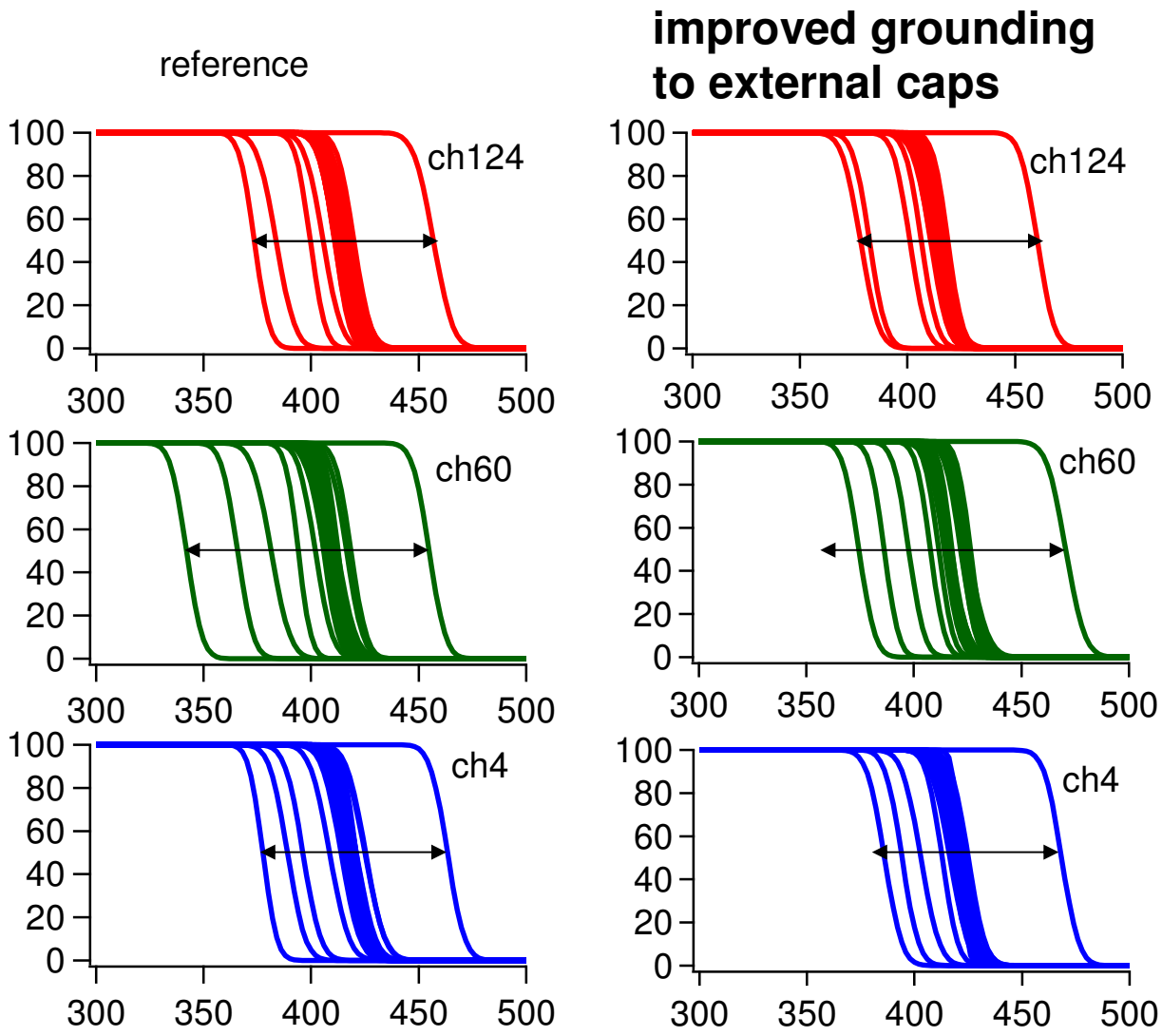


three lengths of tinned copper braid soldered to ground plane on back of CBC board

connected to ground area on external capacitor board

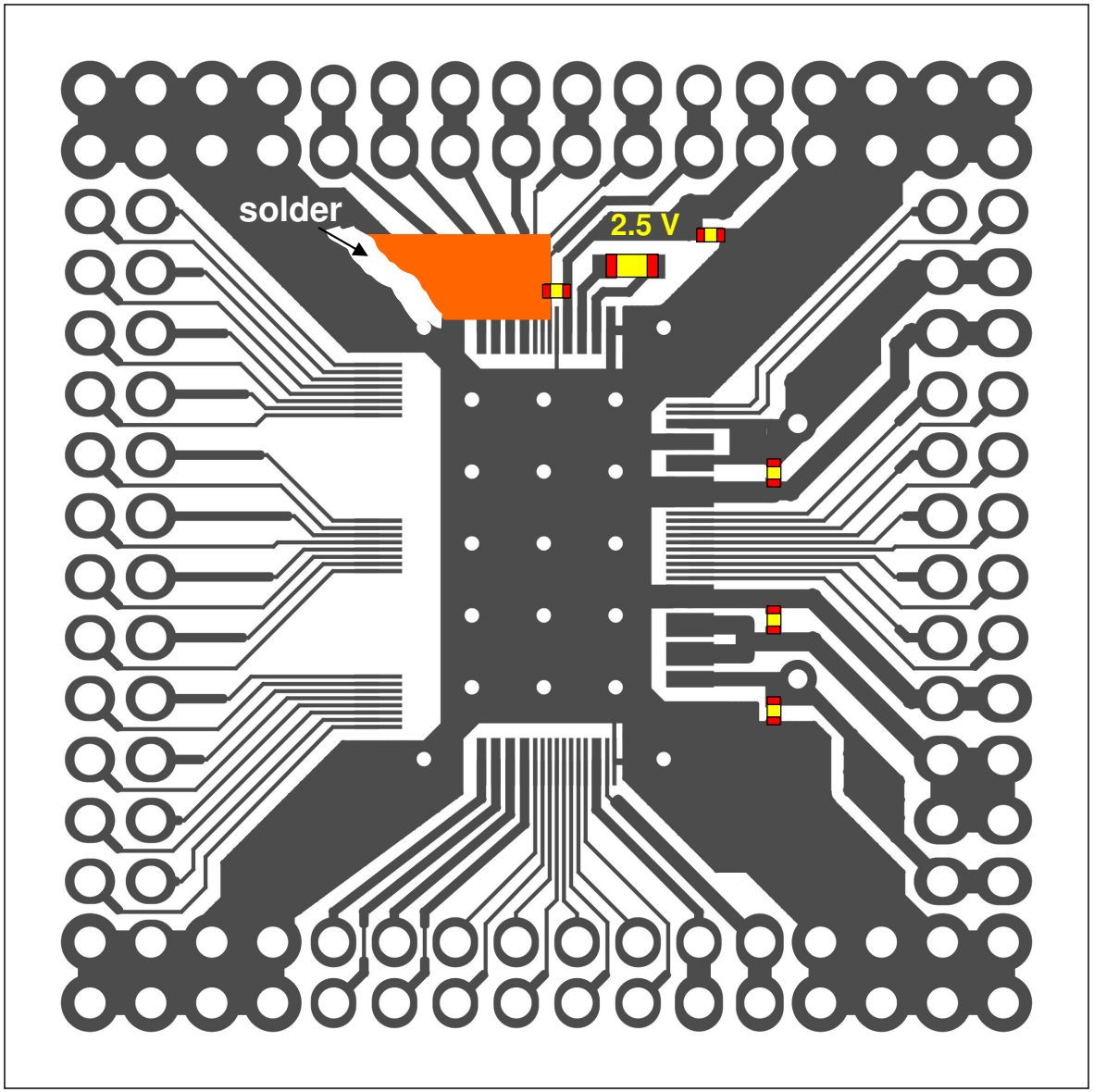


# effect of improved grounding




some differences - most noticeable for channel 60

# improved 2.5 V rail decoupling

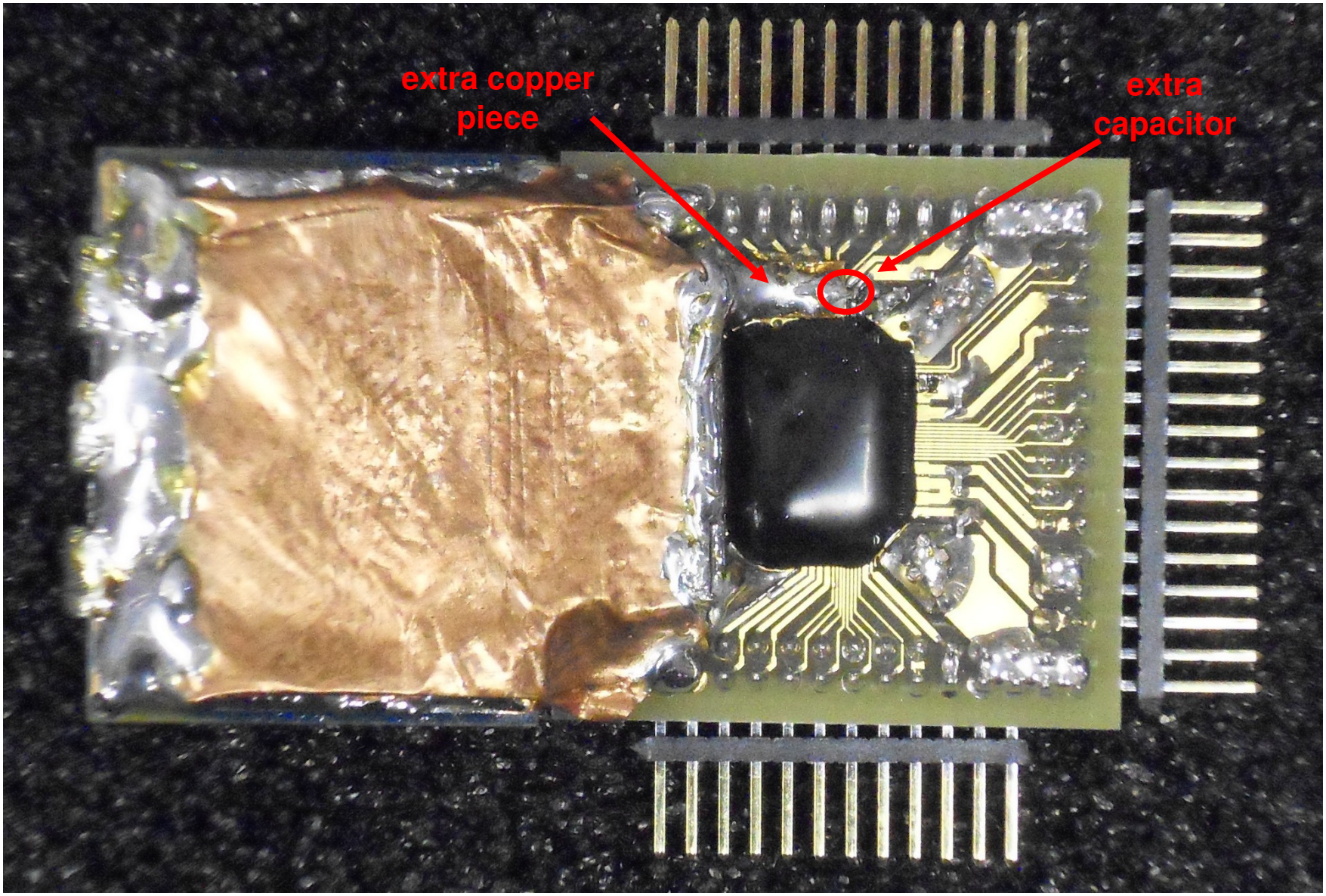



**2.5V decoupled closer to the chip**

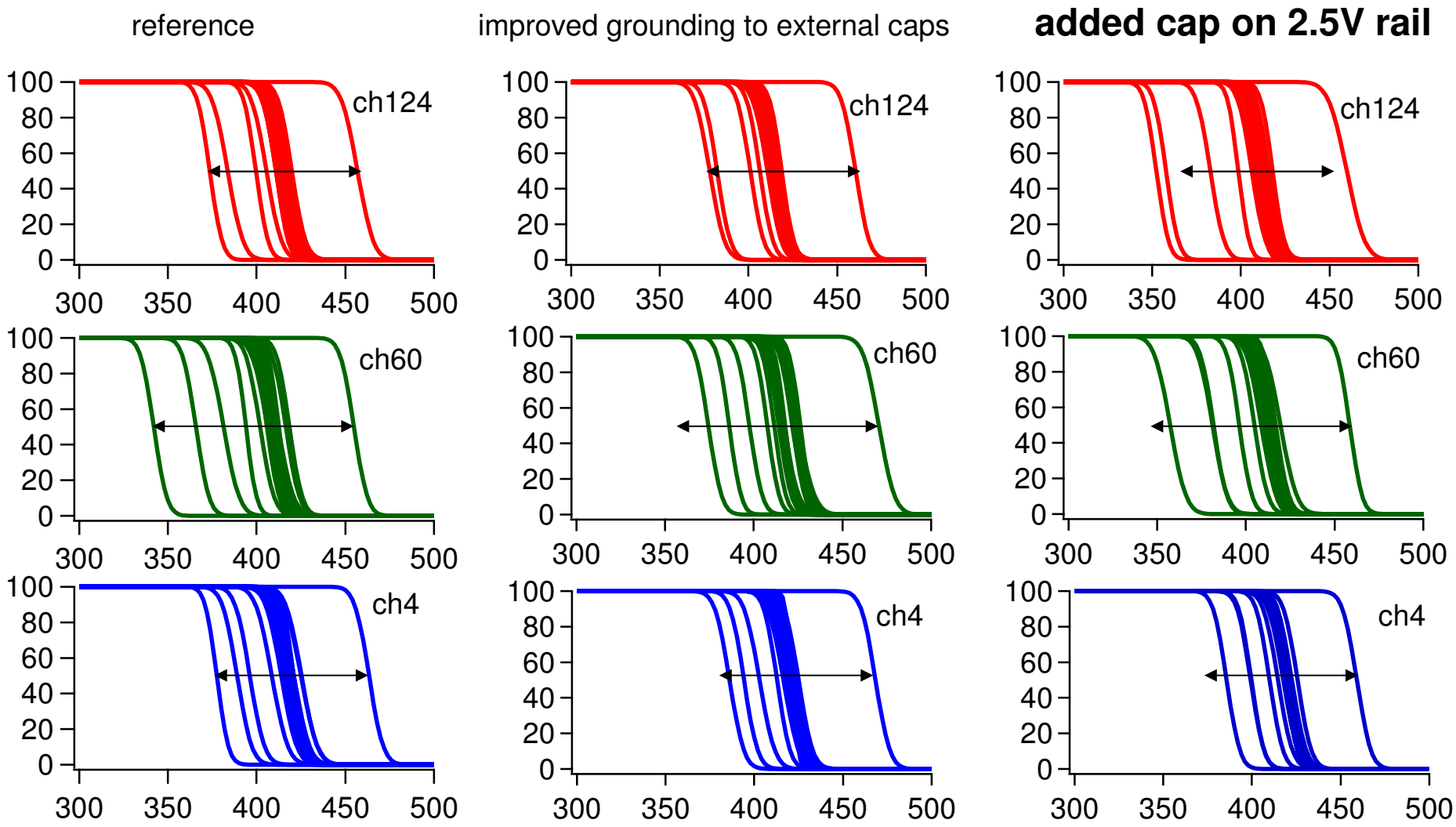
extra copper piece added adjacent to 2.5 V input, soldered to ground

additional 100 nF capacitor soldered as close as possible to bond pad

# improved 2.5 V rail decoupling - reality

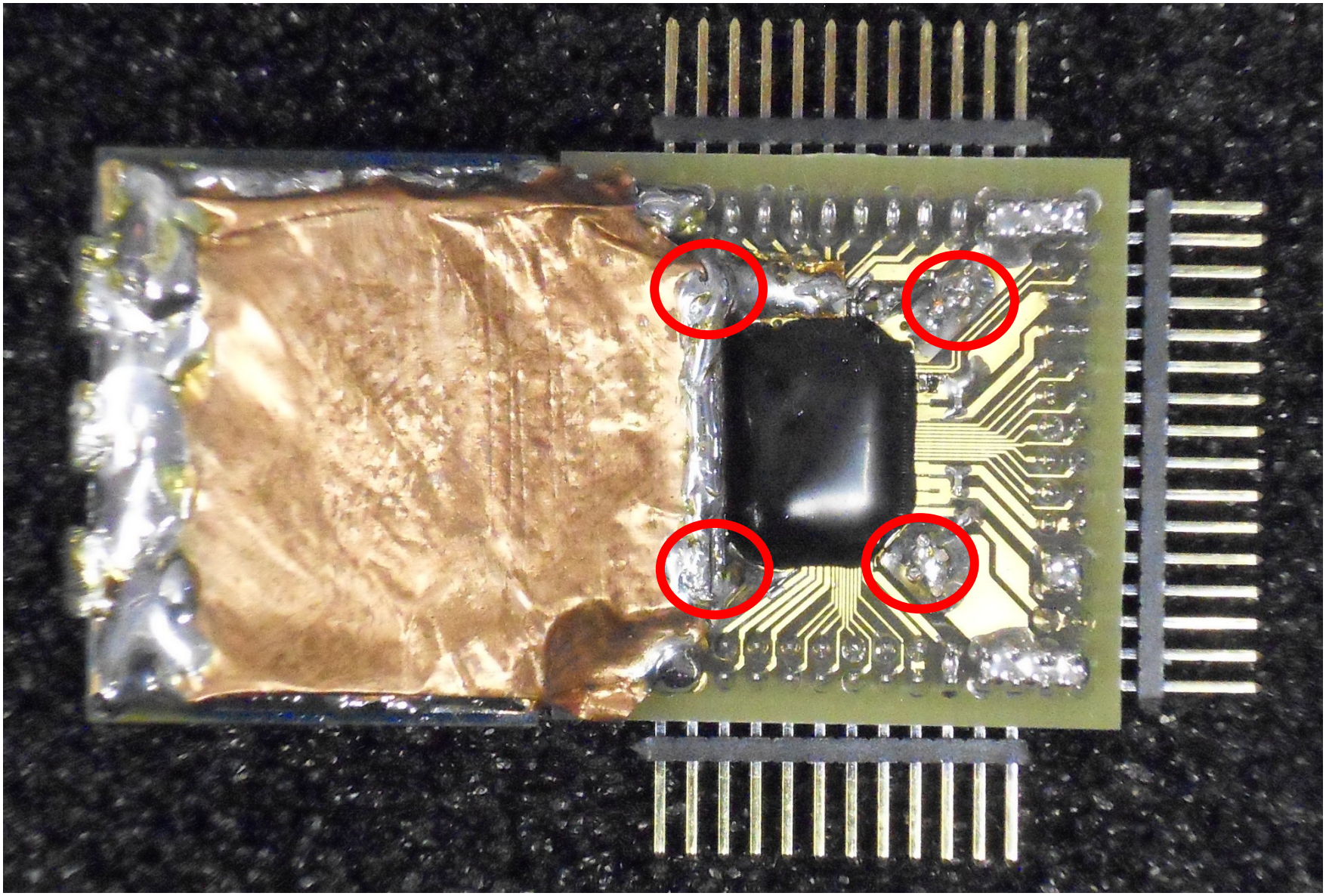


# effect of improved 2.5 V decoupling

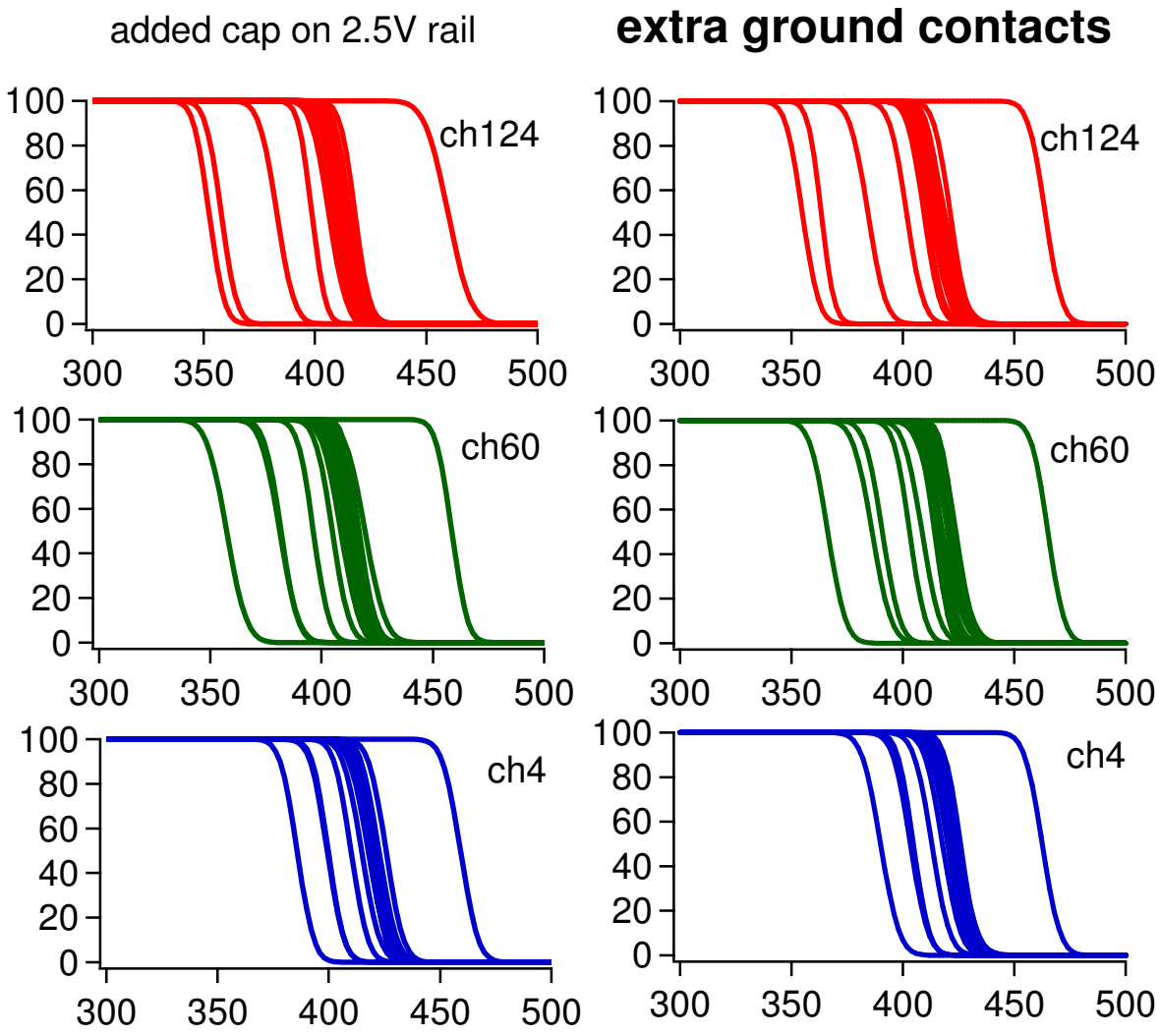



ch124 gets appears to get worse, ch 4 gets better

# extra ground contacts

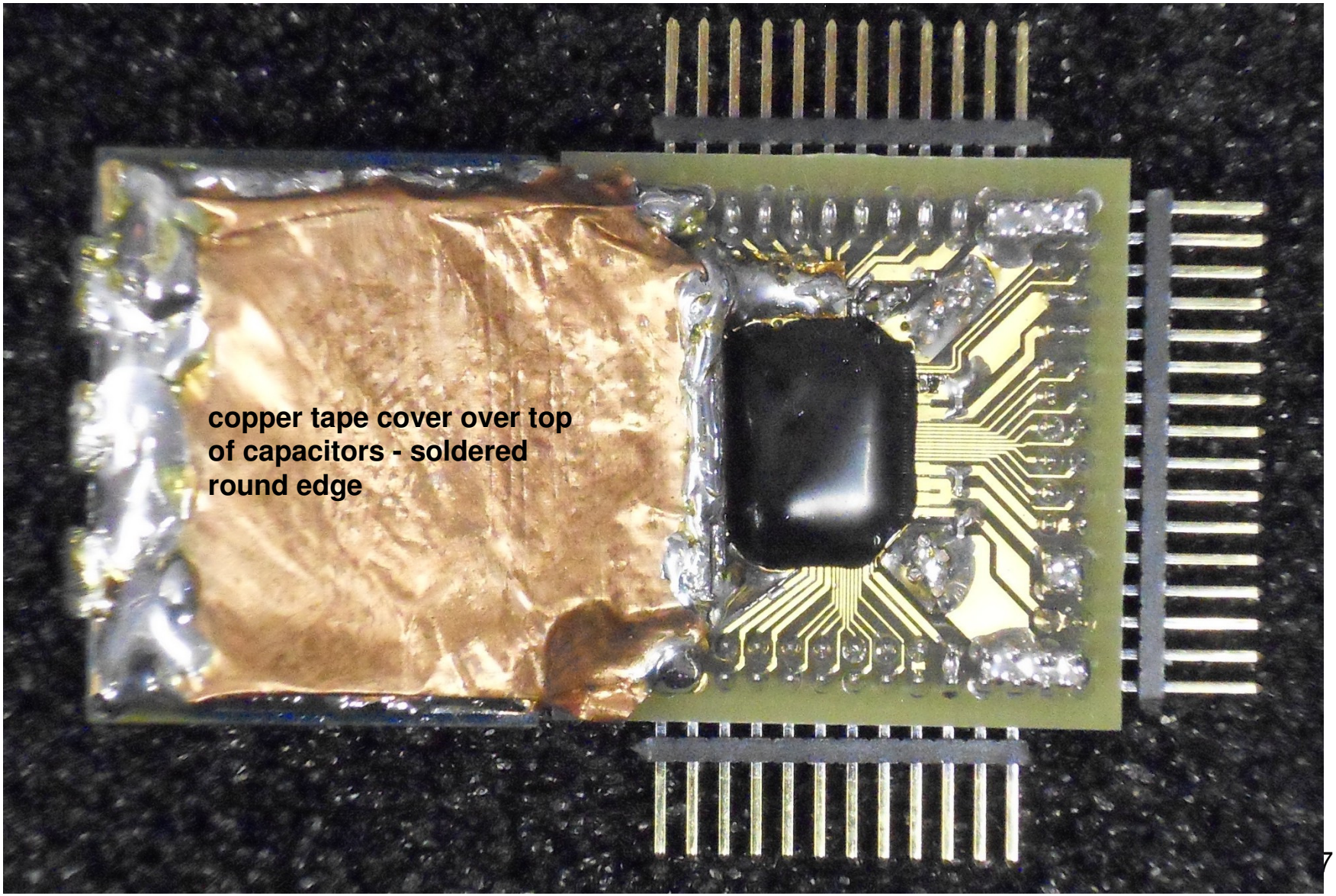


# effect of extra ground contacts

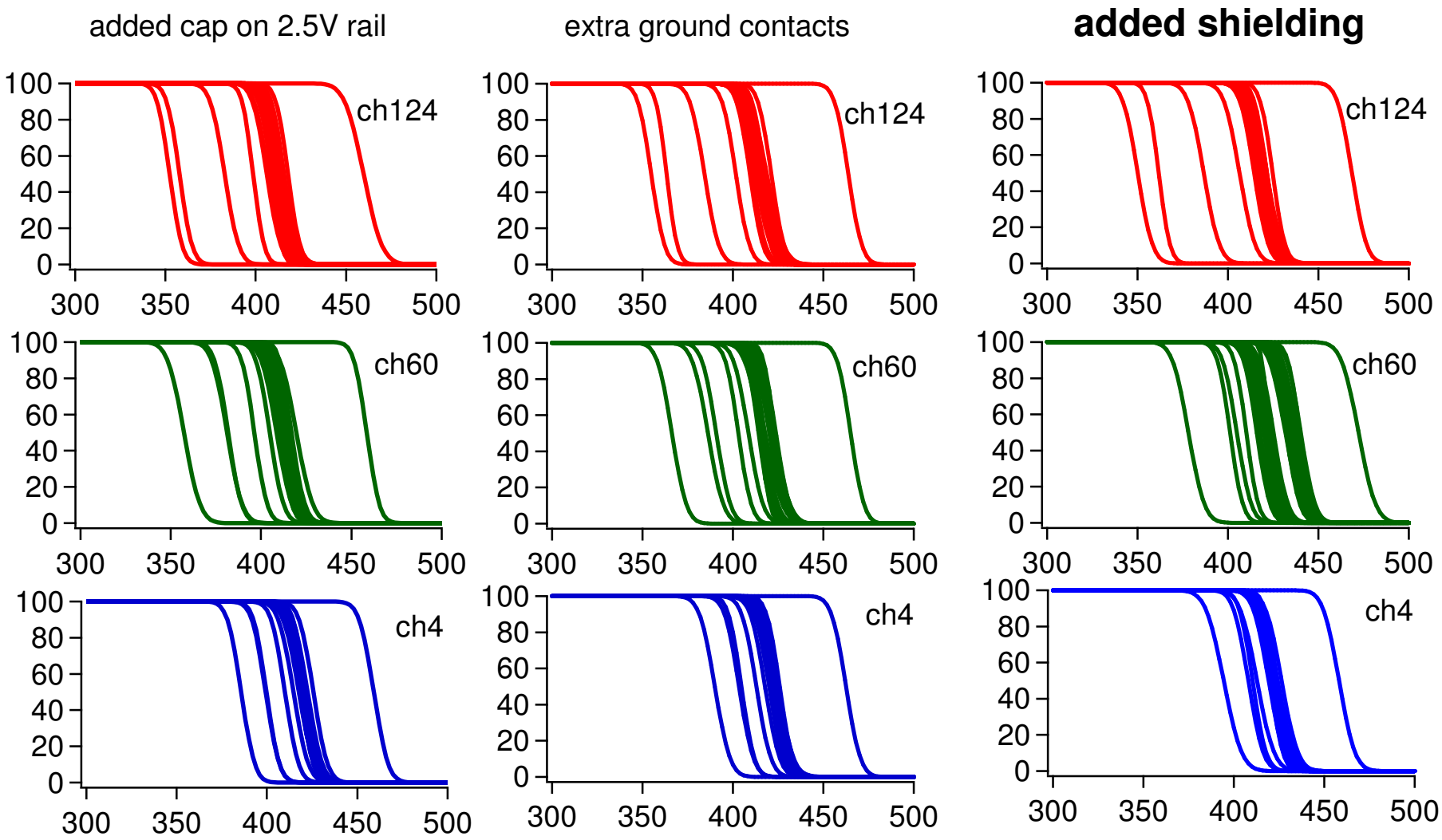



not much difference

# additional shielding

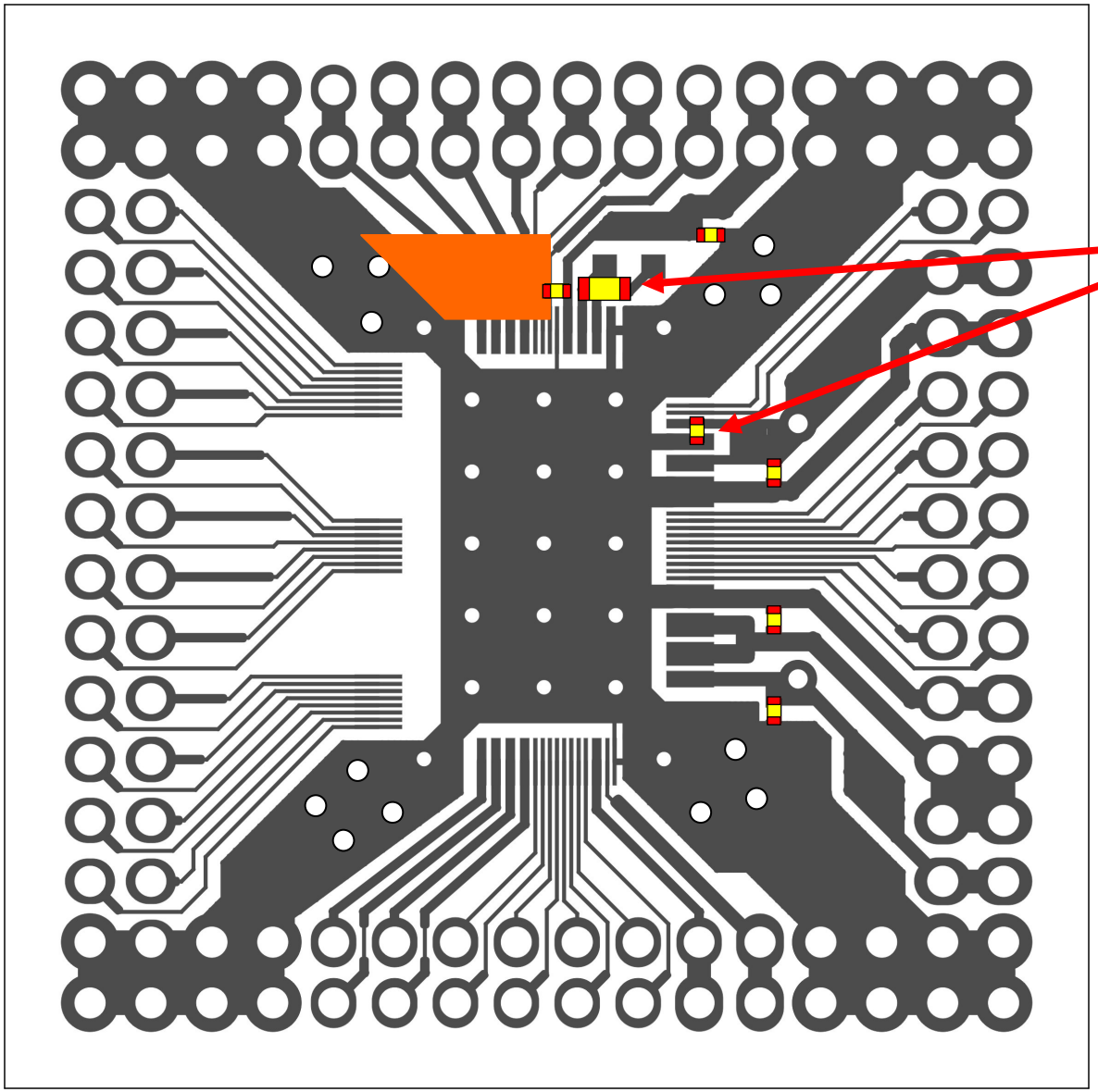


# efect of additional shielding



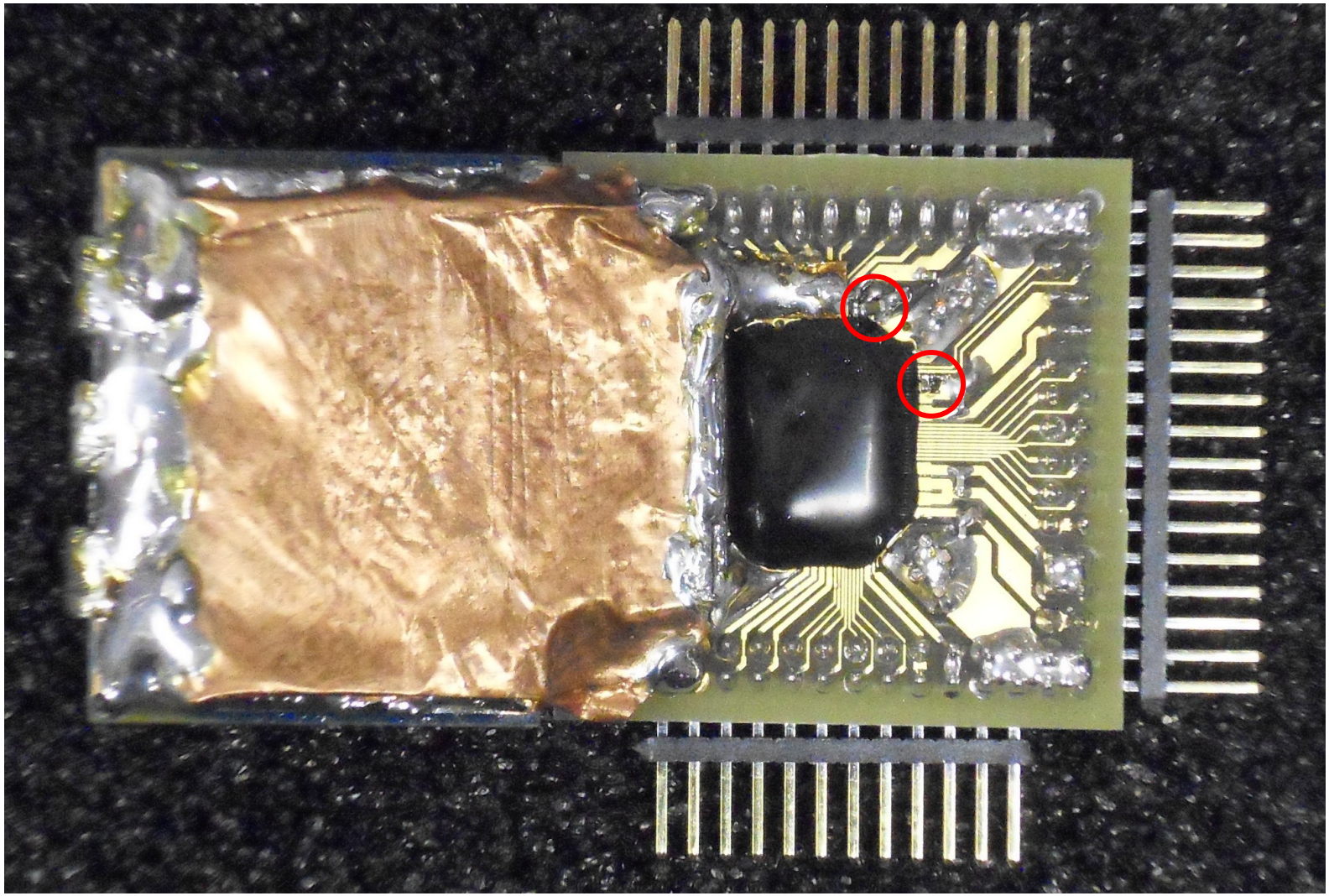

channel 60 now looks a bit strange

# some more capacitor repositioning

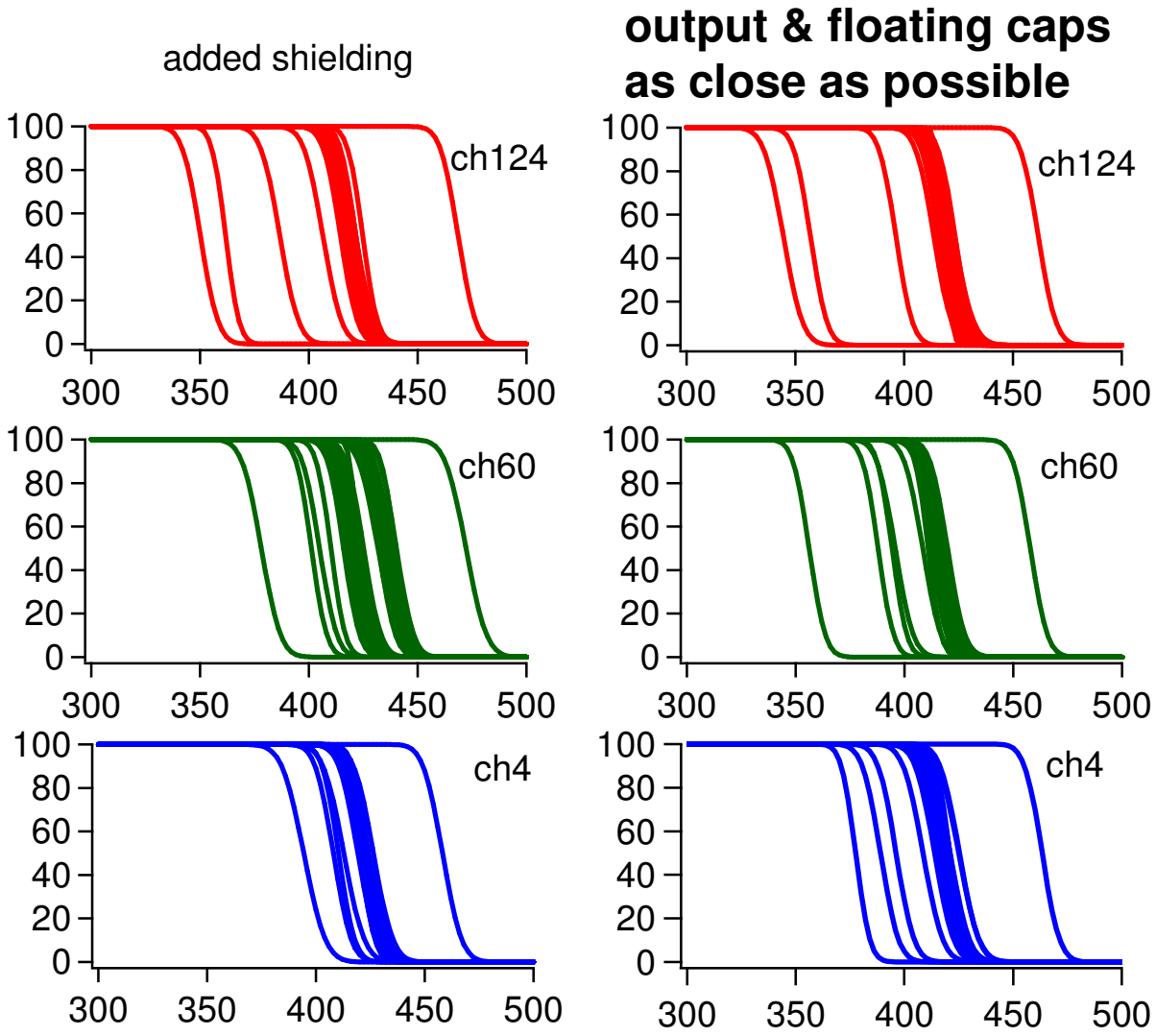


DC-DC output decoupling & floating capacitor as close as possible to chip

# some more capacitor repositioning

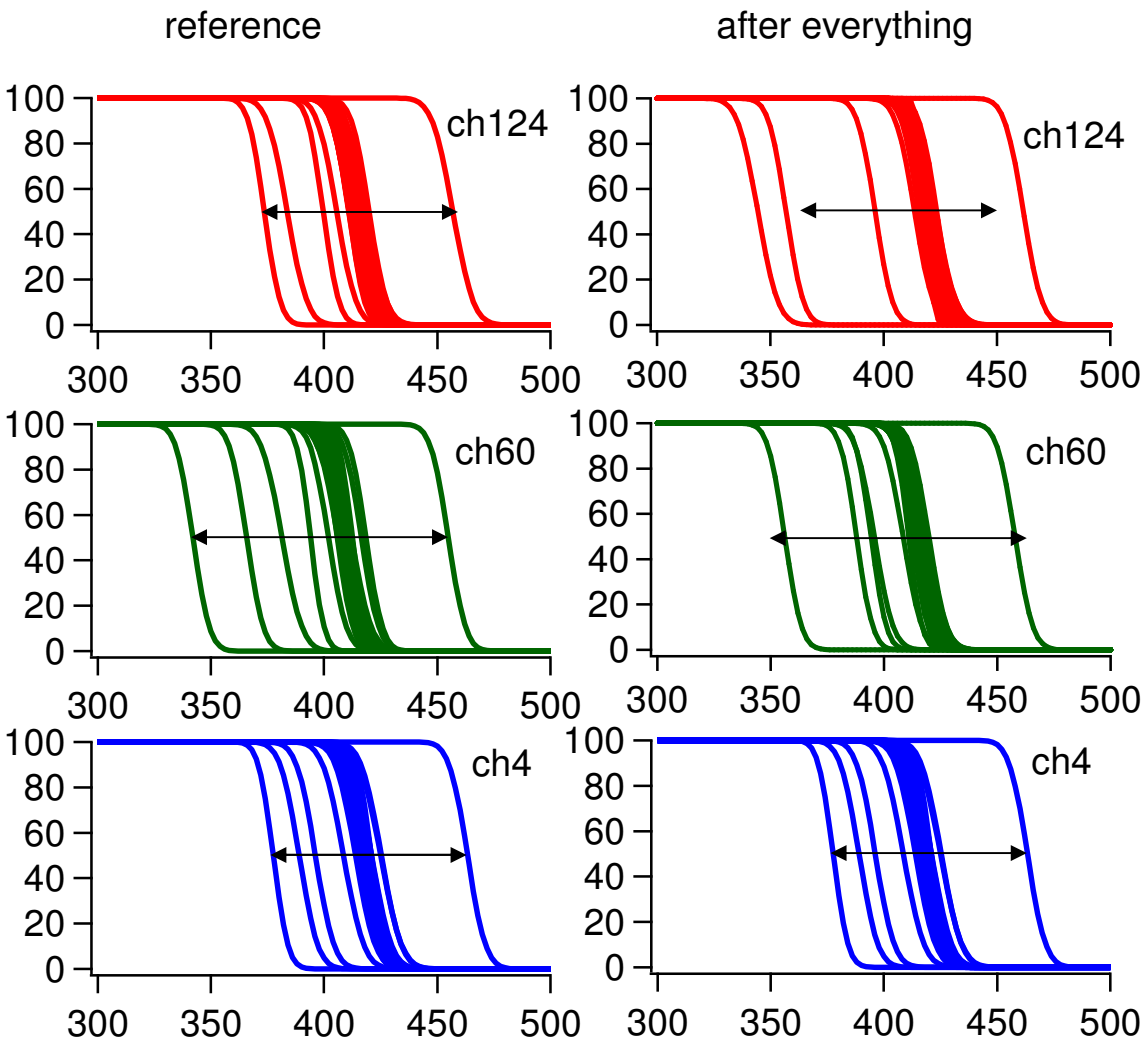


# effect of capacitor repositioning




some effects on all three channels – not obvious what conclusions to draw

# conclusions?



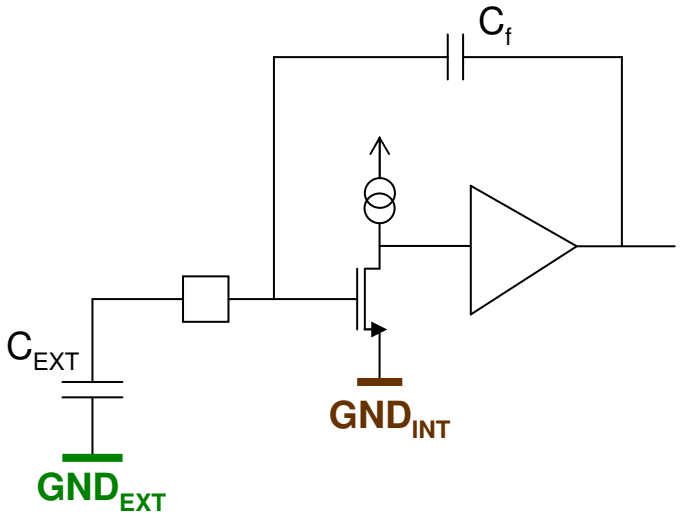

no dramatic improvement in behaviour

clearly some effects but no strong indication of a “magic solution”

might be able to do better with new improved board layout?

but seems unlikely that all “undesirable” effects can be made to go away

# overall DC-DC circuit summary




fundamental performance of DC-DC circuit itself is good

high efficiency for 2:1 step down conversion

no significant effect on intrinsic noise

**but** switching transients appear to couple to internal chip ground causing pedestal shifts

- magnitudes dependent on external capacitance

**worth noting**: this would likely not be a problem for hybrid pixel chips

low sensor capacitance
low inductance bump-bond coupling between sensor and chip grounds

**what next?**

more measurements? - I'm open to suggestions

CBC2 will include same DC-DC circuit

bump-bond layout ought to help significantly with performance
(better coupling between on and off-chip grounds)

# dead time issue

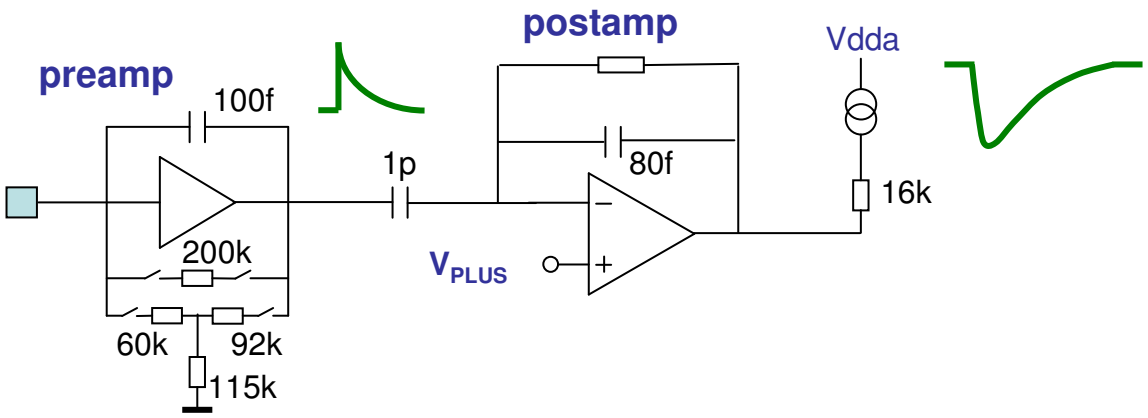
# dead time issue

have we made progress in estimating impact on physics?

**not to my knowledge**

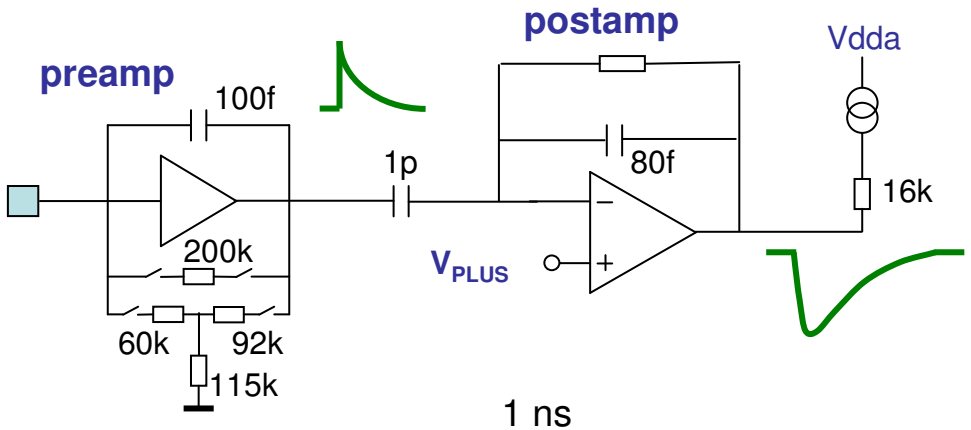
have other shaper designs been evaluated (incl. impact on power consumption)?

**have tried reducing overall pulse width by reducing decay time at preamp output**
**=> reduce feedback resistance**



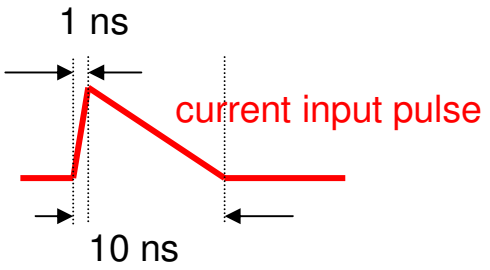

**note: results here of a quick study to give an indication of what might be possible**

# dead time issue




**simulation conditions**

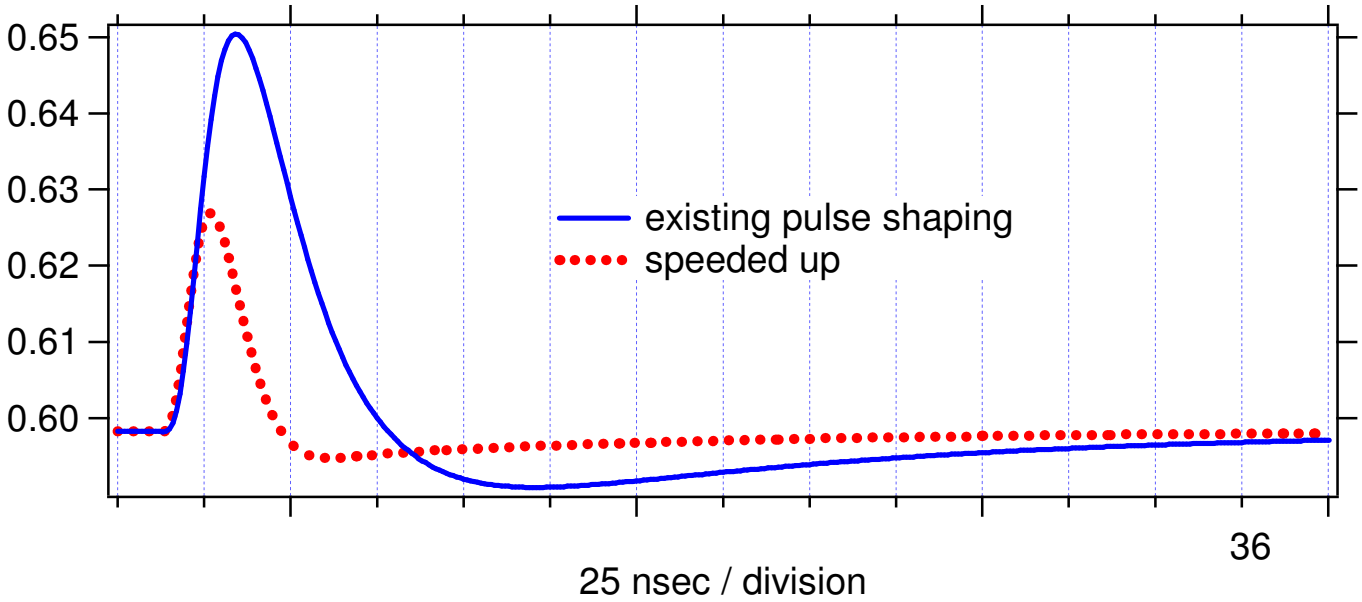
8 pF input capacitance (~ 5 cm sensor)
feedback resistance reduced by factor 4
everything else the same
simulate charge collection time ~ 10 nsec
input device current increased from 160 -> 210 μA
necessary for stability
=> extra 60 μW / chan




**results**

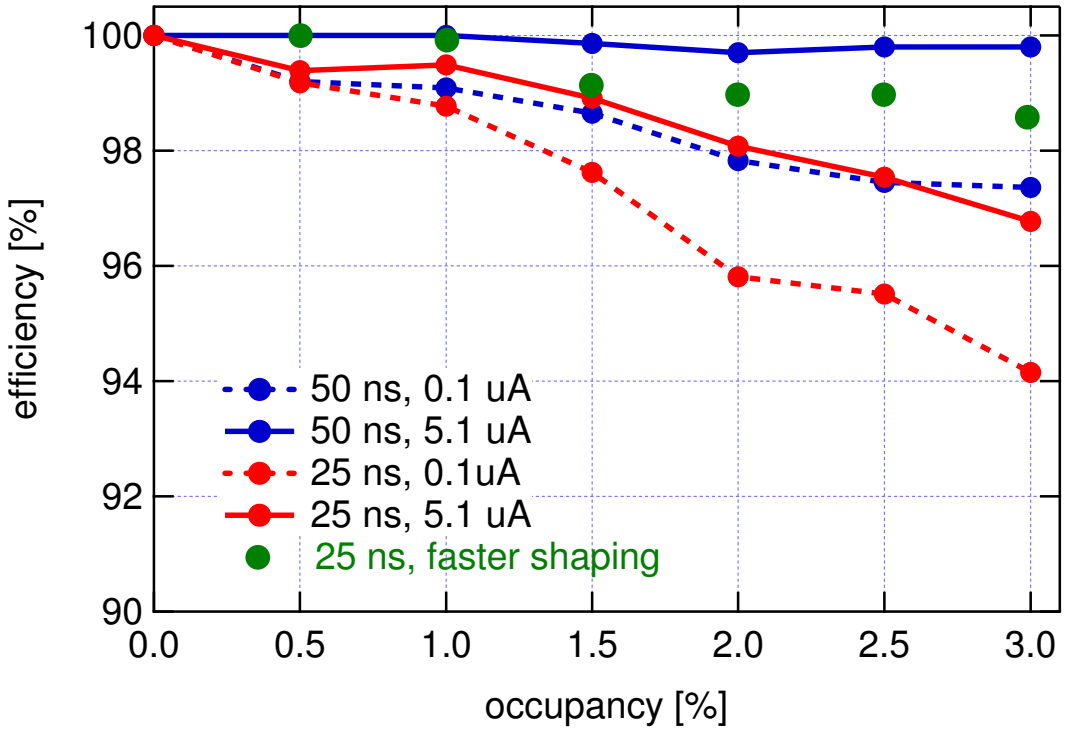
reduced amplitude ( factor ~ 2)

noise goes from
890 -> 1200 e



# efficiency improvement

picture from last time with
faster shaping time results added




some improvement in efficiency, but noise & power penalties (no surprise)
noise effects not included in above plot
another likely issue will be stronger dependence of pulse shape on charge collection time

important note:
this study very preliminary - other problems likely to show up with more careful and detailed simulations

not proposing to modify front end for next CBC submission

# CBC bug fixes

# bug fixes

current plan is to have well-simulated solutions in place to allow front end design to be discussed and frozen at RAL meeting on 7th February

present status:

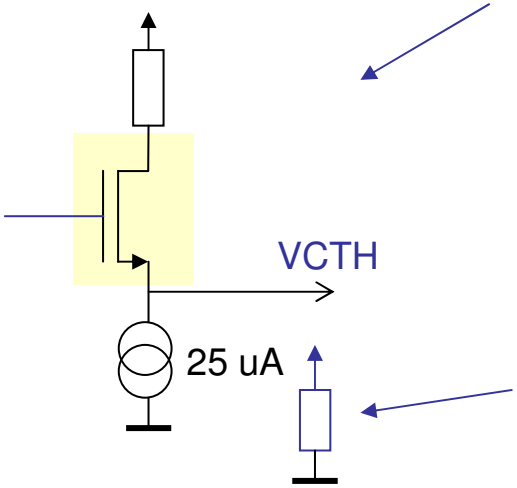
VPAFB: control voltage to postamplifier feedback
- needs external decoupling on present version to achieve stability
- can buffer voltage to each channel using source follower (minimal power)

VCTH: global comparator threshold
- not enough drive to overcome external hysteresis operating in parallel in present version.
- Davide proposes new comparator circuit with internal hysteresis
  - may have difficulties to achieve minimum level of hysteresis
- Mark R proposes individual buffer for VCTH to each channel
  - some power (and space) required
- 2 possible solutions - will review and make decision on 7th Feb

BGO/BGI: bandgap needs decoupling on present chip
- Mark R will advise on simple RC filter values to be implemented on chip
- 1 MΩ x 100pF should work well

no other significant design changes - maybe some tweaks.

# VCTH problem




VCTH drive circuit can source current but sink capability fixed at 25 uA

if VCTH > Postamp output for all channels, then Nint positive for all channels

500k in parallel for all channels = ~4k

~ 0.5 V / 4k = 125 uA

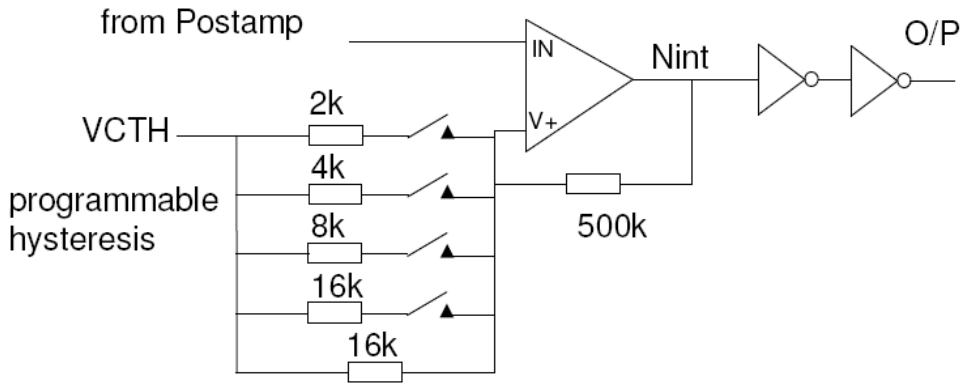
drive circuit can't sink this so VCTH gets pulled high

can fix with external resistor to ground (on VCTH pad) to provide extra current

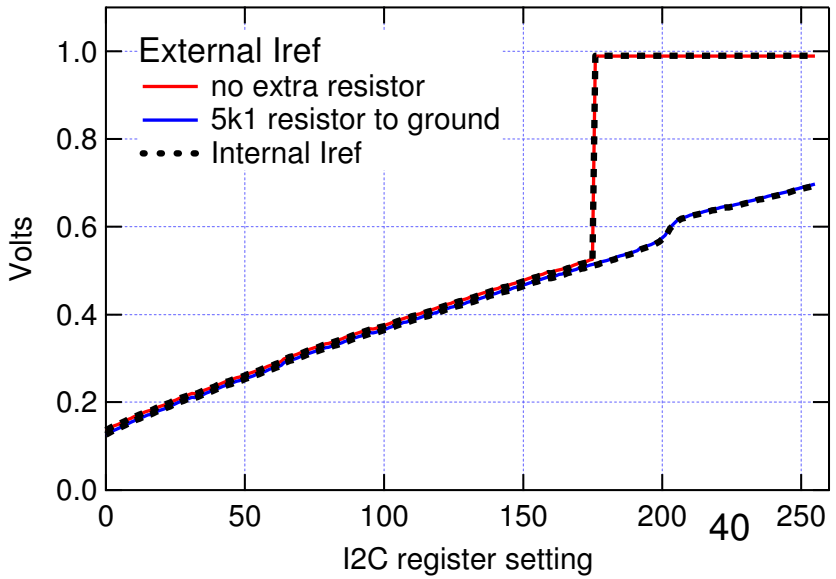
or drive VCTH with external DAC

(look for better fix for next CBC version)

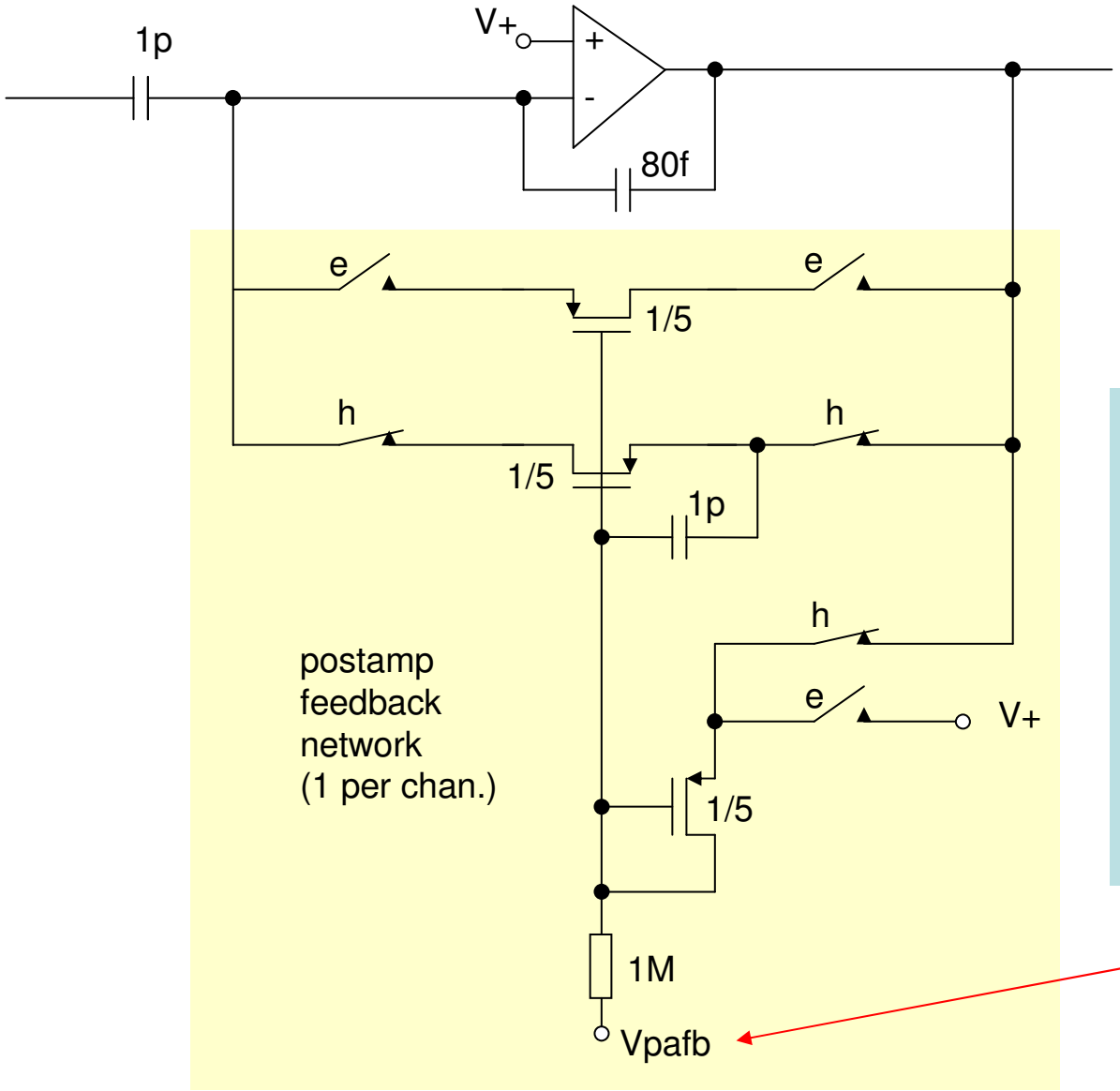
**COMPARATOR CIRCUIT**

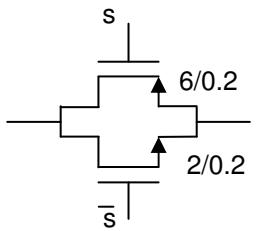



**VCTH vs I2C setting**

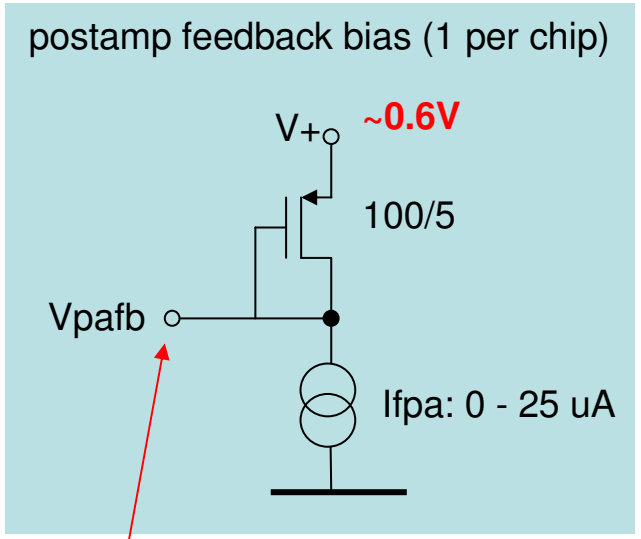


# VPAFB postamp feedback - current situation



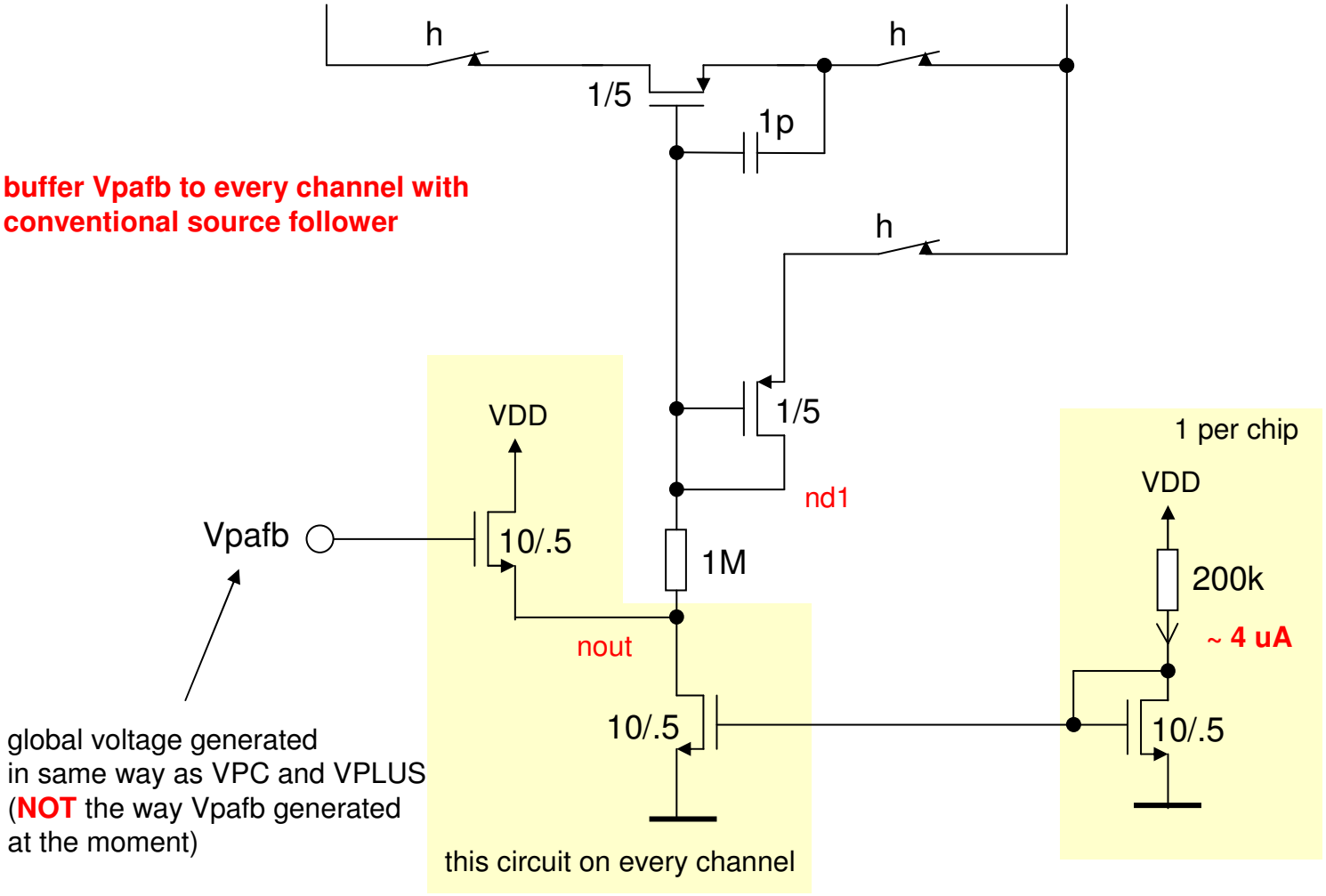




switch
implementation
(NMOS enclosed)



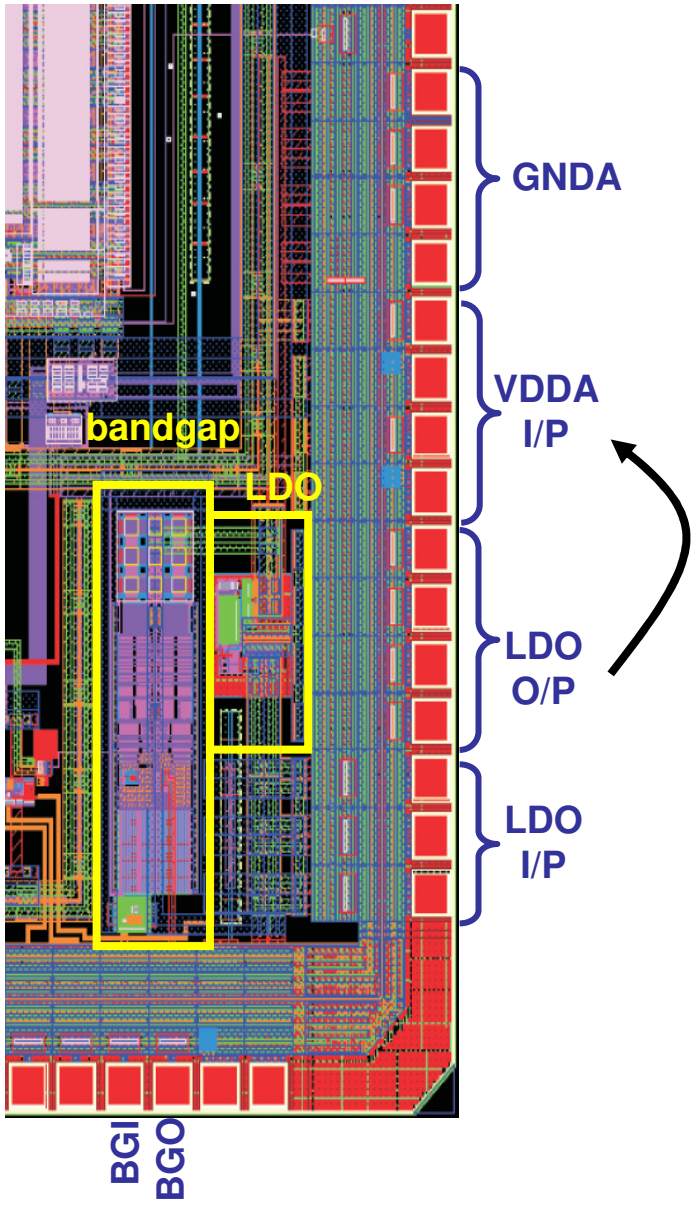

**high impedance node
can be influenced by CM
movement at postamp O/P
1M / 128 = 8k**

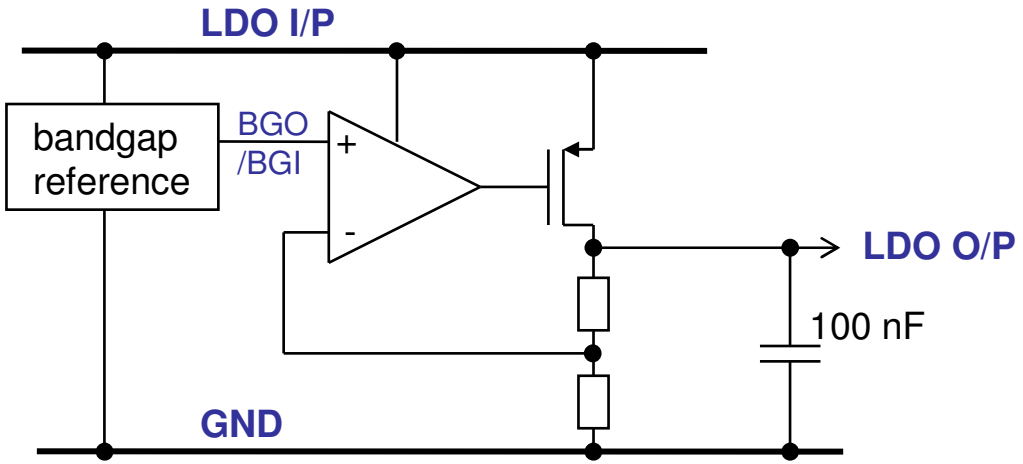
# VPAFB - proposed solution




~ 5 uW / channel extra power

# BGO/BGI bug fix




LDO included to provide clean, regulated rail to analog FE

~ 1.2 Vin, 1.1 Vout

uses CERN bandgap as Vref (0.6 V)

bandgap output (BGO) and input to LDO (BGI) taken to pads to allow to measure and/or over-ride

**problem**

bandgap powered by LDO I/P which can be noisy
noise feeds through to BGO

# LDO - AC performance

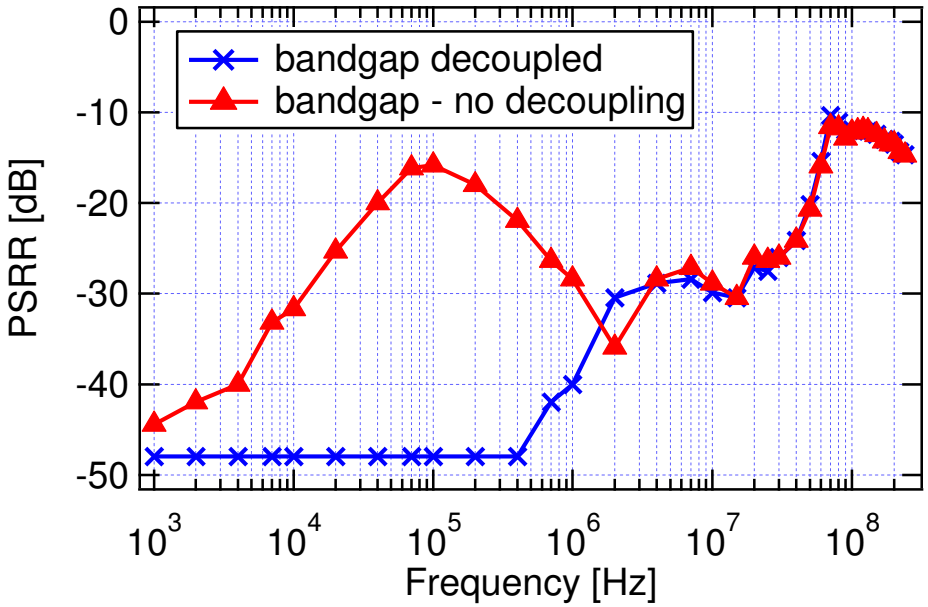
LDO O/P measured for 100 mV p-p sinewave ripple on 1.25 V DC LDO I/P

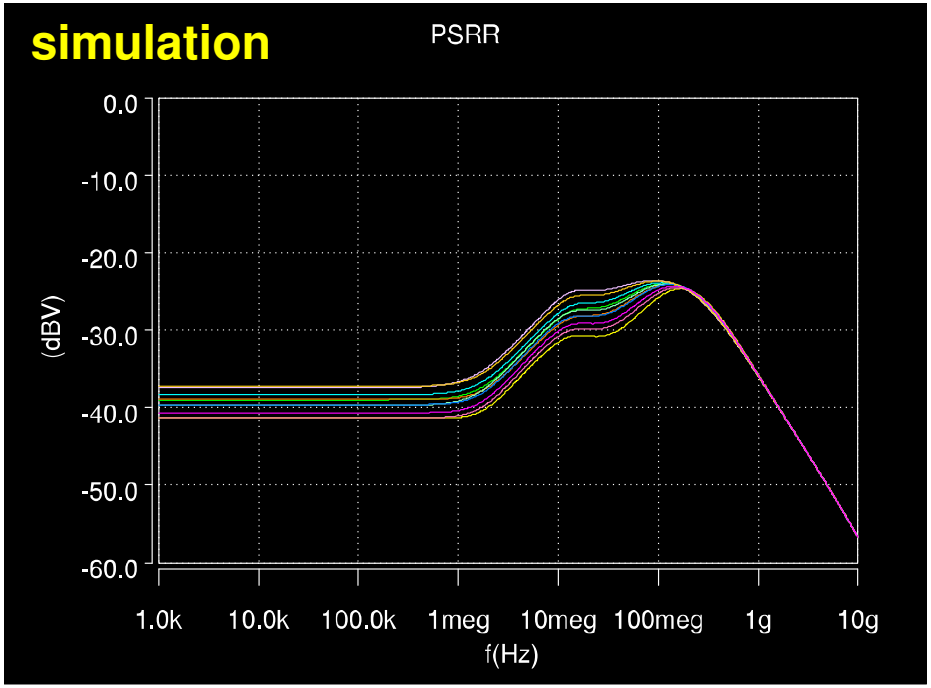
PSRR = 20.log[(LDO O/P)/(LDO I/P)]

measurement has some agreement with simulation
quite good rejection up to ~ 10 MHz

with bandgap decoupled get v.good rejection at low frequencies (signals at limit of measurability)

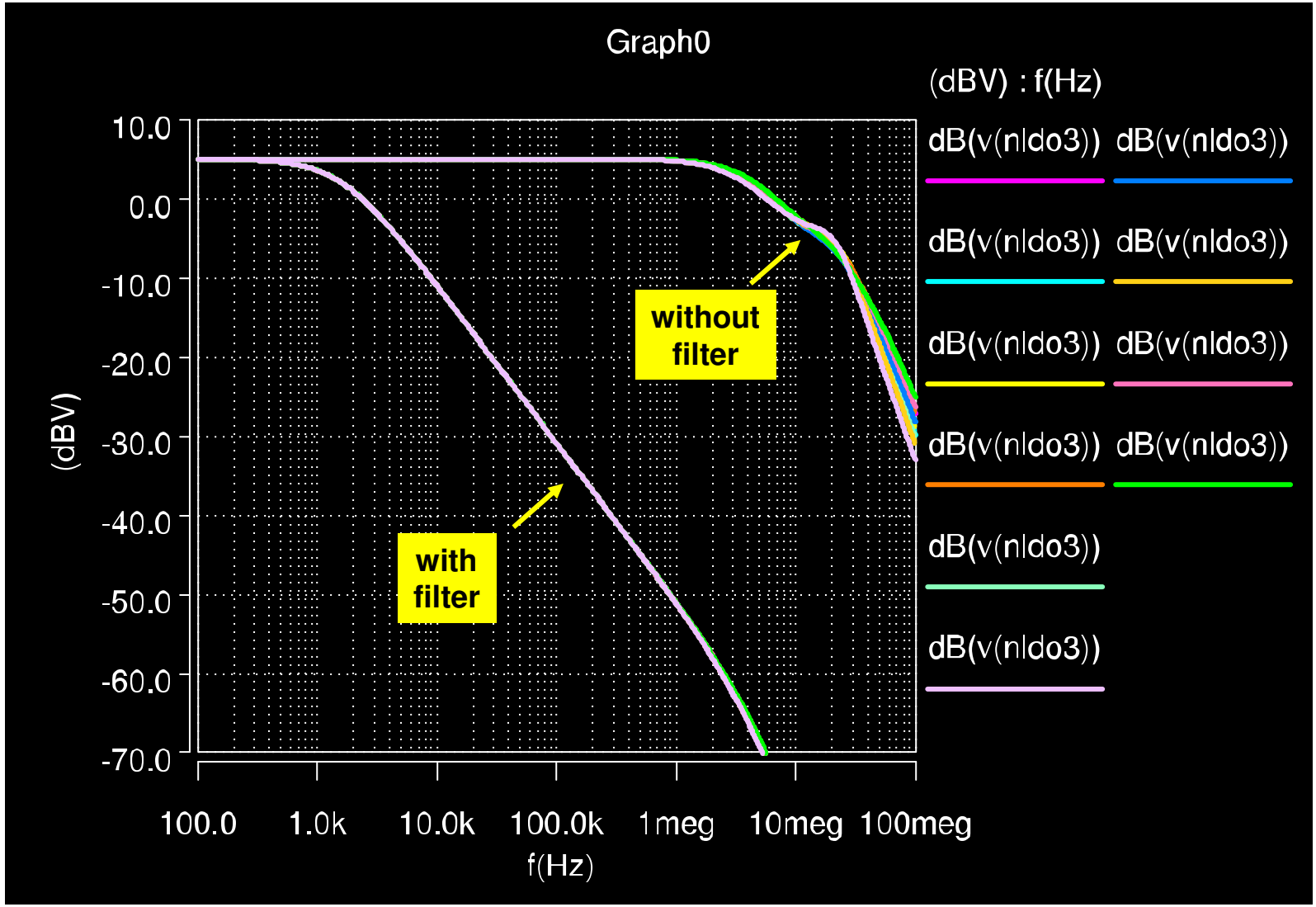
=> need to filter BandGap output voltage fed to LDO



# passive RC filter - 1M x 100pF

LDO output dependence on simulated bandgap output frequency




should be good enough