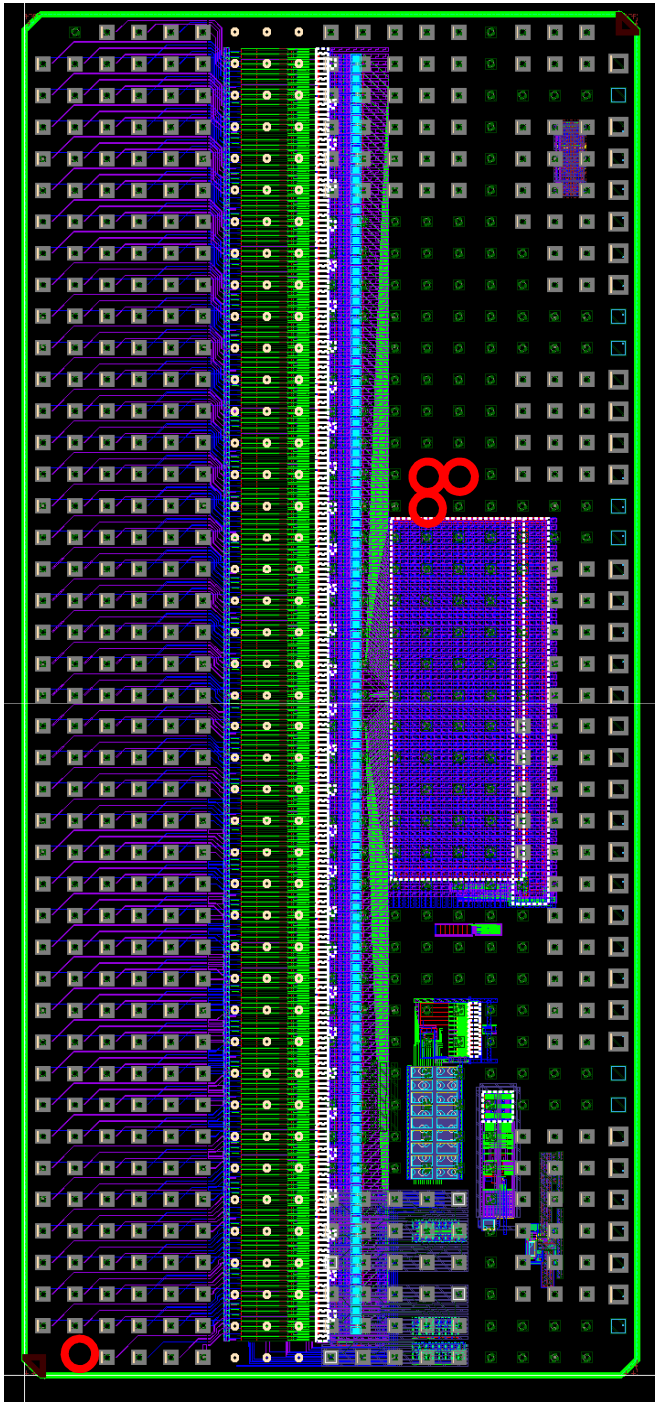
CBC status

M.Raymond

Top Level status - Davide

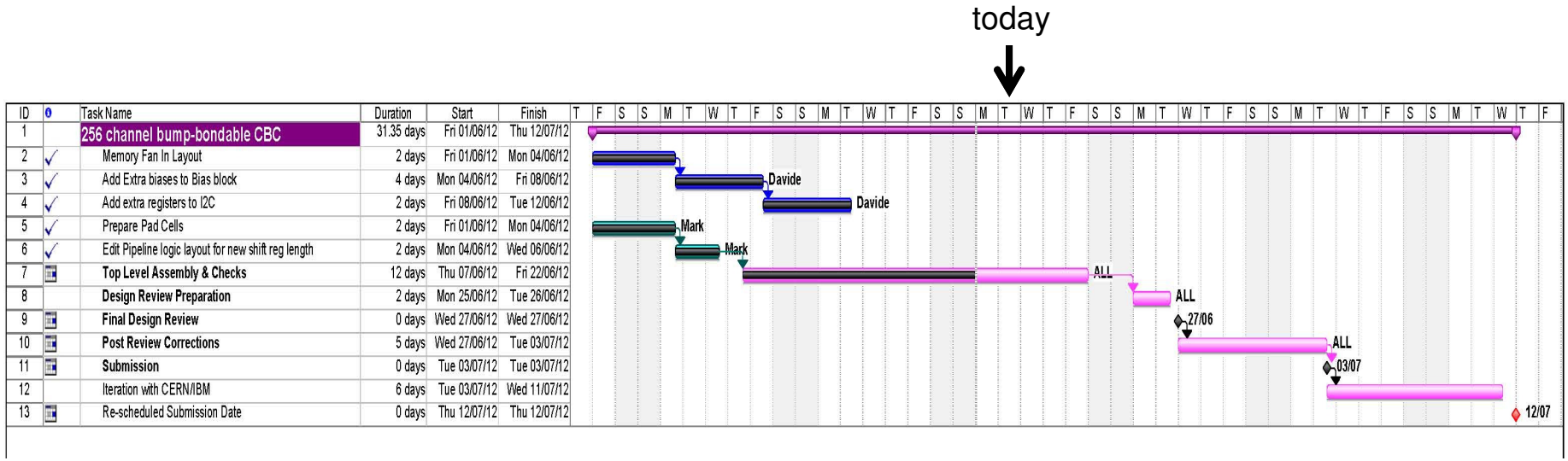
All the blocks are ready, now working on top-level routing and layout checks

Preliminary version sent to CERN to make progress with reticle



missing PAD

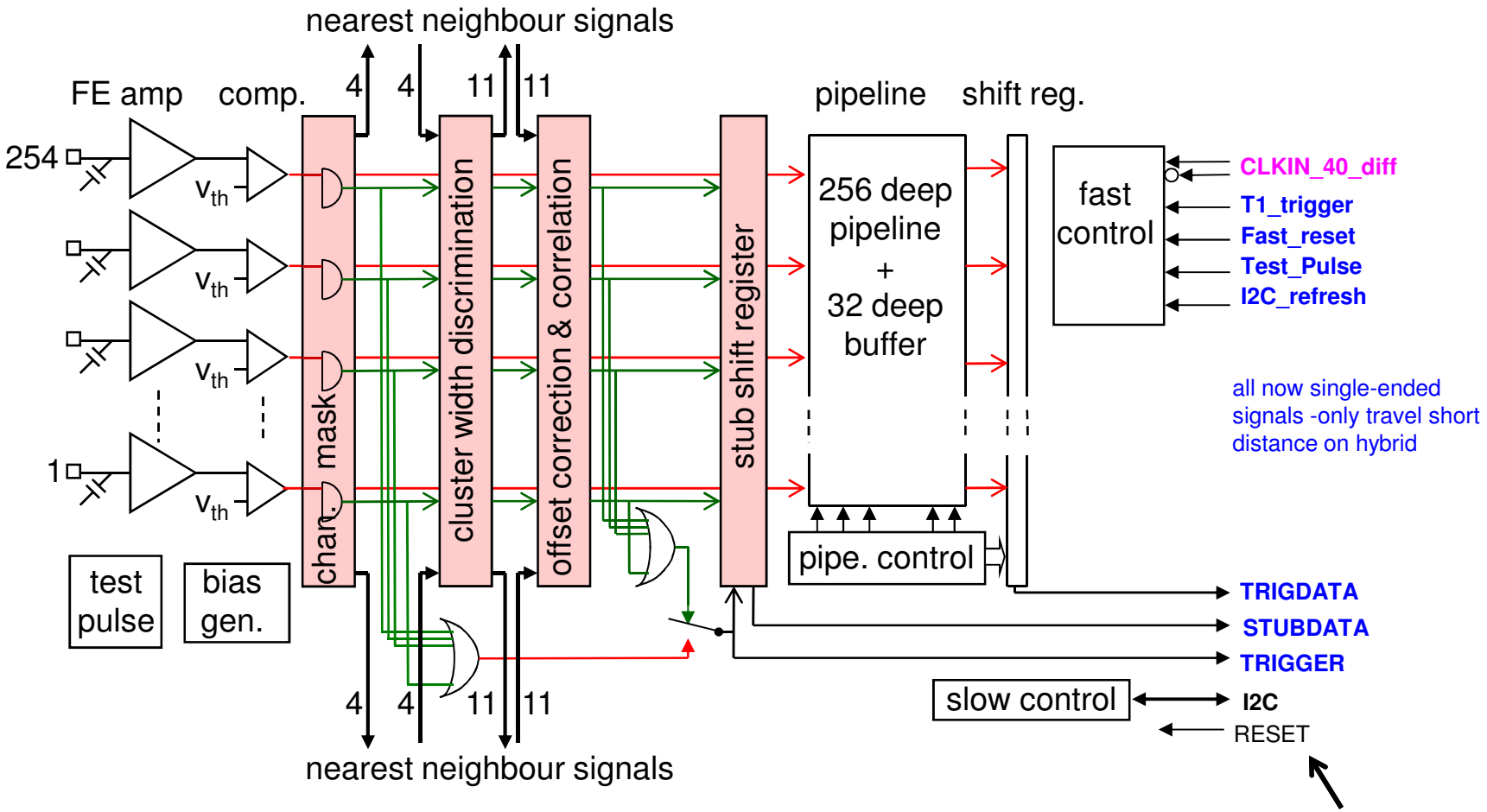
Submission status – Mark Prydderch



ID	Task Name	Duration	Start	Finish
1	256 channel bump-bondable CBC	31.35 days	Fri 01/06/12	Thu 12/07/12
2	Memory Fan In Layout	2 days	Fri 01/06/12	Mon 04/06/12
3	Add Extra biases to Bias block	4 days	Mon 04/06/12	Fri 08/06/12
4	Add extra registers to I2C	2 days	Fri 08/06/12	Tue 12/06/12
5	Prepare Pad Cells	2 days	Fri 01/06/12	Mon 04/06/12
6	Edit Pipeline logic layout for new shift reg length	2 days	Mon 04/06/12	Wed 06/06/12
7	**Top Level Assembly & Checks**	12 days	Thu 07/06/12	Fri 22/06/12
8	**Design Review Preparation**	2 days	Mon 25/06/12	Tue 26/06/12
9	**Final Design Review**	0 days	Wed 27/06/12	Wed 27/06/12
10	**Post Review Corrections**	5 days	Wed 27/06/12	Tue 03/07/12
11	**Submission**	0 days	Tue 03/07/12	Tue 03/07/12
12	Iteration with CERN/IBM	6 days	Tue 03/07/12	Wed 11/07/12
13	Re-scheduled Submission Date	0 days	Thu 12/07/12	Thu 12/07/12

- Pre-submission design review moved to the 27/06/12
- Aim to submit design to CERN 03/07/12.
- Submission date revised from the 27/06/12 to 12/07/12

CBC2 interface specifications



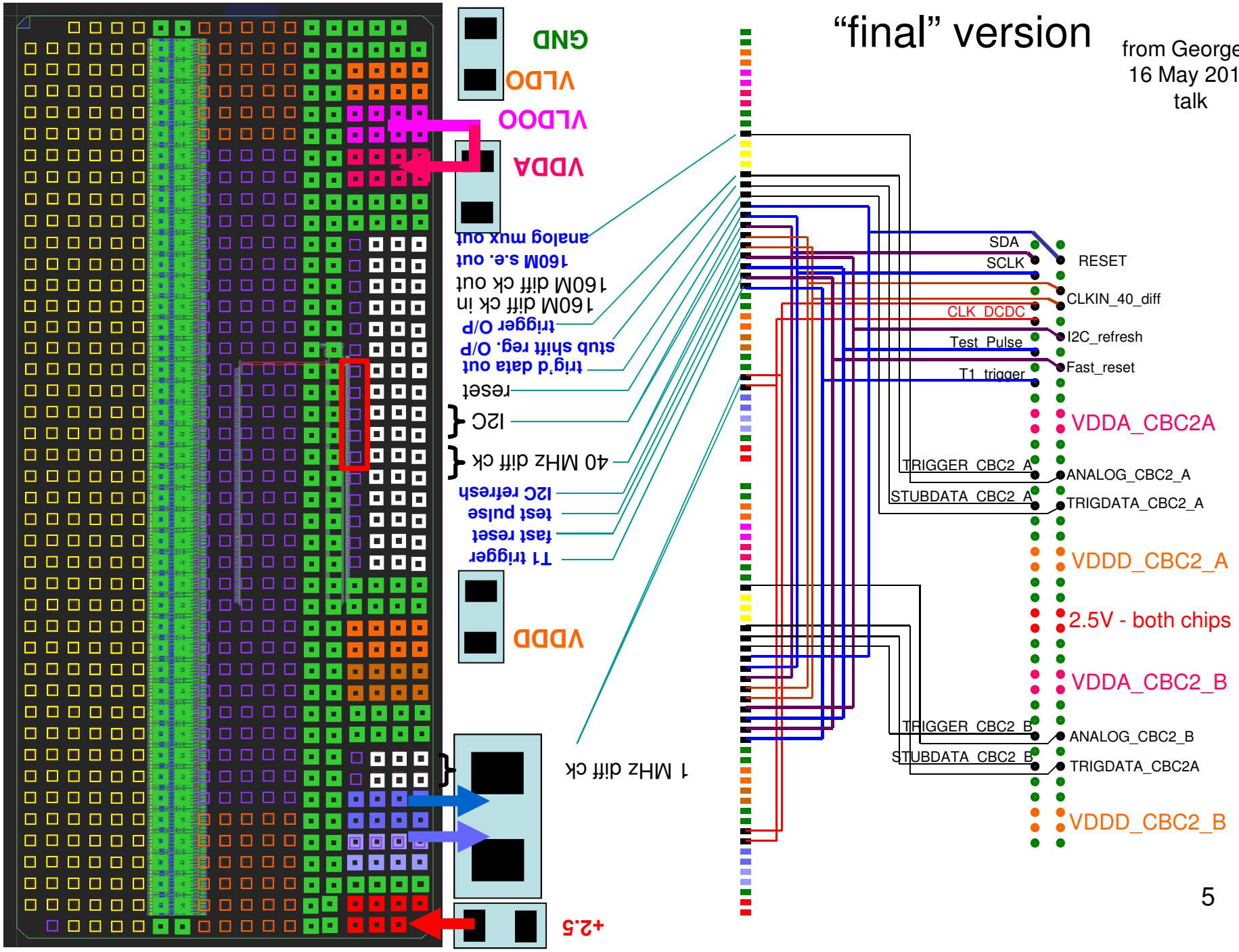
details (exact timing and I2C register definitions) will be specified in CBC2 user manual

hard reset (CMOS level)

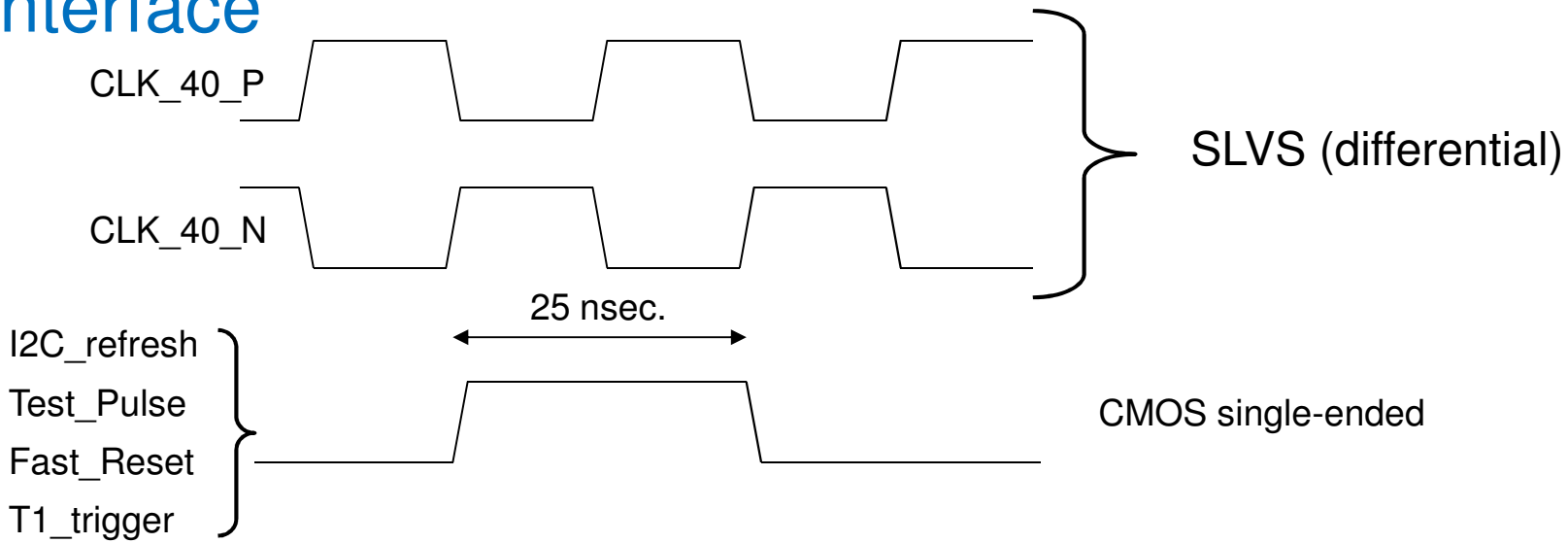
user manual for CBC1 exists (not widely circulated) and is available on request

“final” version

from Georges’ 16 May 2012 talk



Fast interface



I2C refresh

resets all I2C registers to majority value

Test_Pulse

injects charge (programmable amplitude, programmable phase w.r.t. 40 MHz)
8 groups of ~32 channels (programmable selection of group)
follow with T1_trigger ~ latency later

Fast_Reset

like Reset101 for APV (resynch)
resets fast control logic, relaunches pipeline pointers
must hold-off T1_triggers until latency elapsed

T1_trigger

triggers readout of a time-slice of the pipeline memory , consecutive triggers allowed

Slow control I2C interface

up to 1 MHz operation (30 pF, 3.3k pull-up)

5-bit selectable (bonded on substrate) I2C address, CBC is always slave

internal register types include:

FE analogue bias levels, polarity, comp. hysteresis, hit detect operation, …
as in present chip, with minor changes

test pulse features
amplitude, phase w.r.t. 40 MHz (1 nsec steps), which group of 32 channels

individual channel comparator offsets
254 8-bit values

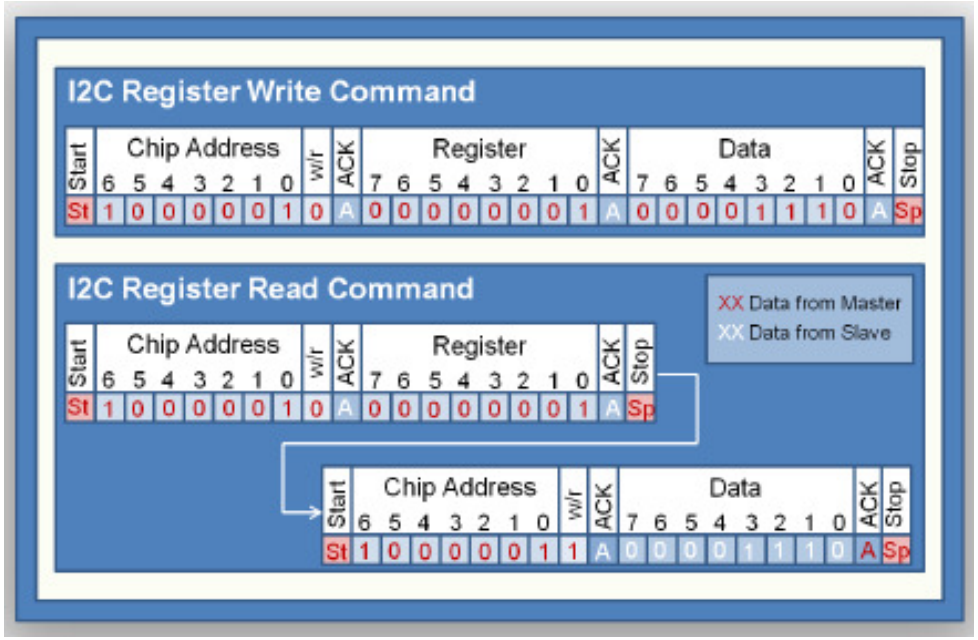
individual channel mask
32 8-bit registers

Pt stub registers
window offset and width

……

details can be made available soon after chip submitted

picture from CBC1 user manual



Outputs – single ended

TRIGDATA

like for CBC1 but longer data packet

⇒ 266 x 25ns = 6.6 usec.

TRIGGER

25 ns duration bit indicates EITHER (programmable):

presence of Pt stub

OR hit on any channel

exact timing rel. to amplifier input to be confirmed

STUBDATA

test feature

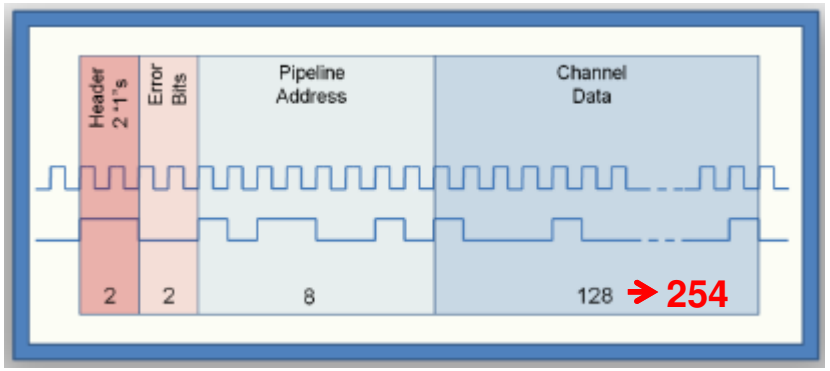
contents of shift reg at correlation output shifted out

at 40 Mbps

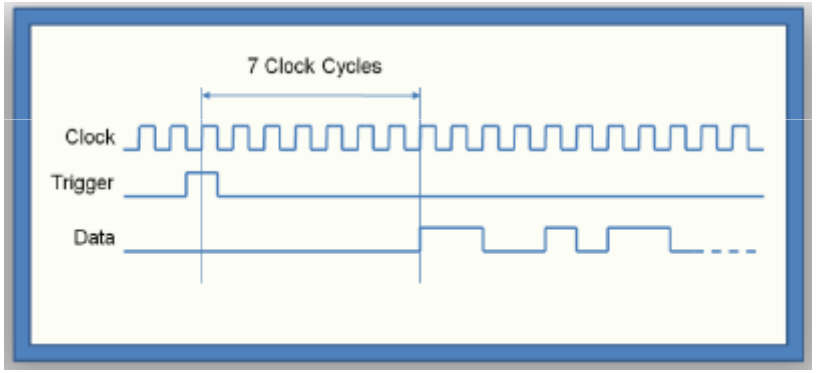
can be disabled

pictures from CBC1 user manual

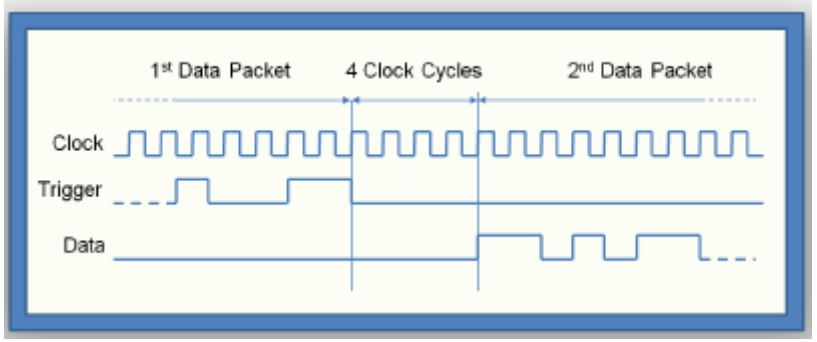
TRIGDATA data frame



TRIGDATA data frame start w.r.t. T1_trigger



TRIGDATA “back-to-back” frame gap



HARD RESET & DC-DC

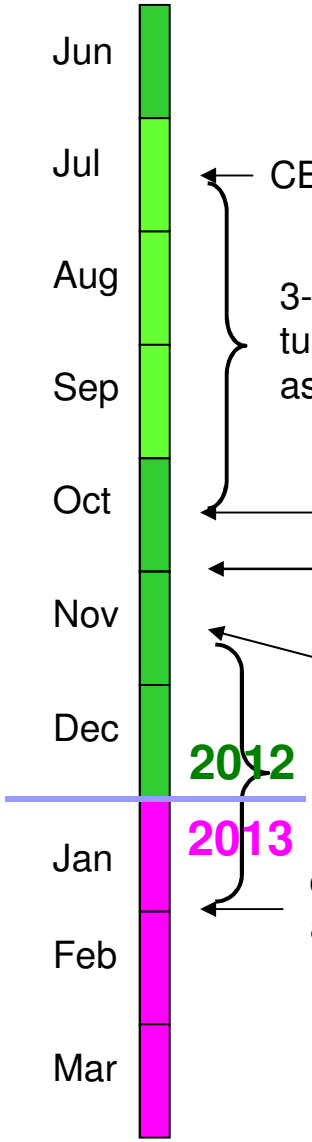
RESET

- CMOS level, active high
- resets I2C registers and interface, and other logic
- after re-programming desired register values, follow with Fast_Reset

CLK_DCDC

- 1 MHz differential clock - 2.5 V levels
- should be synchronous to 40 MHz BX clock

CBC2 test preparations



CBC2 submission

3-month turnaround assumption

wafers back

CBC2 chips from diced wire-bond (XFEL) wafer available for test
(verify functionality before committing to bump-bonding assembly)

submit un-probed CBC2 C4 wafer
+ dual chip substrate for assembly

dual chip CBC2 substrates available for test

have this period to prepare wire-bond board for basic functionality test
(use backend pads)

also begin preparations for wafer probe test

dual CBC substrate interface boards needed ~ end of year
- readout side (level adaption)
  - probably more than one type (custom lab, FMC, ..)
- input side
  - wire-bond boards for charge injection and other tests

plan to have probed wafers available for 8-chip substrates available ~ early 2013

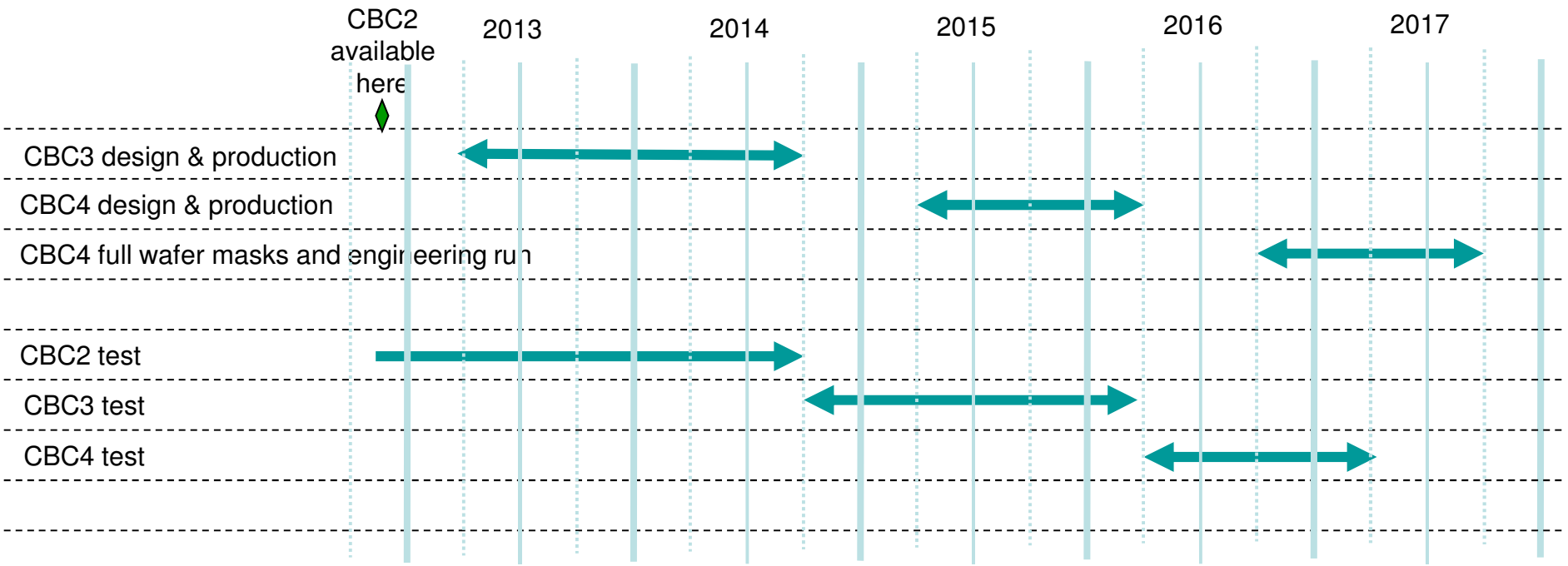
CBC2 testing - division of labour

chip verification will be split between Imperial and RAL (Davide)

some duplication inevitable but will try and avoid too much

will develop more detailed plan once chip gone

UK CBC development plan



submission to UK funding agency very soon – phase II tracker readout main objective is:

- To complete development of a readout and triggering chip suitable for the SS-Pt module bringing the chip to a final state ready for mass production.

CBC3 should be very close to final chip – available late 2014
CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017