2S-Pt module systems meeting, CERN, 22nd March, 2012.

CBC status and plans

M.Raymond

CBC prototype status

no new test results

concentrating now on CBC2 related work

things left to do

radiation tests still outstanding

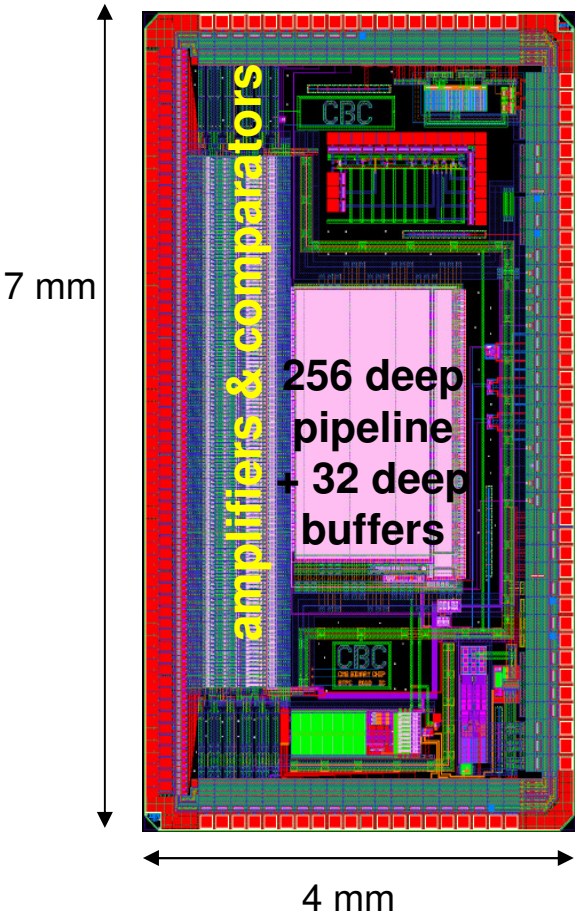
ionising - would still hope to pursue

single event - leave to CBC2 version?

future for this chip?

we have ~ 600 die (untested)
with workarounds they are perfectly usable
the only wire-bond version of this archtecture that will exist

can use (this year) to begin devlopment of wafer probe test
confirm with CBC2 when available



CBC2

bug fixes

solutions now converged on:

VPAFB: control voltage to postamplifier feedback
- needs external decoupling on present version to achieve stability
- can buffer voltage to each channel using source follower (minimal extra power)

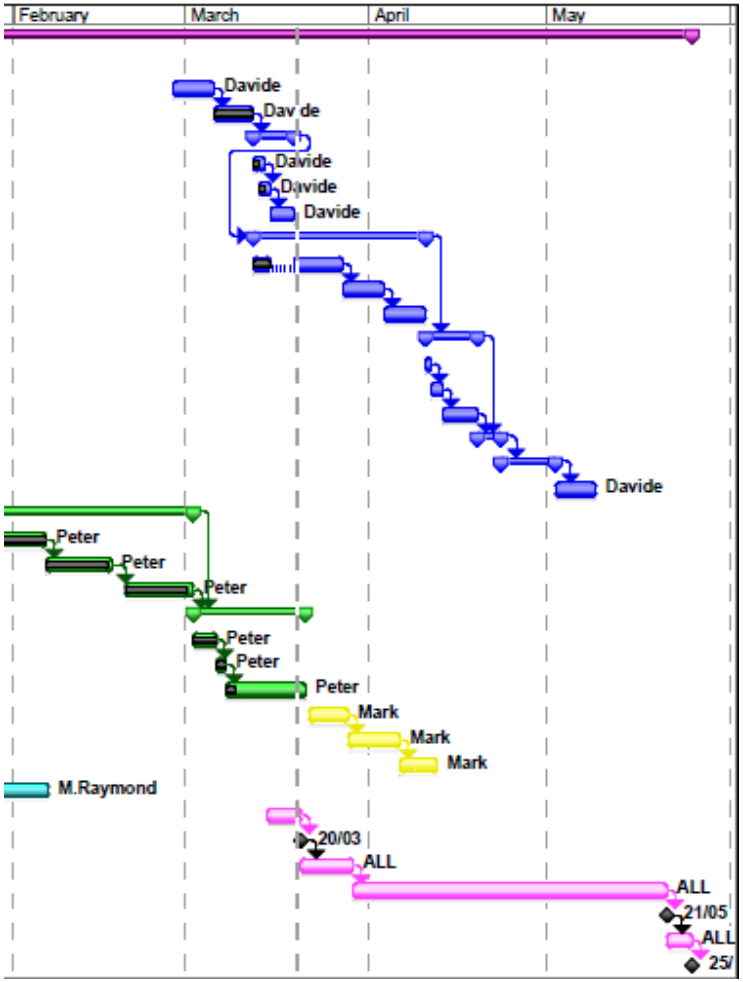
VCTH: global comparator threshold
- not enough drive to overcome external hysteresis operating in parallel in present version
- can modify existing comparator to use internal hysteresis
  - => no load on VCTH

BGO/BGI: bandgap needs decoupling on present chip
- RC filter on chip: 1 MΩ x 100pF should work well

have left details in backup slides

interim design review at RAL this week

ID	Task Name	Duration
1	**256 channel bump-bondable CBC**	178.23 days?
2	Completed Tasks	82.68 days?
23	Simulation of Hit Correlation (OC&C) logic	5.41 days
24	Re-synthesis & Layout of digital circuits	5 days
25	256 bit shift reg for Hit and CWD logic	5 days
26	Schematic	2 days
27	Simulation	2 days
28	Layout	2 days
29	CWD, OC & C prog register	22.89 days
30	Schematic	10 days
31	Simulation	5.41 days
32	Layout	5.41 days
33	OR Transmission Off Chip	7 days
34	Schematic	1 day
35	Simulation	2 days
36	Layout	4 days
37	OR of 256 comparator outputs	2 days
40	hit detect circuit re-triggering	8 days
44	160MHz I/O	5 days
45	I2C modification (1MHz + Voting Logic Refresh)	30.09 days
46	Schematic	10 days
47	Simulation	10 days
48	Layout	10 days
49	I2C Reg modification & extra biases	14 days
50	Schematic	2 days
51	Simulation	2 days
52	Layout	10 days
53	Simulate pipeline with command word	5 days
54	Comparator Modification Layout & Sim	7 days
55	*Bias Monitor Select Mux*	5 days
56	Analogue Design Changes (inc Band Gap)	22.64 days
57	Design Review preparation	4 days
58	Intermediate Design Review	0 days
59	Analogue Layout Changes	7 days
60	Top Level Assembly & Checks	40 days
61	Final Design Review	0 days
62	Post Review Corrections	5 days
63	Submission	0 days



detailed examination of current state of design and layout

Davide Braga,
Peter Murray
Mark Prydderch
Lawrence Jones

a number of issues identified,and actions required - nothing serious

~ on schedule for submission end May

CBC2 architecture and pad definitions

summary of last time + update

I2C

"standard" I2C protocol, CBC always slave
SDA O/P device sized to drive 30 pF with 3.3k pullup, up to 1 MHz operation
> 8 bit address space, so auxiliary address register implemented

Enclose layout transistors

we keep them in the analog front-end (XFEL uses them a lot), Mark P. to modify the LVS rules.

Input descrambler has been dropped: now the pin assignment is fixed (agreed with Georges)

160 MHz diff. input and outputs will be implemented

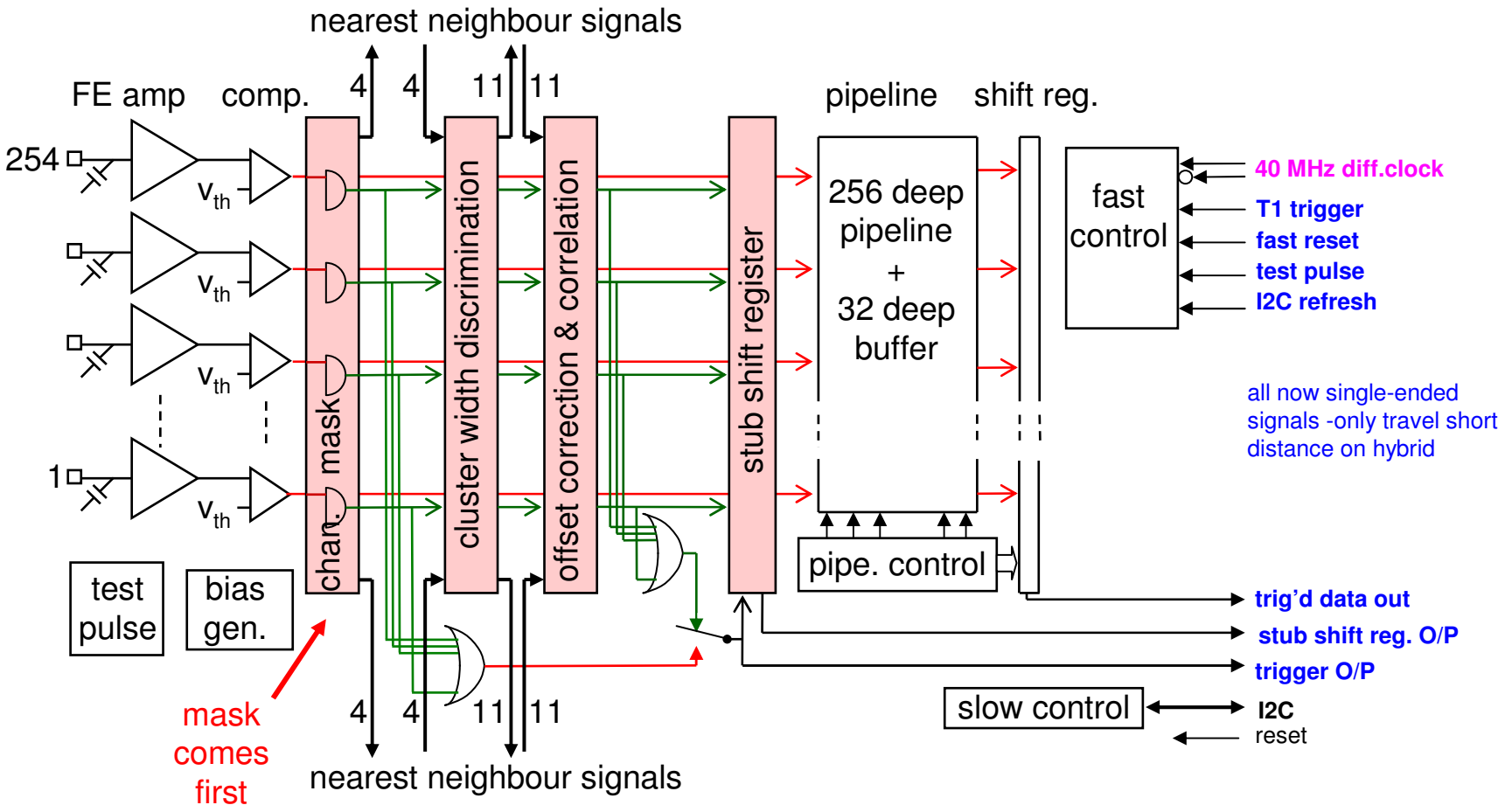
one 160 MHz differential output and one 160 MHz single-ended output

We will use 4 parallel single-ended trigger lines:

bit0 = trigger,
bit1 = fast reset (previously reset101),
bit2 = test pulse trigger,
bit3 = I2C refresh (introduced since last time)

Offset and correlation logic: 2 offset values per chip - up to +/- 3 channels. Window width up to +/- 8 centred on offset channel

CBC2 architecture



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)

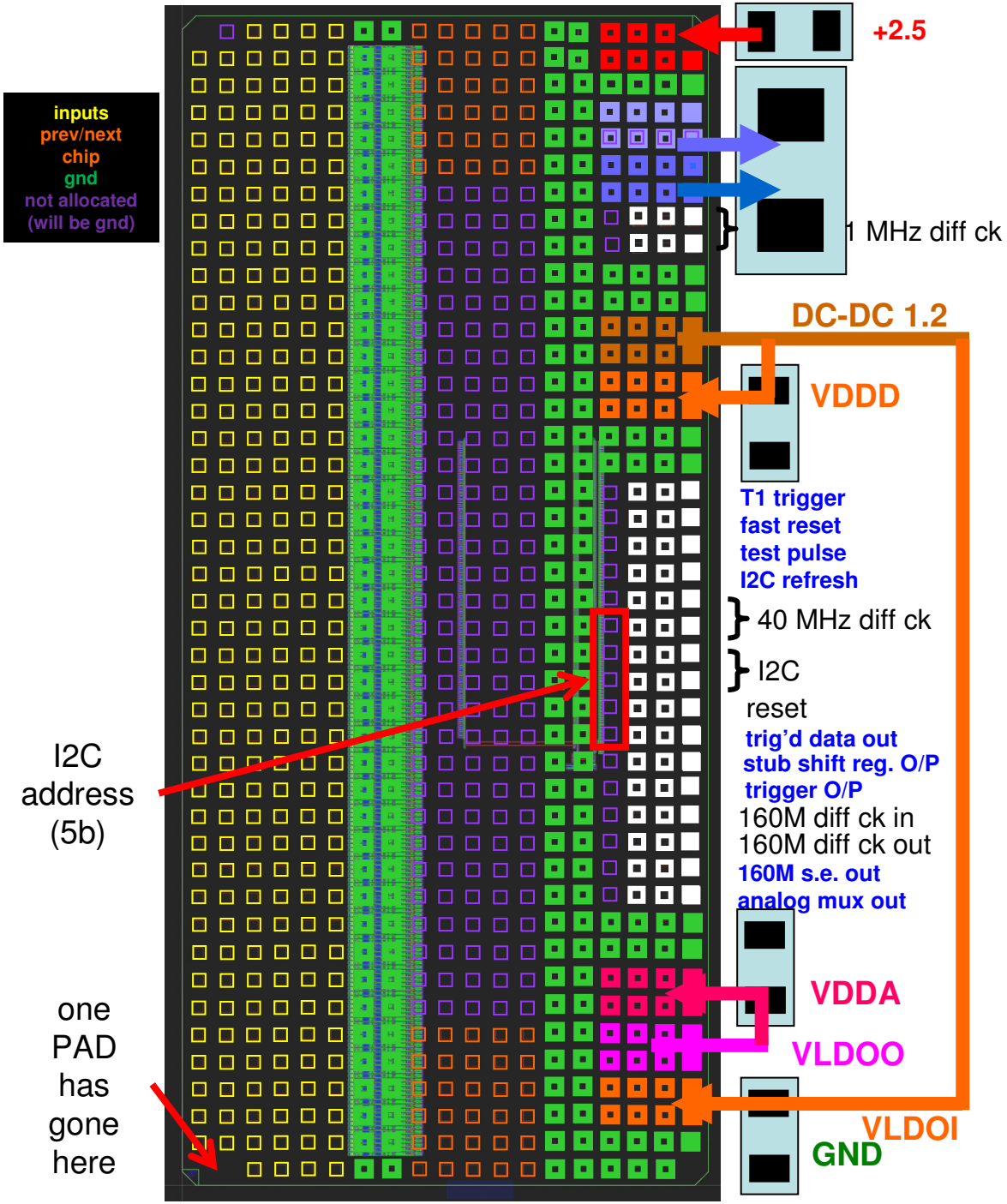
cluster width discrimination: exclude wide clusters

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip
for normal operation choose correlation O/P

CBC2 pads



43 rows x 19 columns

last column of PADs on the right
are probe-able (or wire bondable)
- not C4
- not routed on hybrid

Except for 160M diff pads all the other signals have 2 or more pads shorted together

lines and arrows
show direction of power flow
(GND not shown)

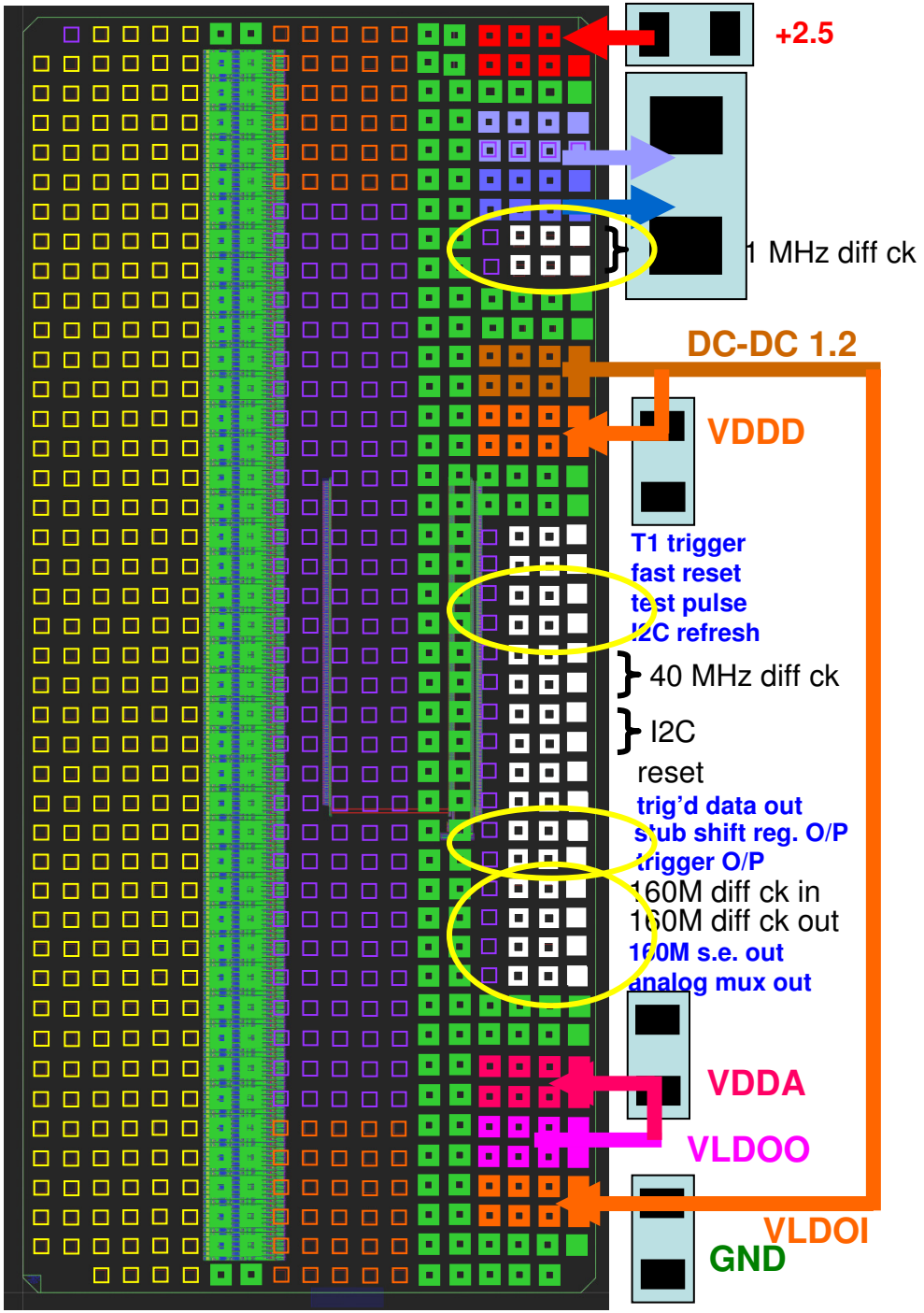
DC-DC 1.2 not connected
to VDDD or VLDOI on-chip

VLDOO (LDO output) not
connected to VDDA on-chip
either

(maximise possible effectiveness
of parasitic off-chip filtering)

analog mux out gives access to
bias generator signals

the future?



need 8 single-ended 160 Mbps lines for trigger stub info

should be ok - all circled lines can go to free up ~10 pads

some pad issues

1) is it ok to have the whole of one edge of the chip not C4?

Kostas will check with IBM if they see any problem

2) from Georges

Endicott would prefer pad opening on substrate to be same size as pad on CBC (assumed 125 um)

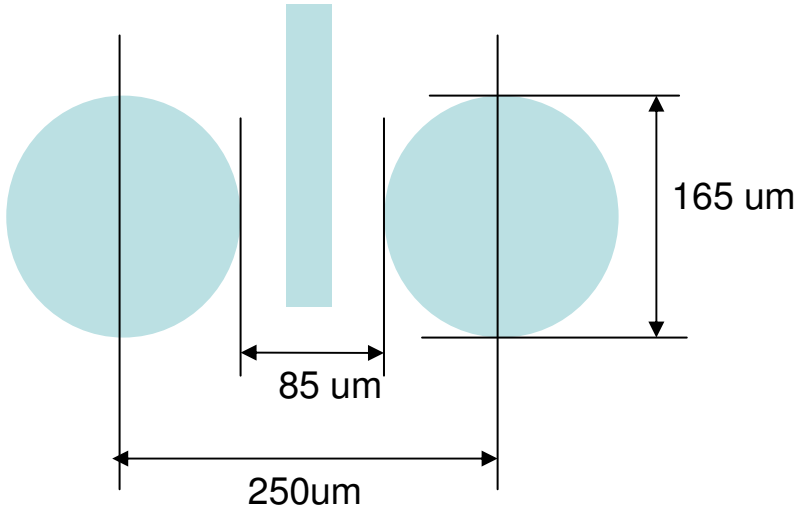
substrate metallisation preferred 40 um larger than pad opening => 165 um

allows for registration mismatch

but not enough clearance to get track between 165 um pads on substrate

need 32 space + 28 track + 32 space = 92 um

not yet clear what solution is here



production plans

Joint CMS XFEL LPD Wafer Submission Plan

- Planned Submission Date: end May
- Wafer Share:
  - 6 Wafers for CMS with C4 finish
    - 1 Wafer for Wafer Probe set up
    - 1 Wafer for single chip modules
    - 3 for the multi-chip substrates (assuming 8 chips/substrate & only 80 KGD/wafer gives10 substrates per wafer allowing 15 full SS-Pt modules from 3 wafers)
    - 1 Wafer contingency
  - 6 Wafers for XFEL LPD with normal finish
- NRE cost split based on die area:
  - XFEL2 65.4%
  - CBC2 34.6%
  - C4 charge to be paid by CBC

Mark Prydderch

Plan for CBC test & Modules

Mark Prydderch

(+ additional comments from me)

1) • Wire bond versions of the CBC2 can be made available from the XFEL wafer dicing. Could be used to test the chip and make a GO/NO GO decision for the C4 finished wafers. **(will incur some delay - is it worth it?)**

propose to make simple wirebond single chip test board (for CBC2)
can also use to decide whether to proceed to next step (single(dual) chip module)

2) • 1 C4 finished wafer will be used (untested) to assemble single chip modules for evaluating the chip, bonding and module.

3) • In parallel 1 C4 finished wafer will be used to trial Wafer Probing

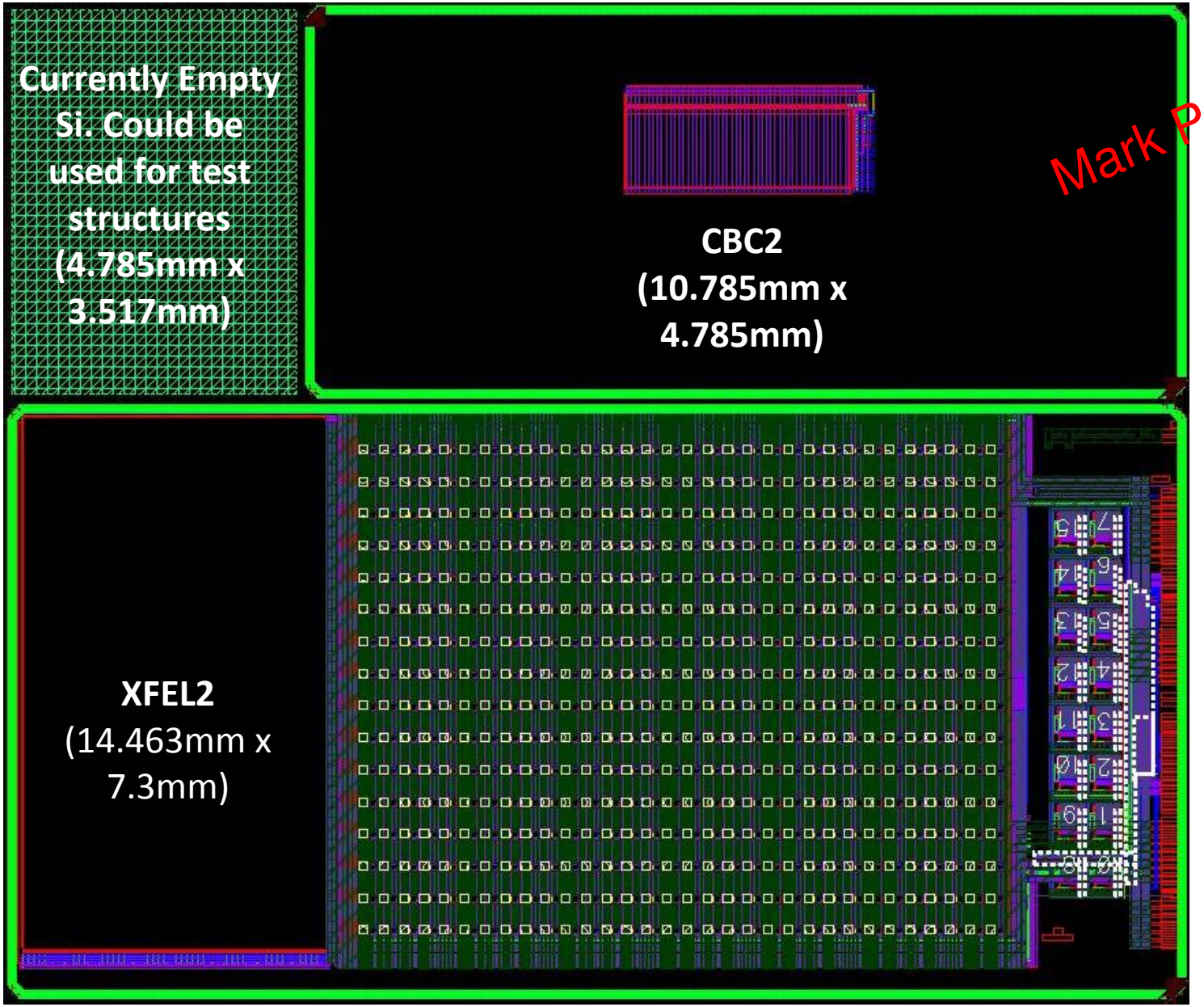
can use single chip test board from step 1) to develop test - don't have to go straight to wafer

4) • Following these trials 3 C4 finished wafers will be probe tested to establish known good die before assembly onto multi-chip substrates.

had thought probe-testing would be carried out by assembly company - but can we afford?
if not - can we do it ourselves?
need high level of cleanliness - some options are:
create (re-create) or find clean room at IC - class 100 seems feasible (good enough?)
find clean-room facility somewhere else - RAL? CERN?

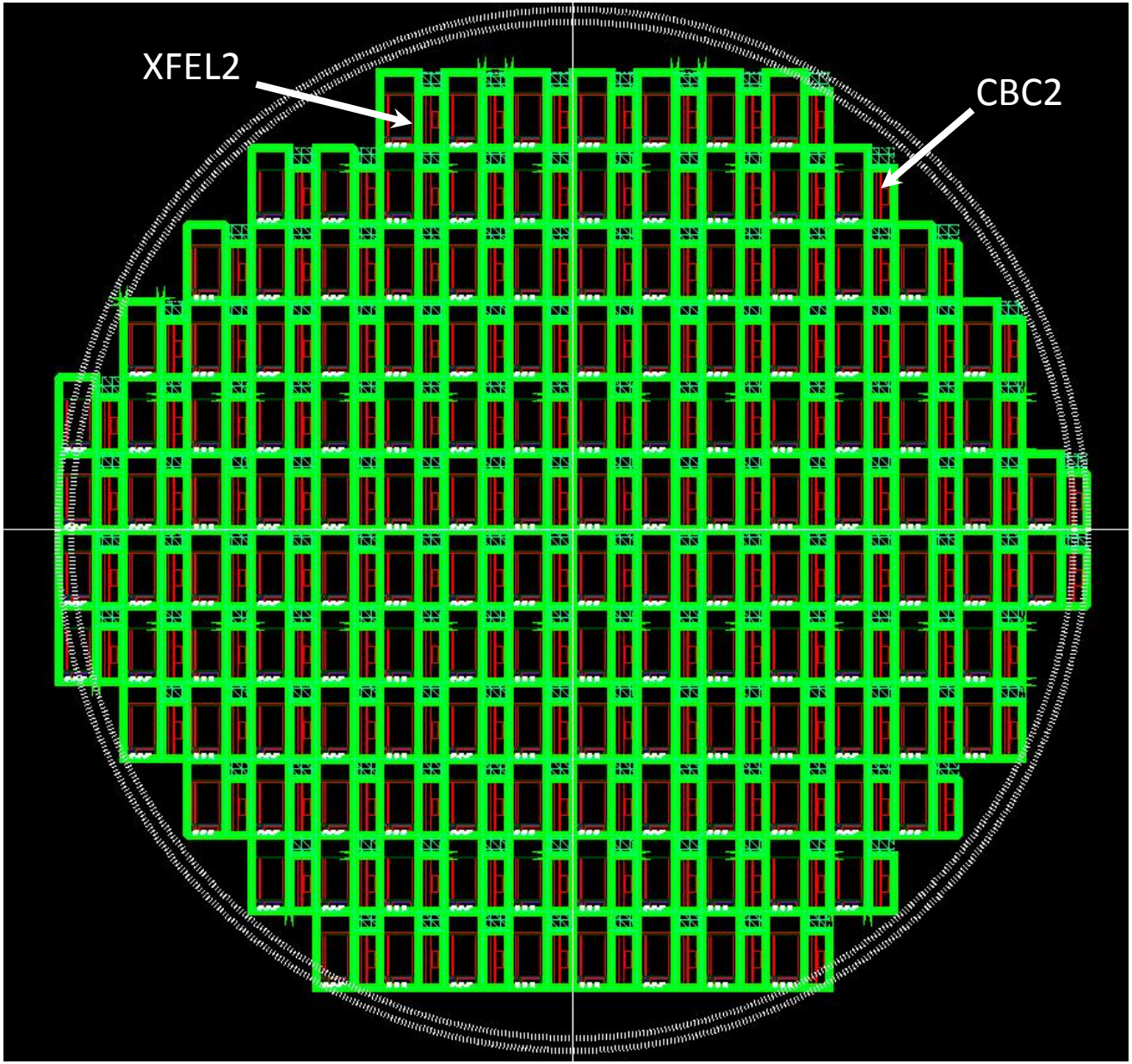
(should consult assembly company about this)

Die Arrangement



Mark Pryderch

Example Wafer Map



~149 viable sites

~143 viable XFEL2 Chips

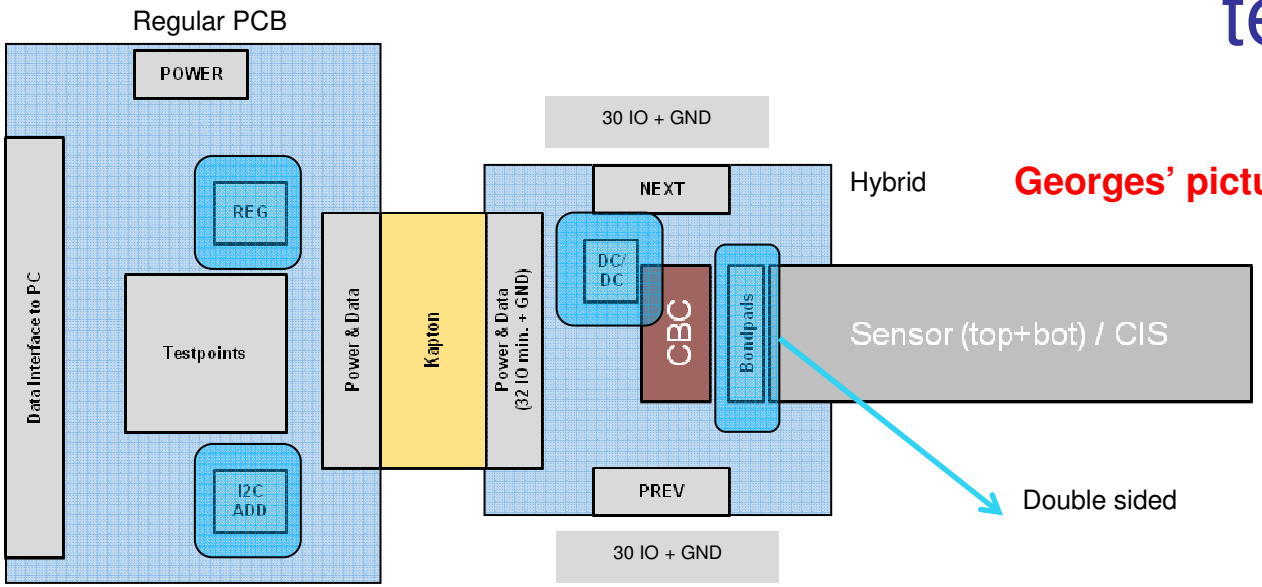
~145 viable CBC2 Chips

A different arrangement of die or site map might improve the number of viable chips, but not significantly.

Mark Pryddercch

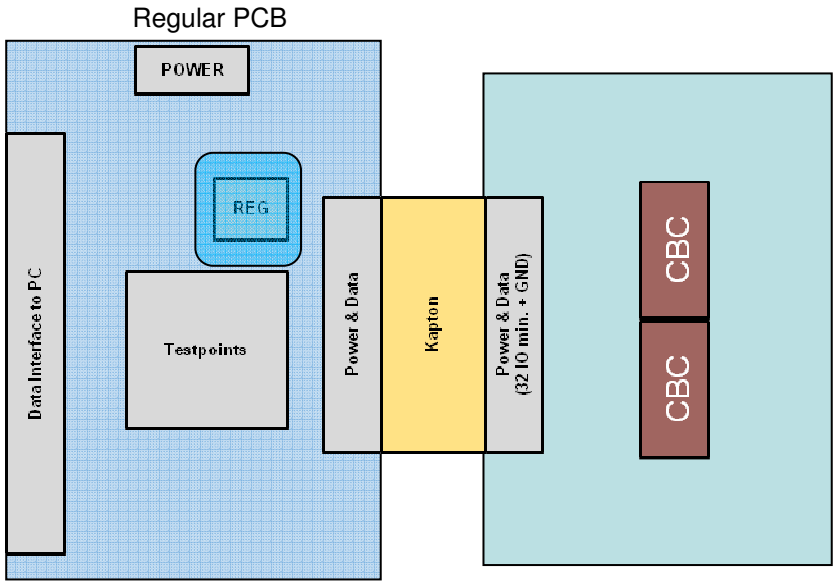
testing ideas

testing thoughts



Georges' picture from last time

2 chip substrate offers a couple of advantages



don't have to bother with top/ bottom connectors - single interchip interface proves functionality (also more realistically)

can investigate effects at chip boundaries (1 sensor bonded to 2 chips)

why not fix I2C addresses? (10101 and 01010)

testing thoughts

CBC + sensor prototype used simple pcb to provide identical functionality to that proposed here →

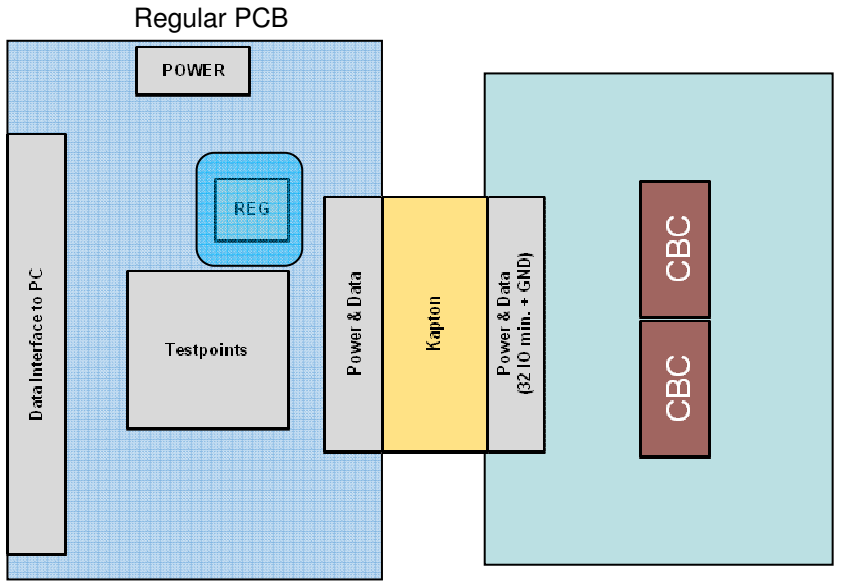
can do something similar for CBC2

note: transition board included to allow long cable between interface board and front end - a useful feature

this →

looks a lot like

this ↓



level shifting interface board

transition board

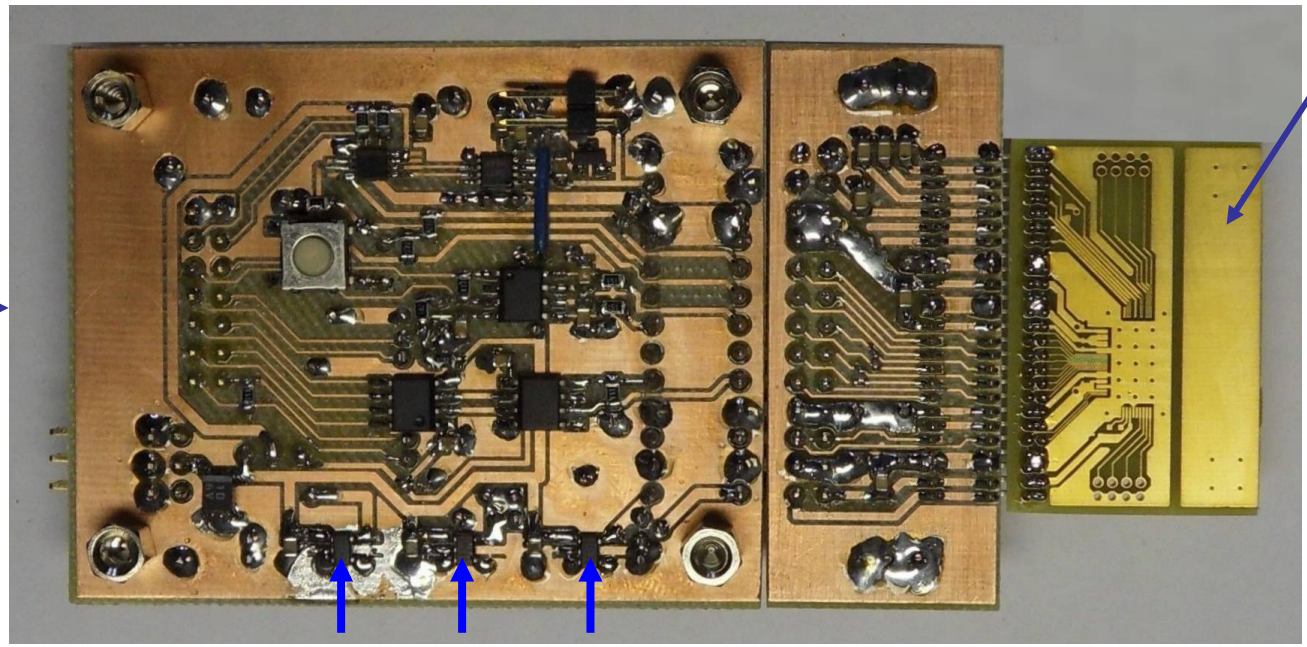
sensor glued here

+5V I2C ↔

LVDS levels
DCDC clock
40 MHz clock
trigger
→

← data out

+/- 5 V
sensor bias →

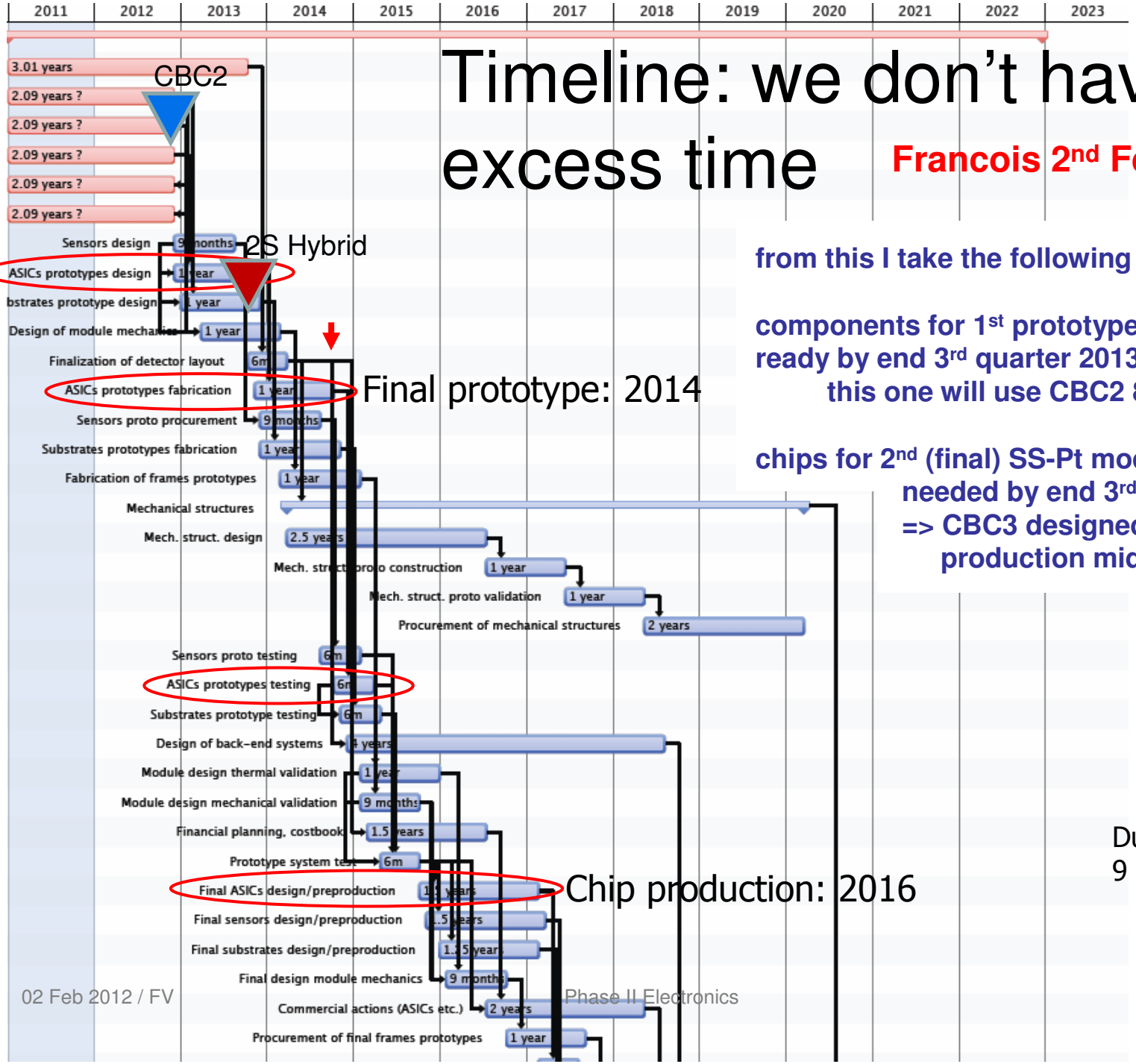


+3.3, +2.5, +1.2 V regulators

planning - short and longer term

Timeline: we don't have excess time

Francois 2nd Feb 2012

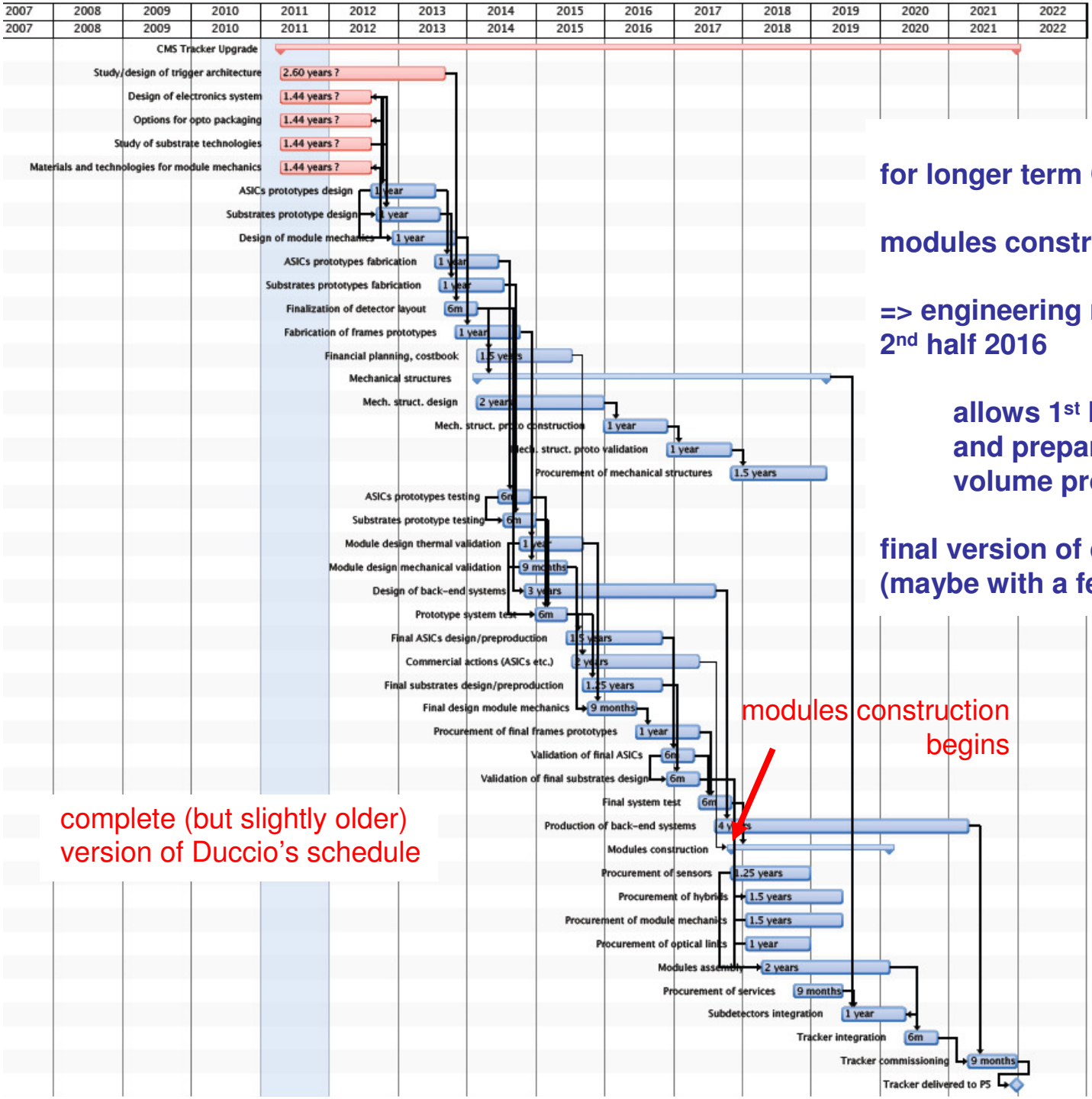


from this I take the following (CBC related):

components for 1st prototype SS-Pt module ready by end 3rd quarter 2013
this one will use CBC2 8-chip substrate

chips for 2nd (final) SS-Pt module prototype needed by end 3rd quarter 2014
=> CBC3 designed and in production mid 2014

Duccio's schedule
9 June 2011



complete (but slightly older) version of Duccio's schedule

modules construction begins

for longer term CBC related planning:

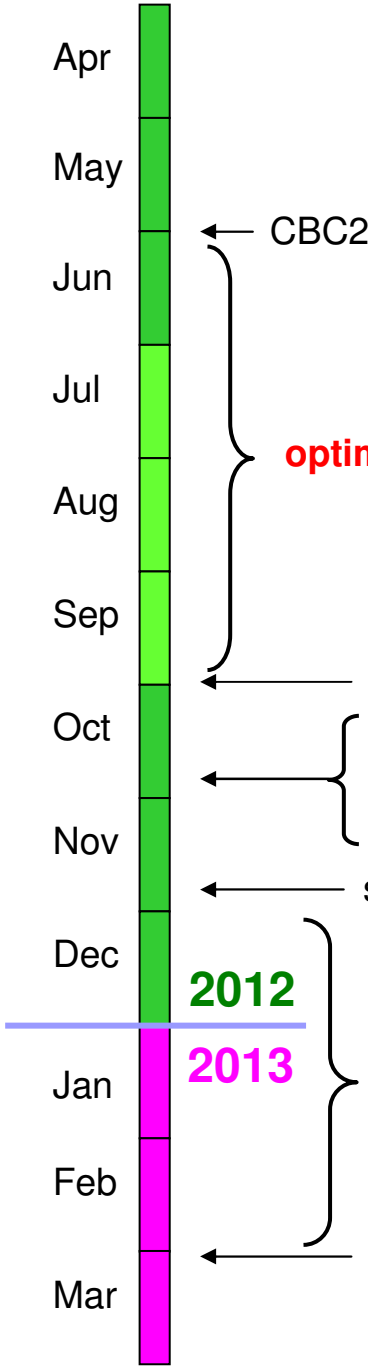
modules construction begins 2nd half 2017

=> engineering run of final version of chip 2nd half 2016

allows 1st half 2017 for final tests and preparations for launching of volume production

final version of chip should be CBC3 (maybe with a few, low-risk, minor tweaks)

short term planning



CBC2 submission

optimistic?

wafers back

CBC2 chips from diced wire-bond (XFEL) wafer available for test
(verify functionality before committing to bump-bonding assembly)
(can also use to finalise wafer probe test)

RAL will look after dicing of wirebond wafers

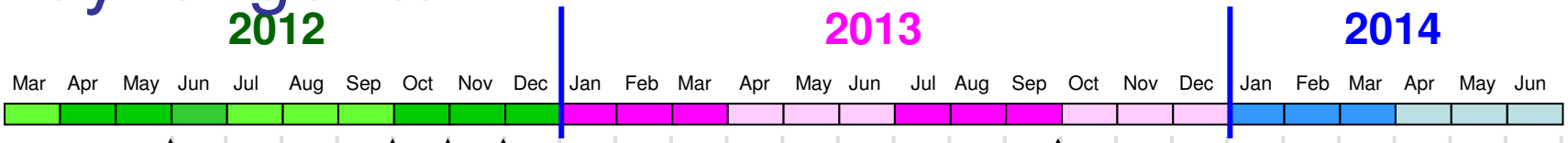
submit CBC2 C4 wafer + single(dual) chip substrate to assembly company

? how much time will this take ?

single(dual) chip substrates back from assembly and testing can begin

OBSERVATIONS/QUESTIONS	responsible (assumptions)
need single chip wire-bond test setup by October	UK
need single(dual) chip test substrates by November	CERN
who will look after dealing with assembly company?	
(arrangements, payment, ..)	?
(who are the assembly company?)	
development of single(dual) chip substrate test setup	UK
testing of single(dual) chip substrates	UK

slightly longer term



CBC2 submitted

wafers back

dice wirebond wafer and bond
single CBC2 to test board
(allows to verify functionality before committing to bump-bonding assembly)
(can also use to develop and verify wafer test hardware and procedure)

submit CBC2 C4 wafer + single
(dual) chip substrate for assembly

back from assembly and under test

2S-Pt module prototype assembly begins

=> submit tested C4 wafers for assembly on multi-chip substrates

? 3 months assumed

? 3 months assumed

2S-Pt module studies

broadly consistent with Duccio's schedule

plenty of uncertainty

e.g. how long will C4 chip/substrate assembly actually take? is it possible to be more accurate here?

PREPARATION/TESTING PERIODS

test setup for wirebond chip

single (dual) chip test setup development

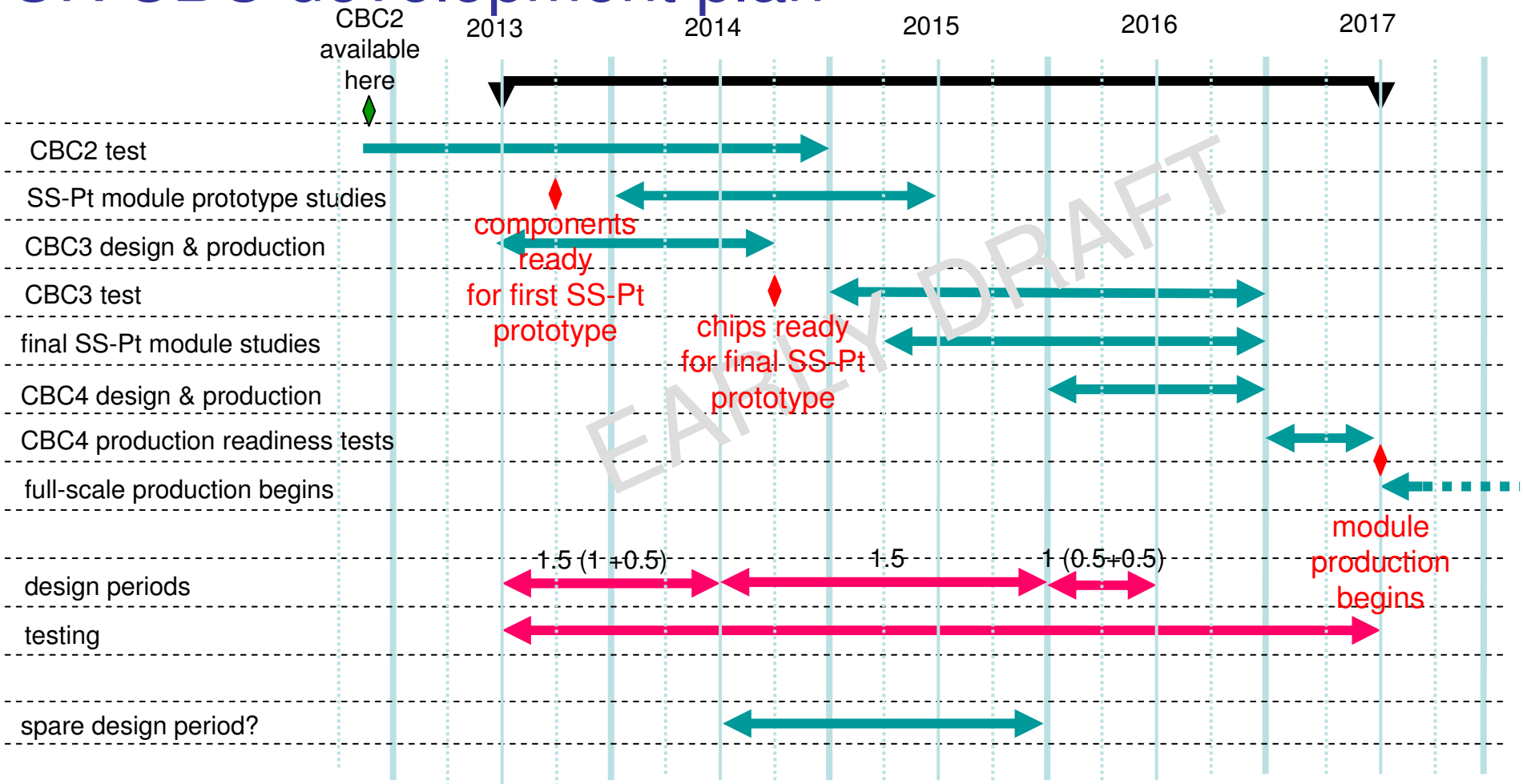
single (dual) chip testing

can continue

wafer probe test setup development

wafer probing

UK CBC development plan



- new CMS-UK upgrade proposal, for period mid 2013 onwards, currently under development
- to bring CBC development to production readiness - 4 years seems appropriate
  matches with schedule on previous slides - module production starts 2nd half 2017
- CBC design and manufacture periods ~ match module prototyping schedules

- 1.5 years microelectronics design effort could be available beginning mid 2014
  useful? (concentrator? (not unless final SS-Pt prototype delayed), PS system?...)

extra

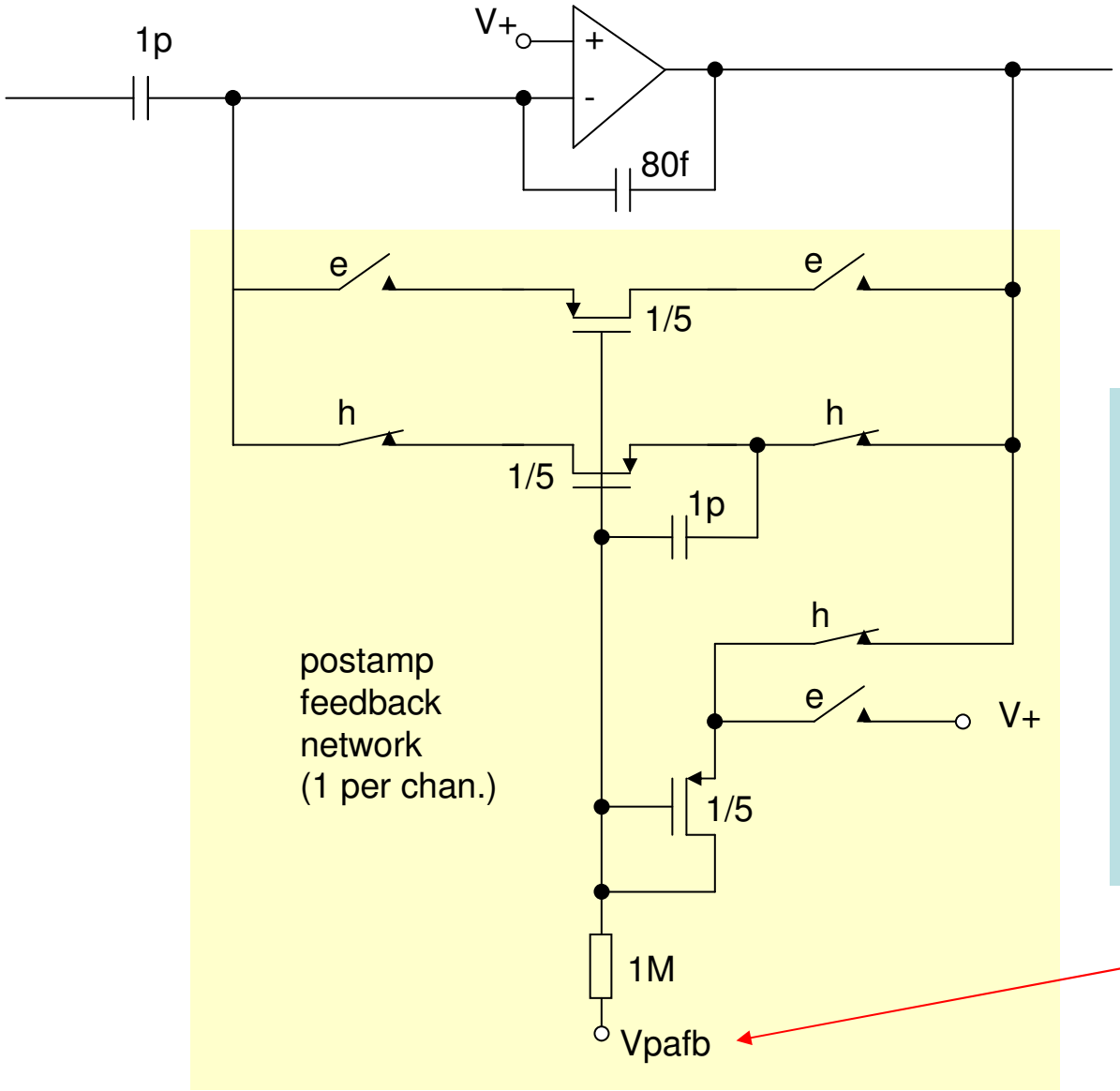
Process Layer Options Used

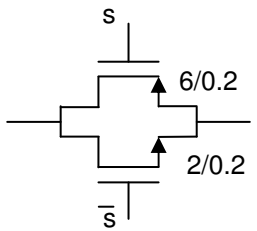
- Common:
  - Metal stack: 3-2-3 DM
  - 3.3V I/O PFET, 3.3V I/O NFET, Regular vt NFET, Regular vt PFET, OP N DIFF, OP PPOLY, RPres, single MiMs, dual MiMs, 3.3V DG devices, Vertical Natural Capacitor, No Dense SRAM, ESD devices, Standard IBM crack stops

- CBC specific:
  - Thin PI Triple Well NFET
  - C4 bond pads.

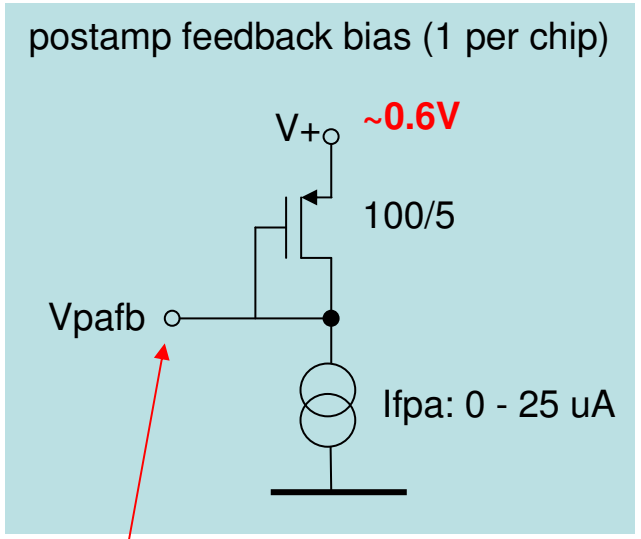
- XFEL specific:
  - Zero-Vt NFET Thick-oxide, Thick PI Triple Well NFET.

VPAFB postamp feedback - current situation



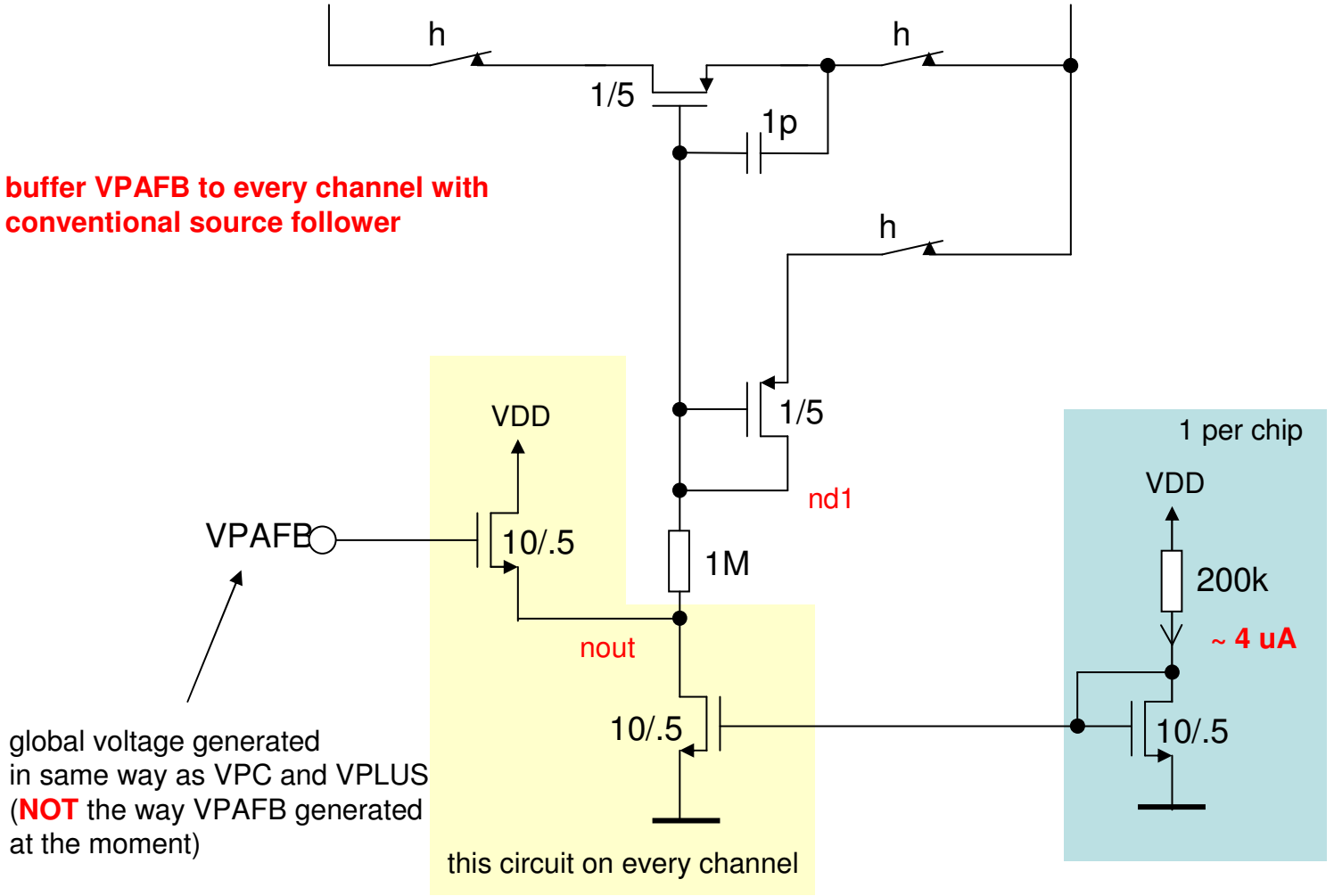


switch
implementation
(NMOS enclosed)

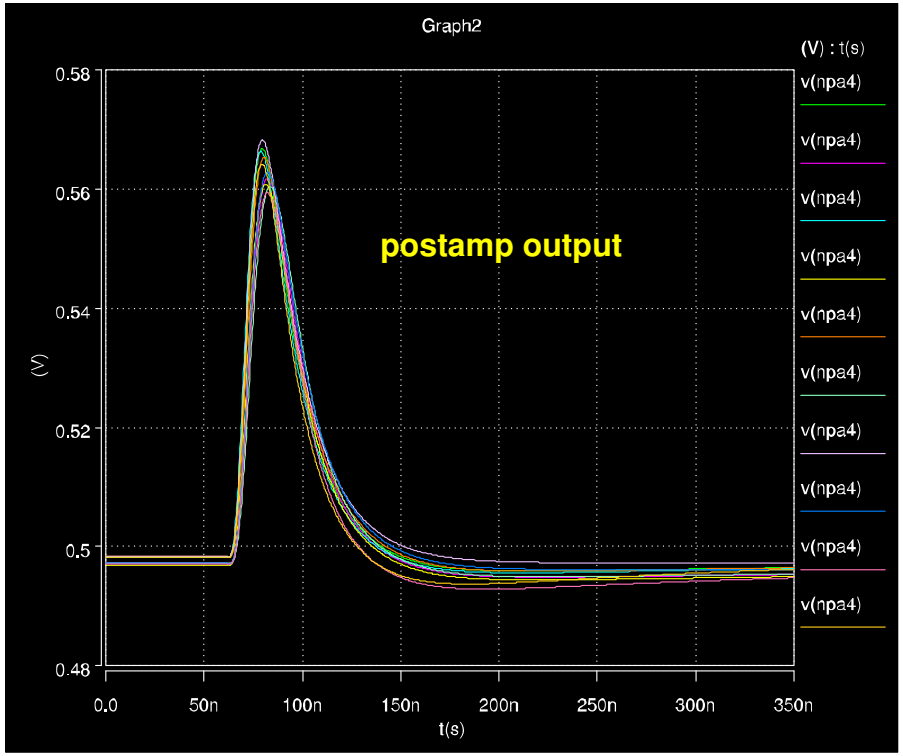


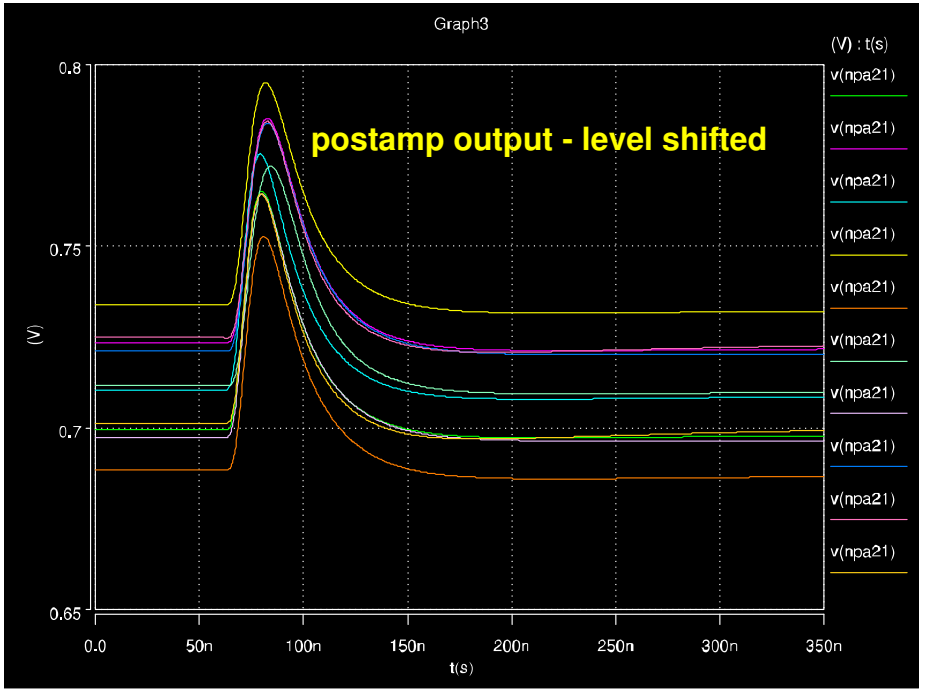
high impedance node can be influenced by CM movement at postamp O/P
1M / 128 = 8k

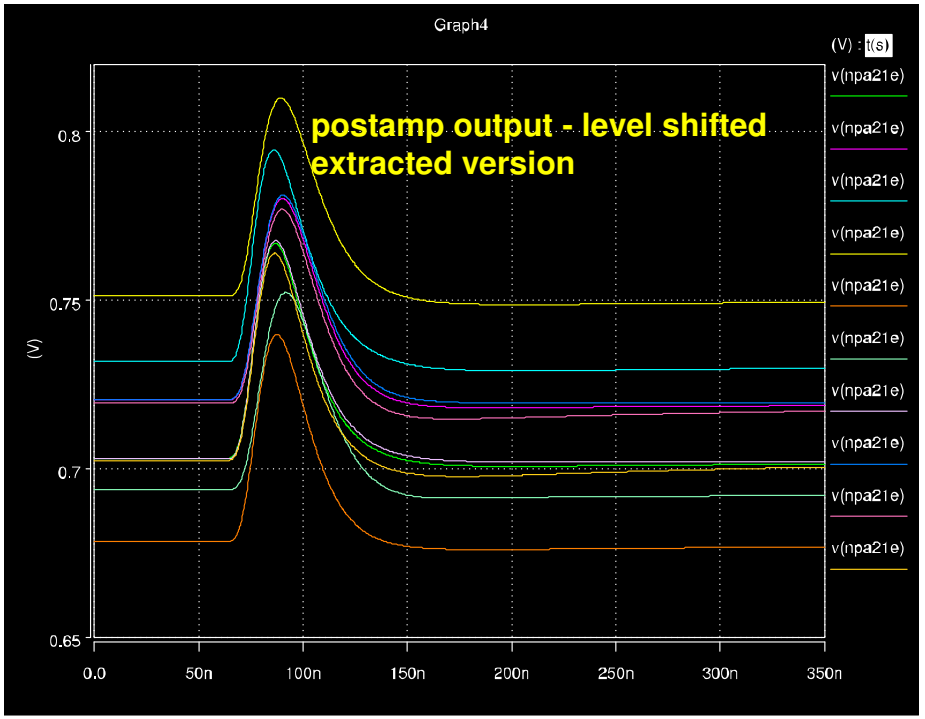
VPAFB - proposed solution



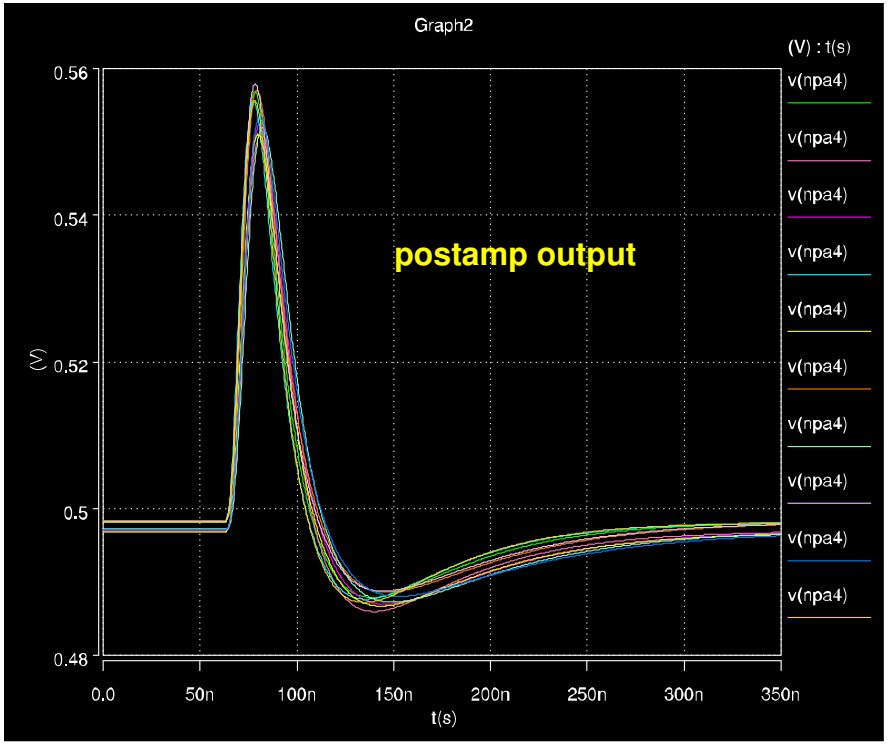
~ 5 uW / channel extra power

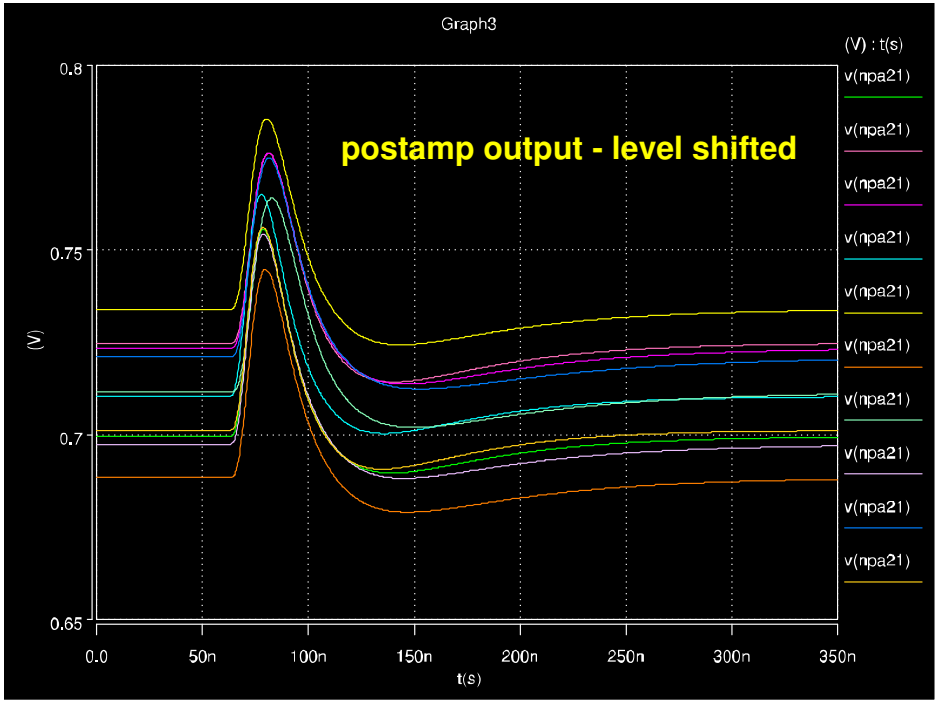


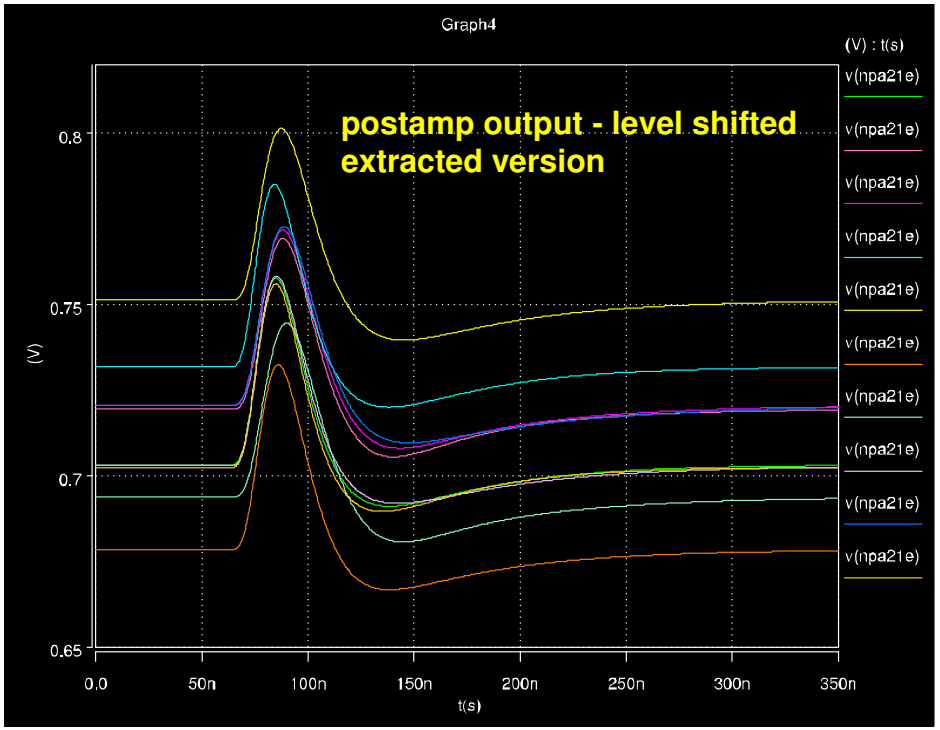




Vplus = 0.5
Vpafb = 0.5
all corners, +/- 40 deg.

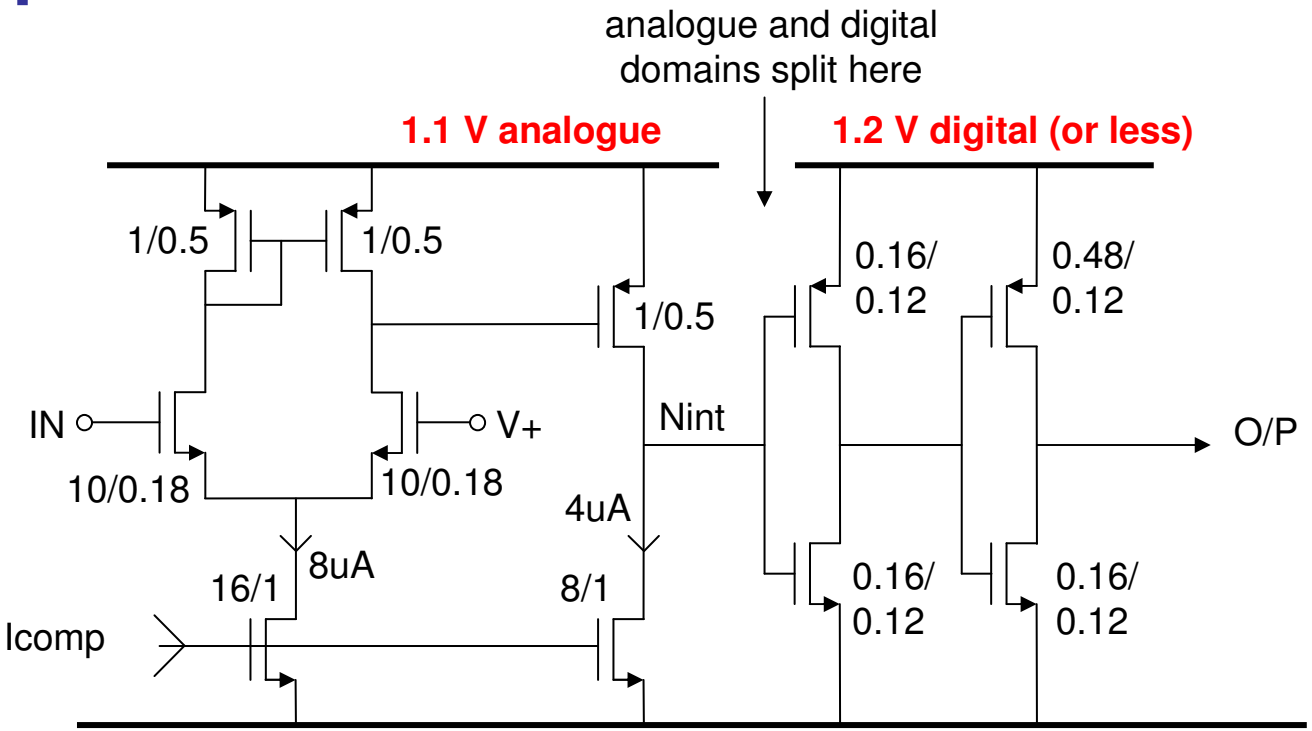


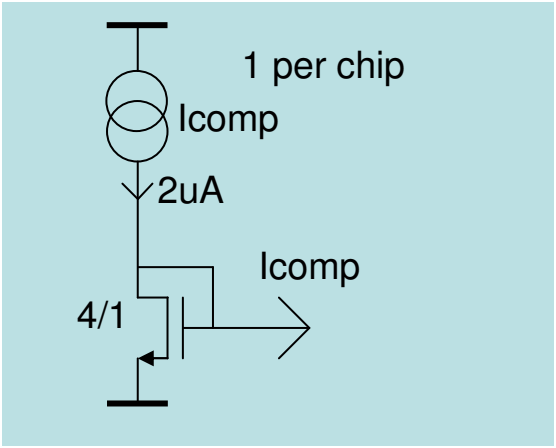




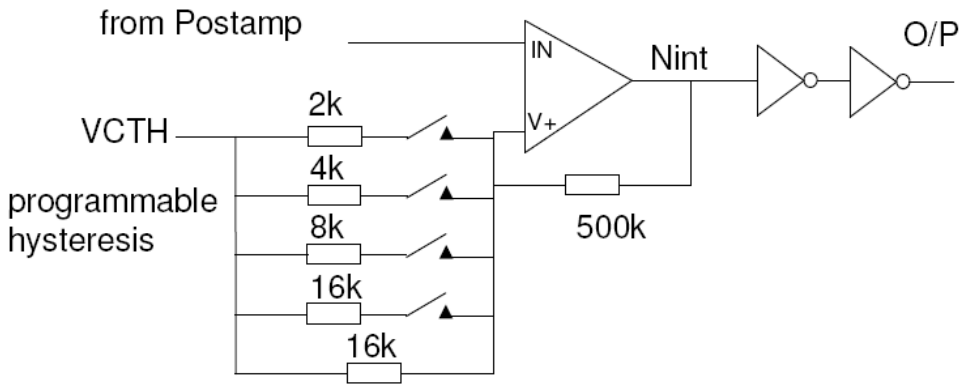
Vplus = 0.5
Vpafb = 0.25
all corners, +/- 40 deg.

comparator

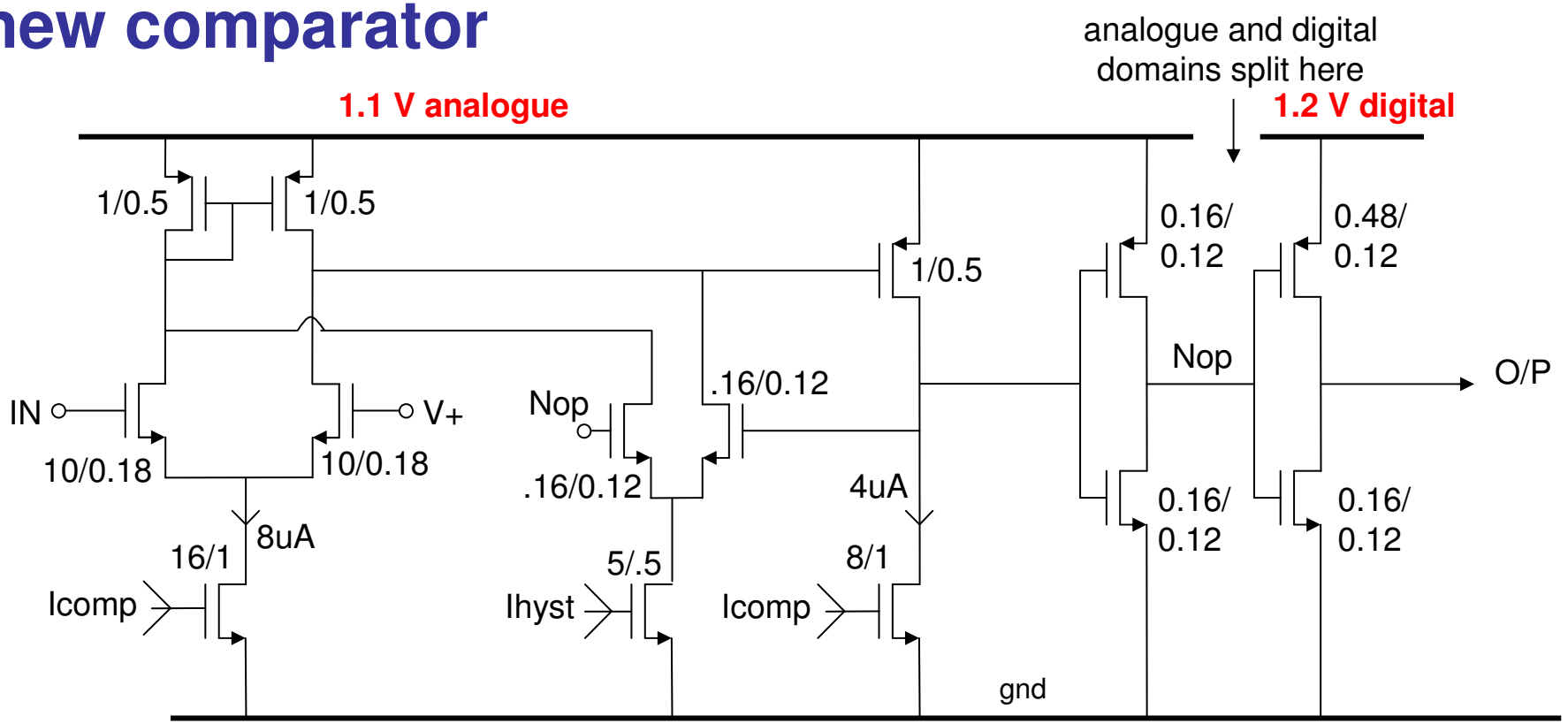


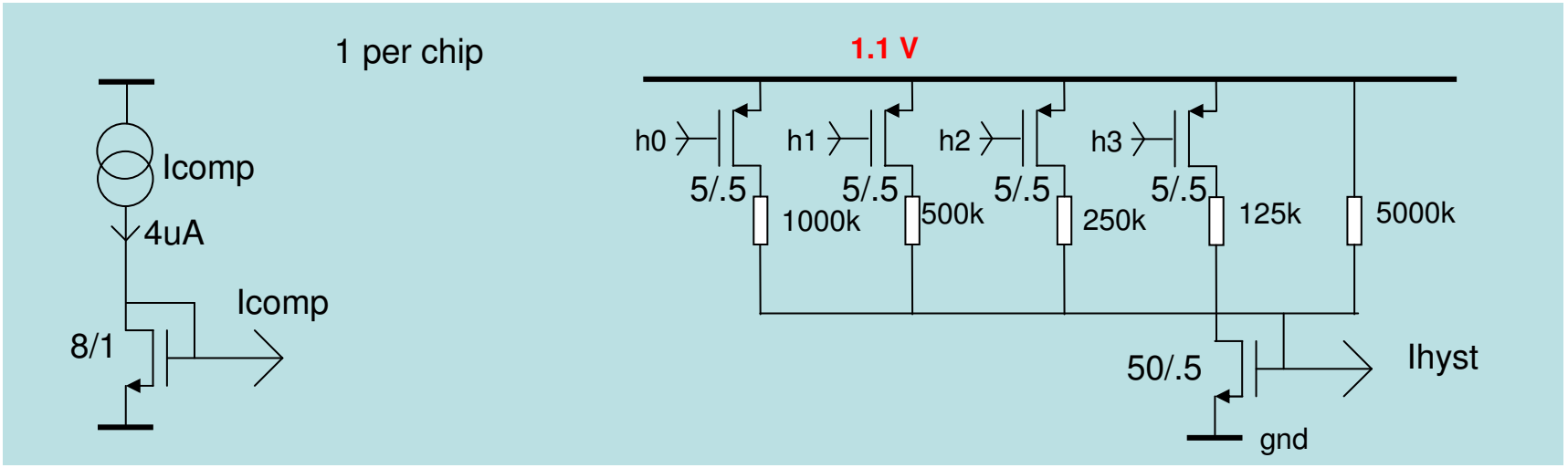


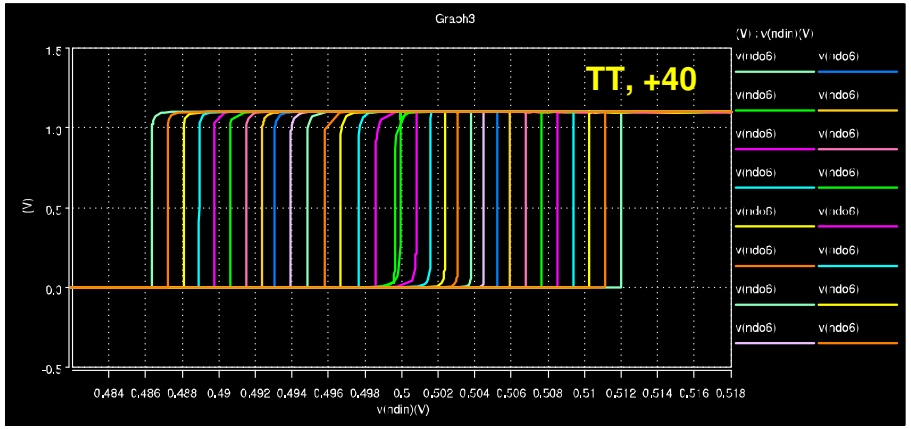
external hysteresis

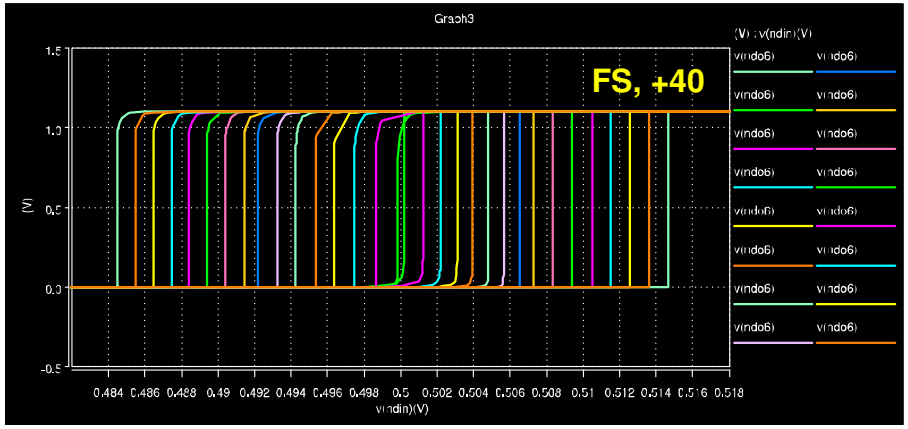


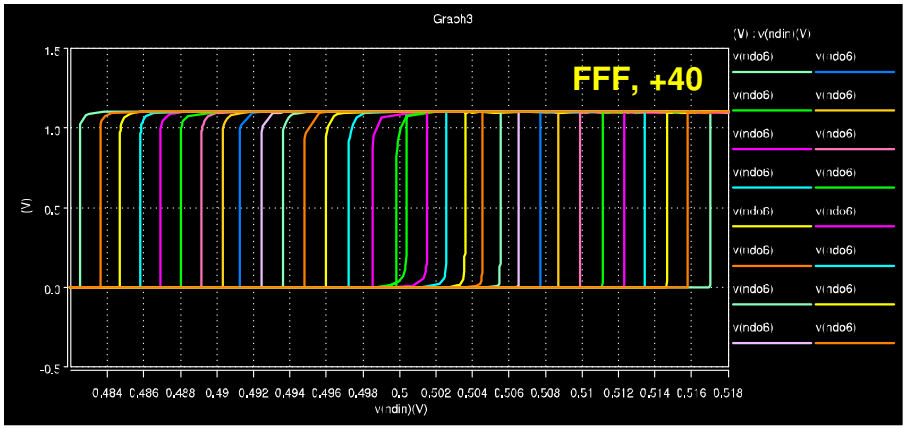
new comparator

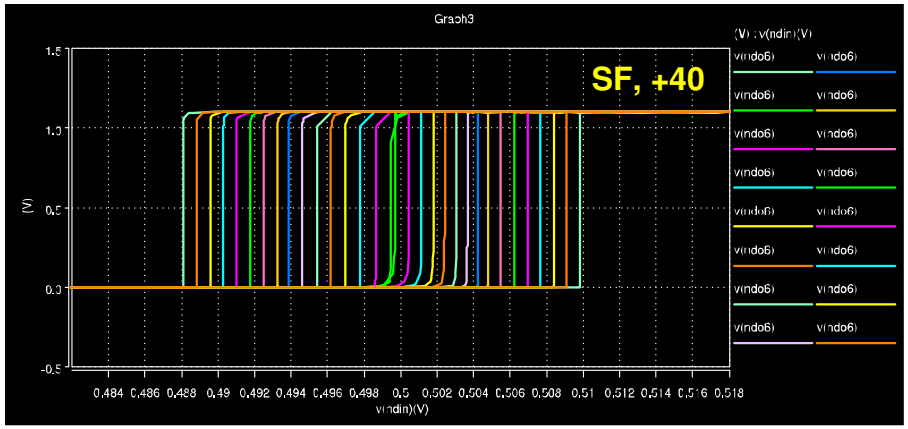


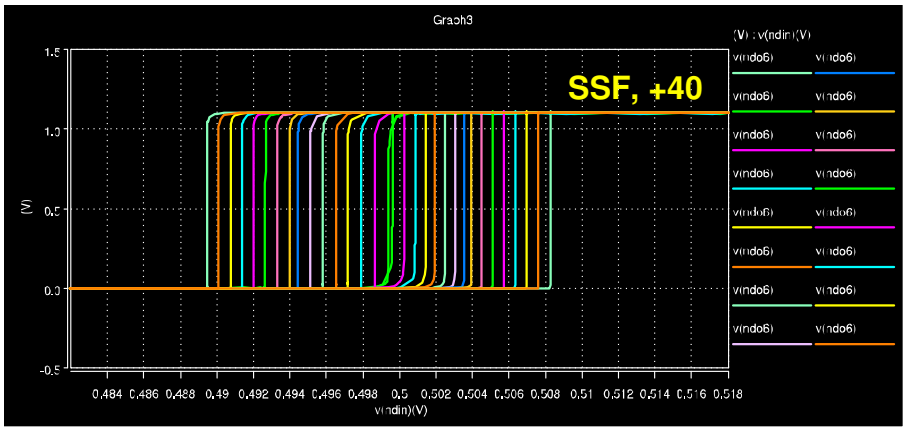










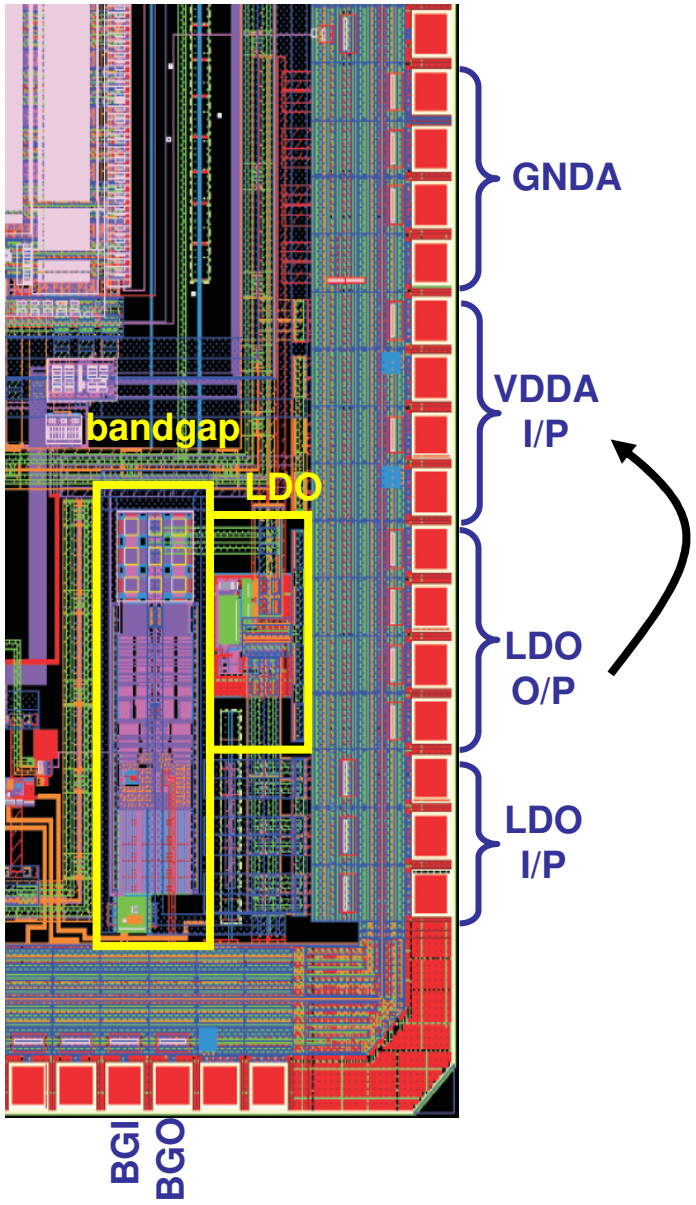


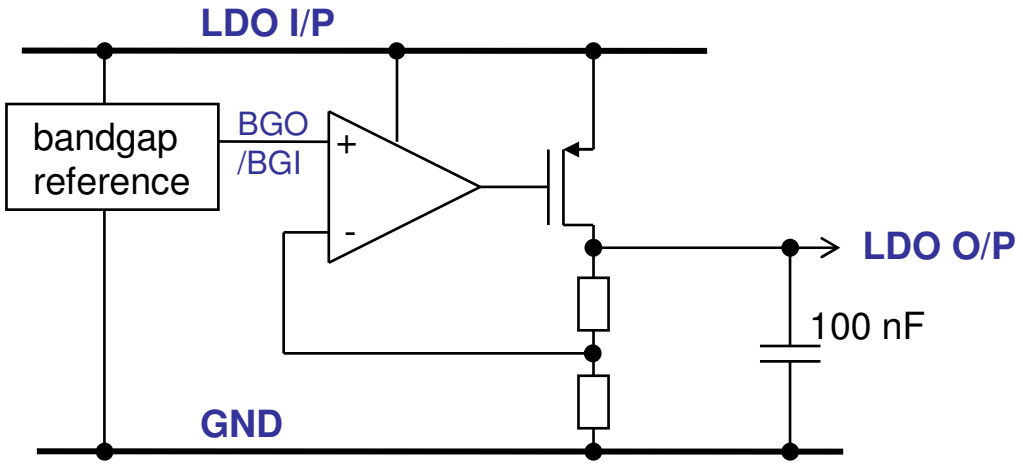
amount of hysteresis has process variations

but well-controlled

(debatable whether we need it at all but conservative to leave it in)

BGO/BGI bug fix





LDO included to provide clean, regulated rail to analog FE

~ 1.2 Vin, 1.1 Vout

uses CERN bandgap as Vref (0.6 V)

bandgap output (BGO) and input to LDO (BGI) taken to pads to allow to measure and/or over-ride

problem

bandgap powered by LDO I/P which can be noisy
noise feeds through to BGO

LDO - AC performance

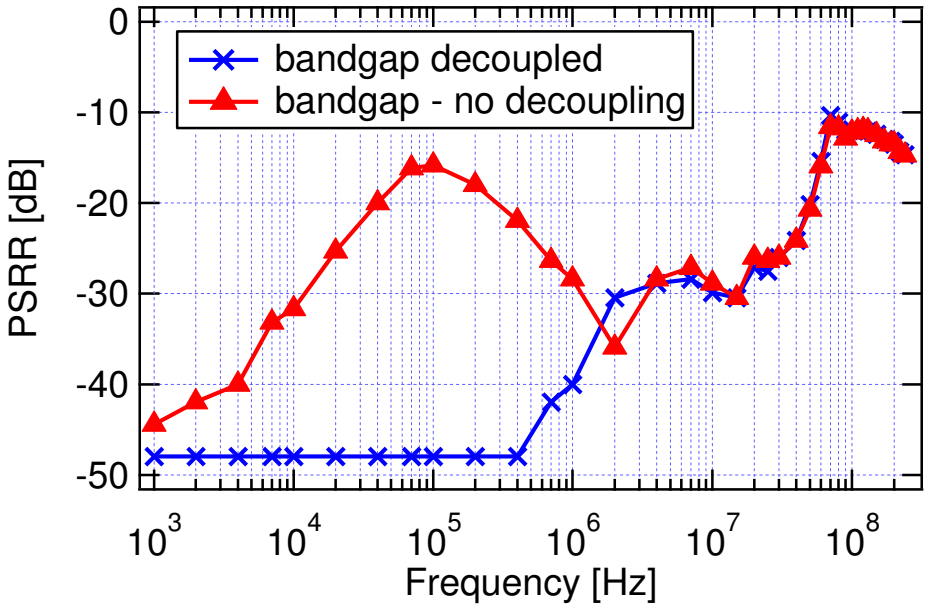
LDO O/P measured for 100 mV p-p sinewave ripple on 1.25 V DC LDO I/P

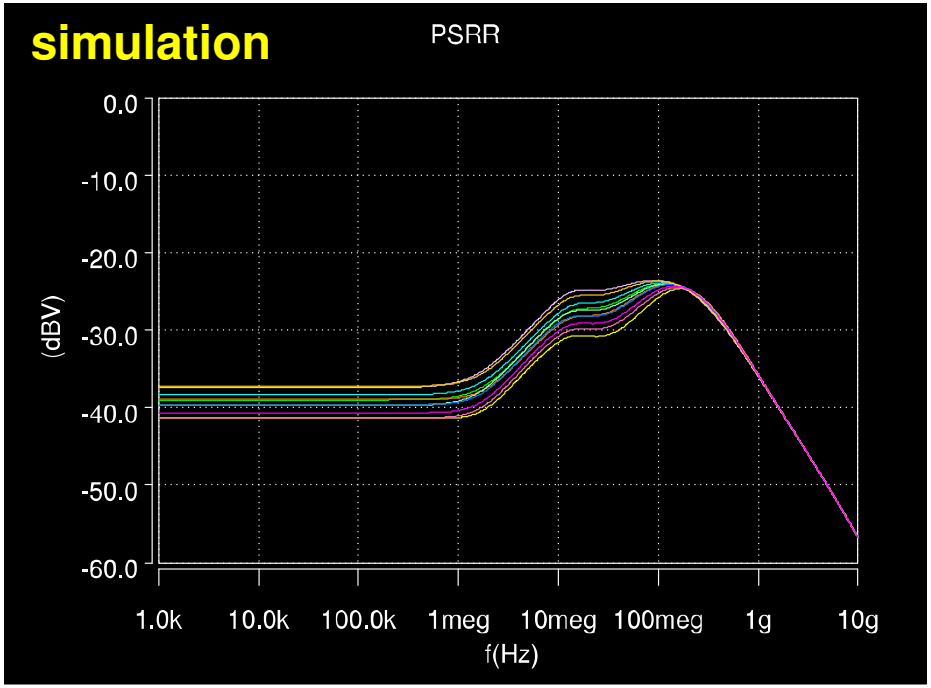
PSRR = 20.log[(LDO O/P)/(LDO I/P)]

measurement has some agreement with simulation
quite good rejection up to ~ 10 MHz

with bandgap decoupled get v.good rejection at low frequencies (signals at limit of measurability)

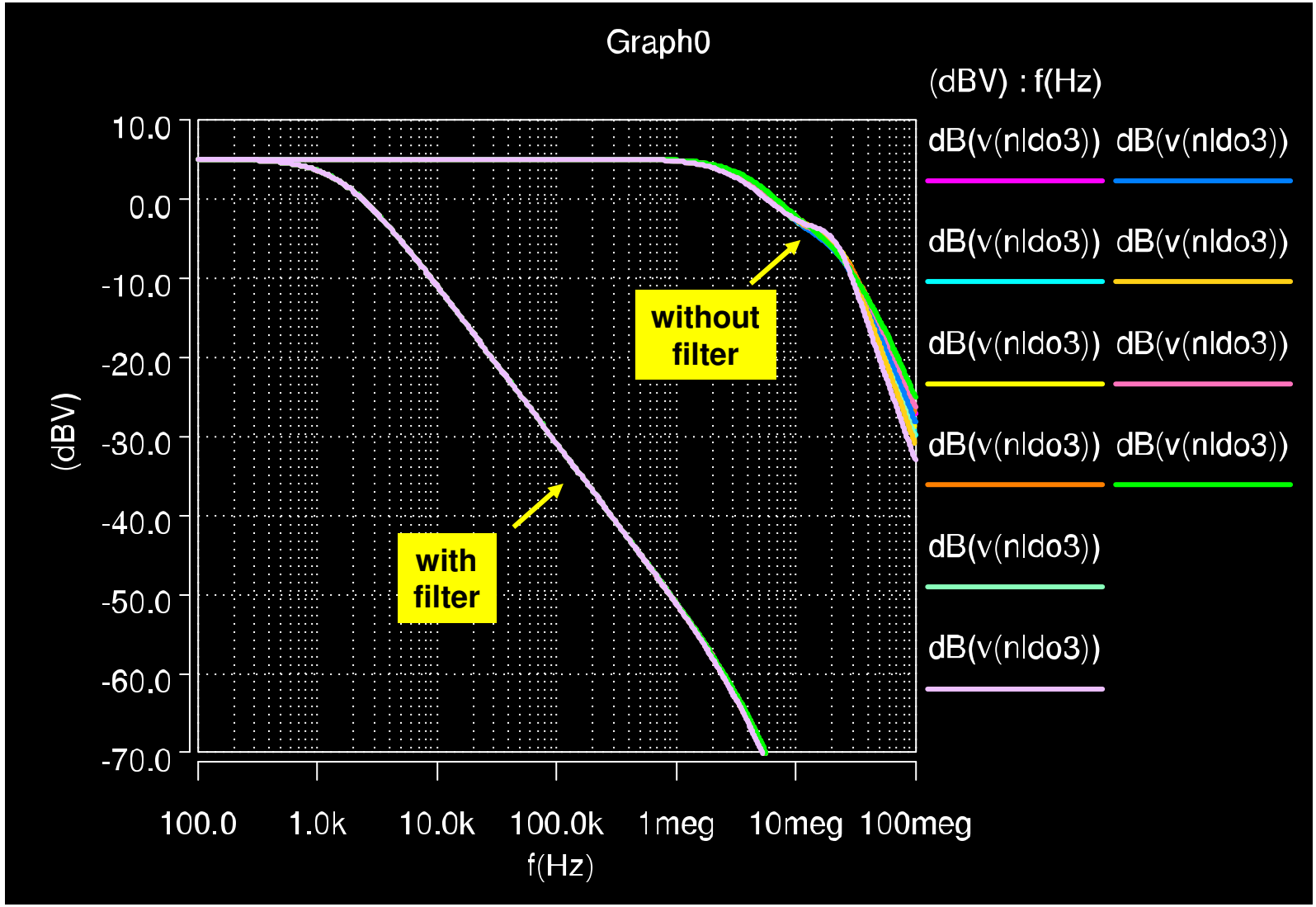
=> need to filter BandGap output voltage fed to LDO





passive RC filter - 1M x 100pF

LDO output dependence on simulated bandgap output frequency



should be good enough