# CBC status and plans

M.Raymond

# CBC prototype status

no new test results

concentrating now on CBC2 related work

things left to do

radiation tests still outstanding

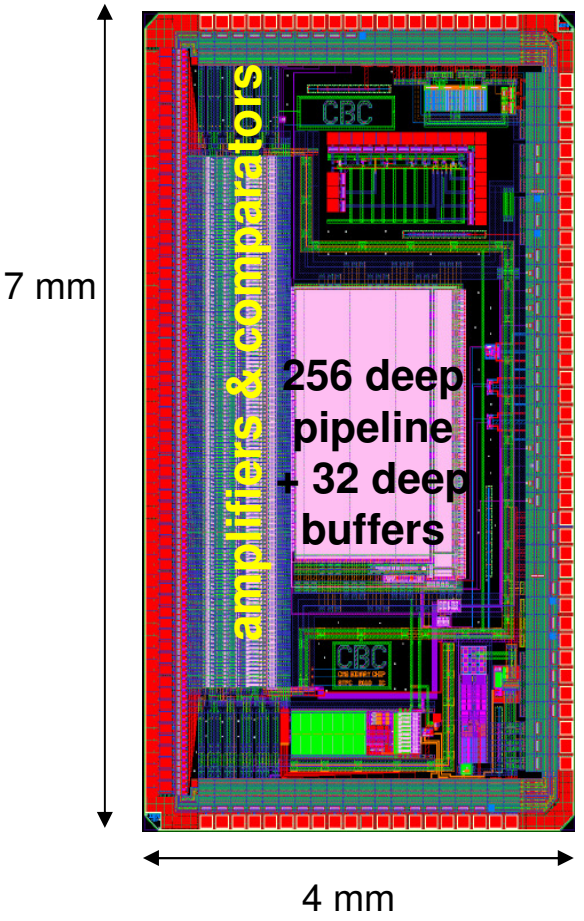
**ionising - would still hope to pursue**

single event - leave to CBC2 version?

future for this chip?

we have ~ 600 die (untested)
with workarounds they are perfectly usable
the only wire-bond version of this archtecture that will exist

can use (this year) to begin development of wafer probe test
confirm with CBC2 when available



# irradiation test plans - CBC prototype

laptop based CBC interface under development
portability will make irradiation procedure easy
should be adaptable for easily adaptable for CBC2

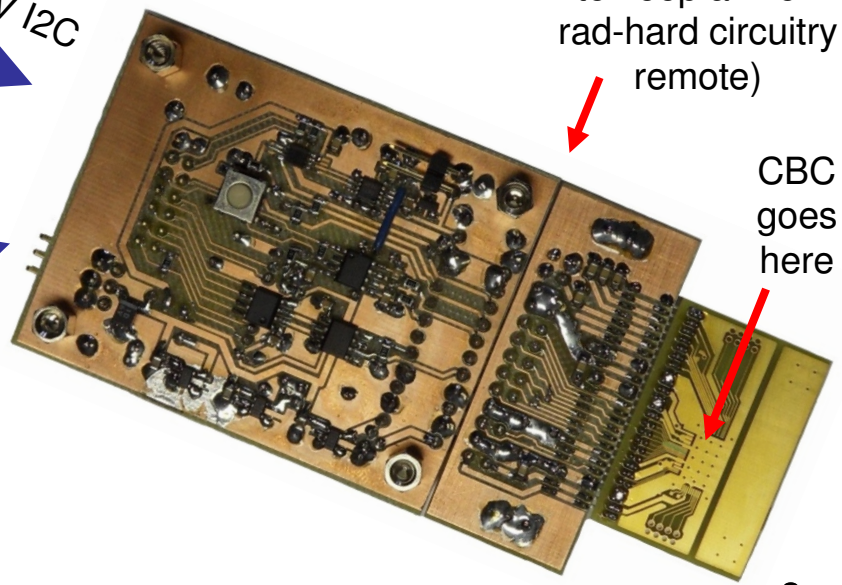
USB FPGA module

LVDS, 3.3V I2C

+/- 5V

front end can be separated here (cable interconnect to keep all non rad-hard circuitry remote)

CBC goes here

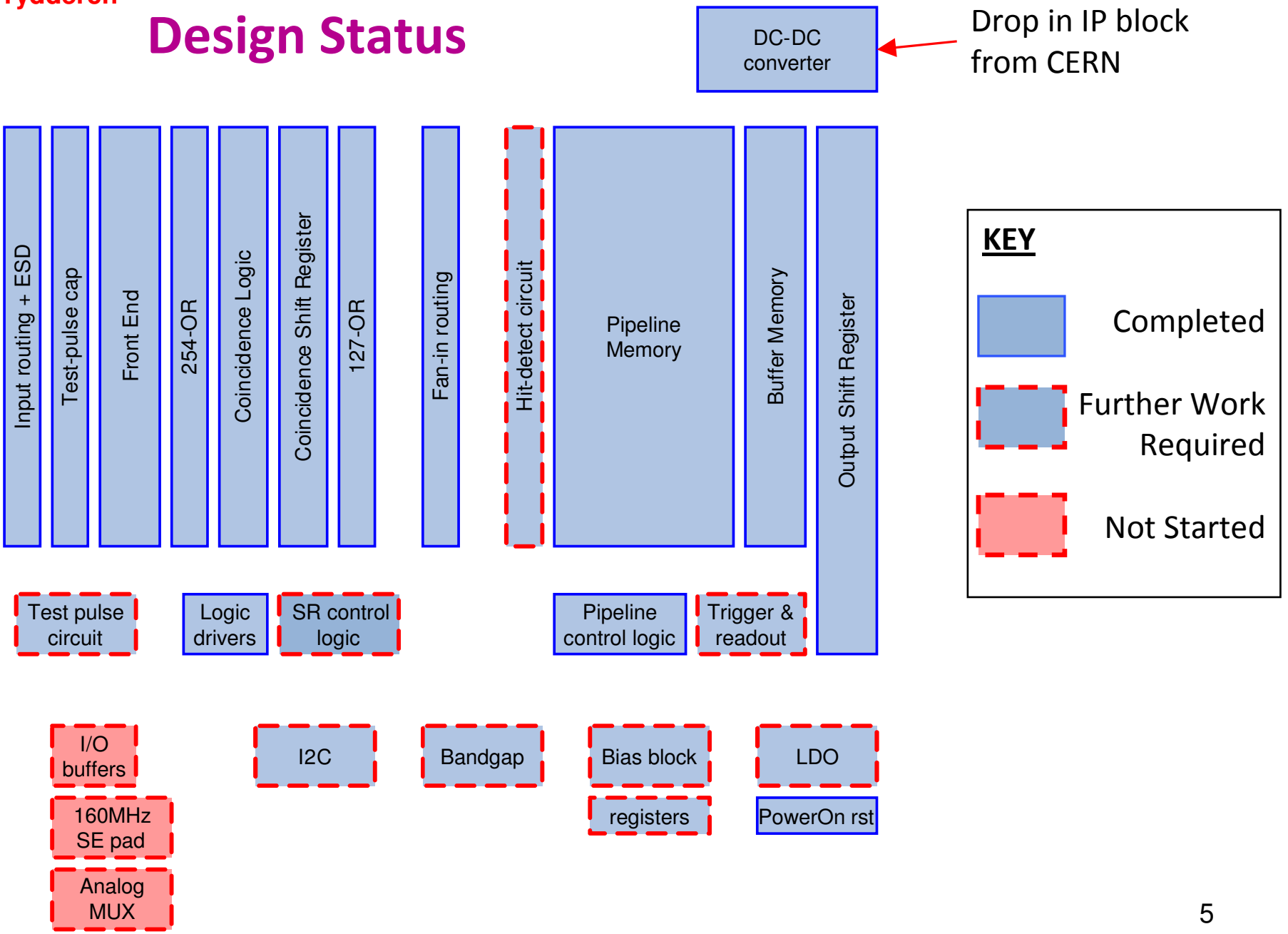


# CBC2 design and submission status

M Prydderch

M Prydderch

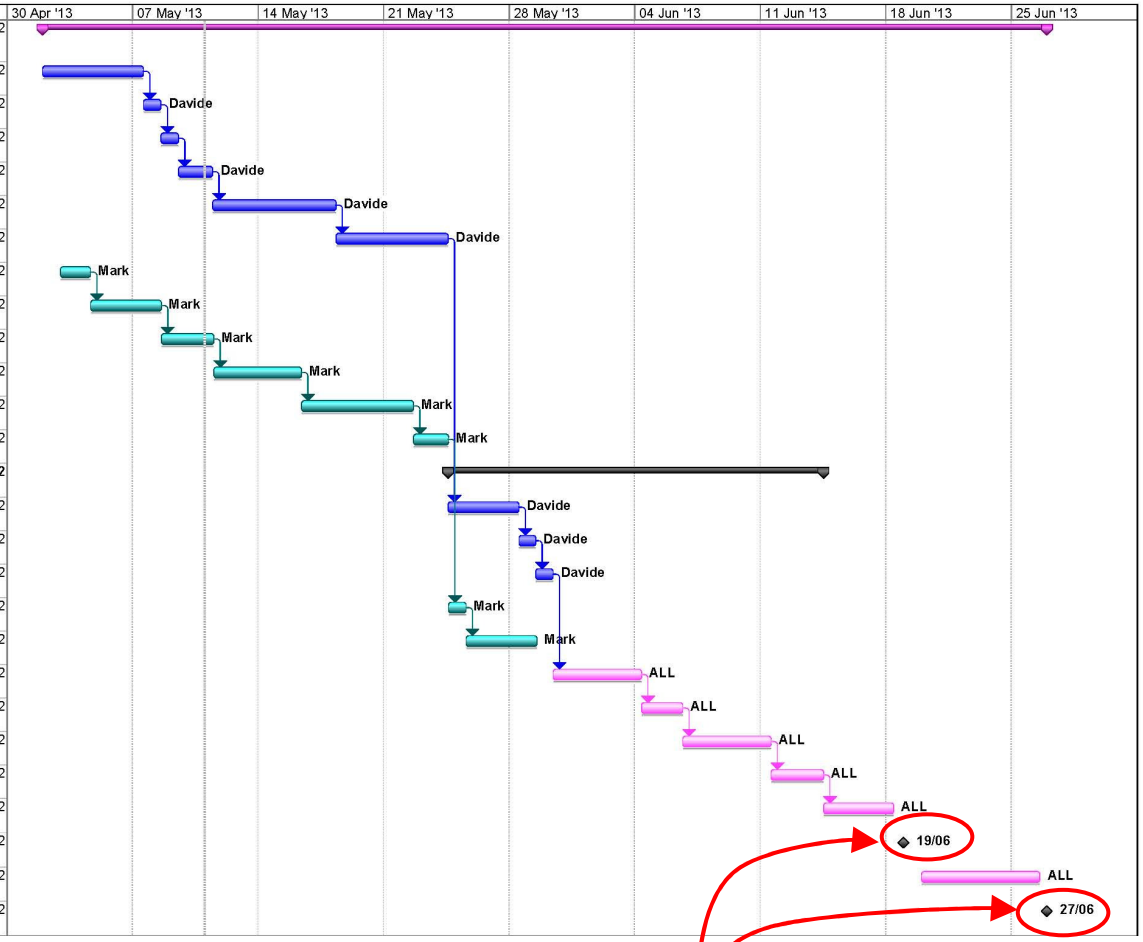
# Design Status



M Prydderch

# Remaining Schedule

| ID | Task Name | Duration | Start | Finish |
|---|---|---|---|---|
| 1 | **256 channel bump-bondable CBC** | 43.24 days? | Wed 02/05/12 | Wed 27/06/12 |
| 2 | WIT | 4 days | Wed 02/05/12 | Mon 07/05/12 |
| 3 | Input fan In layout | 1 day | Mon 07/05/12 | Tue 08/05/12 |
| 4 | Memory Fan In Layout | 1 day? | Tue 08/05/12 | Wed 09/05/12 |
| 5 | Double SR readout count | 2 days | Wed 09/05/12 | Fri 11/05/12 |
| 6 | Add Extra biases to Bias block | 5 days | Fri 11/05/12 | Fri 18/05/12 |
| 7 | Add extra registers to I2C | 5 days | Fri 18/05/12 | Thu 24/05/12 |
| 8 | Layout OR Register Control Logic | 2 days | Thu 03/05/12 | Fri 04/05/12 |
| 9 | Layout New Hit Detect | 2 days | Fri 04/05/12 | Tue 08/05/12 |
| 10 | Simulate pipeline with command word | 3 days | Tue 08/05/12 | Fri 11/05/12 |
| 11 | Check Overflow Error Bit Logic | 3 days | Fri 11/05/12 | Wed 16/05/12 |
| 12 | Bias Monitor Select Mux | 5 days | Wed 16/05/12 | Tue 22/05/12 |
| 13 | Check Test Pulse Generator | 2 days | Tue 22/05/12 | Thu 24/05/12 |
| 14 | **Top Level Assembly & Checks** | **16 days?** | **Thu 24/05/12** | **Thu 14/06/12** |
| 15 | Place IO Circuits | 2 days | Thu 24/05/12 | Mon 28/05/12 |
| 16 | Drop in new DC-DC converter | 1 day? | Mon 28/05/12 | Tue 29/05/12 |
| 17 | Place Bandgap & add Output Filter | 1 day? | Tue 29/05/12 | Wed 30/05/12 |
| 18 | Place LDO & add output resistance | 1 day? | Thu 24/05/12 | Fri 25/05/12 |
| 19 | Place Test Pulse generator | 2 days | Fri 25/05/12 | Tue 29/05/12 |
| 20 | Top Level Routing | 3 days | Wed 30/05/12 | Mon 04/06/12 |
| 21 | Top Level Fill | 3 days | Mon 04/06/12 | Wed 06/06/12 |
| 22 | Top Level DRC | 3 days | Wed 06/06/12 | Mon 11/06/12 |
| 23 | Top Level LVS | 3 days | Mon 11/06/12 | Thu 14/06/12 |
| 24 | **Design Review Preparation** | 2 days | Thu 14/06/12 | Mon 18/06/12 |
| 25 | **Final Design Review** | 0 days | Tue 19/06/12 | Tue 19/06/12 |
| 26 | **Post Review Corrections** | 5 days | Wed 20/06/12 | Tue 26/06/12 |
| 27 | **Submission** | 0 days | Wed 27/06/12 | Wed 27/06/12 |




NOTE: Dates have shifted by 1 month

# Die Arrangement


- Reticles/Wafer ~115
- 1 of each chip per reticle
- Room for test structures.

# Joint CMS & XFEL LPD Wafer Submission Plan

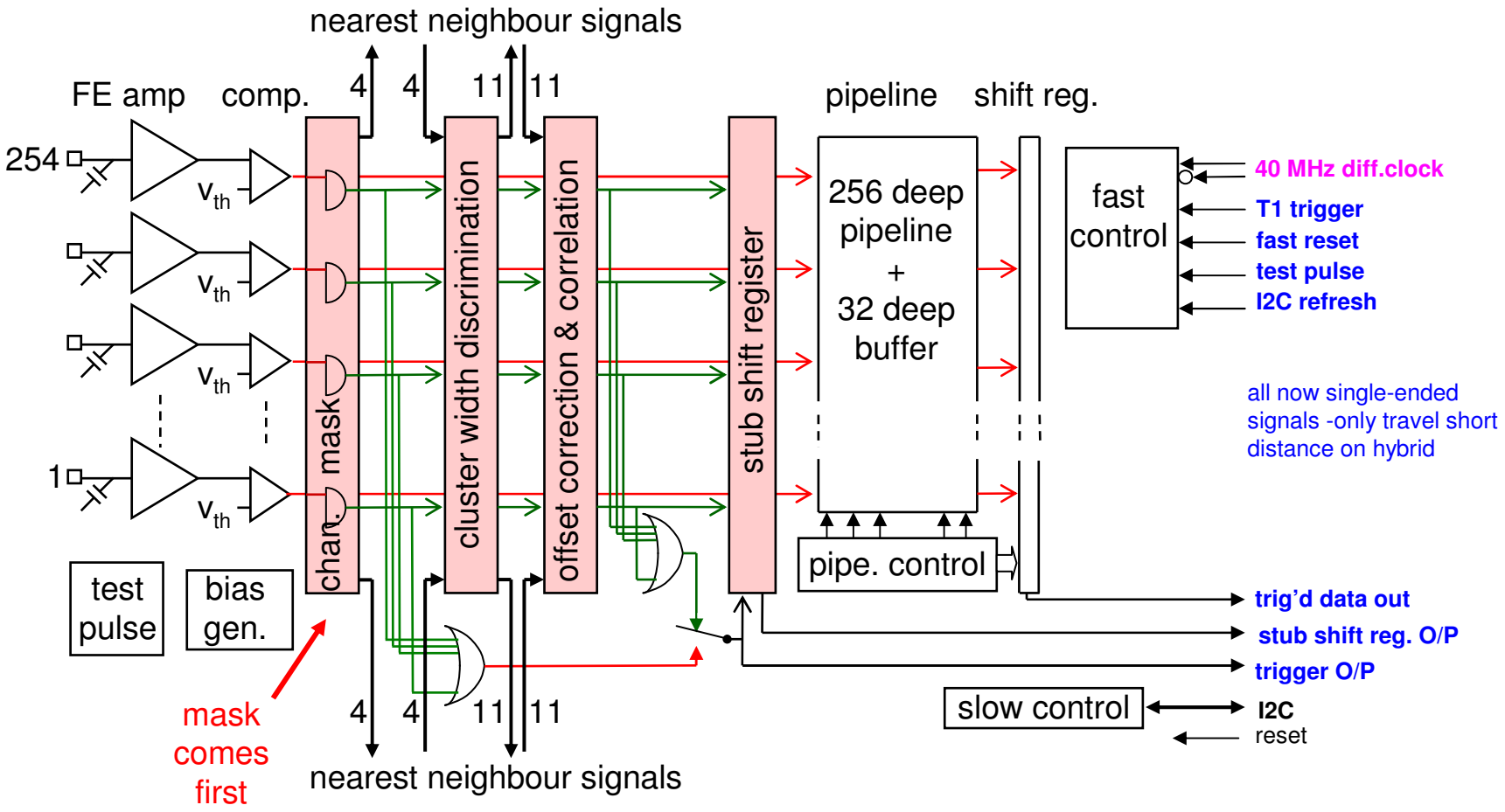
M Prydderch

- Planned Submission Date: ~~4/06/2012~~ Now 27/06/2012
- Wafer Share:
  - 8 Wafers for CMS with C4 finish & Bump balls (leaded)
    - 1 Wafer for Wafer Probe set up
    - 2 Wafer for single chip modules
    - 4 for the multi-chip substrates (assuming 8 chips/substrate & only 67 KGD/wafer gives 8 substrates per wafer allowing 15 full SS-Pt modules from 4 wafers)
    - 1 Wafer contingency
  - 6 Wafers for XFEL LPD with normal finish
  - 4 wafers for TOPFET with normal finish

# other CBC2 items

# CBC2 architecture

for reference - nothing new here




**blocks associated with Pt stub generation**

**channel mask**: block noisy channels (but not from pipeline)

**cluster width discrimination**: exclude wide clusters

**offset correction and correlation**: correct for phi offset across module and correlate between layers

**stub shift register**: test feature - shift out result of correlation operation at 40 MHz

**fast OR at comp. O/P and correlation O/P**: - can select either to transmit off-chip
for normal operation choose correlation O/P

# DC-DC

new version of 2.5 -> 1.2 DC-DC converter (F. Faccio, S. Michelis)

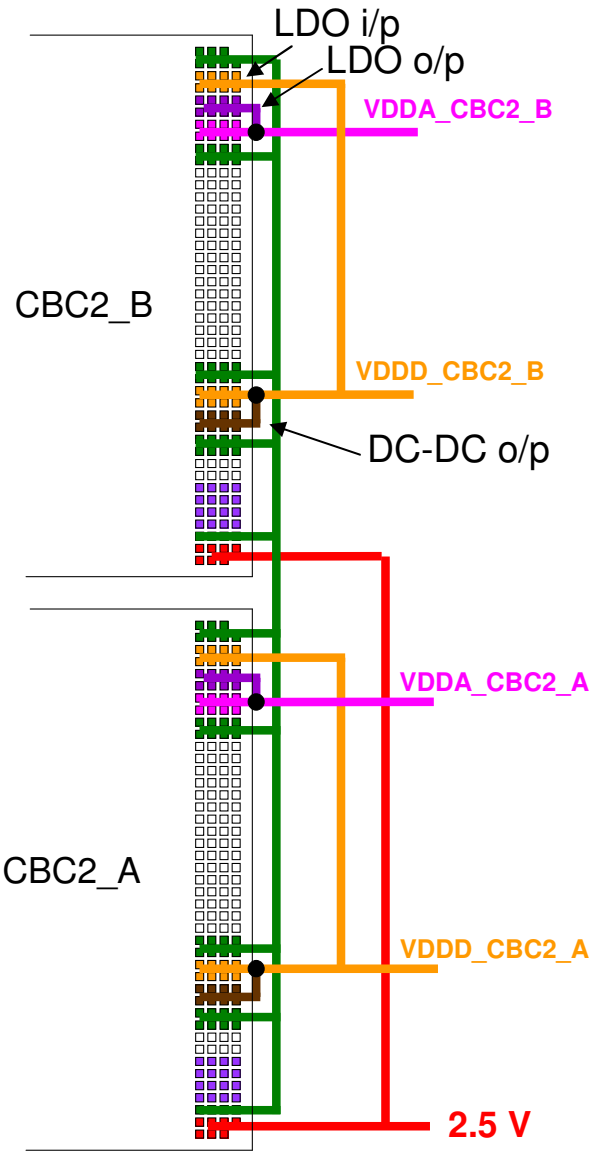
- enclosed layout transistors
- slower transition times for signals to off-chip capacitors
  - substantial reduction in voltage spikes
- layout compatible with existing version

for details see S. Michelis PWG talk - 26th April

https://indico.cern.ch/getFile.py/access?contribId=1&resId=0&materialId=slides&confId=186428

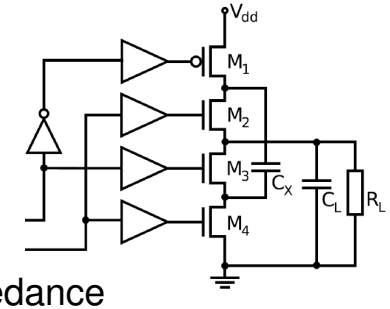
currently waiting for design block – expected soon

# CBC2 powering scheme on 2-chip substrate




backend pads as viewed through CBC2 substrate

after some thinking and discussion with Georges we have arrived at this scheme




2.5 V common to both chips

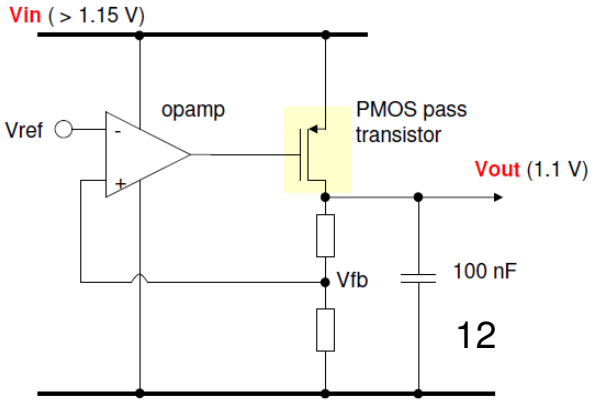
if DC-DC not clocked then output -> high impedance
=> DC-DC o/p can be shorted to VDDD
VDDD can be provided externally if not using DC-DC

connect VDDD directly to LDO i/p
keeping separate would allow to run VDDD at low voltage
but no significant power advantage to doing this

connect LDO o/p directly to VDDA
if want to supply VDDA externally then provide at slightly higher voltage than normal LDO o/p level

=> LDO shuts down (pass transistor turns off)
verified on CBC prototype

**=> no jumpers required at all on substrate**



# what to do with 160 MHz signals

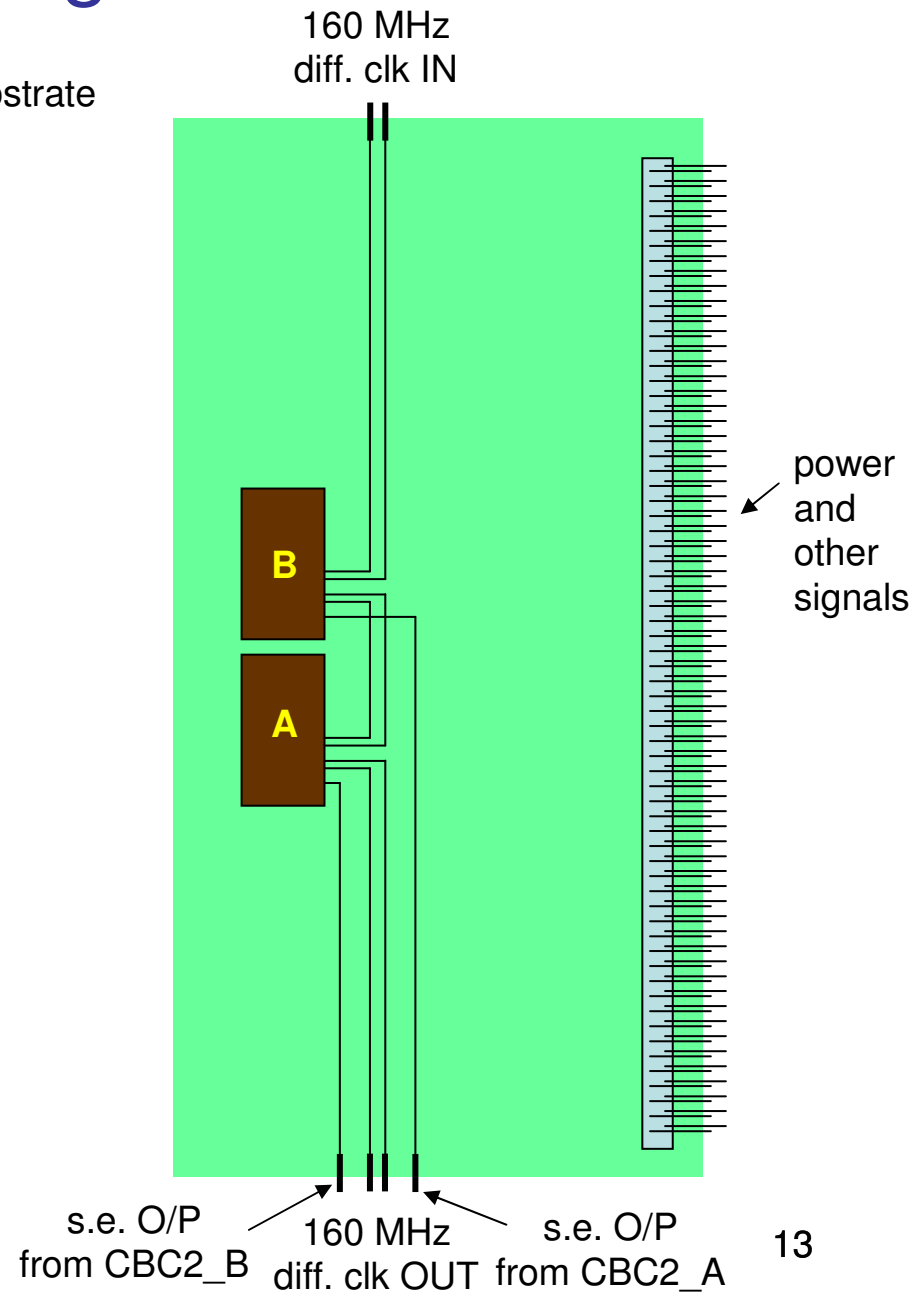
want to study effects of routing fast signals across substrate

one possible approach is shown

fast signal brought in at top edge

- feeds diff input of chip B
- diff output of chip B feeds diff input of chip A
- diff output of chip A routed to bottom edge
- single-ended outputs of chips A and B both routed to bottom edge

any other ideas?



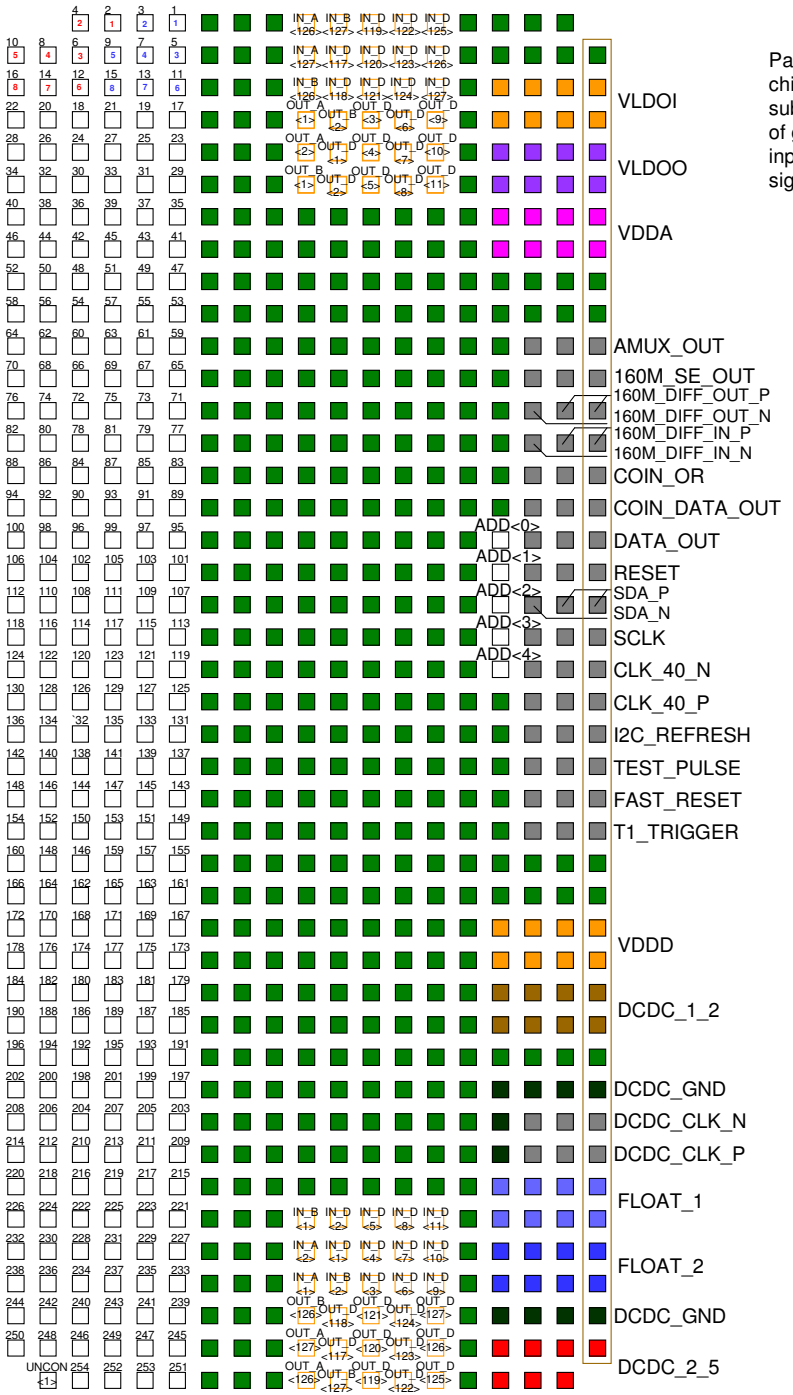
# CBC2 pad changes

had to shift interchip digital signal groups one further column to right

solves problems of fitting in ESD protection and pitch adaption

increases separation between input pads and digital signals

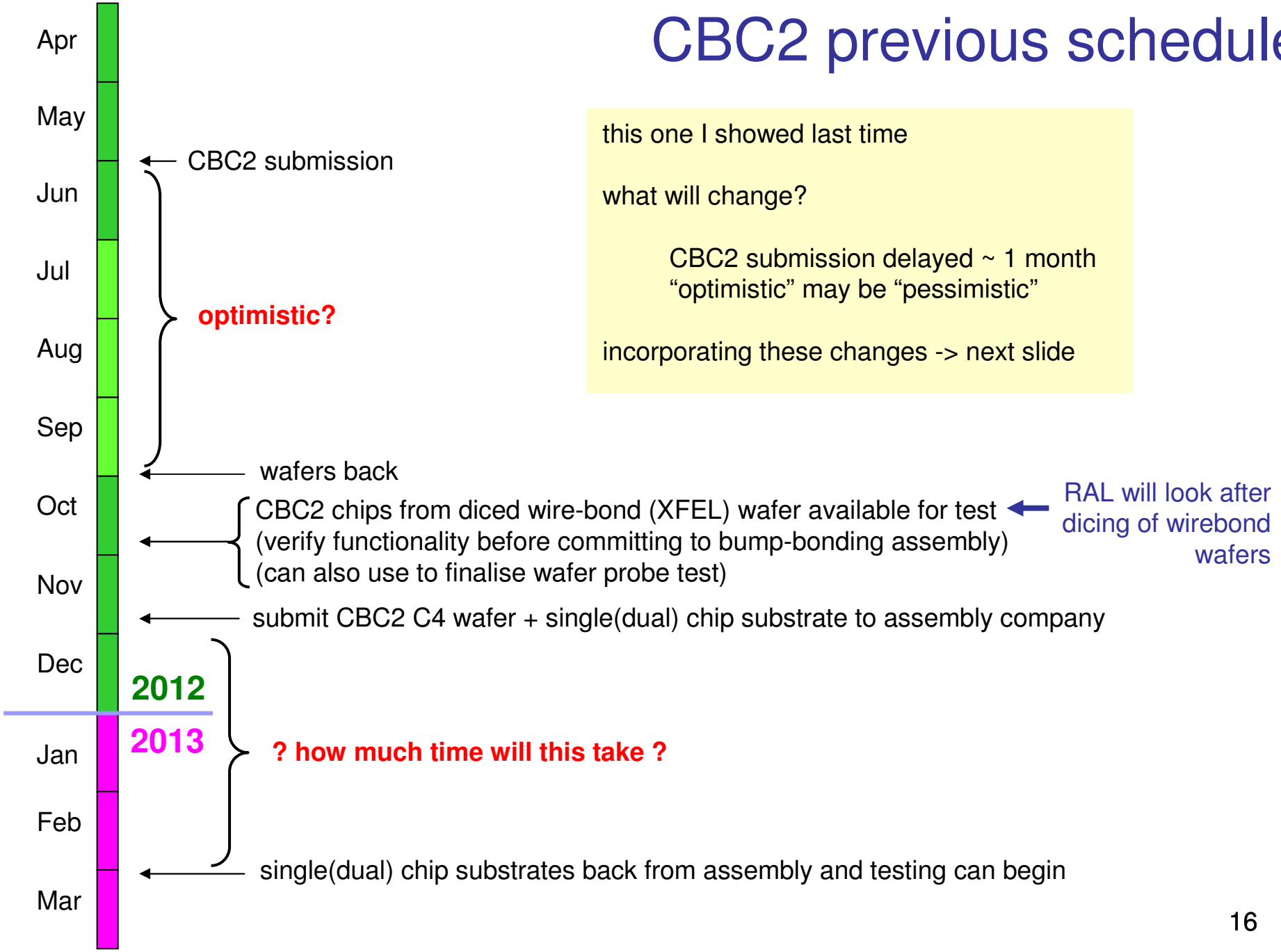
Georges notified




Pads as viewed through chip (i.e. pad pattern on substrate). Now 3 columns of ground pads between inputs and interchip digital signals.

# planning

# CBC2 previous schedule



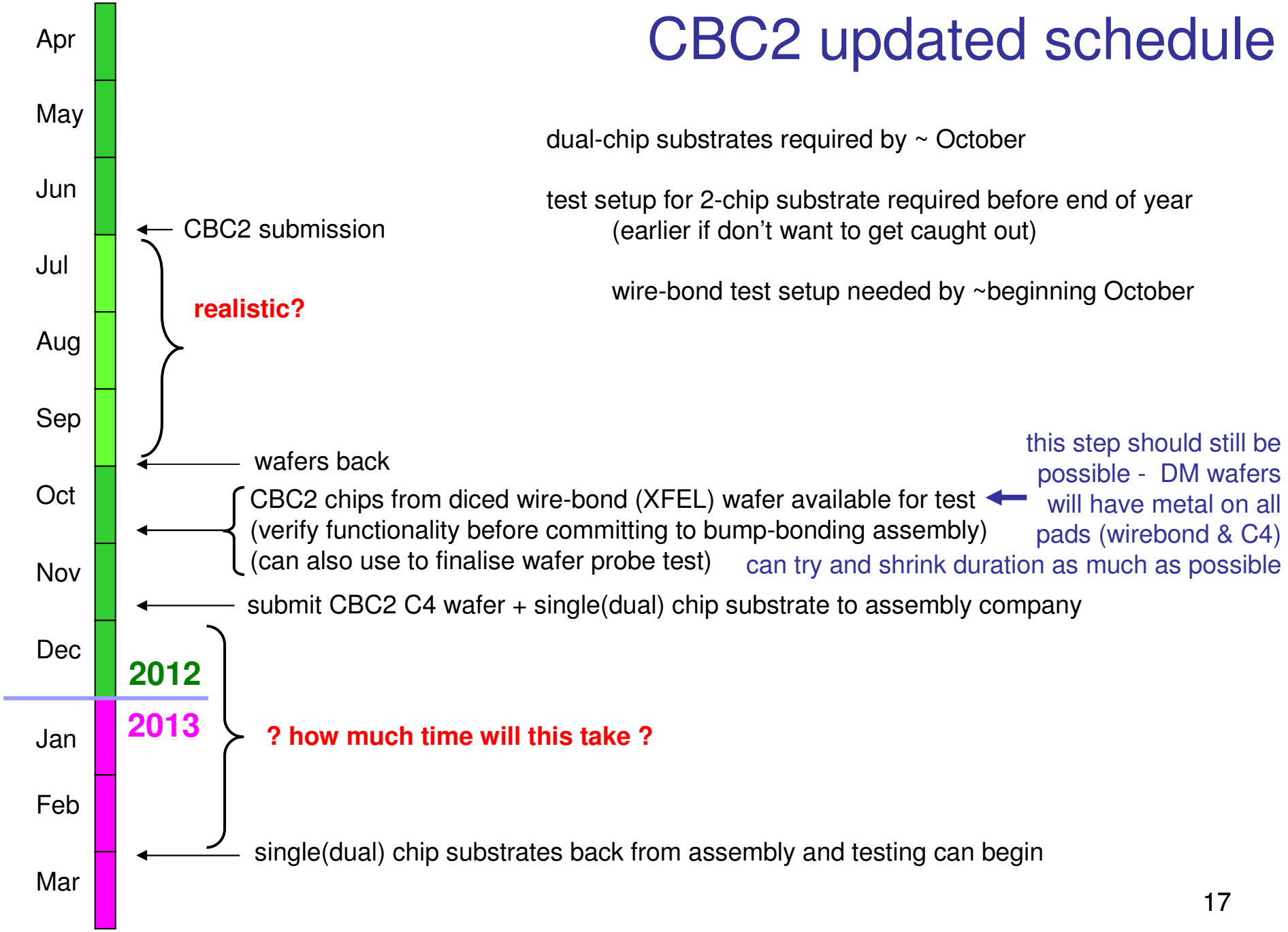

this one I showed last time

what will change?

CBC2 submission delayed ~ 1 month
"optimistic" may be "pessimistic"

incorporating these changes -> next slide

# CBC2 updated schedule




dual-chip substrates required by ~ October

test setup for 2-chip substrate required before end of year
(earlier if don't want to get caught out)

wire-bond test setup needed by ~beginning October

# dual CBC2 substrate test plans

*(no dedicated thoughts yet - below is just previous CBC prototype test items)*

**baseline performance** (conventional (clean) powering scheme)

- **digital functionality**
  - fast (Ck/T1 - SLVS) & slow control (I2C) interfaces setup and operation
- **analogue functionality**
  - amplifier
    - pulse shape, noise, linearity, overload tolerance, ..
      - $C_{IN}$ dependence, signal polarity dependence, across chip & chip-to-chip uniformity
    - leakage current tolerance
- **comparator**
  - timewalk, threshold tuning and uniformity, hysteresis

all above will depend on bias generator settings
  - => large parameter space to cover

- **power consumption**

**powering options studies**
  - supply sensitivity with/without various on-chip options

**longer term**
  - temperature effects (~ all of above vs. T)
  - tests with sensors
  - radiation: ionizing & SEU sensitivity
  - test beam

**will try and give more thought to dual substrate test setup and plans for next time**

# dead time issue

# dead-time caused by pile-up

**the story up to now**

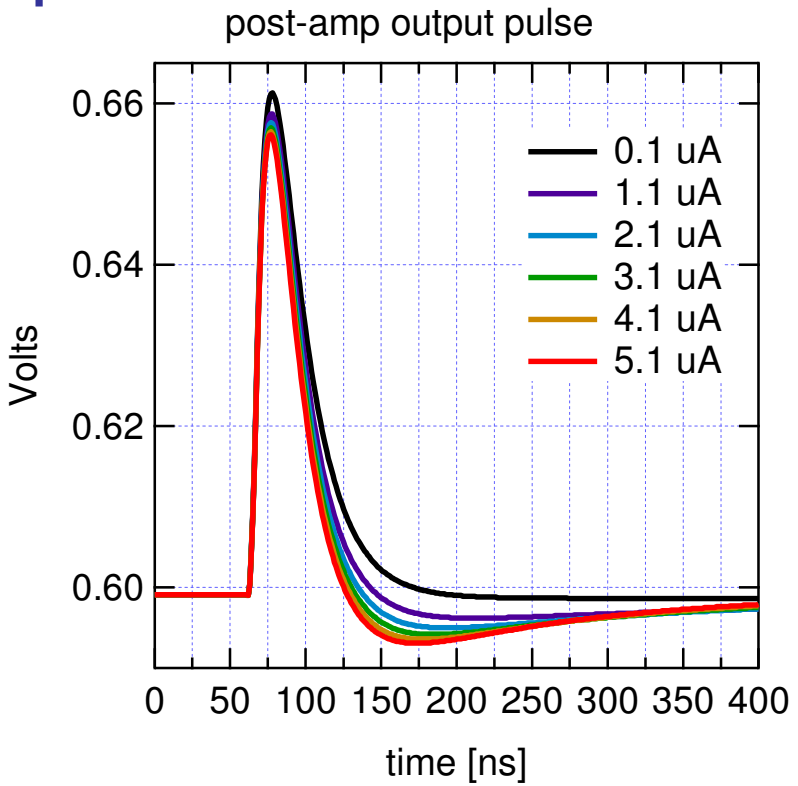
pulse shape longer than single bunch crossing
(can be shortened at expense of undershoot)

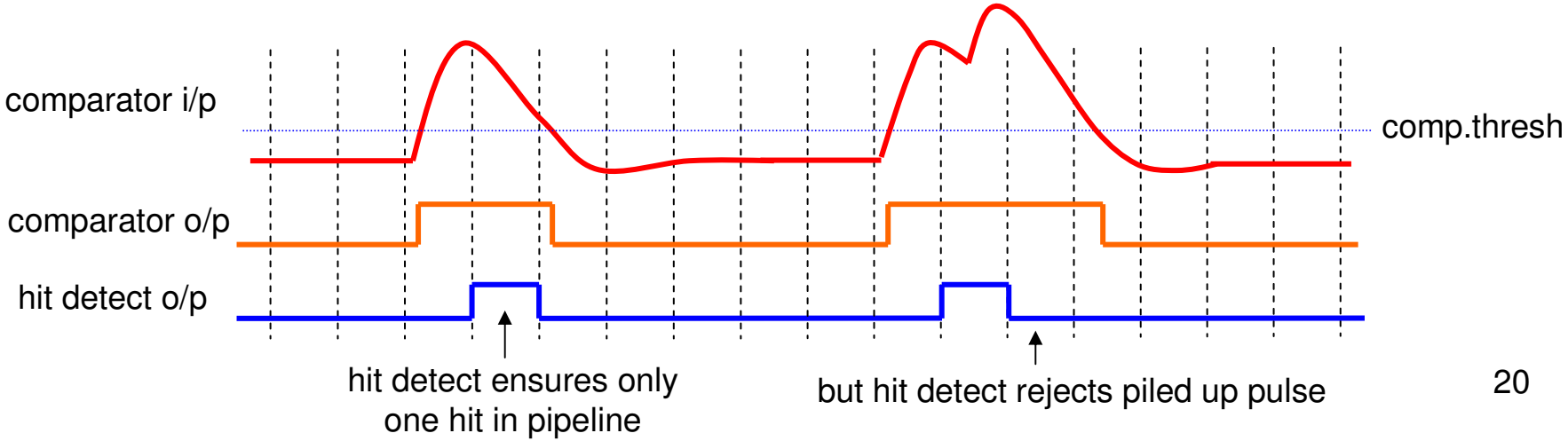
=> comparator output high for > 25 nsec

**for triggered readout**

use “hit detect” circuit to ensure that only one ‘1’ is loaded into pipeline
=> when you read out triggered data you don’t get a spurious hit from a previous BX

but a hit from pile-up signal is lost
=> dead-time



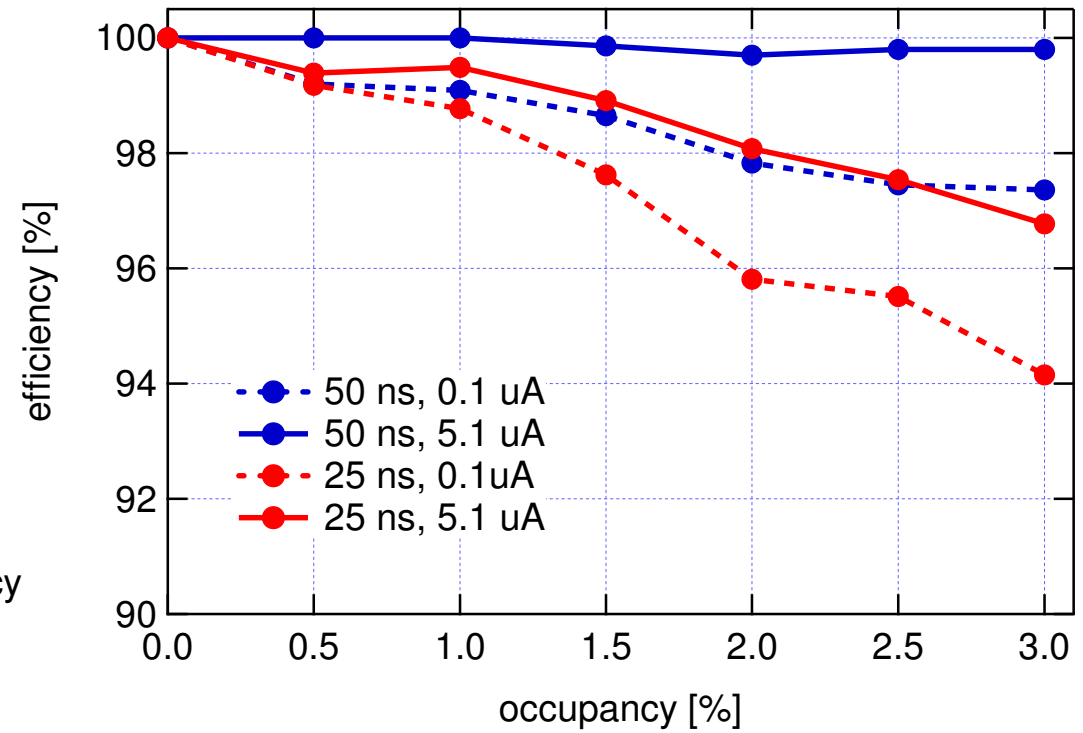
# effects of dead-time

simulation results from ~3 meetings ago

random time distribution of hits generated for specific occupancy

SPICE simulated pulse-shapes

Landau distributed amplitudes




get loss of efficiency depending on occupancy

(100% efficient if all hits identified)

shorter pulse shape (with undershoot) gives higher efficiency

~ 100% efficient for 50 ns bunch spacing

efficiency will mostly impact on Pt stub identification

# shorter pulse shape?

results from ~2 meetings ago

pushing existing front-end hard
(very preliminary study)

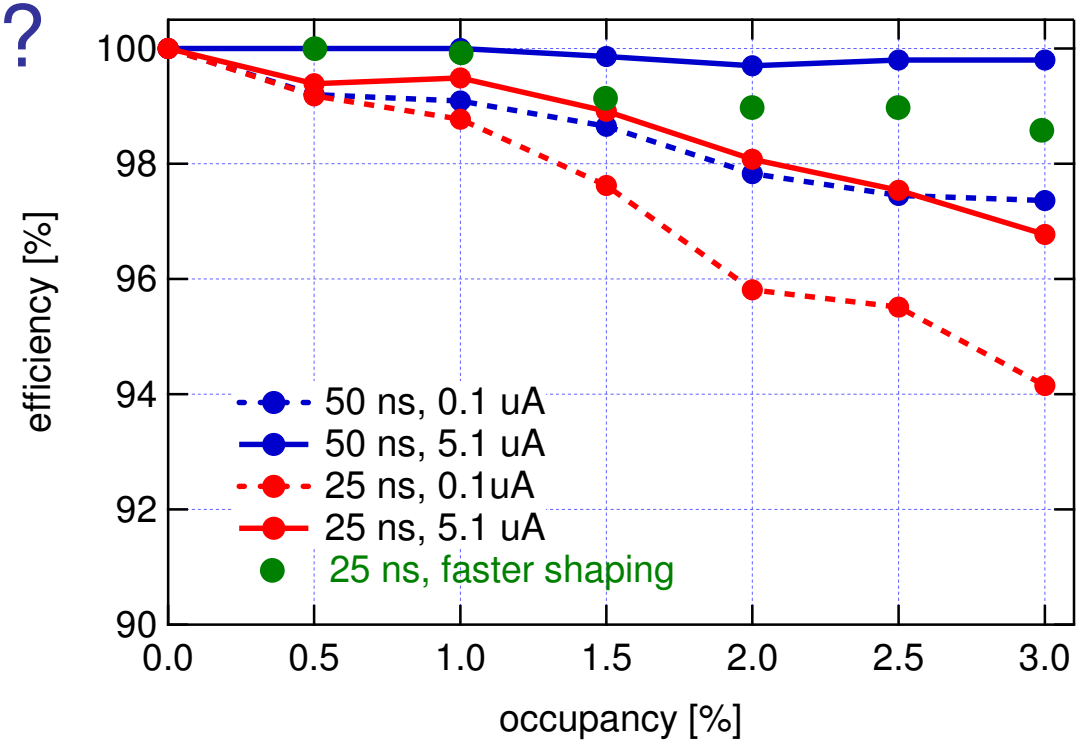
input device current increased
160 -> 210 uA

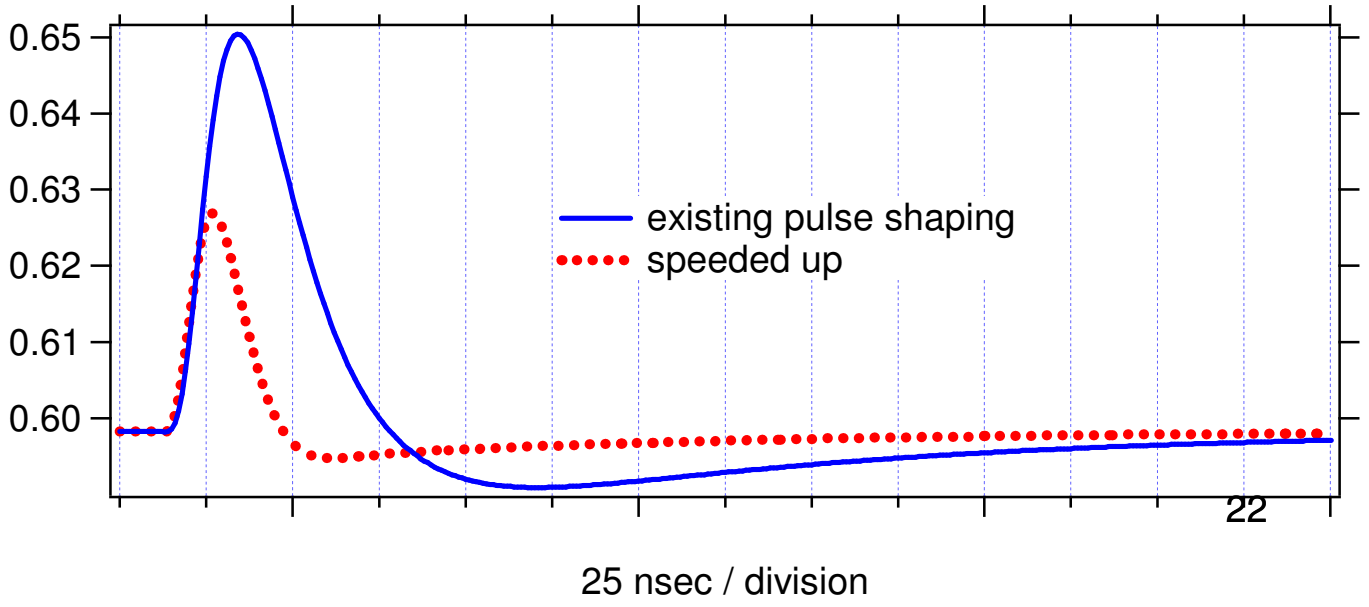
reduced amplitude ~ factor 2

noise increase 890 -> 1200 e

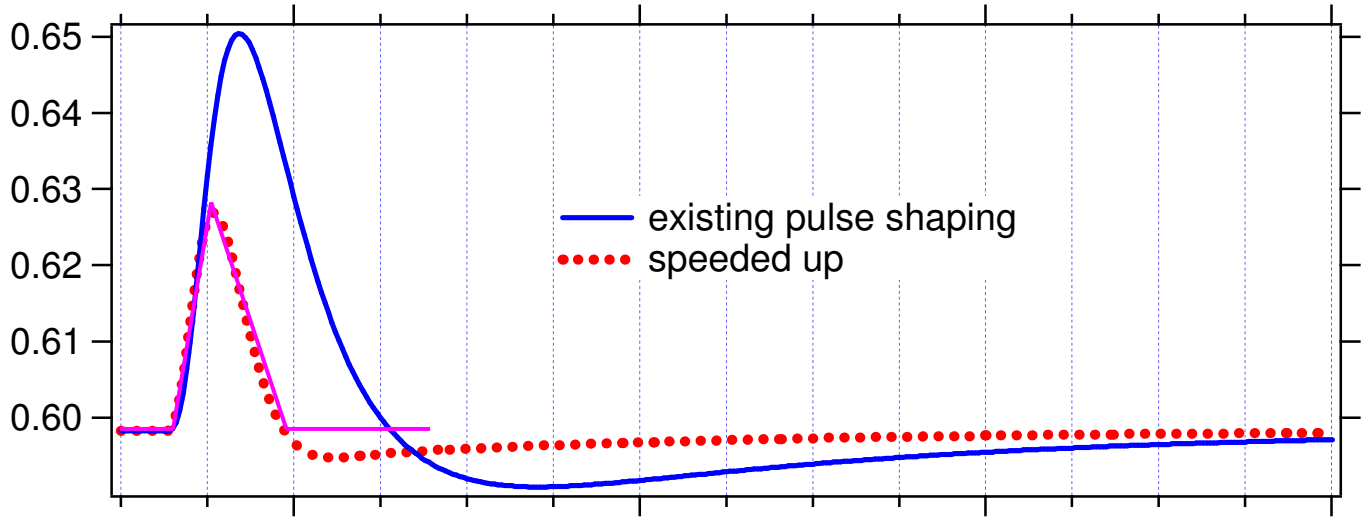
10 ns charge collection in sensor assumed
(will be sensitive to this)

but efficiency improved

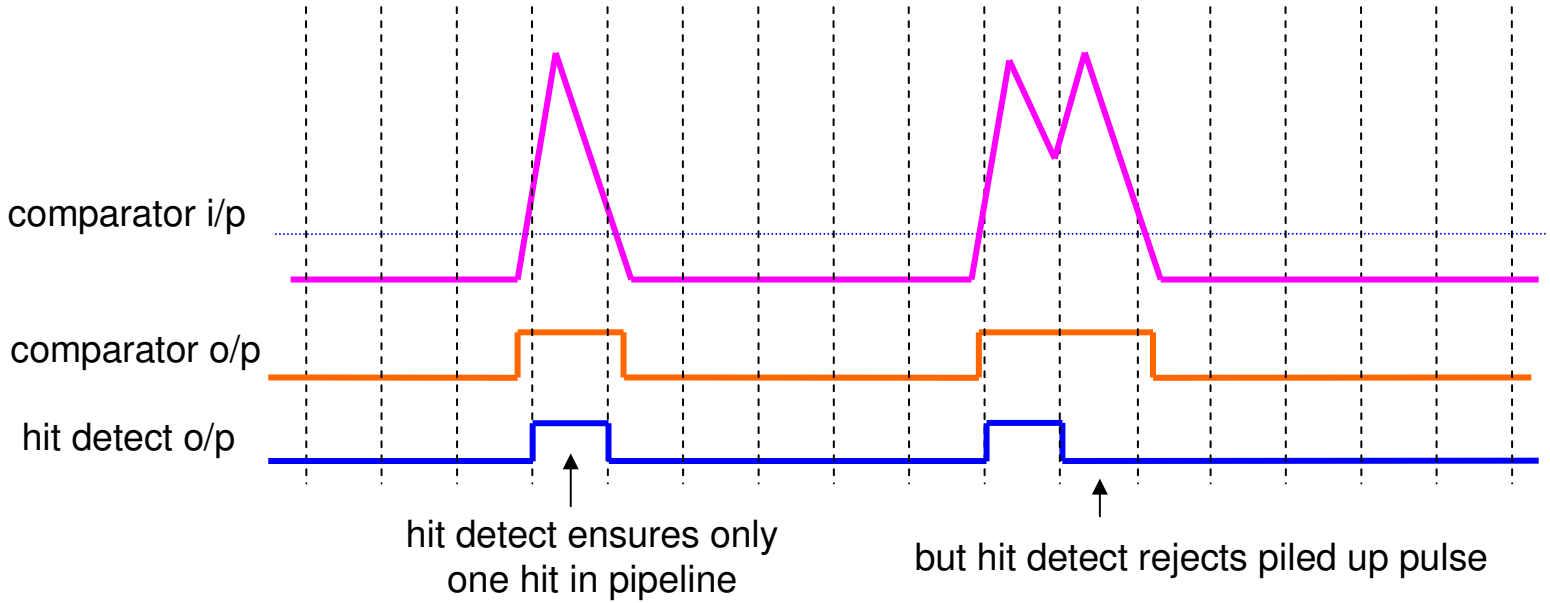


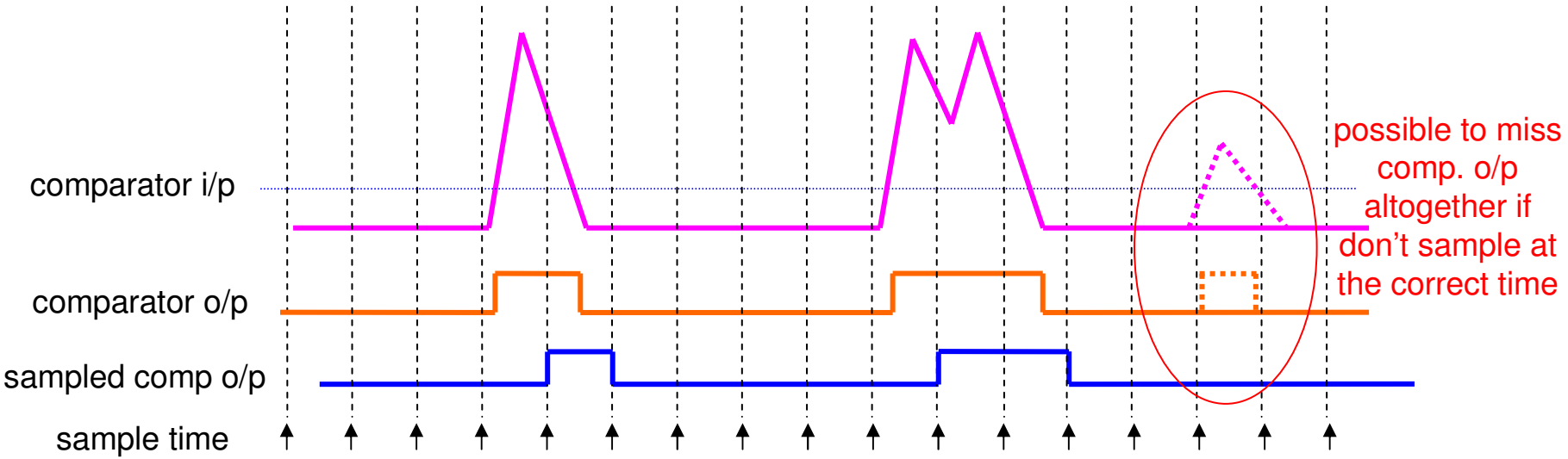
# why is short pulse shape not 100% efficient?




can understand basic behaviour 25 nsec / division
using crude triangular approximation to pulse shape
ignore undershoot for now (will come back to later)



# but what if don't use "hit detect" ?



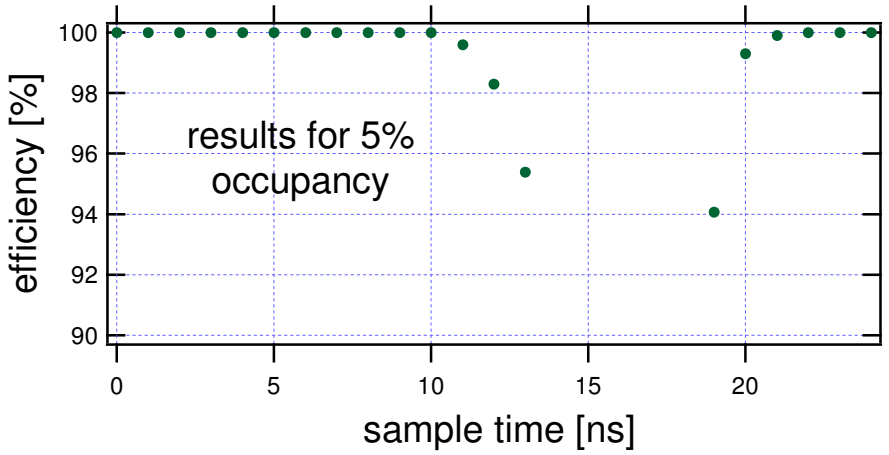

just sample the comparator output at the right time

appropriate adjustment of this time is important

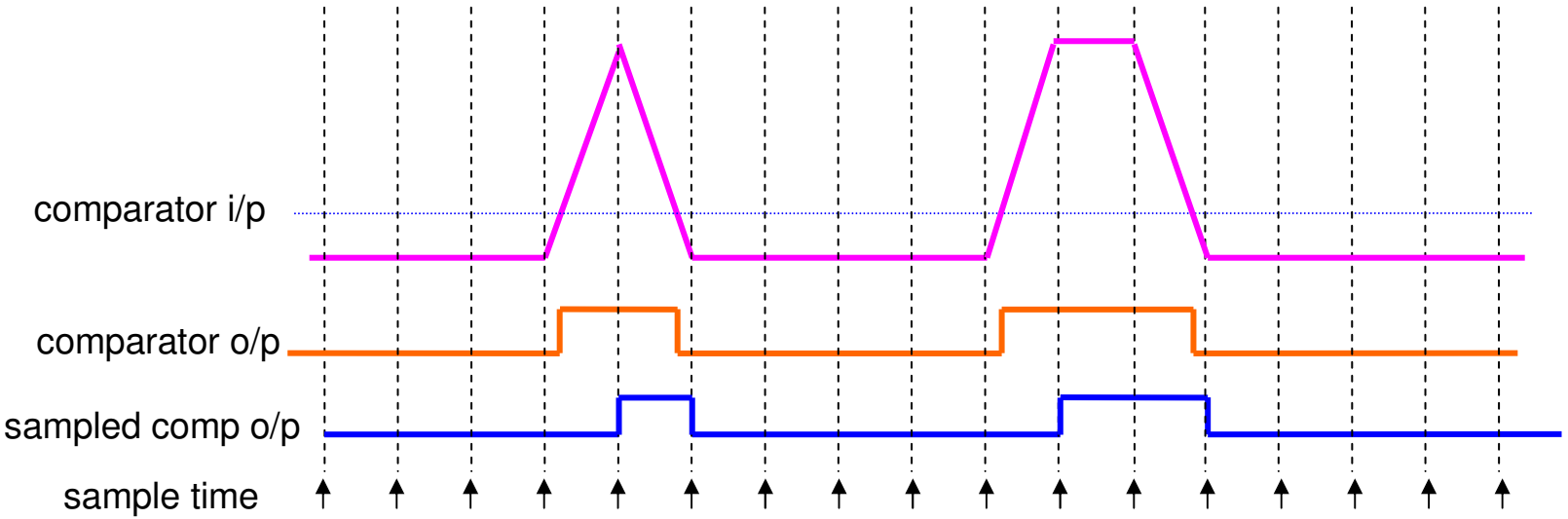
**but** 100% efficiency is now possible

can we get this without going for so short a pulse?

how long can pulse actually be?



# optimal length pulse

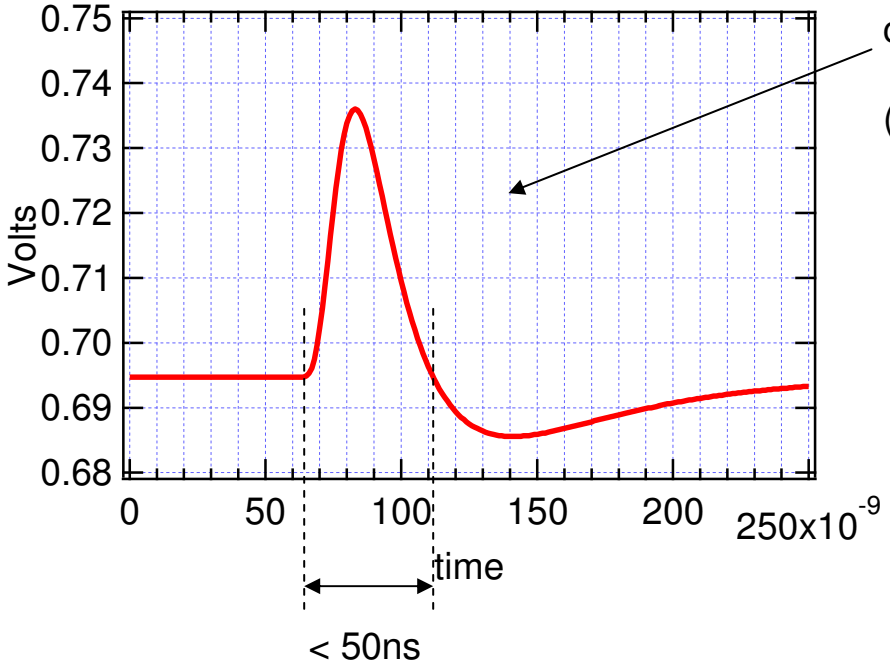



intuitively can be seen that optimum pulse shape rises, peaks and returns to baseline within 50 ns
(actually what we have in the APV after deconvolution)

if this condition met then pile-up is **not** an issue

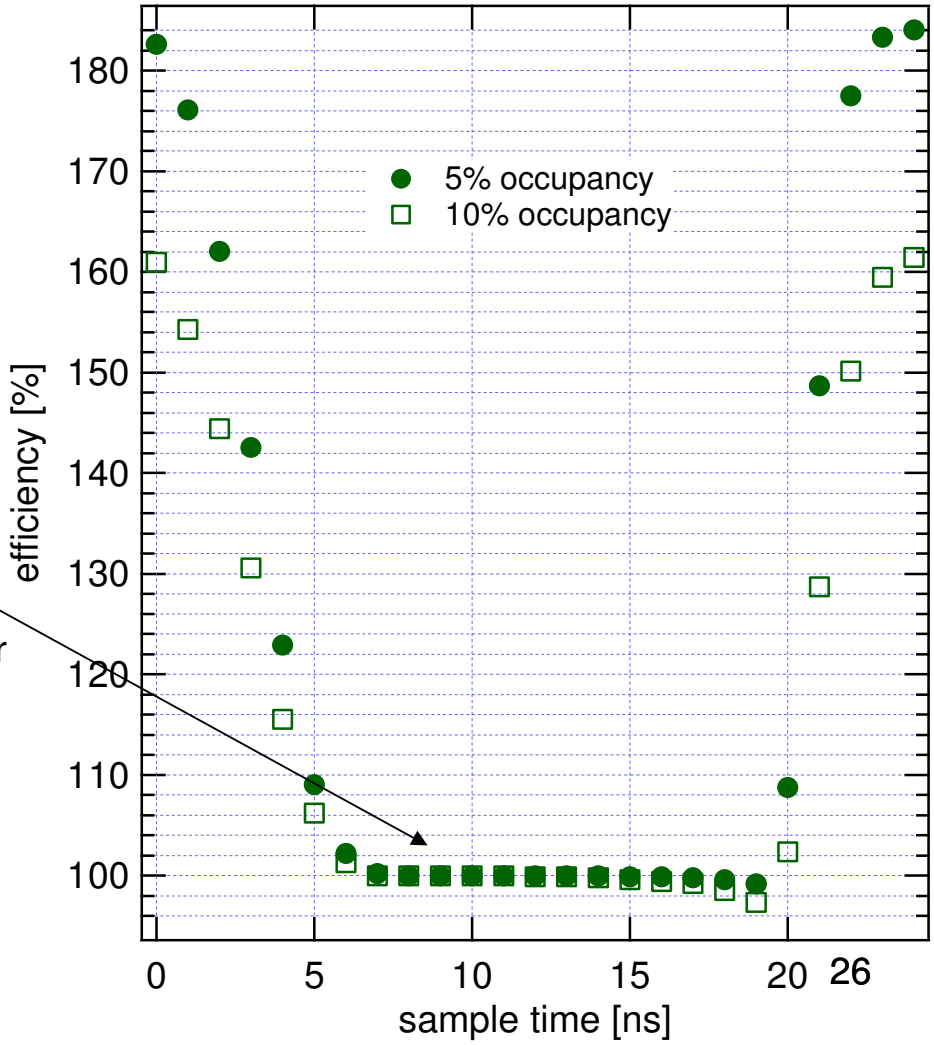
=> very fast pulse shape is **not** required (I think)

# close-to-optimum pulse shape?




can get this pulse shape by tuning existing CBC front end

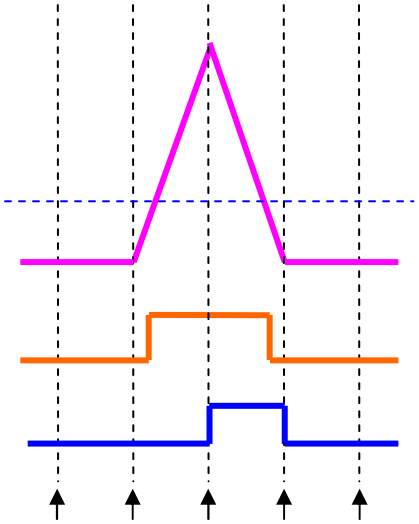
(note: noise increase ~ 10% over more unipolar shape
but maybe we can live with that)



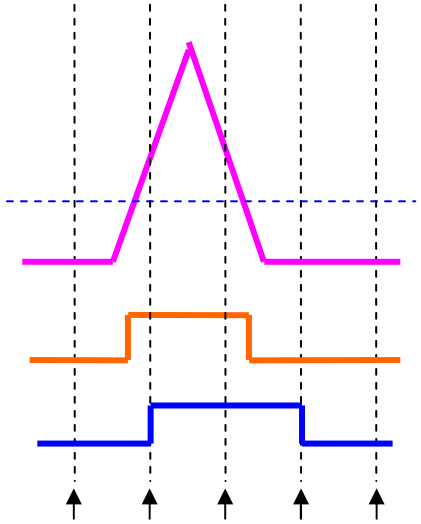

100% efficiency plateau attainable even for
very high occupancies

get >100% in places because sampling comparator
output from same pulse more than once

# > 100% efficiency explanation

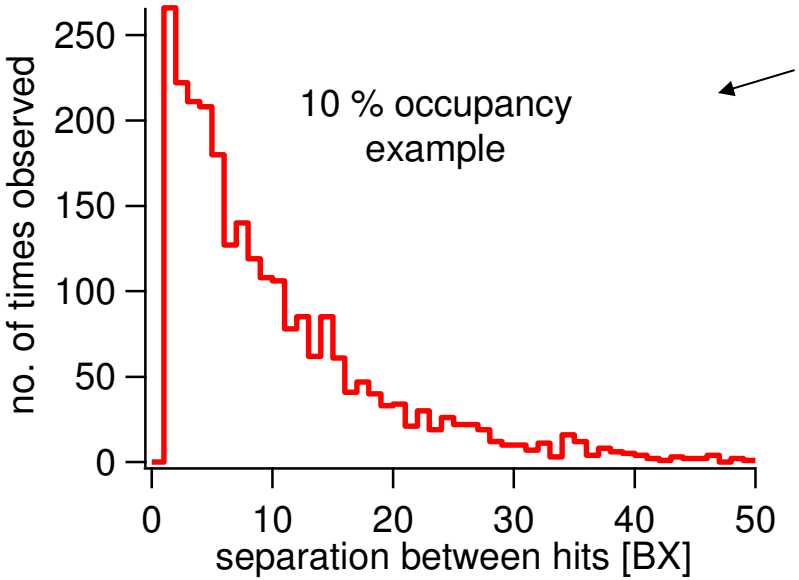


optimal sampling



non-optimal sampling

# what about undershoot effect?



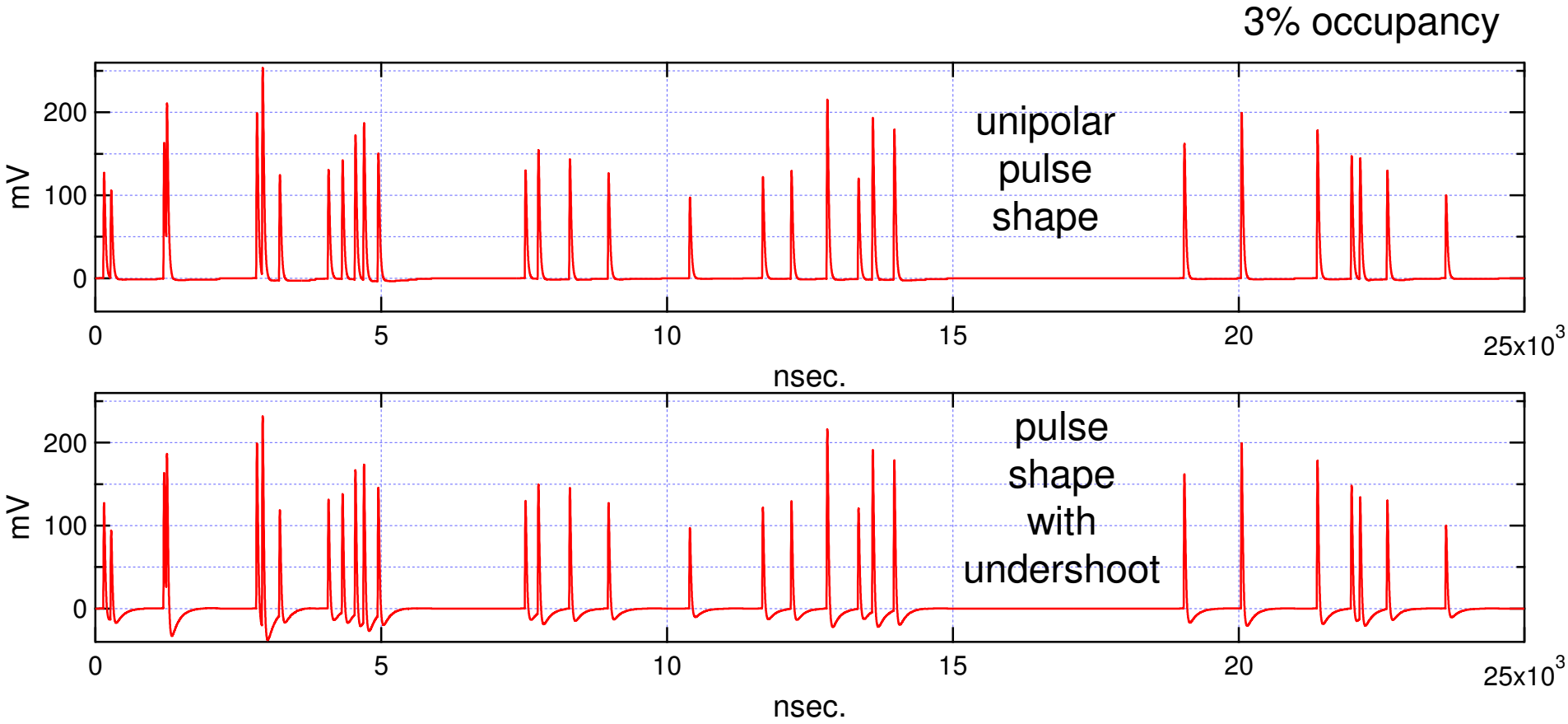

plot shows frequency of observing a particular separation between hits generated randomly

average interval is 10 (for 10% occupancy)
but more likely to see a shorter interval than a longer one

the higher the occupancy the more likely a following pulse will sit on the undershooting tail of the previous pulse

will have a distorting effect on the pulse height distribution

# reminder of pulse generation method



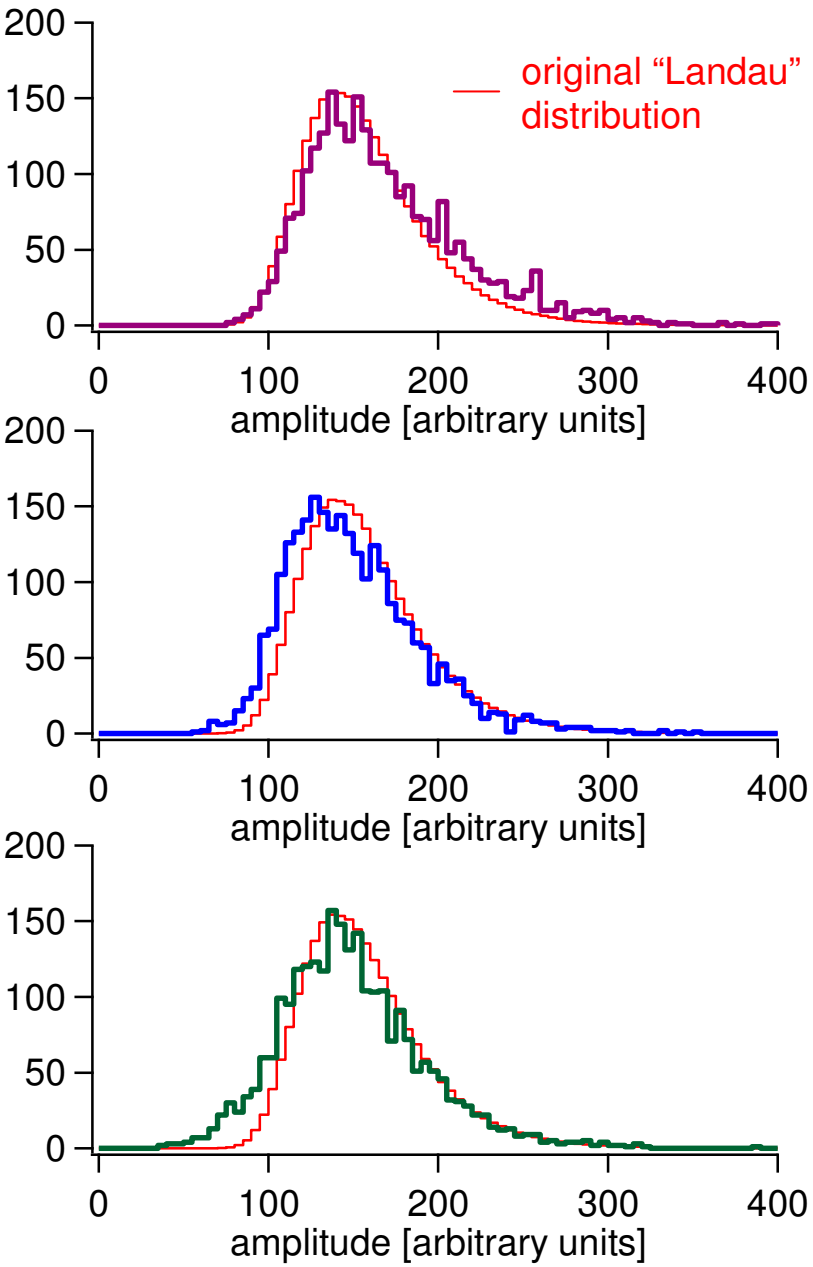

randomly generate time distribution of hits with desired occupancy

for each hit generate an output pulse shape (from SPICE) scaling the amplitude using a value randomly sampled from a “Landau-like” distribution

combine into single data stream

can now re-generate pulse height distribution from single data stream and compare with original Landau

# undershoot effect on pulse height distributions




**unipolar pulse (no undershoot)**

"landau" skewed to higher amplitudes

**very fast pulse (undershoot)**

"landau" skewed to lower amplitudes

**"optimum" pulse (undershoot)**

"landau" skewed to even lower amplitudes

notes:

these results are for 10% occupancy
to exaggerate effect

no electronic noise included

# dead-time effects summary

- further work needed, but
  - seems as though very fast pulse shape may not be required
    - return to baseline within 50 ns is sufficient
  - baseline undershoot does not seem to cause a big effect