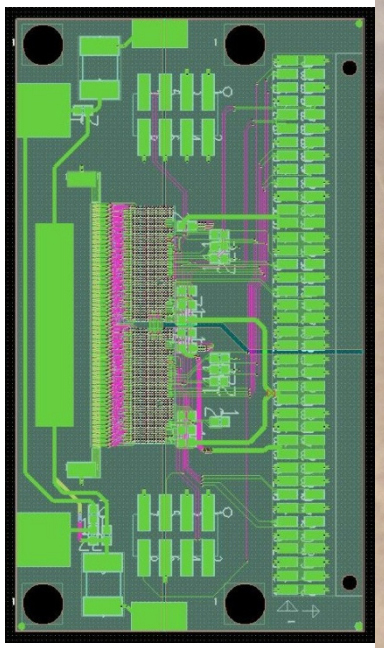
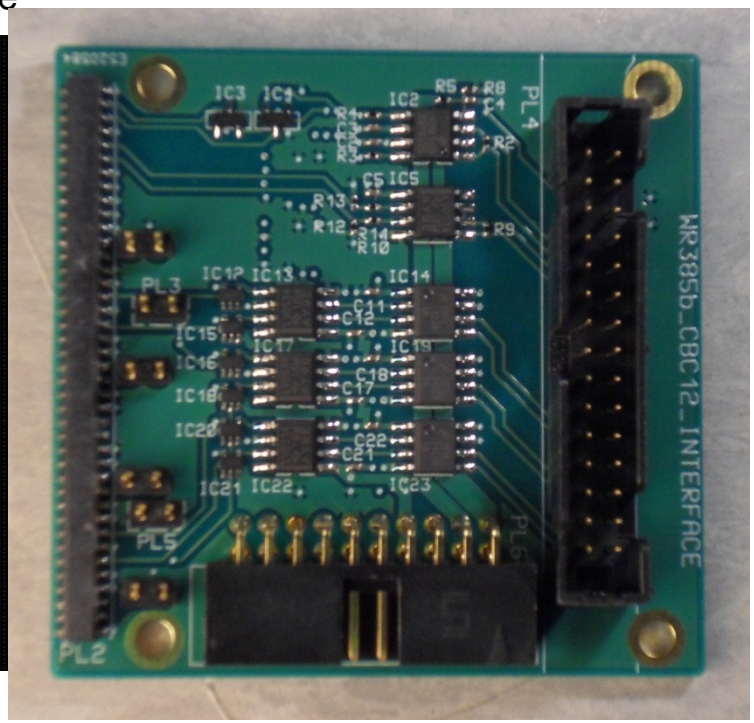
dual CBC2 hybrid & module testing

dual-CBC2 substrate interface board

dual-CBC2 substrate



interface board



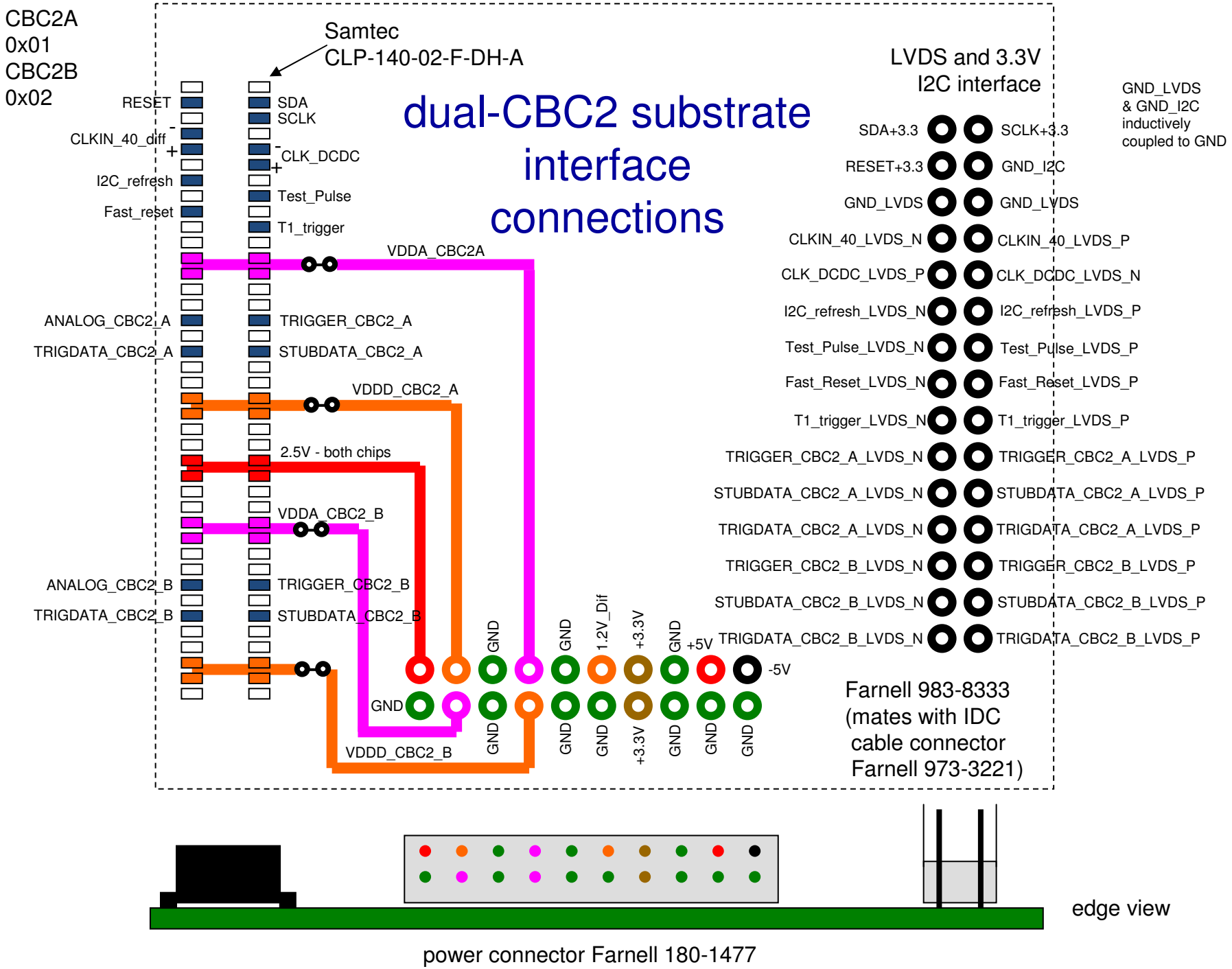
LVDS signal levels

3.3V I2C

3 now populated

- 2 at Imperial
- 1 at Bristol for tests with FMC

20 pcbs available


CBC2A
0x01
CBC2B
0x02
Samtec
CLP-140-02-F-DH-A
dual-CBC2 substrate interface connections
LVDS and 3.3V I2C interface
GND_LVDS & GND_I2C inductively coupled to GND
RESET
CLKIN_40_diff
I2C_refresh
Fast_reset
SDA
SCLK
CLK_DCDC
Test_Pulse
T1_trigger
VDDA_CBC2A
ANALOG_CBC2_A
TRIGDATA_CBC2_A
TRIGGER_CBC2_A
STUBDATA_CBC2_A
VDDD_CBC2_A
2.5V - both chips
VDDA_CBC2_B
ANALOG_CBC2_B
TRIGDATA_CBC2_B
TRIGGER_CBC2_B
STUBDATA_CBC2_B
VDDD_CBC2_B
GND
1.2V_Dif
+3.3V
+5V
-5V
SDA+3.3
SCLK+3.3
RESET+3.3
GND_I2C
GND_LVDS
CLKIN_40_LVDS_N
CLKIN_40_LVDS_P
CLK_DCDC_LVDS_P
CLK_DCDC_LVDS_N
I2C_refresh_LVDS_N
I2C_refresh_LVDS_P
Test_Pulse_LVDS_N
Test_Pulse_LVDS_P
Fast_Reset_LVDS_N
Fast_Reset_LVDS_P
T1_trigger_LVDS_N
T1_trigger_LVDS_P
TRIGGER_CBC2_A_LVDS_N
TRIGGER_CBC2_A_LVDS_P
STUBDATA_CBC2_A_LVDS_N
STUBDATA_CBC2_A_LVDS_P
TRIGDATA_CBC2_A_LVDS_N
TRIGDATA_CBC2_A_LVDS_P
TRIGGER_CBC2_B_LVDS_N
TRIGGER_CBC2_B_LVDS_P
STUBDATA_CBC2_B_LVDS_N
STUBDATA_CBC2_B_LVDS_P
TRIGDATA_CBC2_B_LVDS_N
TRIGDATA_CBC2_B_LVDS_P
Farnell 983-8333
(mates with IDC cable connector Farnell 973-3221)
edge view
power connector Farnell 180-1477

what are the jumpers for?

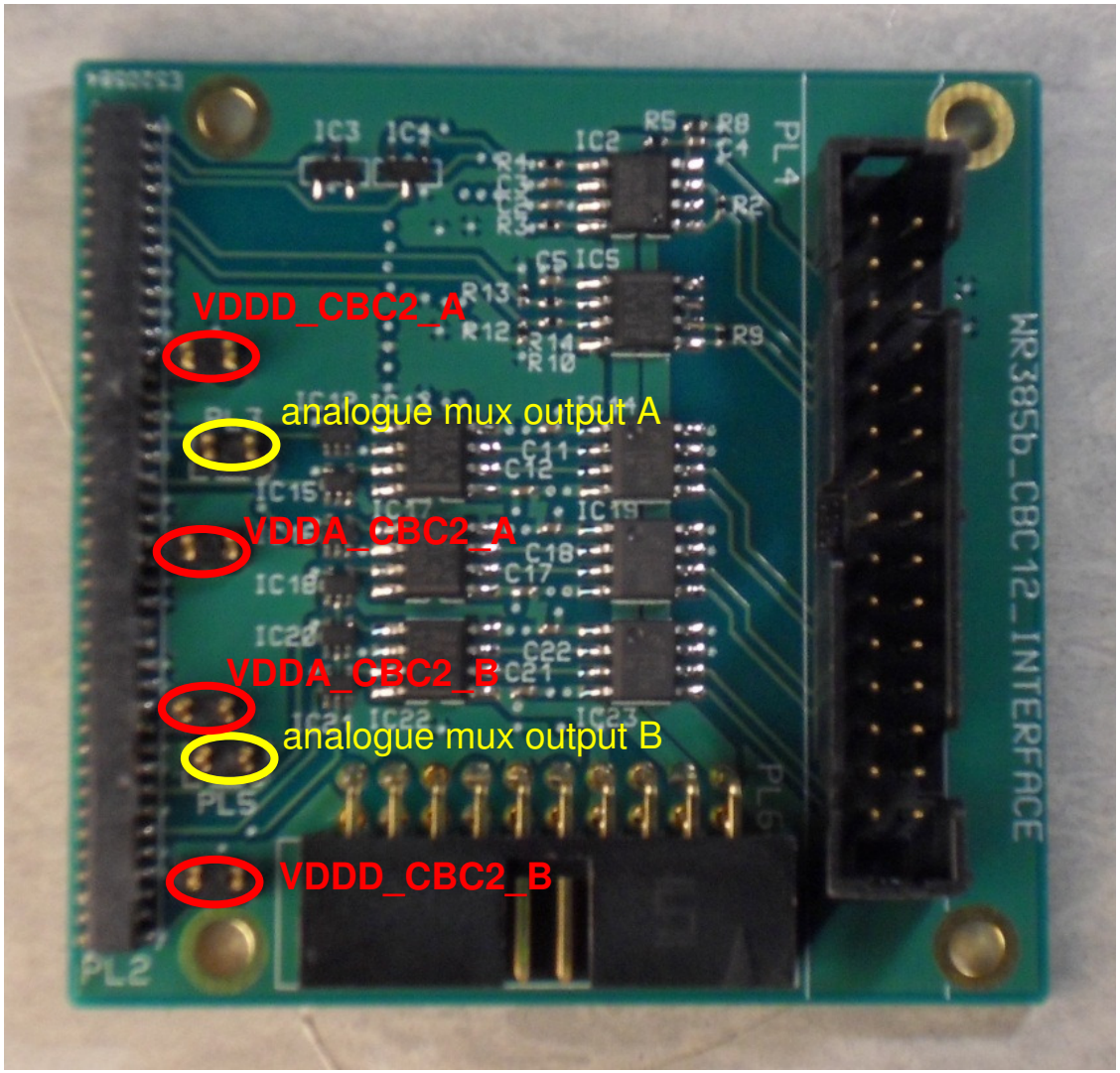
can use if want to monitor power drawn by each chip on the substrate

recommended user's configuration

VDDD jumpers present
VDDA jumpers NOT present

CBCs powered from 1.2 VDDD
(analogue also from VDDD via LDOs)

other two headers included to allow to monitor analogue MUX O/Ps



first five substrates acceptance test plans at IC

hardware

- prototype test system: VME based
  - VI2C module
  - custom digital interface to capture CBC2 outputs
  - NI VME interface to Windows PC running LabVIEW

tests

- response to control signals: fast and slow
- test pulse response, all channels
- trigger output and triggered output frames
- DC-DC circuits and LDOs operational, power consumption
- s-curves, offsets tuning, gain

- software to perform these measurements already developed for the wire-bond substrate tests

how long will this take?

- if no problems, maybe a week or two?
- note: this is for acceptance tests on bare substrates
  - looking to confirm basic functionality and performance as for wire-bond substrate tests
  - not looking to study subtle effects

first five substrates - what happens next?

if majority/all are working

some to be returned to CERN (would like to keep at least one at Imperial)

CERN to begin construction of “mini” pT modules using Infineon sensors

can launch assembly of remaining substrates with Endicott

if low yield

…..

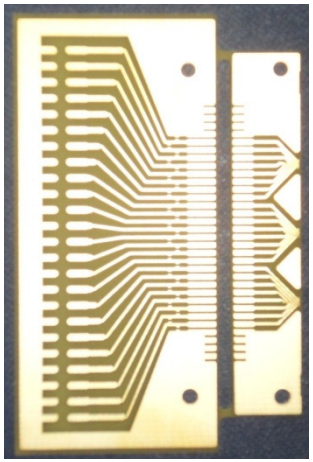
first and/or later substrates - further tests at Imperial

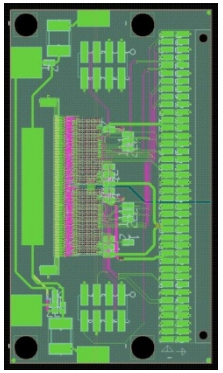
can construct “electrical” pT module

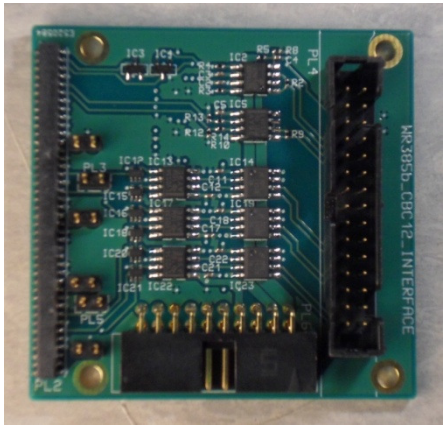
will have to work out how to do it

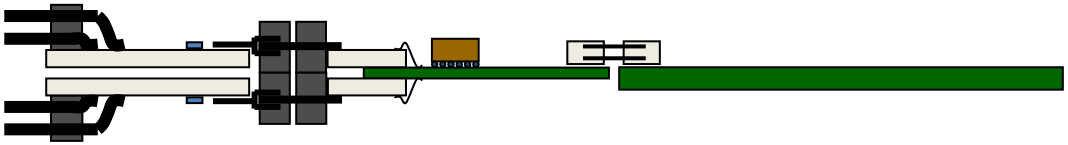
double-sided bonding may be difficult

will use prototype test system initially



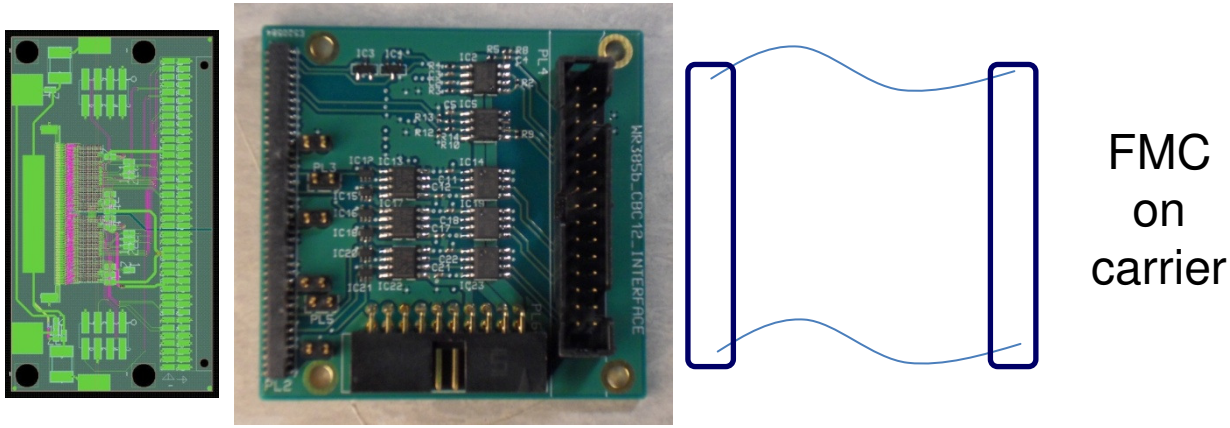






if successful, can make more of these assemblies if useful to others

first and/or later substrates - tests with FMC



can start with hybrid only (sensor not required)

need initial software to:

- program I2C registers
- tune channel offsets - example algorithm on next slide

later on:

- receive triggers generated by CBCs (can use on-chip test pulse)
  - responding with readout triggers and data acquisition

offsets tuning algorithm example

repeat this procedure
for all 8 test groups

32 channels / test group

set up initial conditions
    test pulse group, timing, amplitude
    set channel offsets MSB only

1) acquire S-curves
for each channel in test group
    S-curve mid-points > target value?
        yes: reset MSB, set MSB-1
        no: set MSB-1

2) acquire S-curves
for each channel in test group
    S-curve mid-points > target value?
        yes: reset MSB-1, set MSB-2
        no: set MSB-2

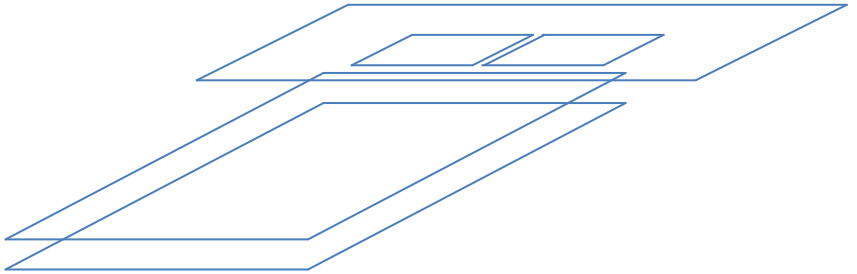
3) acquire S-curves
for each channel in test group
    S-curve mid-points > target value?
        yes: reset MSB-2, set MSB-3
        no: set MSB-3
        .
        .
8) acquire S-curves
for each channel in test group
    S-curve mid-points > target value?
        yes: reset LSB

mini pT modules plans

lab tests

can verify many aspects of performance using electrical tests

could be useful to have single sensor layer versions? (studies with source)



complete double layer assemblies

not clear how to get at performance without beam

might learn something with light pulse system from above and below?

should aim for beam test at early opportunity

could aim for a telescope constructed from mini-pT modules

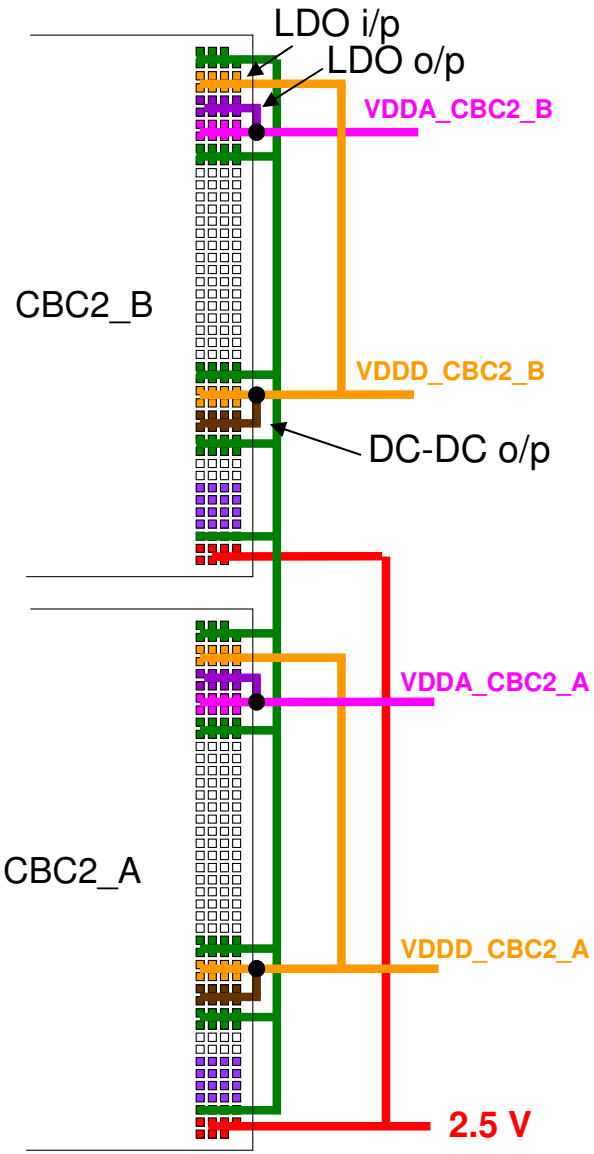
would give a focus for collaborative effort to develop complete readout and DAQ system

hardware, firmware, software, mechanics and cooling

not a small task….

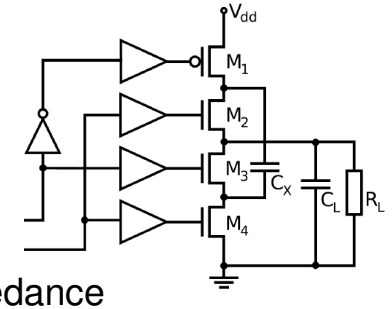
extra

CBC2 powering scheme on 2-chip substrate



backend pads as viewed through CBC2 substrate

after some thinking and discussion with Georges we have arrived at this scheme



2.5 V common to both chips

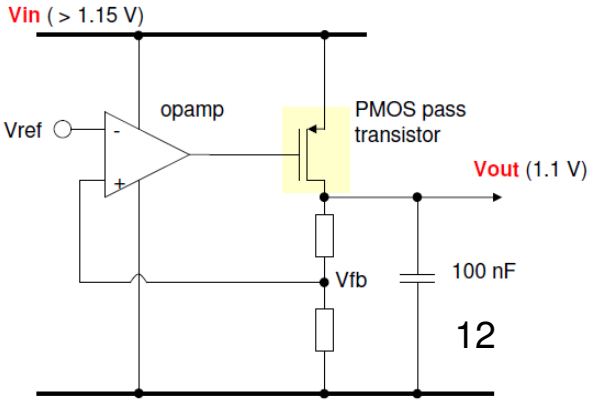
if DC-DC not clocked then output -> high impedance
=> DC-DC o/p can be shorted to VDDD
VDDD can be provided externally if not using DC-DC

connect VDDD directly to LDO i/p
keeping separate would allow to run VDDD at low voltage
but no significant power advantage to doing this

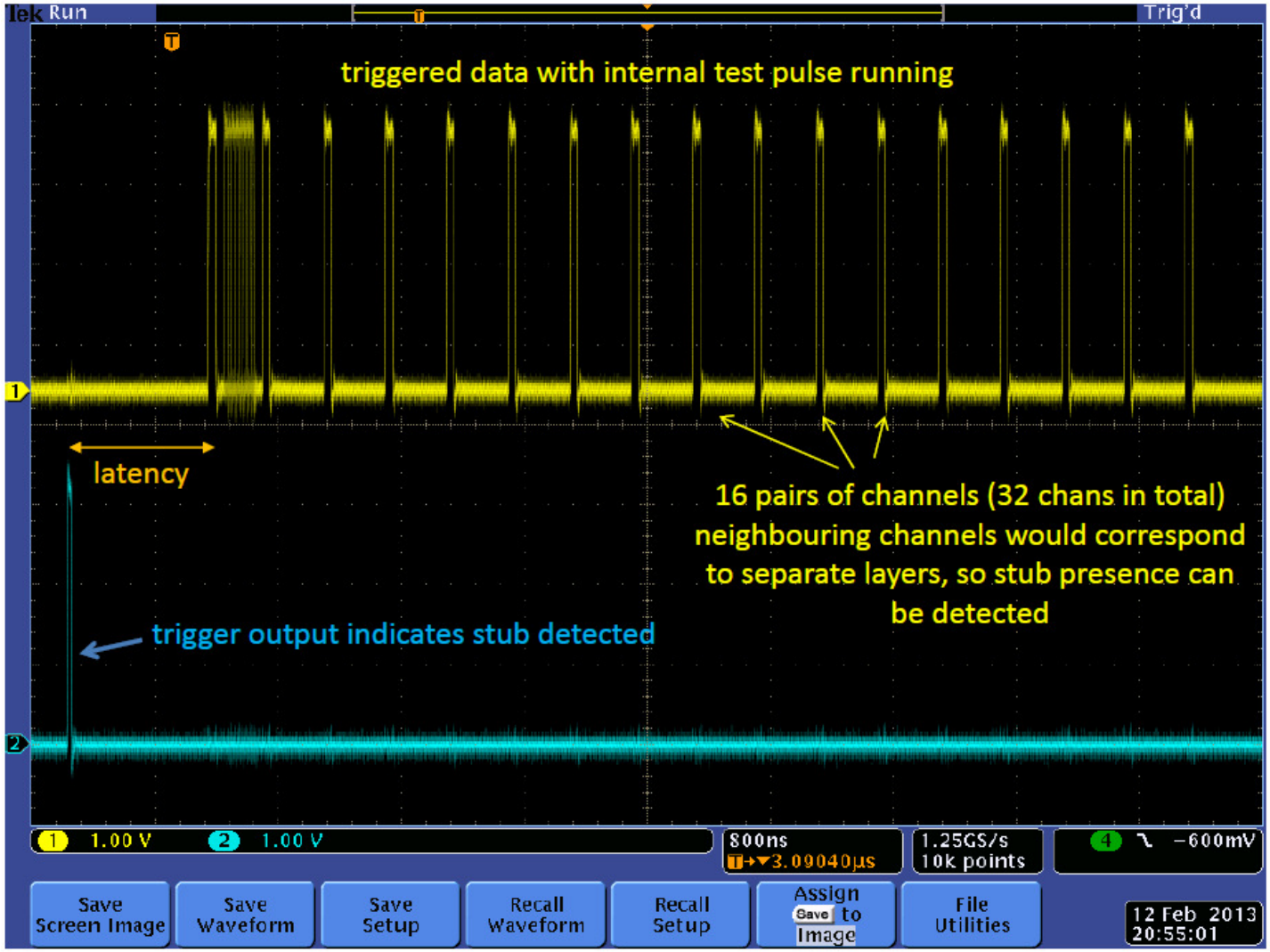
connect LDO o/p directly to VDDA
if want to supply VDDA externally then provide at slightly higher voltage than normal LDO o/p level

=> LDO shuts down (pass transistor turns off)
verified on CBC prototype

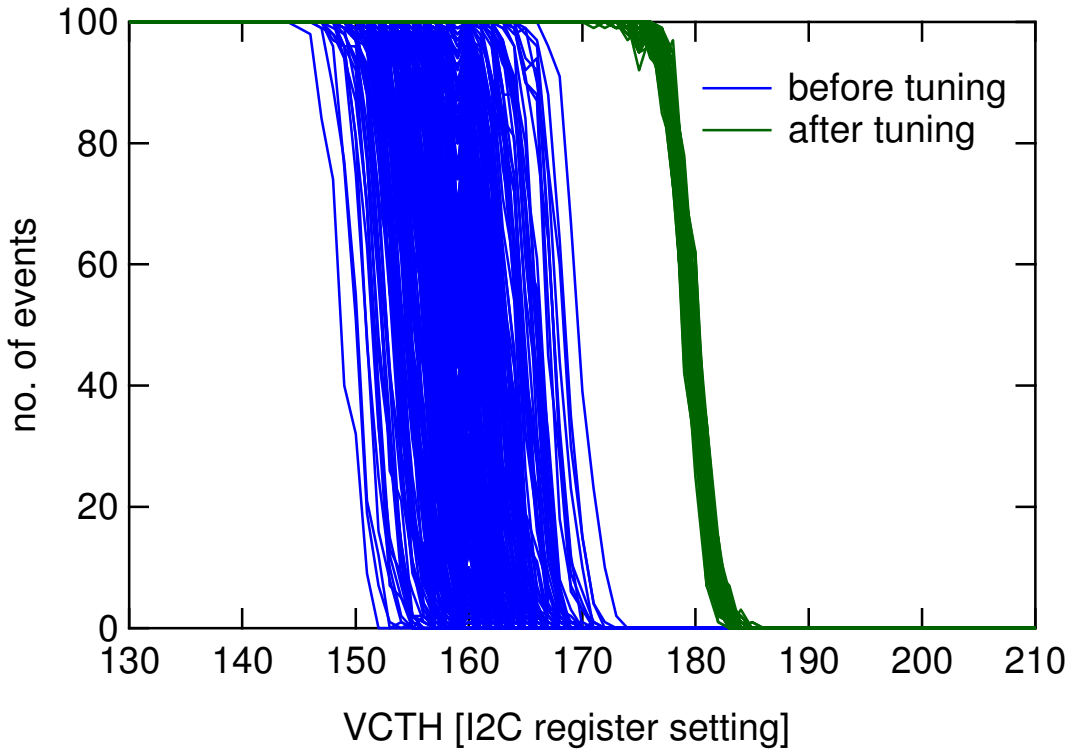
=> no jumpers required at all on substrate



first result



S-curves and tuning



254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to VCTH setting of 180

254 offset values after tuning