CBC2 testing status

CMS Tk phase II electronics meeting – April 16th, 2013

since last time

have concentrated on wire-bond setup

learn as much as possible about CBC2 performance with this non-optimal bonding setup

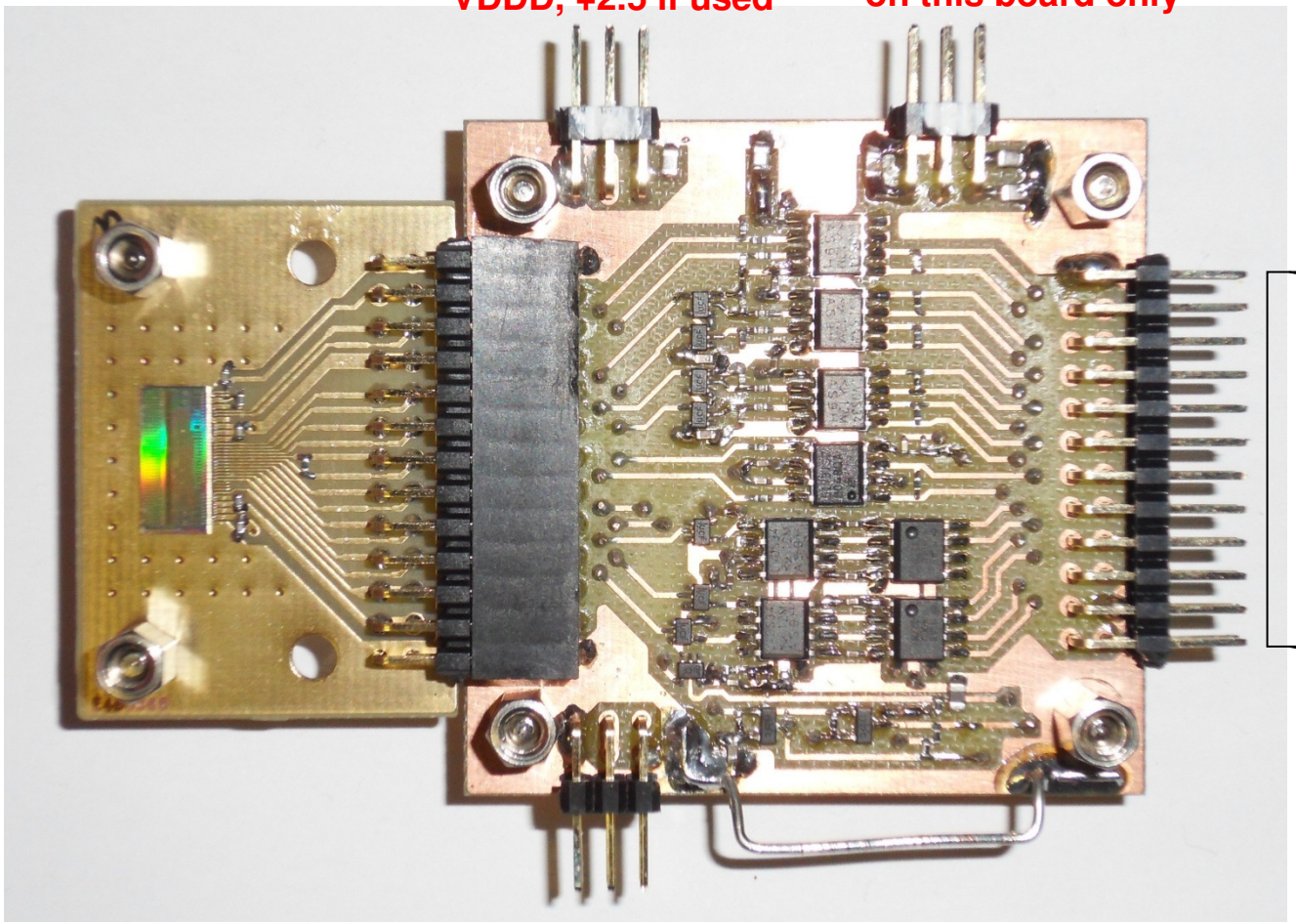
objective to develop further and refine chip setup and evaluation software procedures

relevant to wafer probe test for remaining wafers

wirebond CBC2 test setup

power to CBC2
VDDD, +2.5 if used

power to circuitry
on this board only



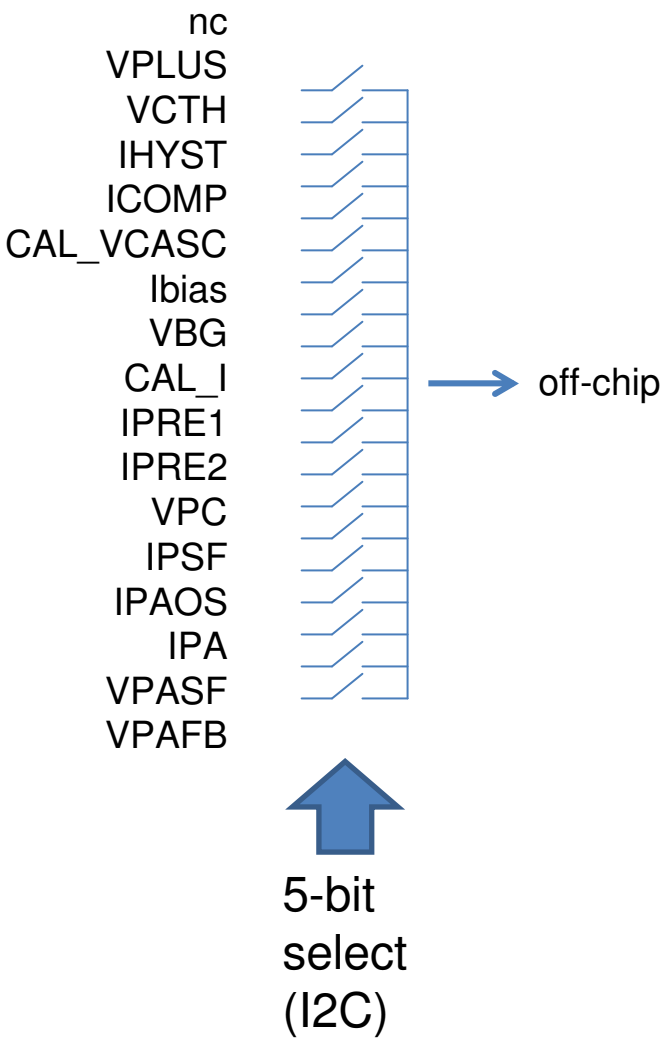
LVDS signal levels
3.3V I2C

VME based
DAQ

LDO O/P (VDDA input) (if required)
analogue mux output

all testing performed using 1.2V VDDD supply only
VDDA provided by LDO on CBC2
appears to work without problems

analogue mux



gives access to bias levels for diagnostic purposes

most useful for bias voltages (e.g. comparator threshold), bandgap

not so useful for currents - actually looking at current mirror outputs

future for this?

- could be used to feed on-chip slow ADC in CBC3
- not clear how useful this ADC would be
- may decide to just keep mux output to be used during probe test

bias voltages

shape as expected

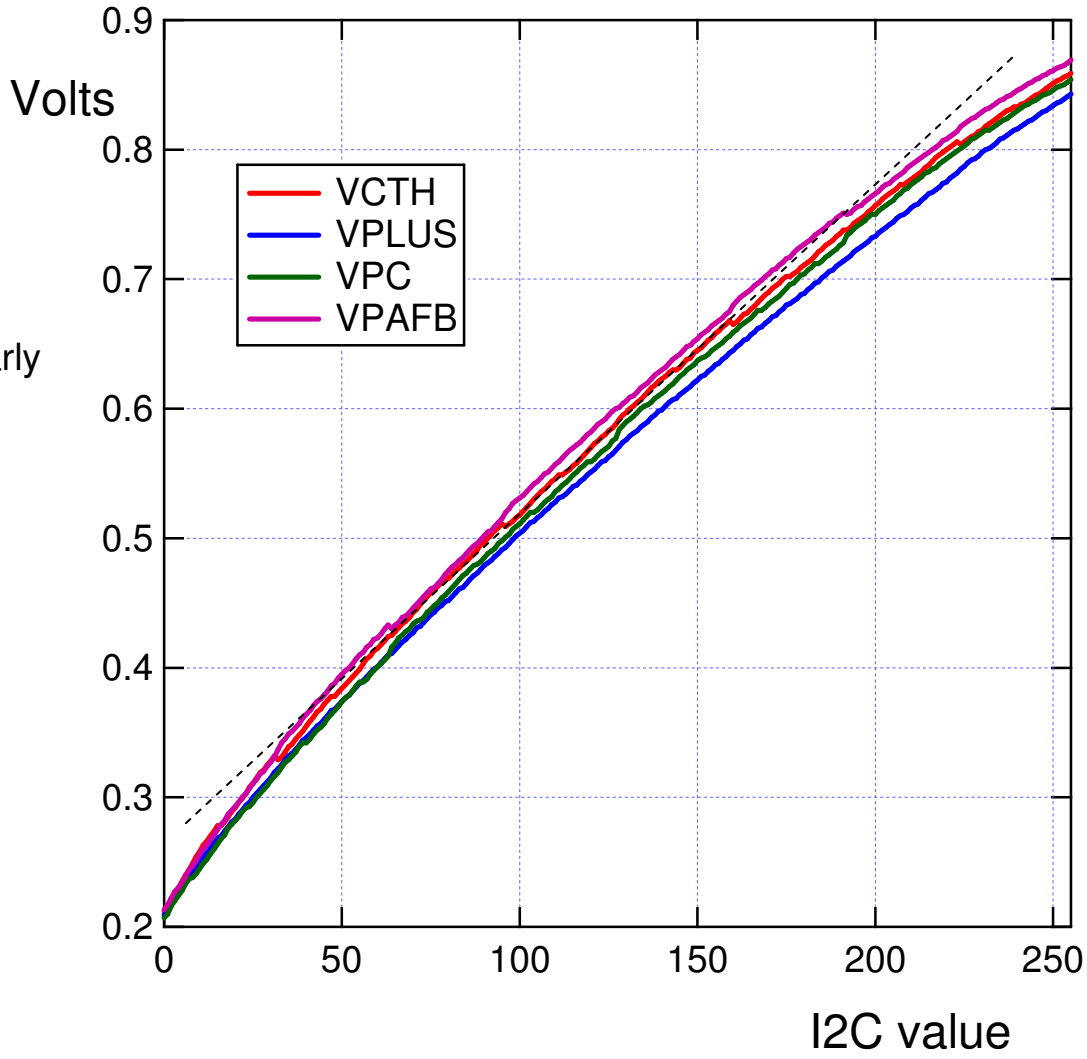
linearity not important

discontinuities (diff. non-linearity), particularly for global comparator threshold VCTH causes some difficulties

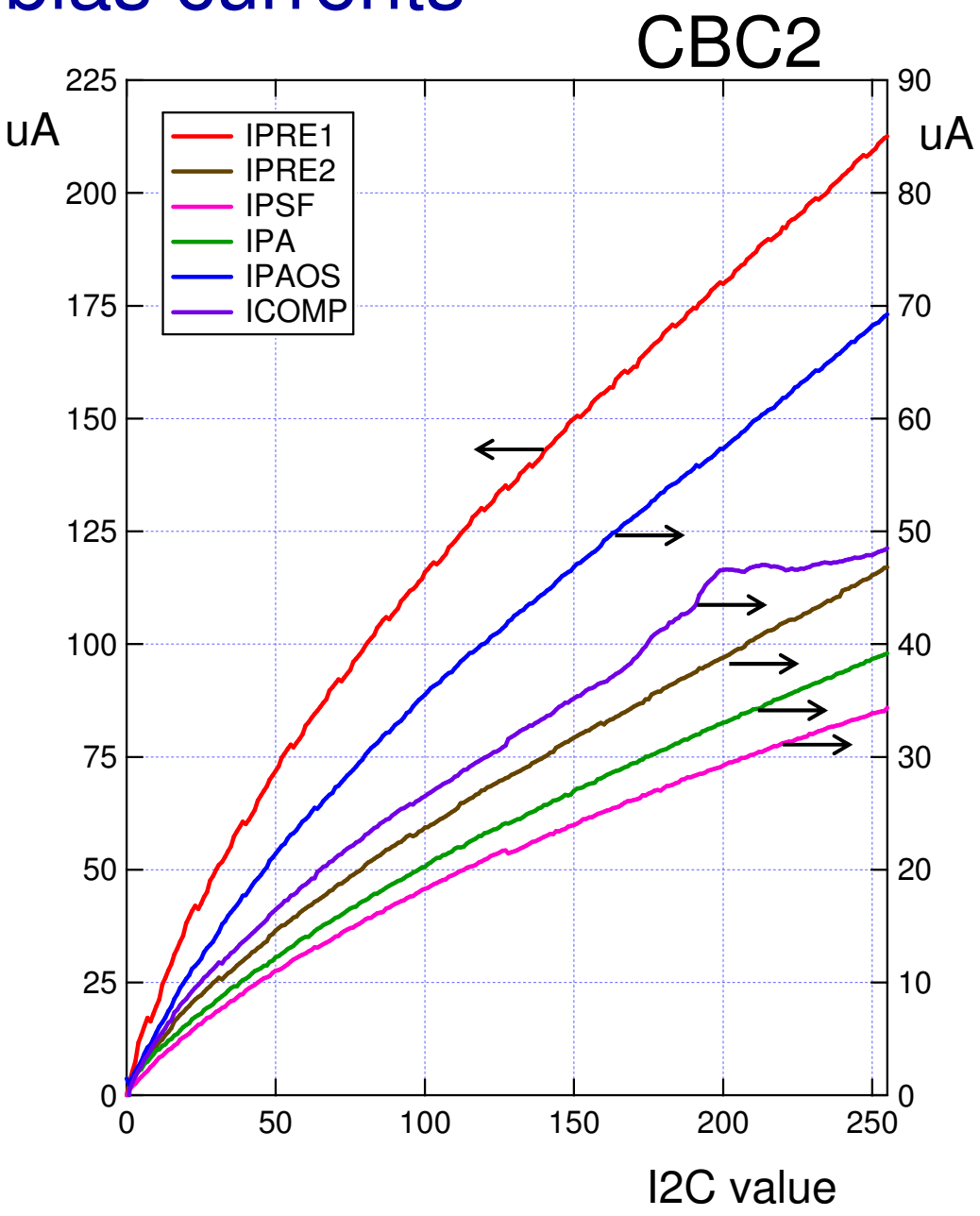
will see why later

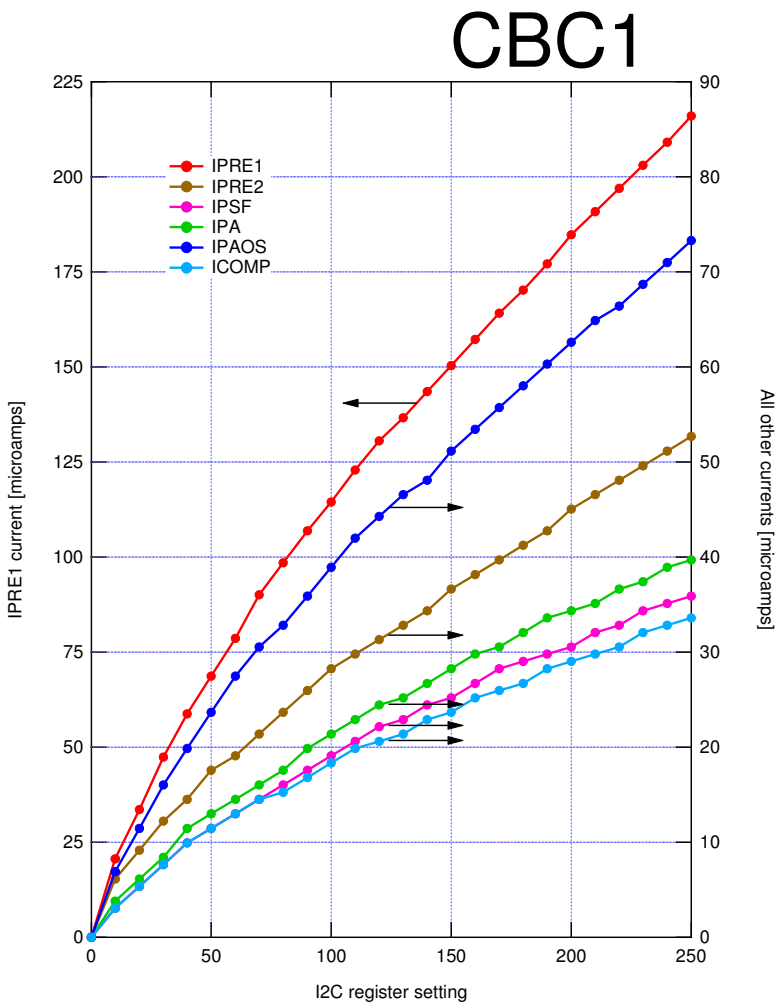
(can try and improve for CBC3)

rough fit -> 2.5 mV / I2C value



bias currents



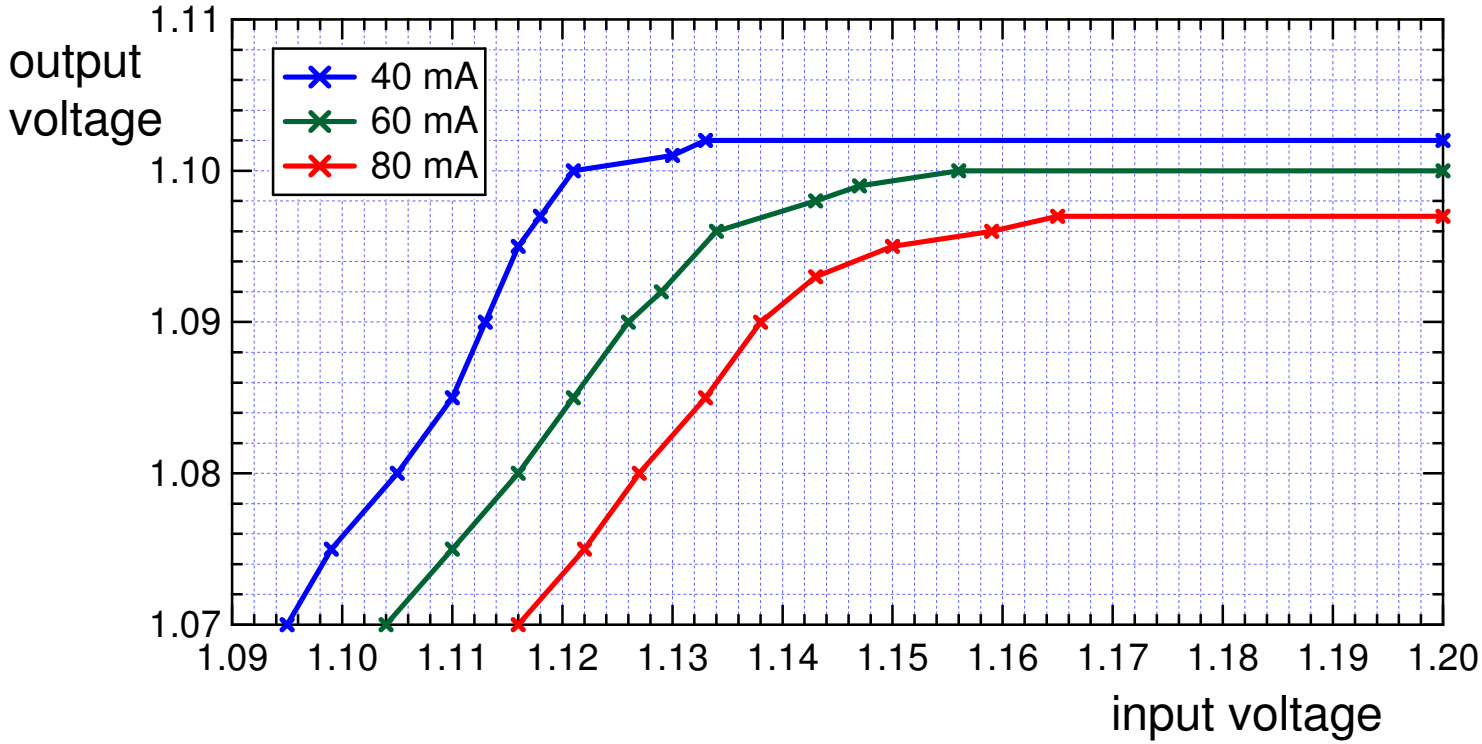


currents/channel deduced from current drawn from VDD as register value swept

magnitudes v. similar to CBC1

something weird happening with ICOMP but a long way from normal operating region

LDO performance



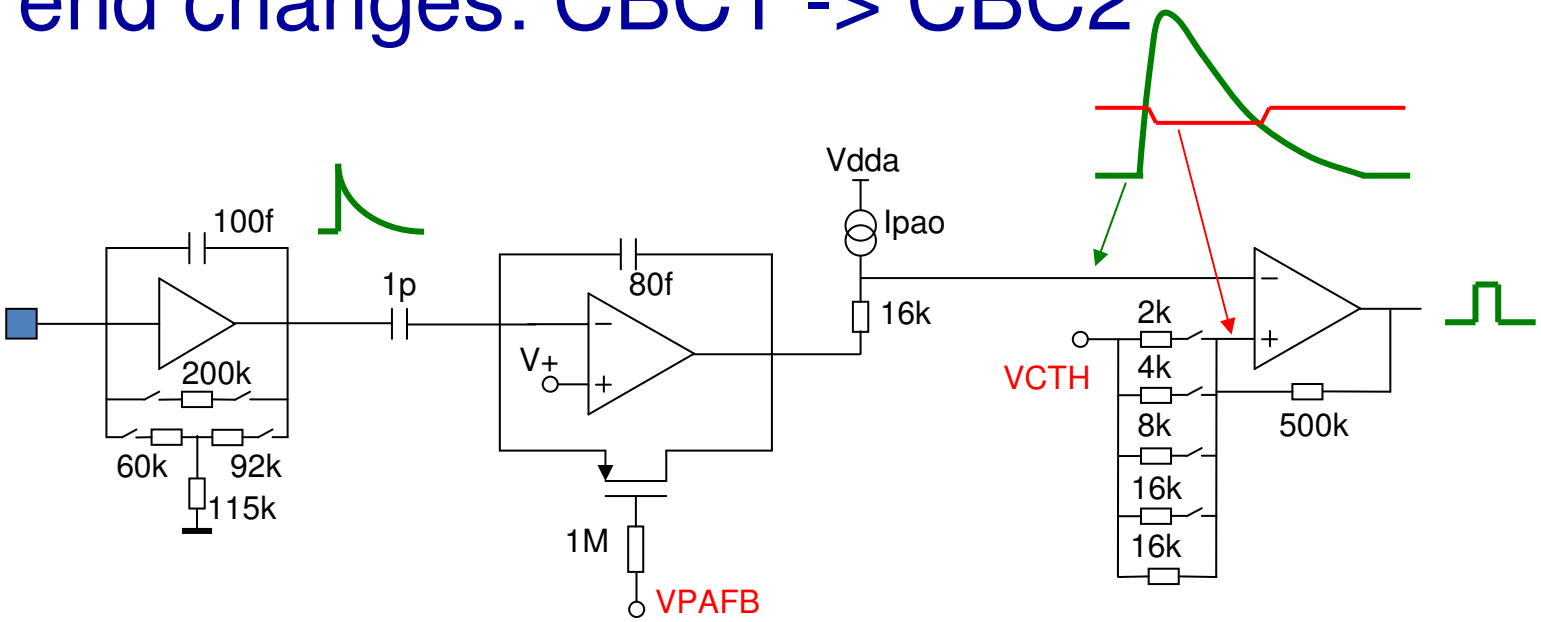
LDO

load currents 40, 60, 80 mA
dropouts ~ 30, 55, 70 mV (approx.)
DC shift due to series resistance
50 mOhm on-chip + wire-bond resistance (which will go away when bump-bonded)

other power related measurements

measured band-gap voltage: 0.604 (for this chip)
quiescent power consumption from VDDD
all bias currents set to zero, SLVS off ~4.4mA
all bias currents set to zero, SLVS ON ~6.7mA

front end changes: CBC1 -> CBC2



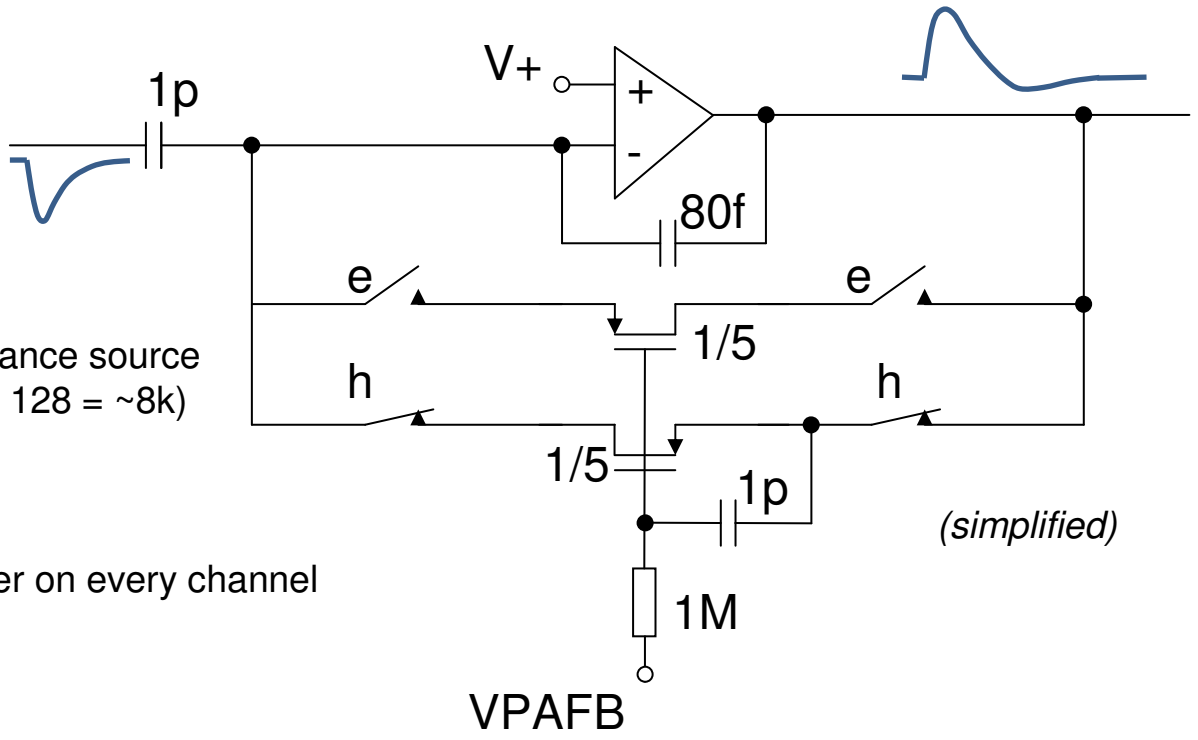
2 significant problems

postamp: VPAFB susceptible to CM effects
needed external decoupling for stability

comparator: VCTH affected by external hysteresis network
external overdriving solved the problem

also input test pulse caps there, but no on-chip circuit to drive

post-amplifier

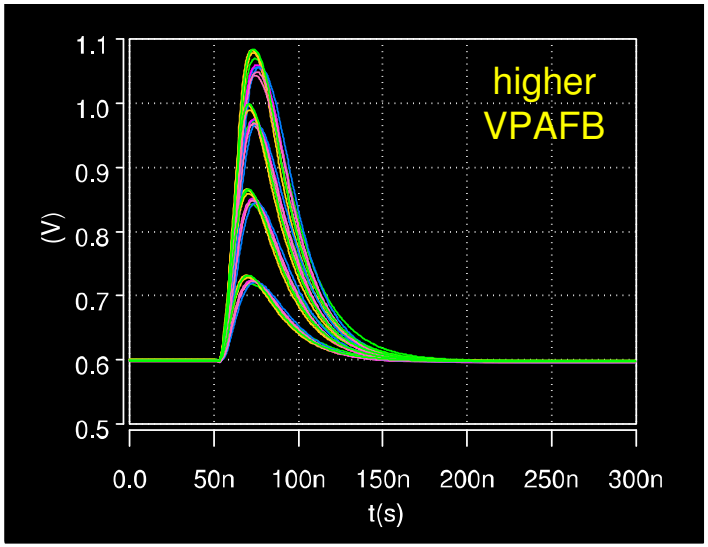


CBC1

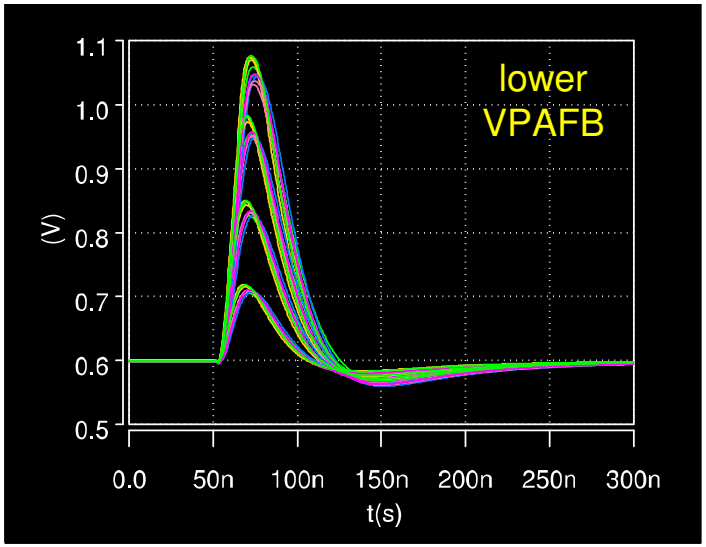
VPAFB provided from high impedance source susceptible to CM instability (1M / 128 = ~8k) solved by external decoupling

CBC2

VPAFB buffered by source follower on every channel

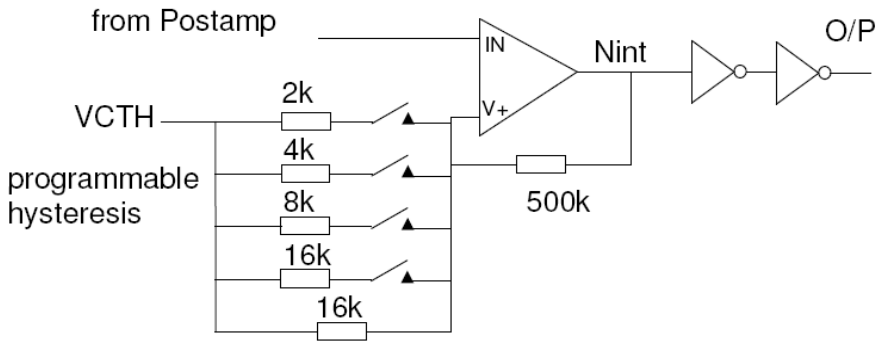


VPAFB controls back edge of postamp O/P pulse shape

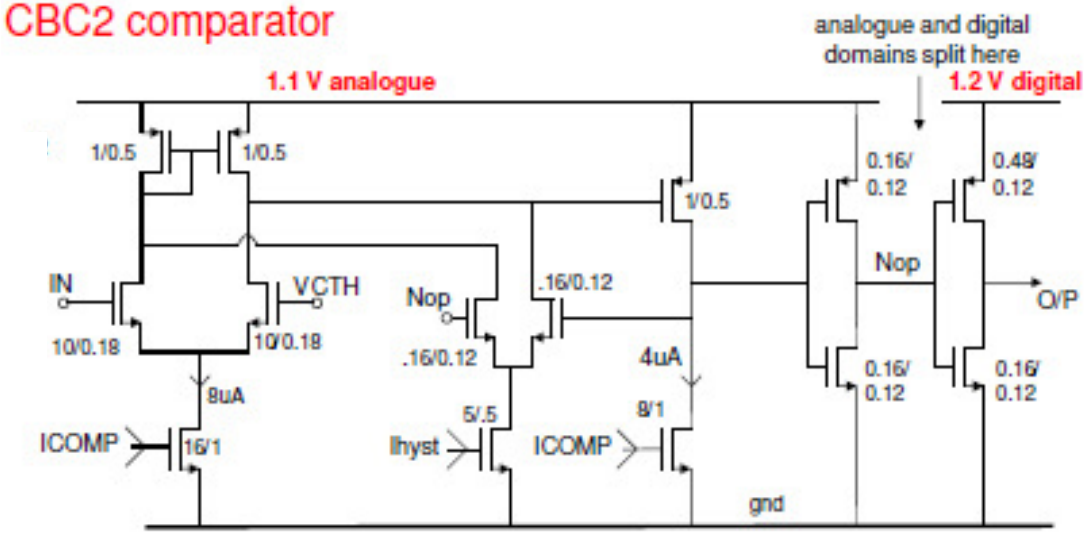


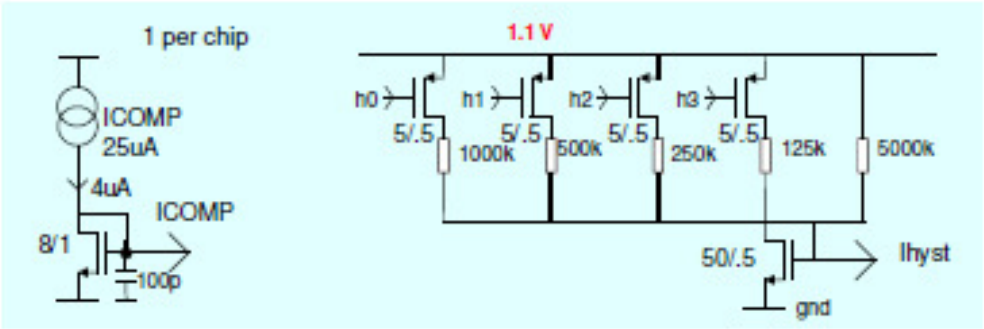
comparator
CBC1 vs. CBC2

HYSTERESIS CIRCUIT on CBC1



CBC2 comparator





new comparator uses internally generated hysteresis - no load on VCTH

but so far have not found it necessary to use hysteresis anyway

CBC1 or CBC2

on-chip test pulse

DLL circuit allows to inject charge with programmable phase relative to 40 MHz clock

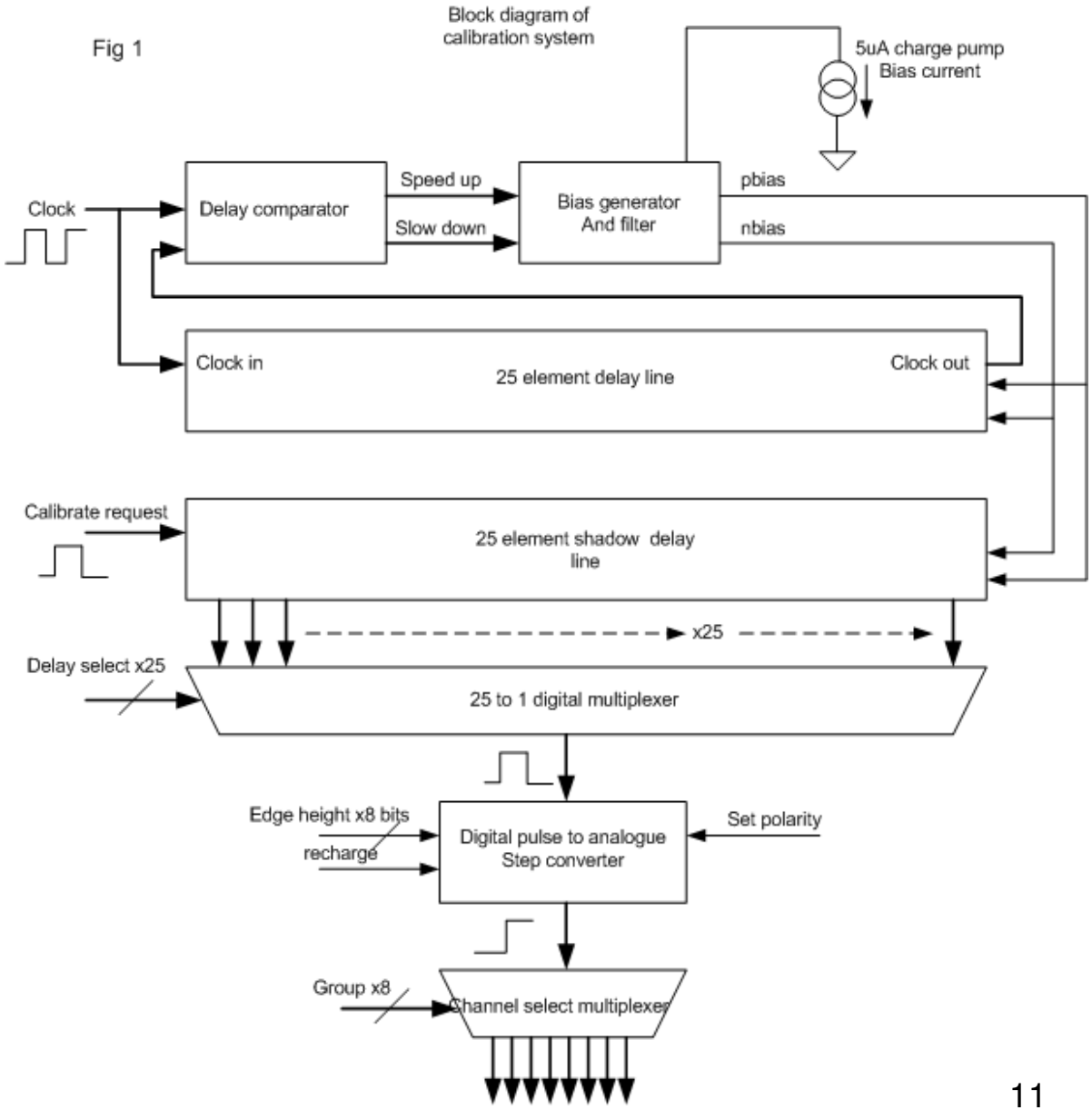
25 steps of 1 nsec

some evidence (during testing) of DLL losing lock occasionally

can be restarted by disabling and re-enabling via I2C

needs further investigation

figure from CBC2 manual



on-chip test pulse

test pulse amplitude provided by resistor string between 1.1V & GND
256 steps

charge inject polarity depends on which switch closed

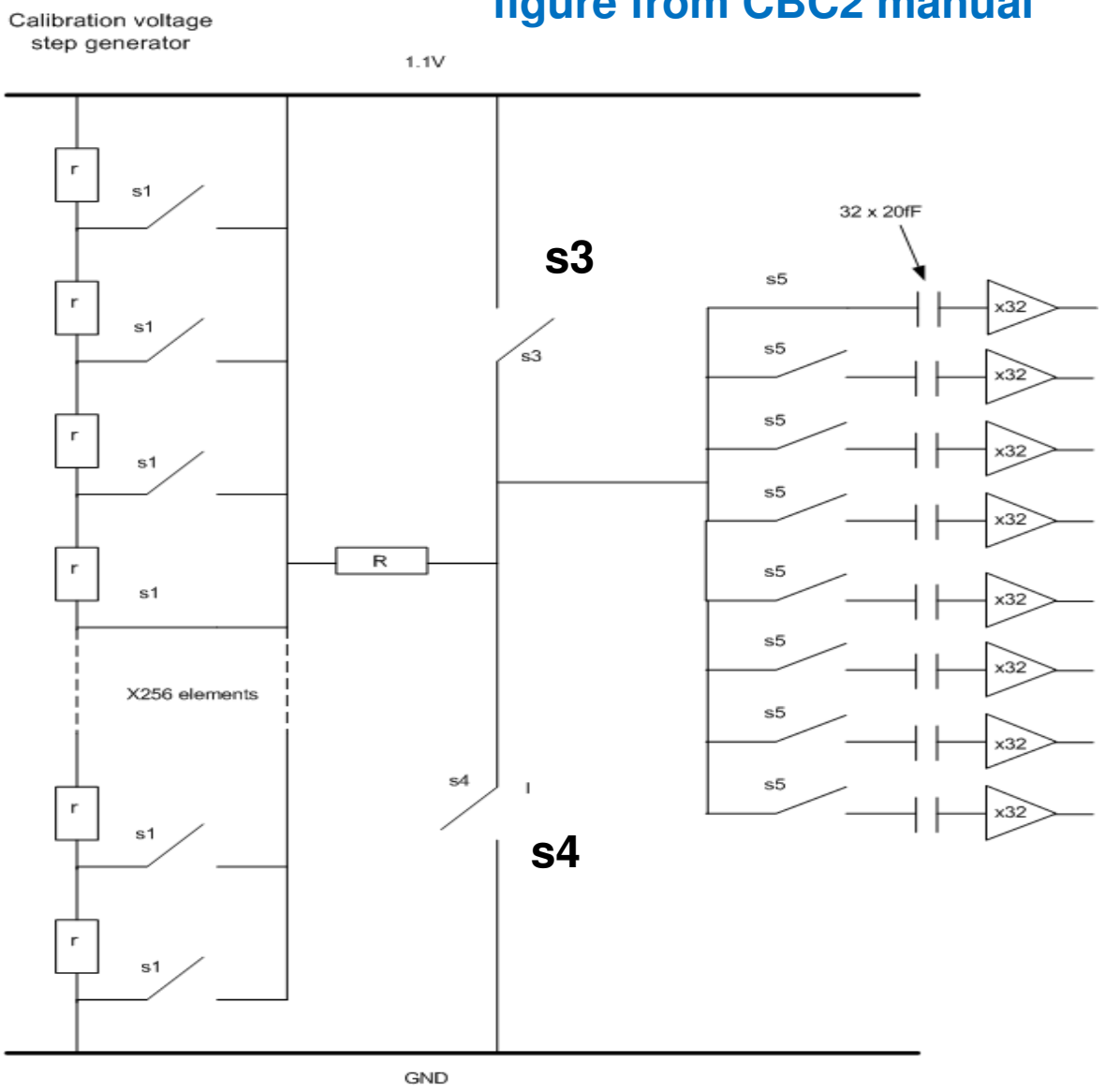
charge injected into 32 channels simultaneously through 20 fF caps

20fF largest source of uncertainty

20fF x (1.1V / 256)
= 0.086 fC step resolution

e.g. value of 12 corresponds to
~ 1 fC (+/- 10%)

figure from CBC2 manual



test pulse sweep

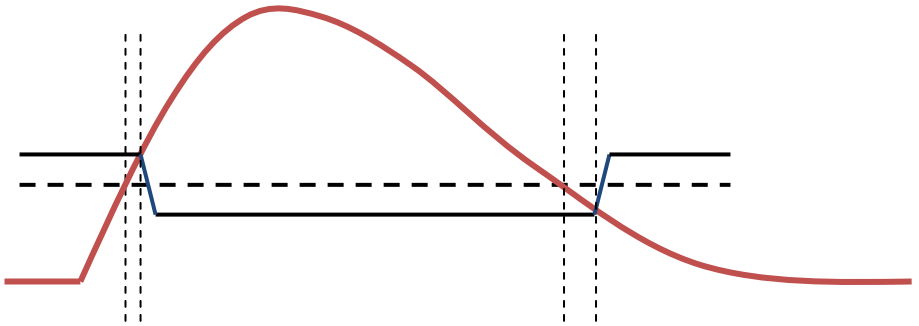
sweeping charge injection time allows to study comparator behaviour

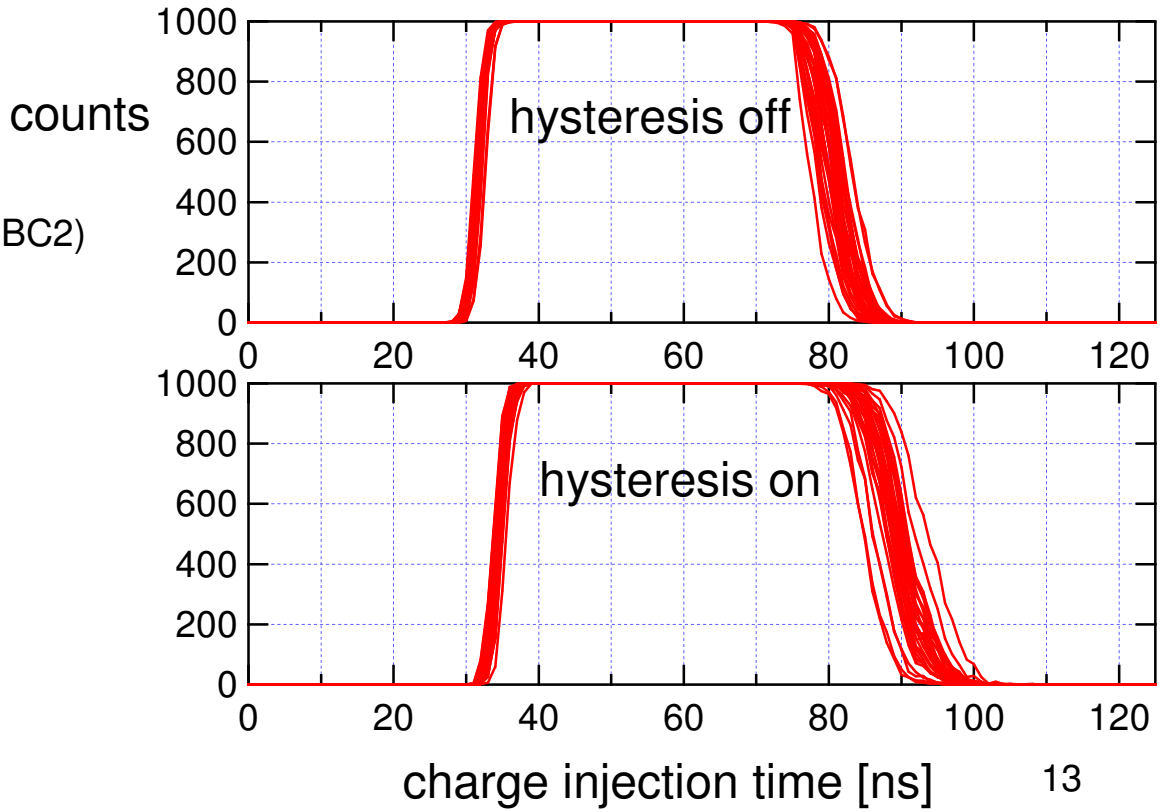
count the number of times hit observed for fixed number of triggers, for each timestep

get coarse steps of 25 nsec by moving test trigger fast control pulse

get 1 nsec resolution using DLL steps

hysteresis circuit working as expected (note: new method of implementing in CBC2)



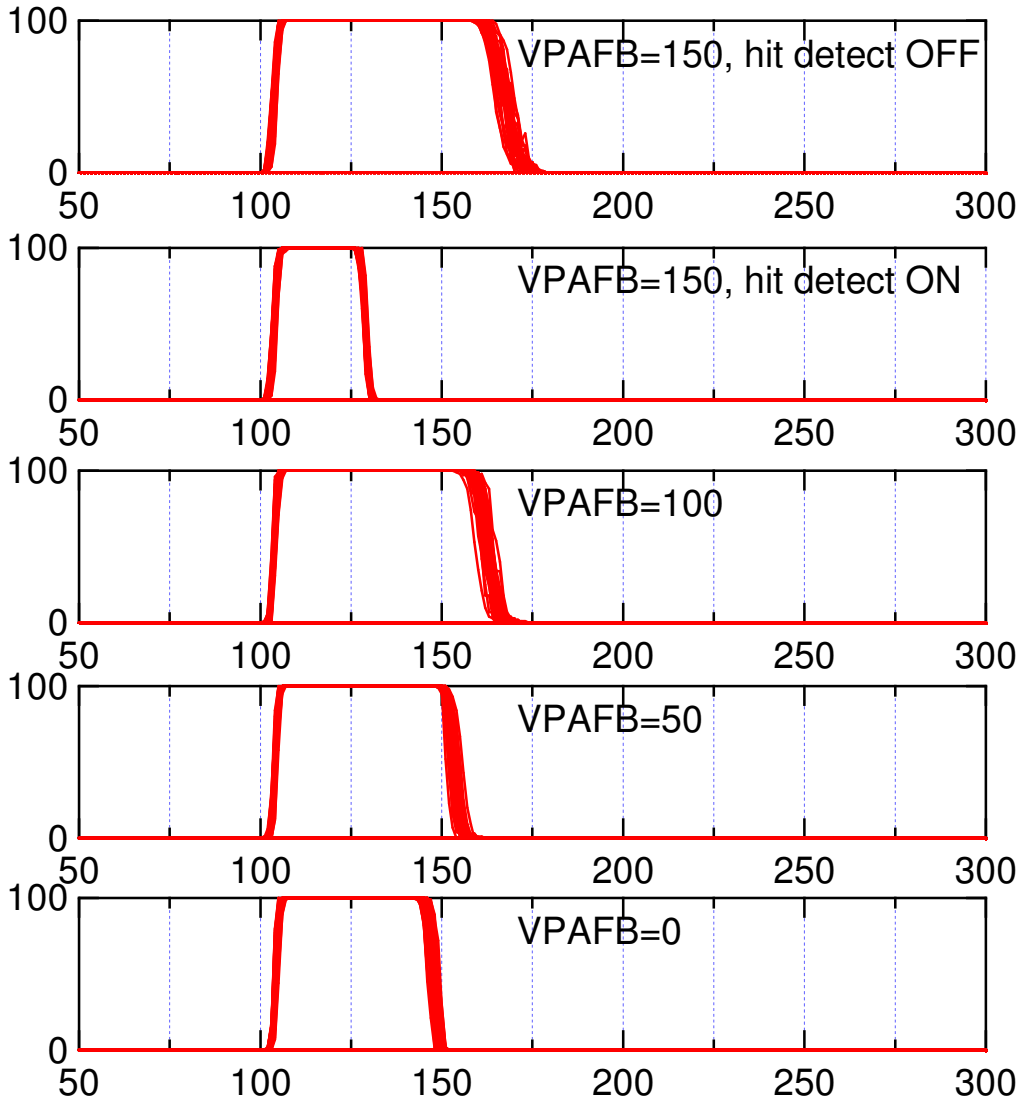


post-amp feedback resistor control

can see effect of VPAFB using
test pulse sweep - smaller values give
shorter pulse length

hit detect circuit works - only single hit
in pipeline irrespective of how long comp
O/P stays high

~ 2 fC signal
~ 1 fC comp. thresh



pulse length vs. amplitude

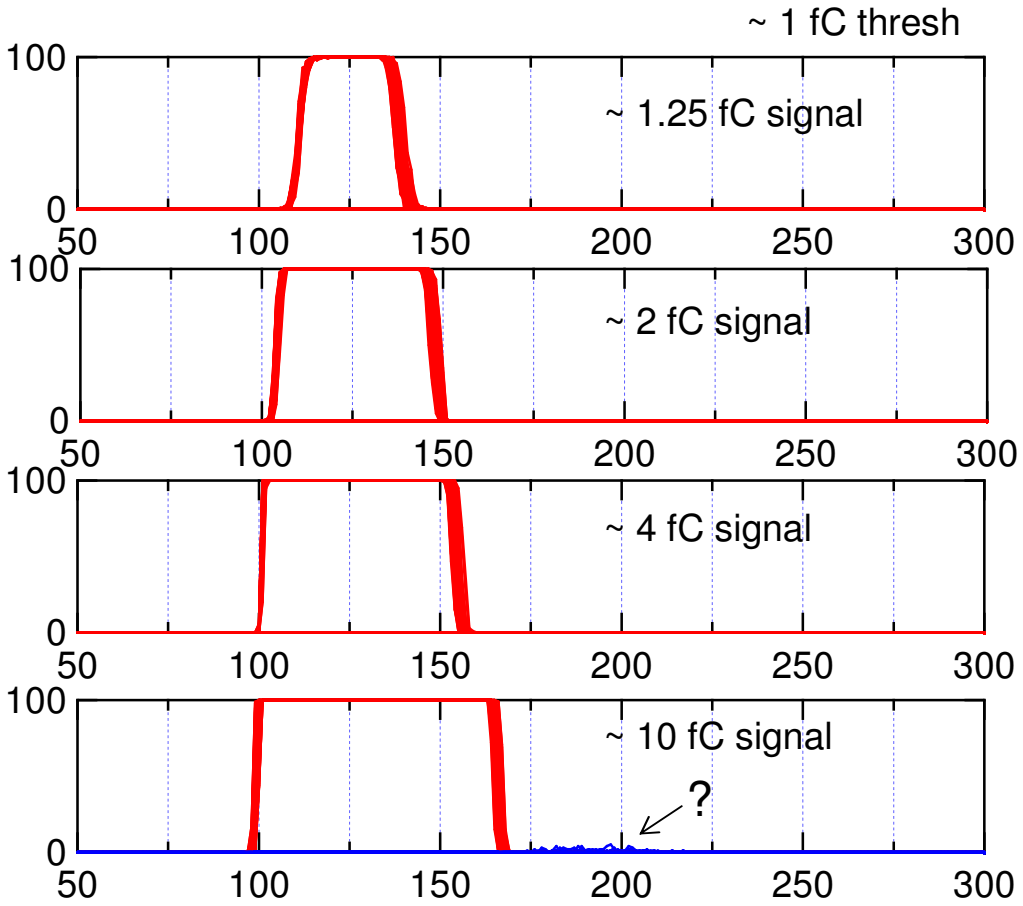
ideally (to address dead-time issue) want comparator high for less than 50 ns

not case for signals > ~ 2 fC

=> can study dead-time vs. pulse length using CBC2 but postamp feedback FET will probably need tweaking for CBC3

note: all plots contain 254 channels data
10 fC plot shows activity in channels not being driven by test pulse

crosstalk? power supply disturbance?



gain

sweep global comparator threshold VCTH
to get s-curves for different TP amplitudes

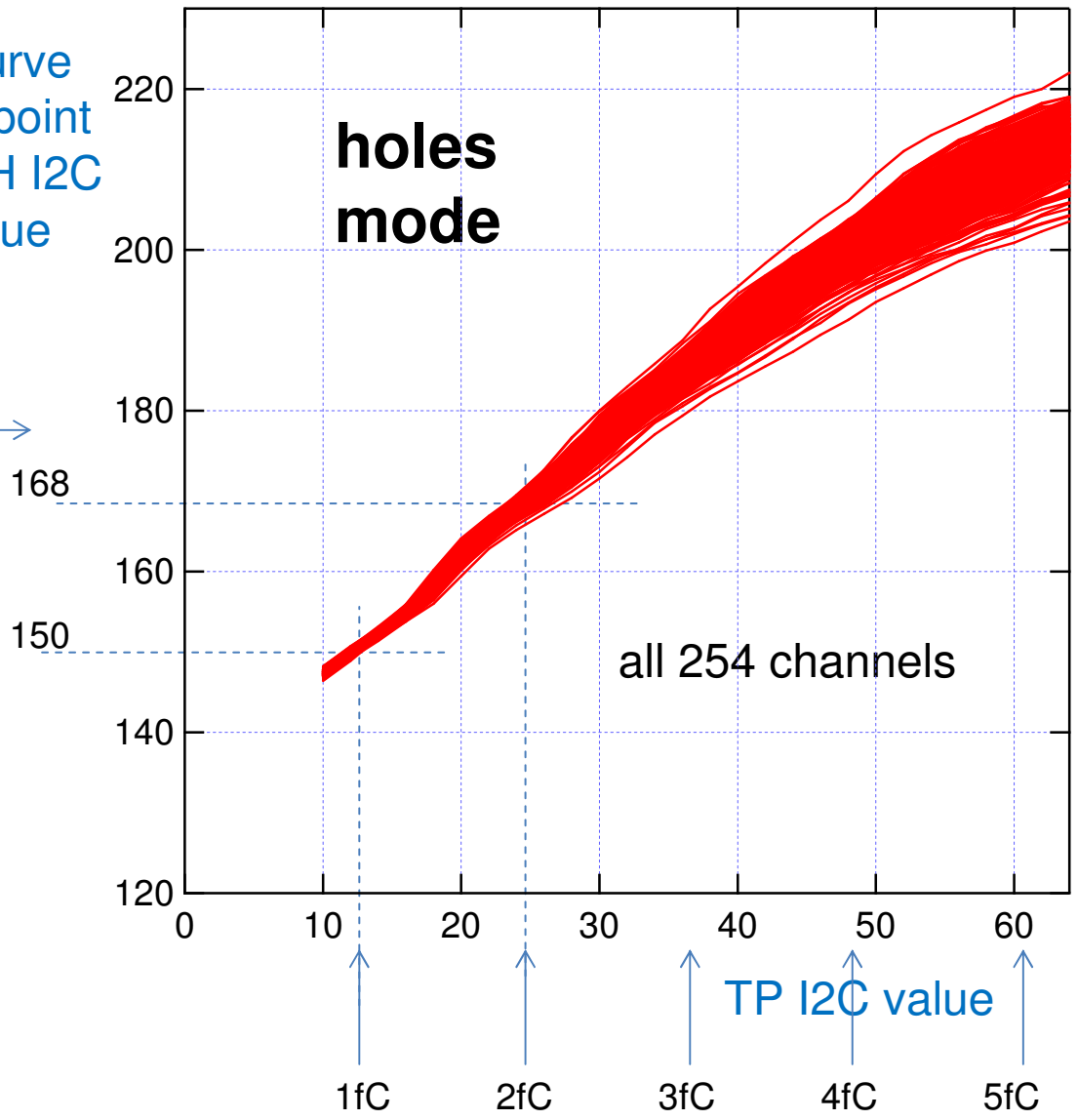
plot s-curve mid-points vs. TP amp →

rough calculation
(assumes TP value of 12 / fC)

(168 - 150) x 2.5 mV

= 45 mV / fC

note: “wavy” nature of characteristic

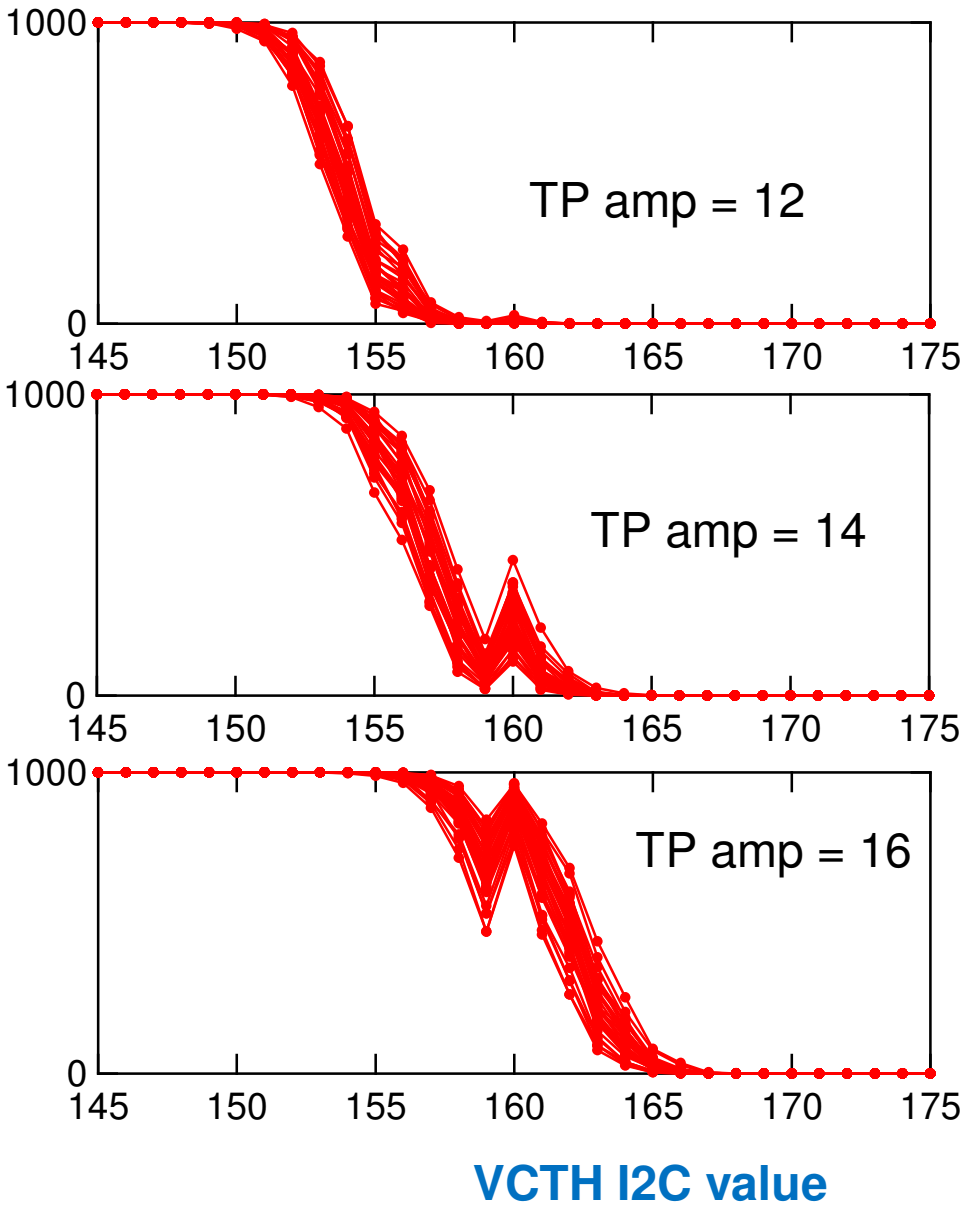


s-curve skew

s-curve mid-points obtained by fitting raw data with erfc function

value gets skewed by non-linearity of VCTH

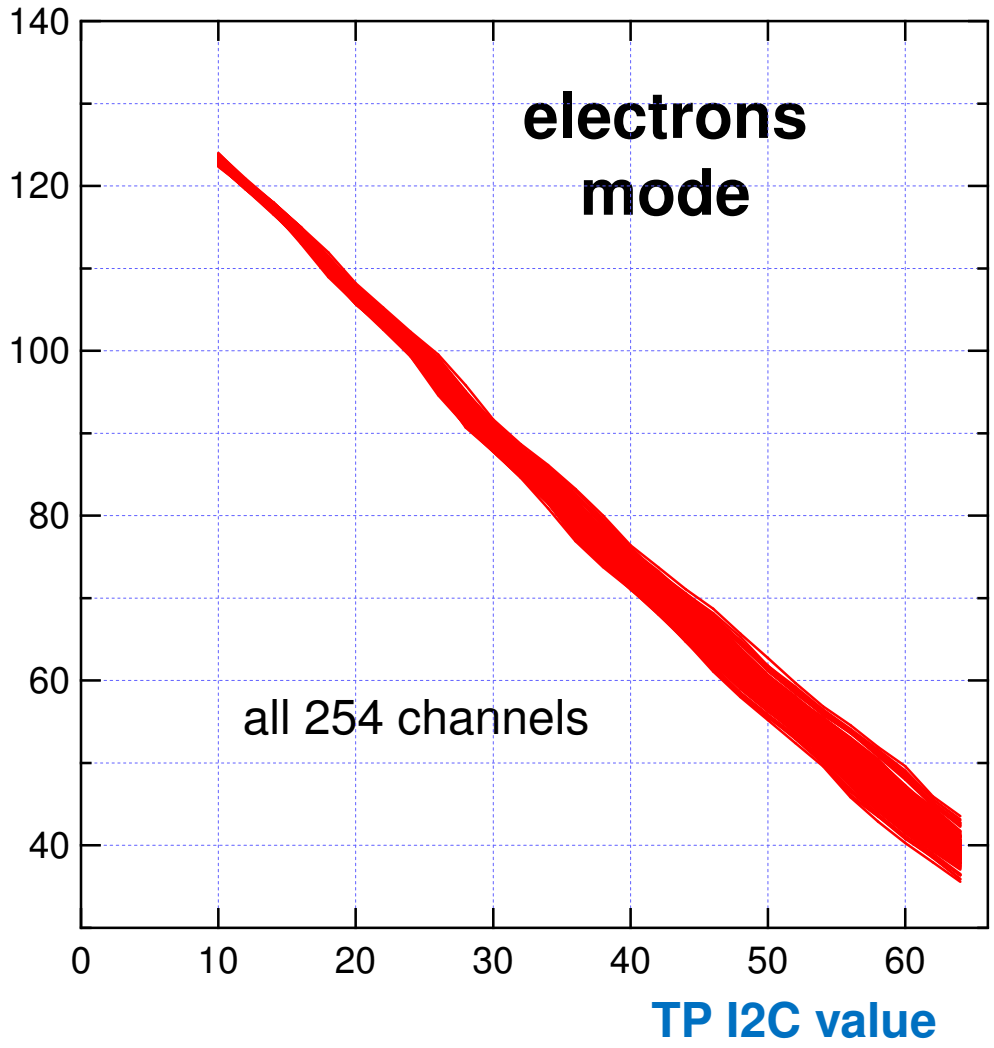
not a big problem, but worth trying to improve



gain - electrons mode

have concentrated on results in holes mode, but electrons mode ok too

all results and characteristics similar



summary

early conclusion still stands

> “CBC2 working well enough to allow progress with module development”

only minor problems/inconveniences identified so far

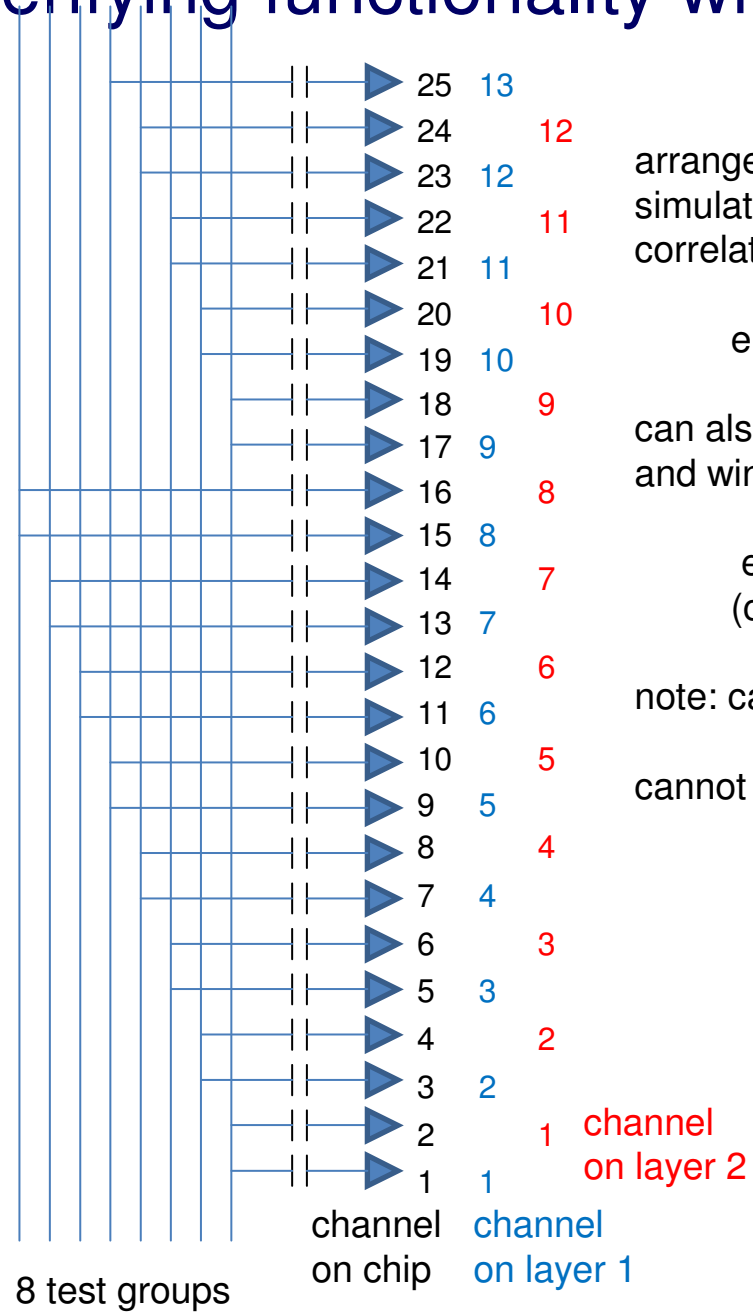
> test pulse DLL occasionally loses lock
> VCTH differential non-linearity
> evidence of crosstalk for high test pulse amplitudes
>
> better to study further on bump-bonded setup

future for wire-bonded chip setup

> now ready to refine wafer probe procedure
>
> could be useful for ionising radiation studies using X-rays

extra

verifying functionality with test pulse



arrangement of 8 groups of test pulse connections allows to simulate signals from different layers and therefore exercise correlation logic

e.g. channels 1 & 2, or 17 & 18 would originate in different layers

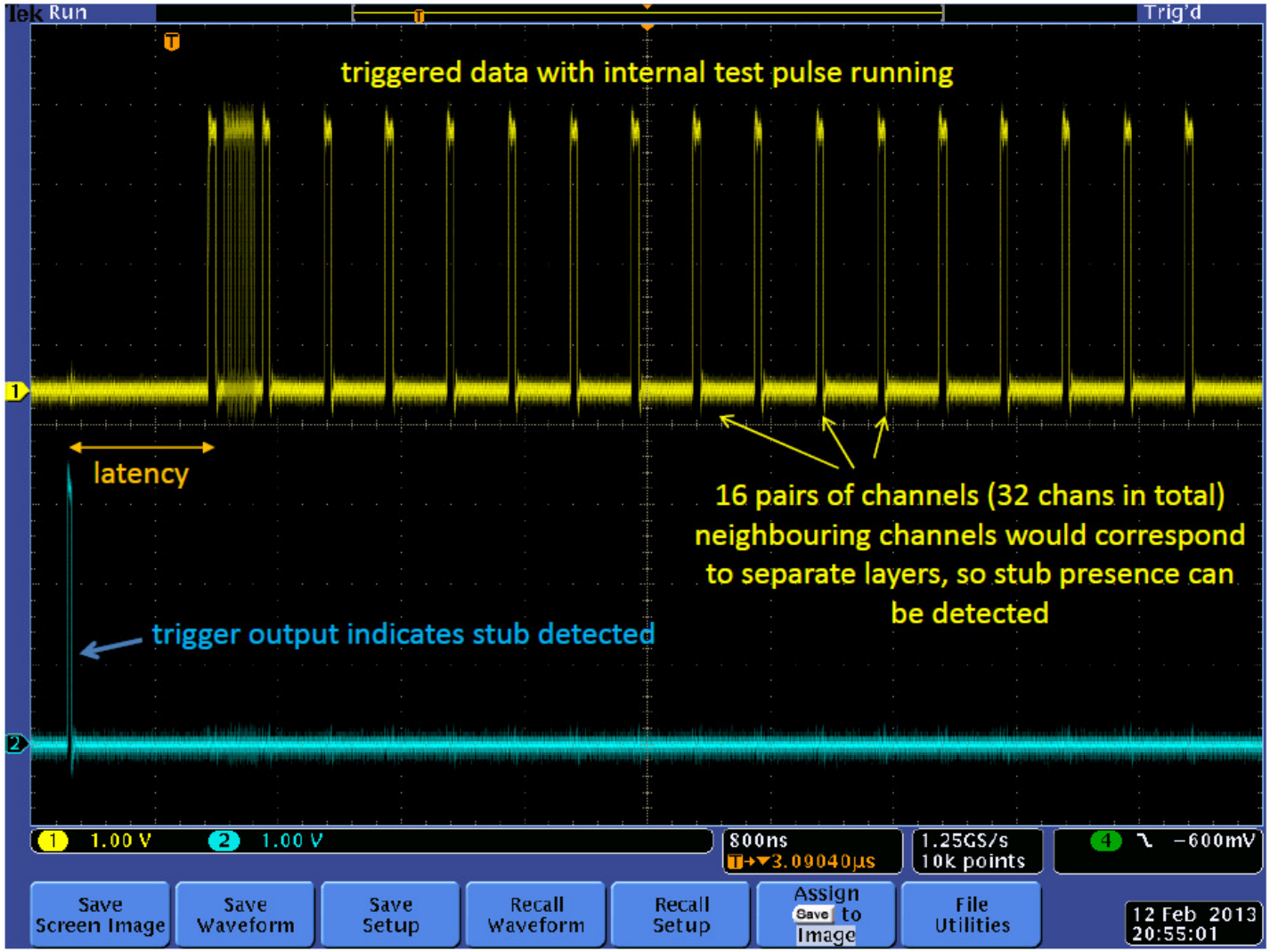
can also verify correlation window width using channel mask register and window offset

e.g. mask all channels except 1 and 18 and use wide window (correlate channel 1 on layer 1 with channel 9 on layer 2)

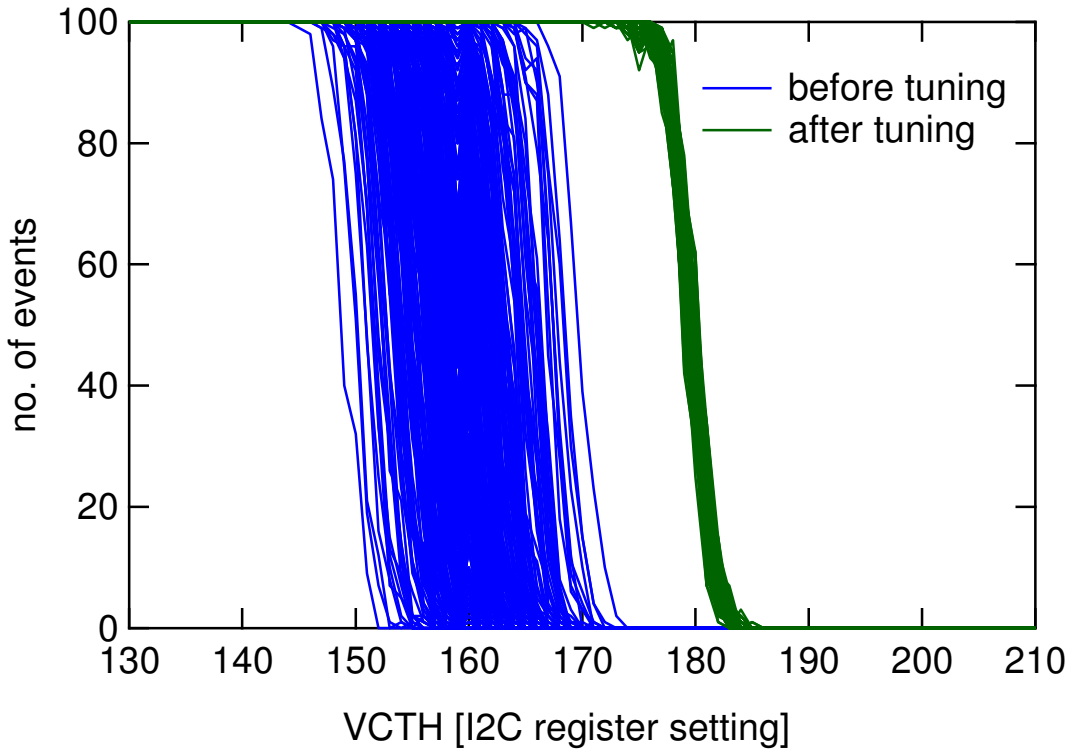
note: can only use one test group at a time

cannot exercise CWD logic

first result



S-curves and tuning



254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to VCTH setting of 180

254 offset values after tuning