CBC2 testing status

CMS Tk phase II electronics meeting – March 7th, 2013

the last few weeks

17th Jan: 6 wire-bond wafers arrived RAL
- C4 pads on CBC2 unfinished, but back edge probe test pads available
- 1 wafer sent for dicing

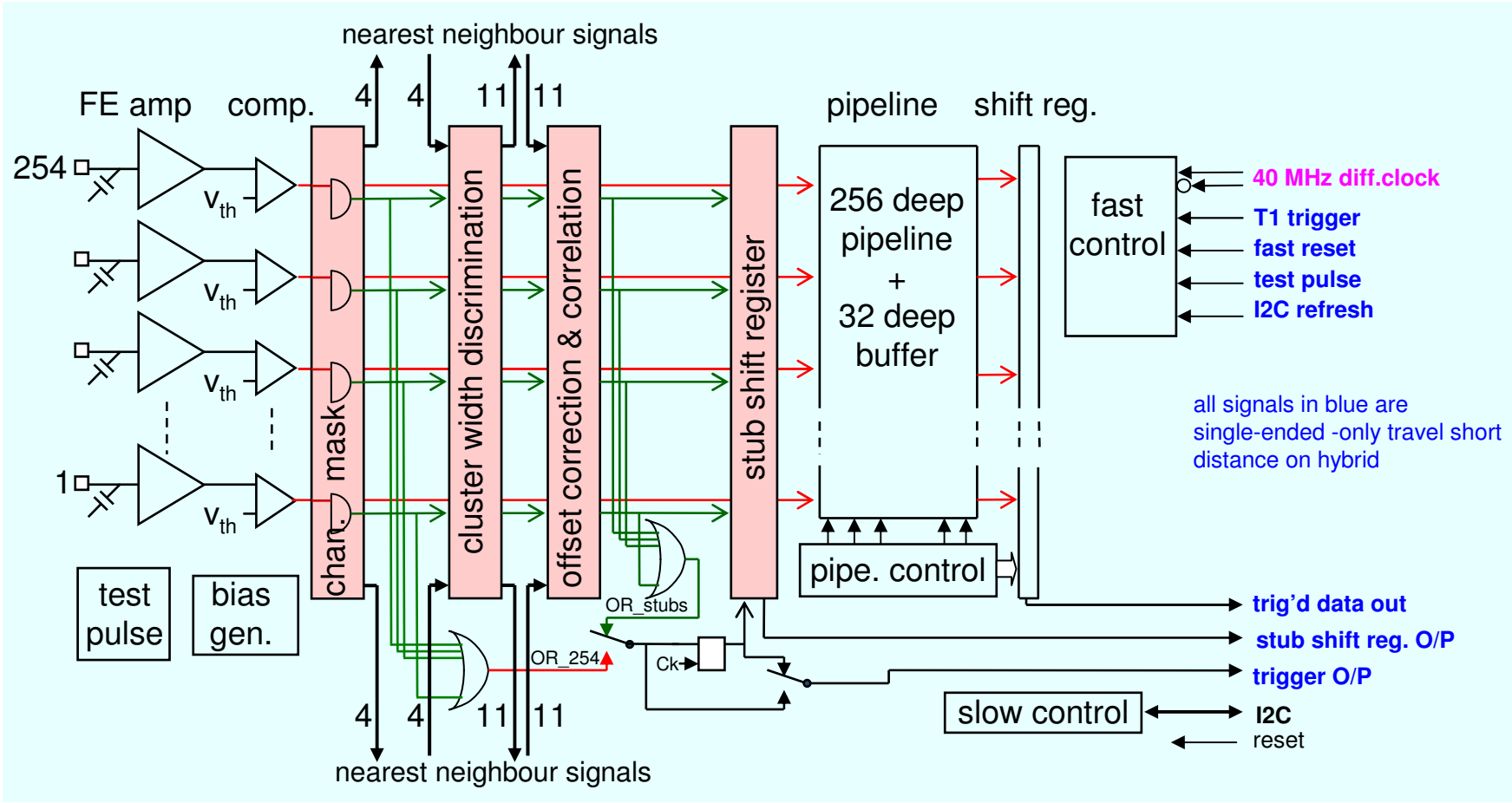
21st Jan: 8 C4 wafers arrived RAL

8th Feb: wire-bond chip mounted on test board at IC
- single chip testing begins
  - emphasis on verifying basic functionality
  - quickly move to developing wafer screening procedure

27th Feb: wafer testing begins

1st March: 1st C4 wafer to cutting company

CBC2 architecture



main changes from prototype

fixes some front end bugs: postamp feedback CM instability, comparator external hysteresis problem

added features: test pulse to all channels, programmable delay and amplitude

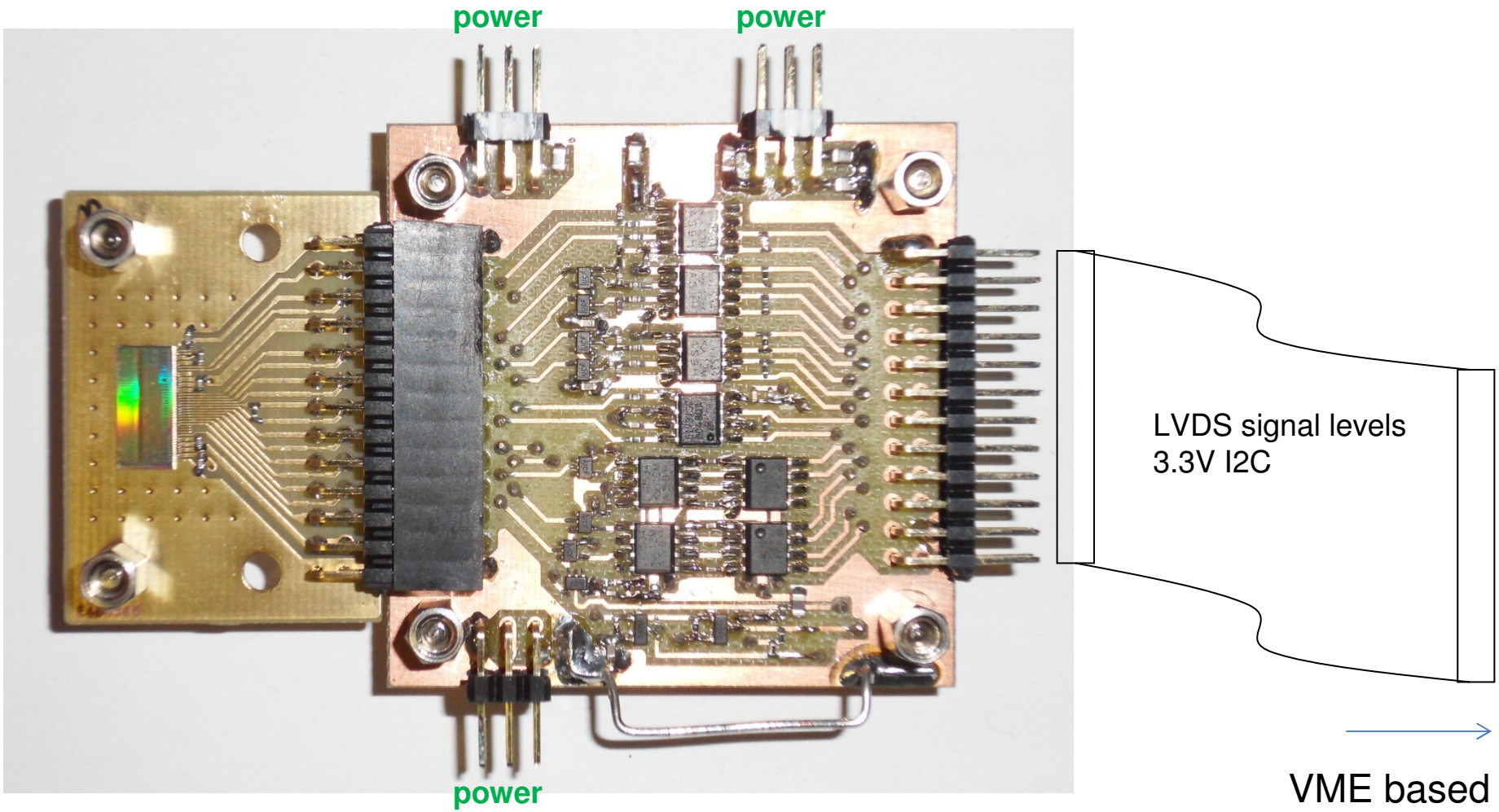
channel masking, CWD and correlation logic, trigger output (single 25ns bit => correlation found)

stub shift register test feature

254 channels, bump-bond layout

all control signals single-ended except for 40MHz clock

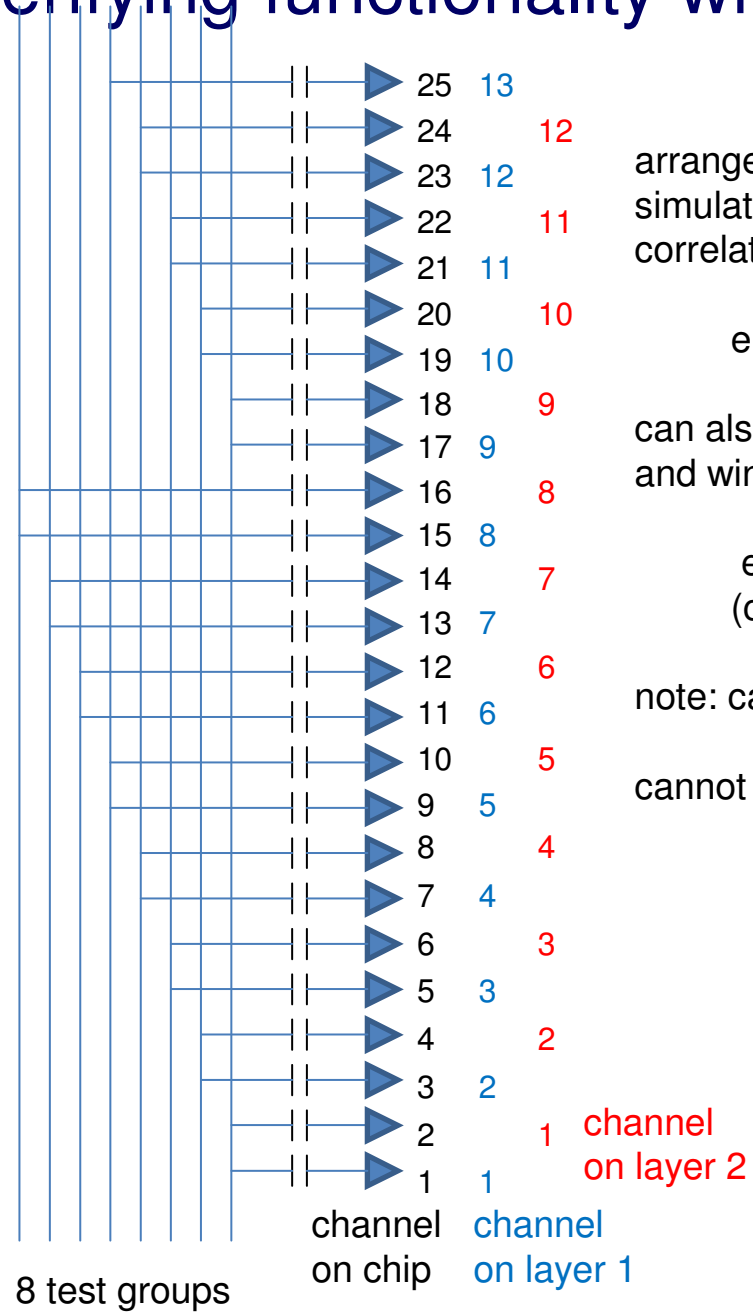
wirebond CBC2 test setup



use wafer probe pads to wirebond single CBC2 die to carrier
(CBC2 chips from diced wire-bond (XFEL) wafer)

convenient setup for developing detailed wafer probe procedures

verifying functionality with test pulse



arrangement of 8 groups of test pulse connections allows to simulate signals from different layers and therefore exercise correlation logic

e.g. channels 1 & 2, or 17 & 18 would originate in different layers

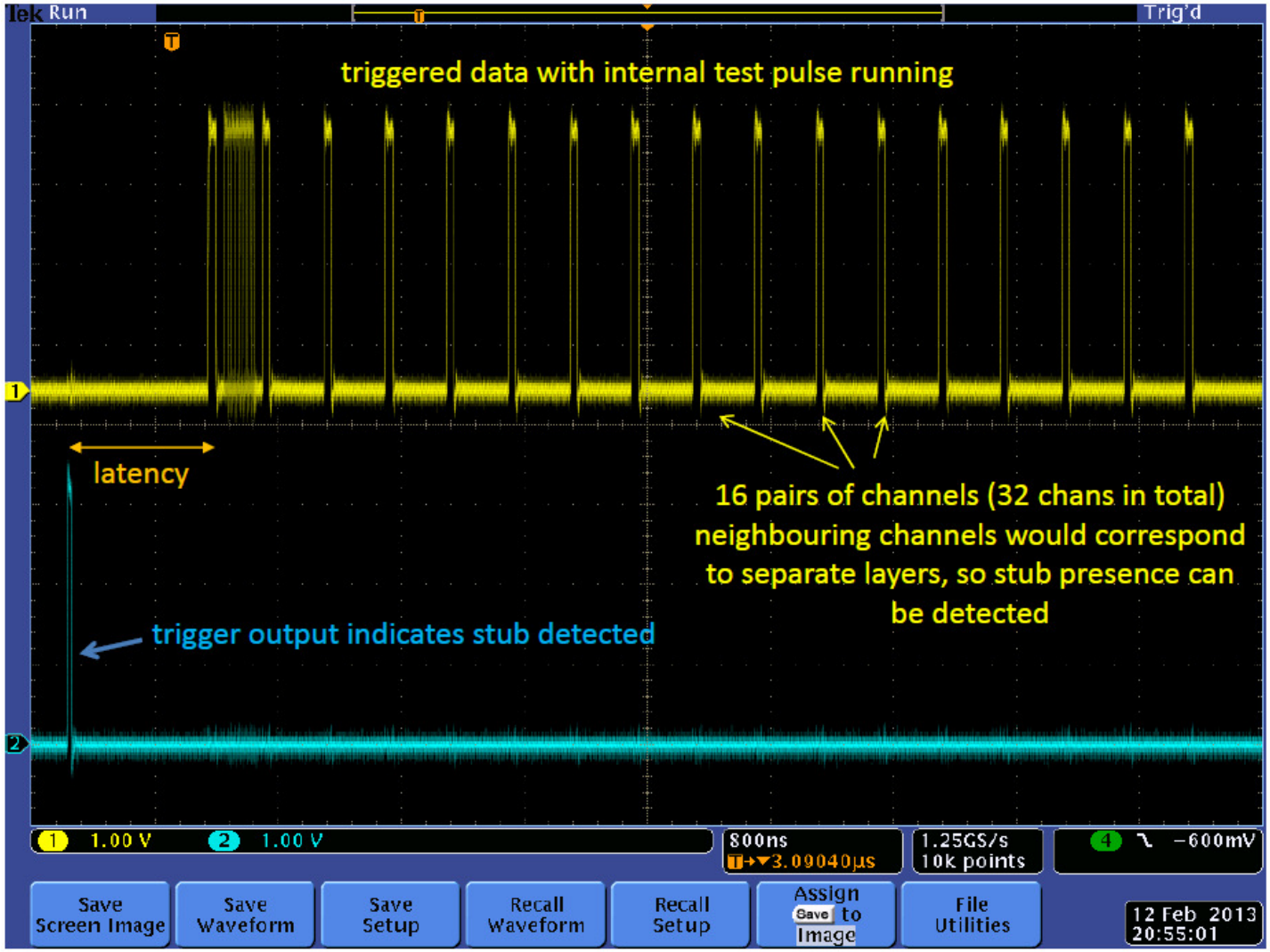
can also verify correlation window width using channel mask register and window offset

e.g. mask all channels except 1 and 18 and use wide window (correlate channel 1 on layer 1 with channel 9 on layer 2)

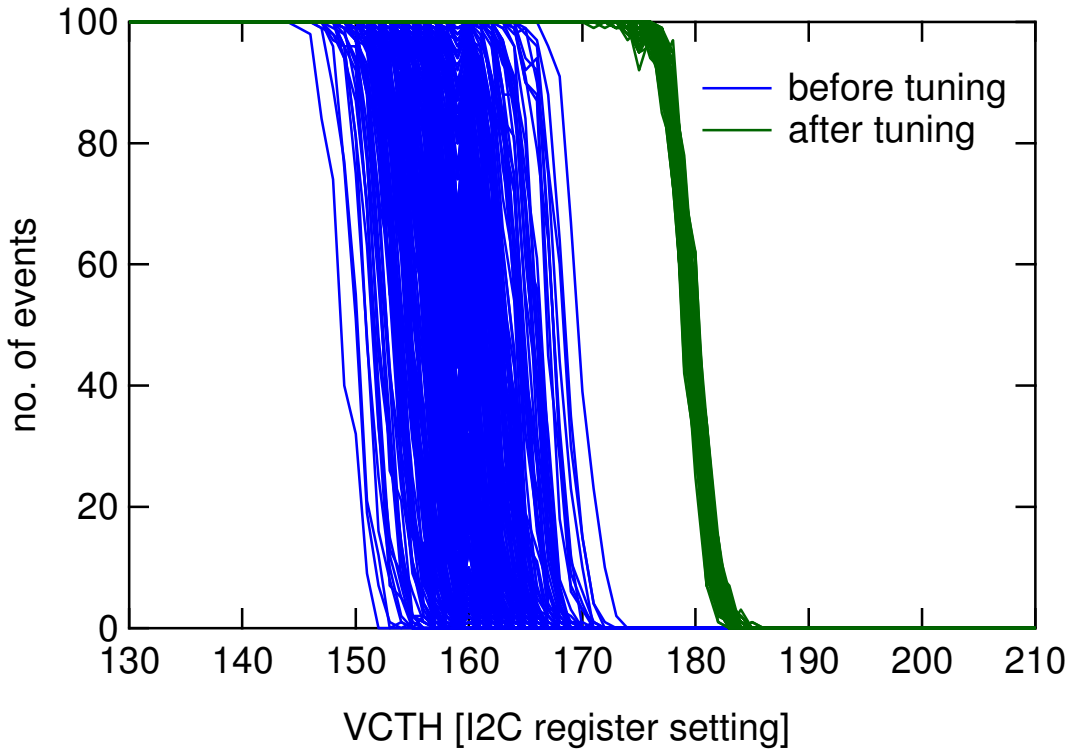
note: can only use one test group at a time

cannot exercise CWD logic

first result



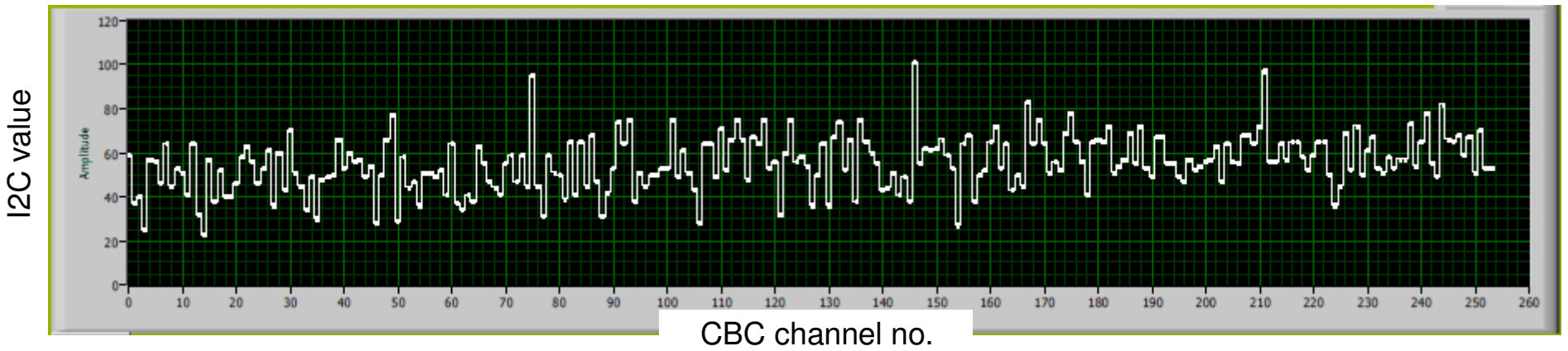
S-curves and tuning



254 S-curves measured with on-chip test pulse

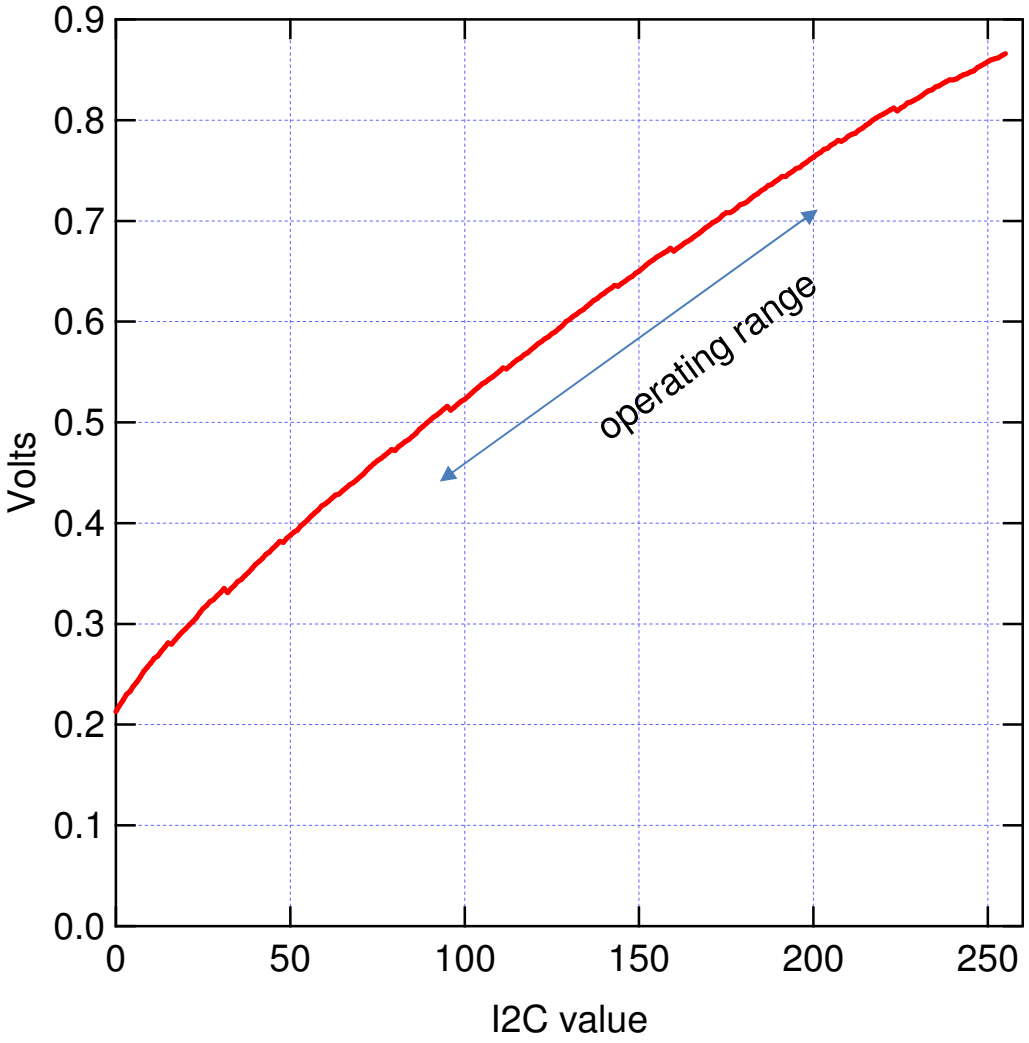
S-curve mid-points tuned to VCTH setting of 180

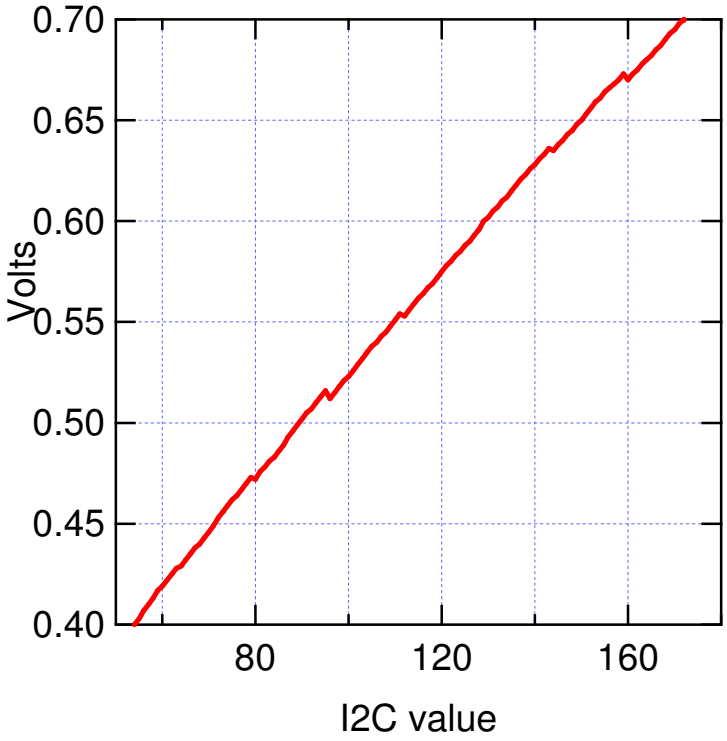
254 offset values after tuning



VCTH vs I2C setting

analogue mux gives access to all bias generator outputs





~3.3 mV / I2C value

=> ~ 450 electrons / I2C value

qualitative observations

approach to chip measurements so far rather superficial
emphasis on verifying functionality without detailed study

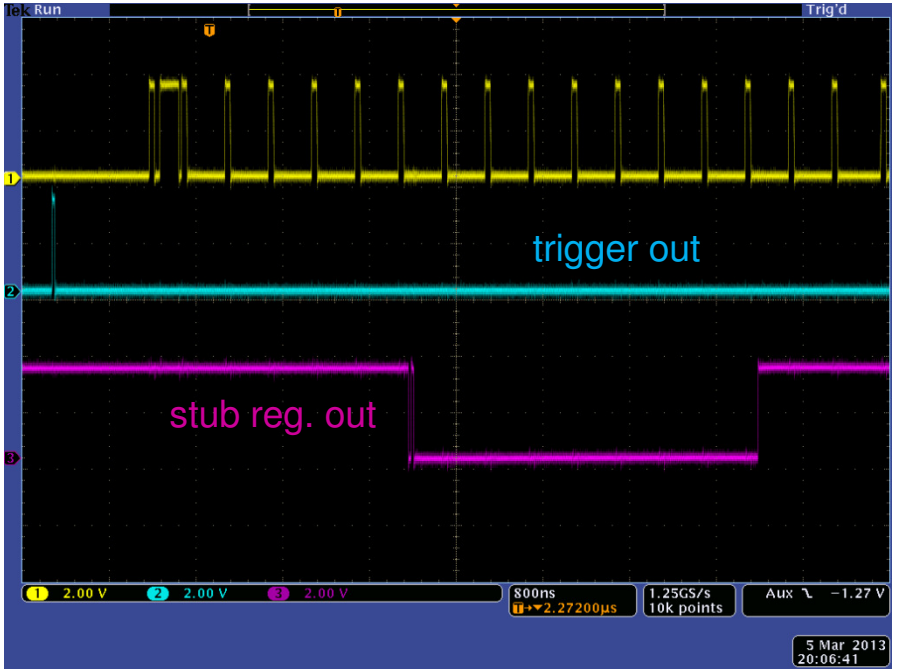
what can be said?

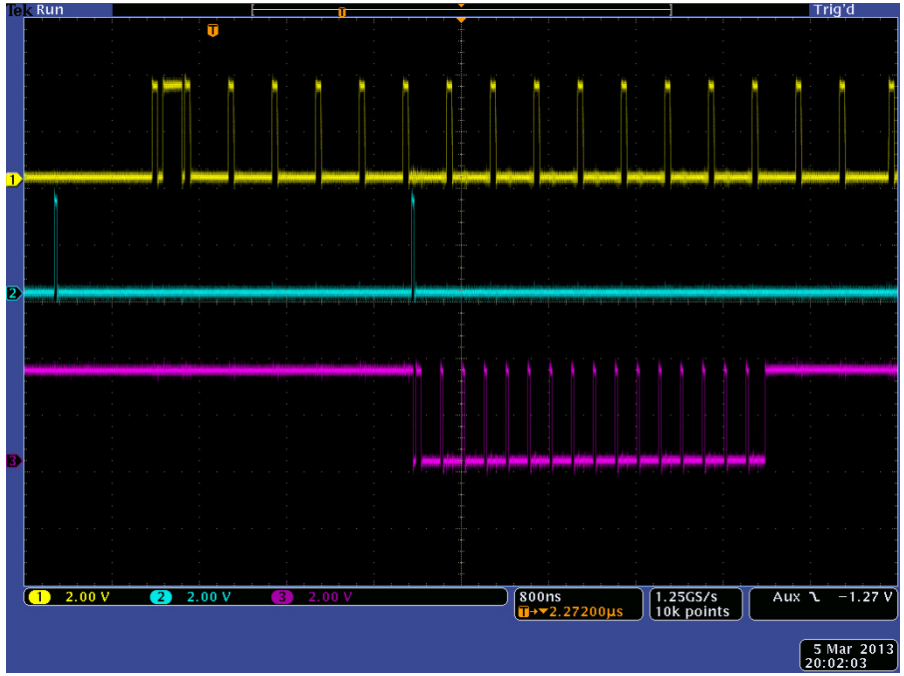
no signs of instability => fixes have worked
power consumption seems “about right”
LDO functioning as expected
2.5 -> 1.2 DC-DC converter also functioning
correlation and window logic verified as far as possible

detailed studies may yet show undesirable features, but chip almost certainly working well enough to allow module development to progress

=> have spent most time preparing basic wafer probe test procedure

stub shift register has a bug



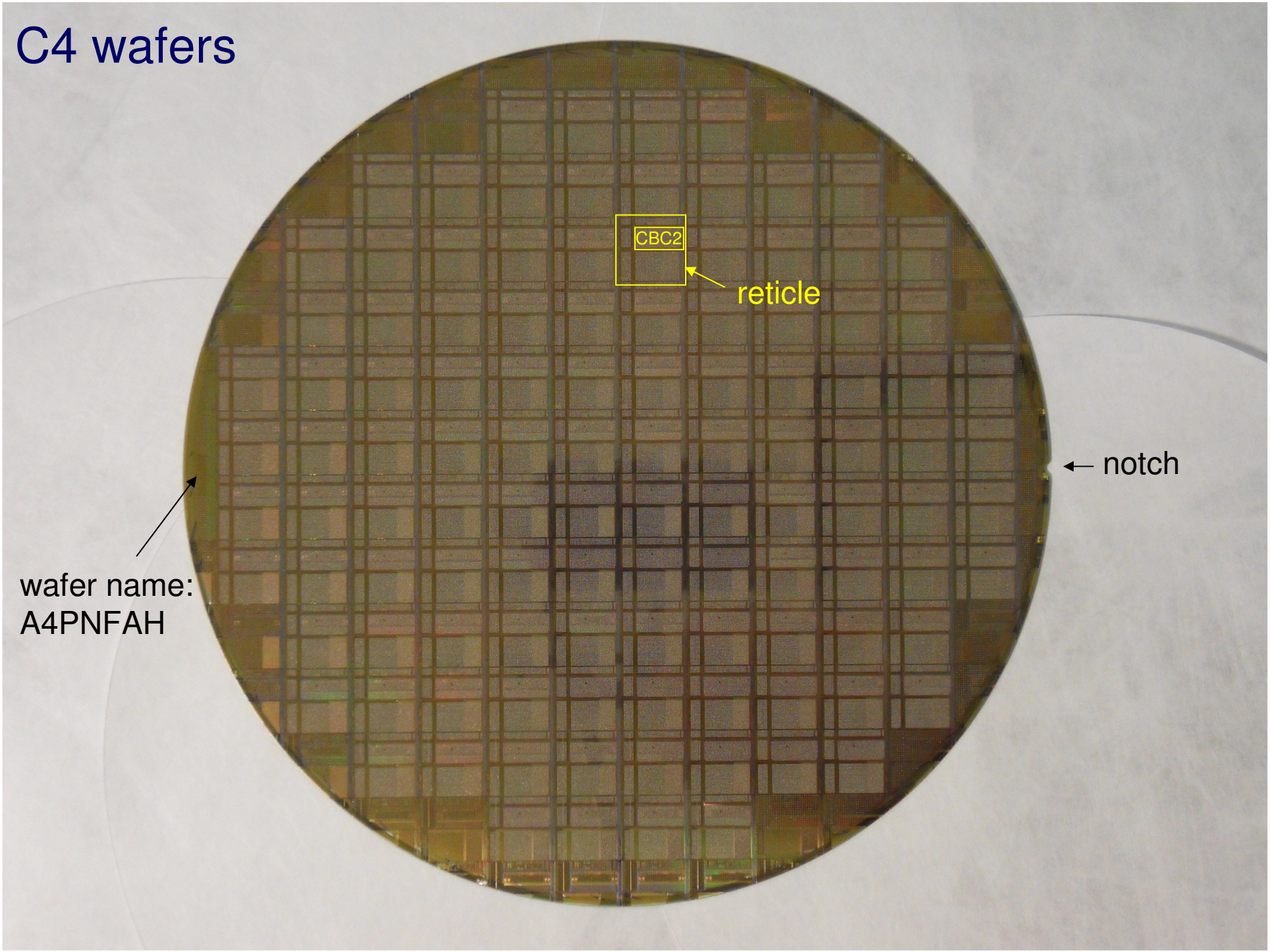


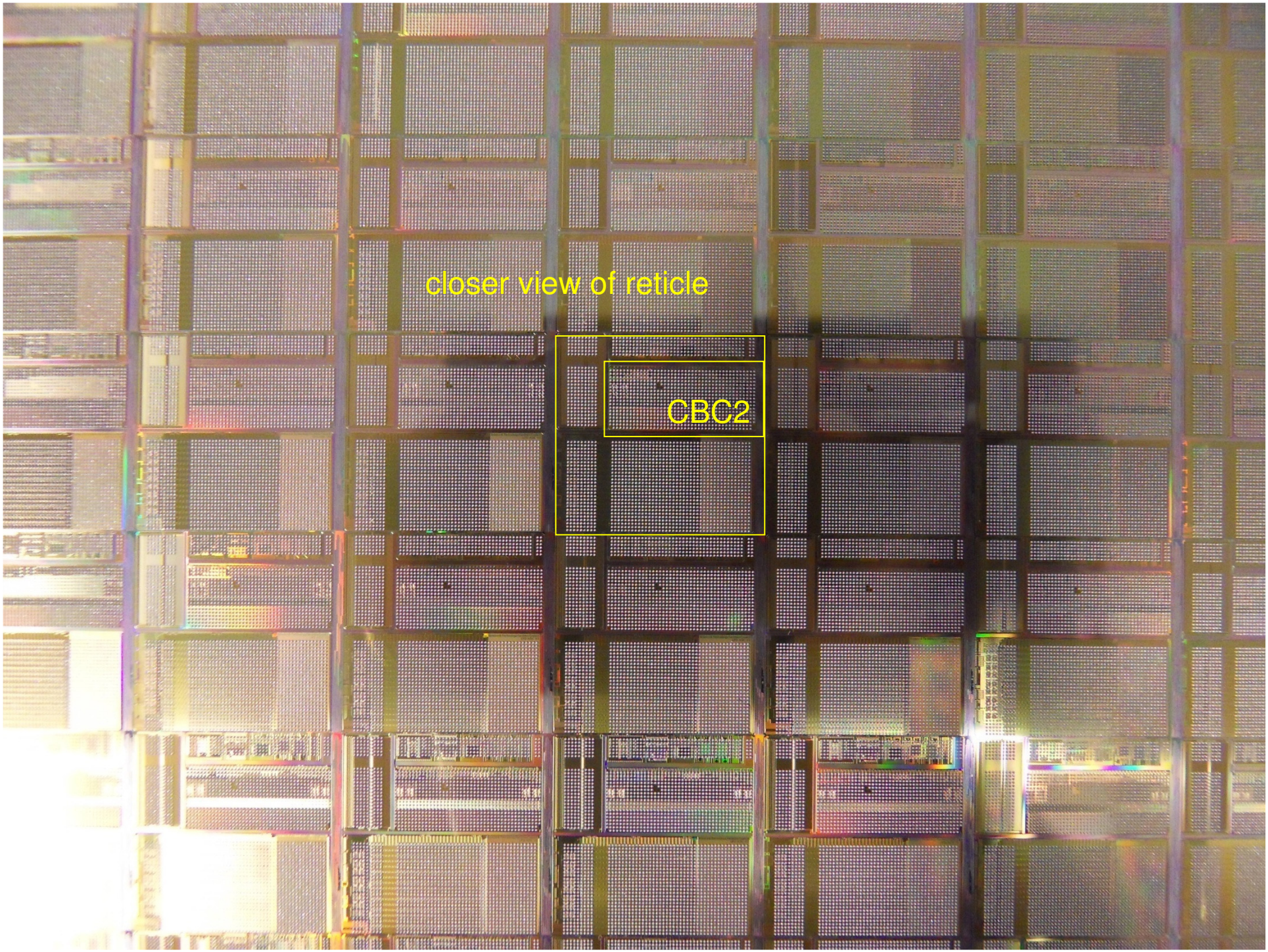
logic mistake when assembling chip

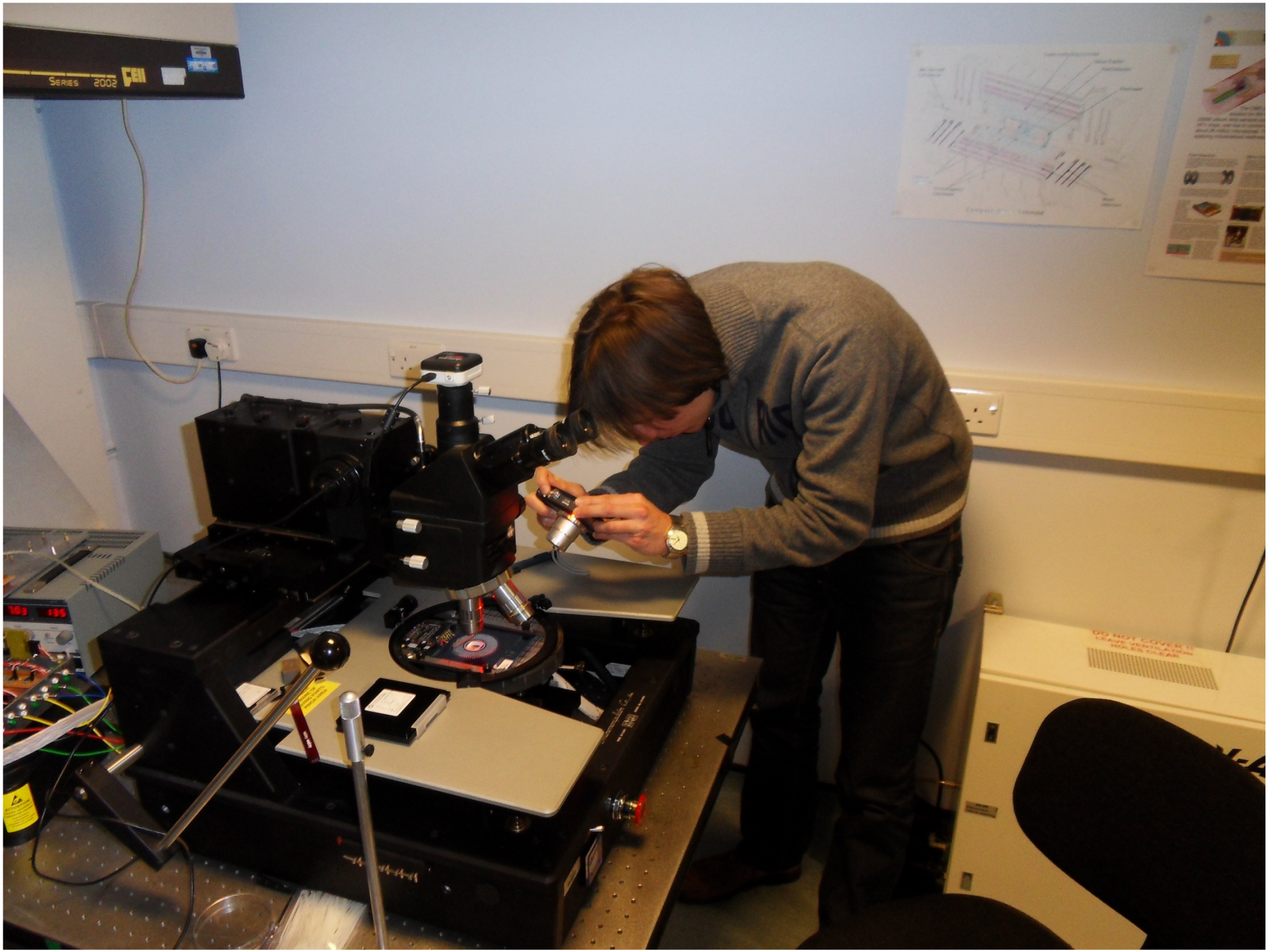
have to fire test pulse twice to get stubs loaded into shift reg

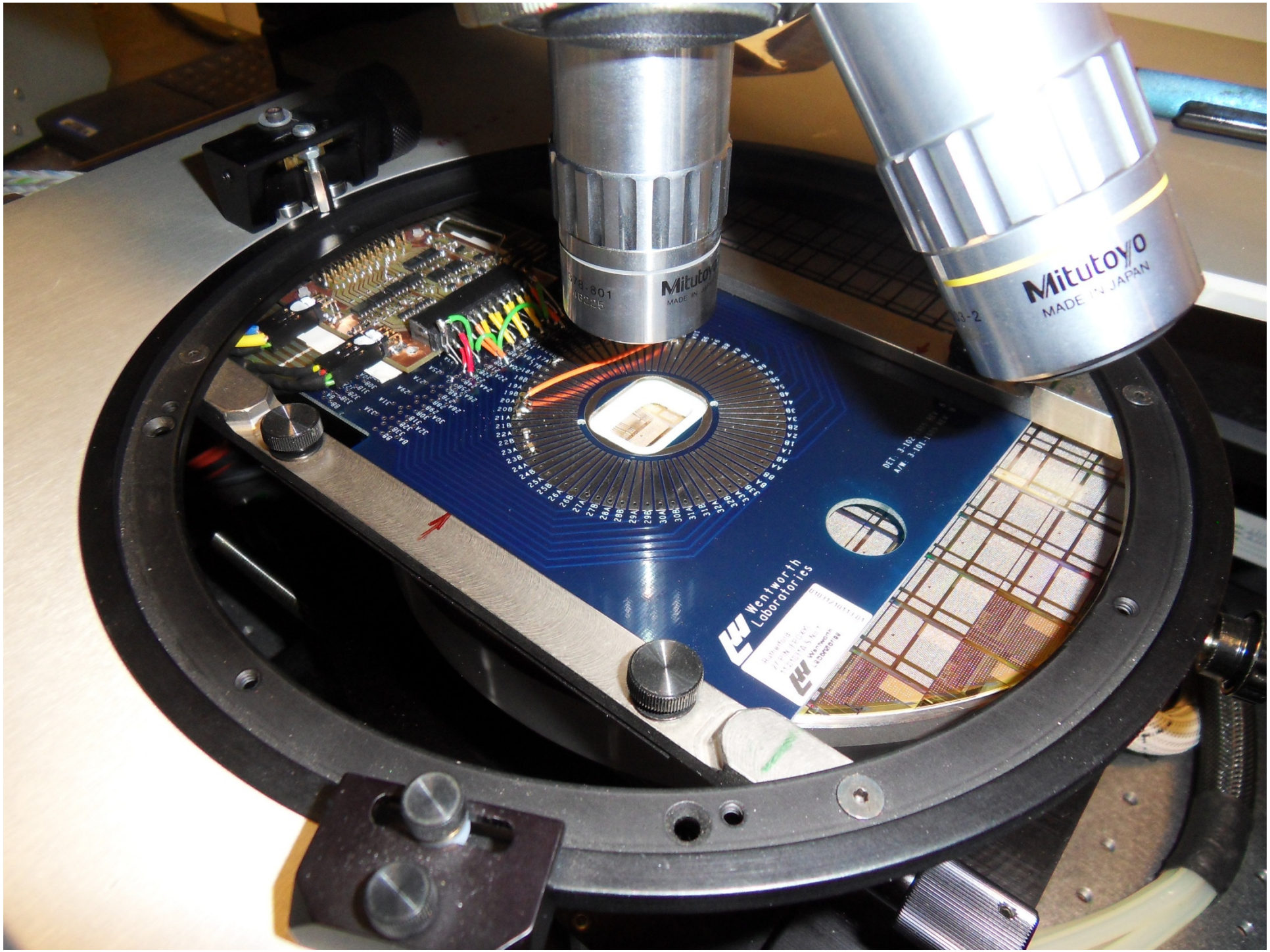
a pity, but this functionality only included as a test feature

C4 wafers



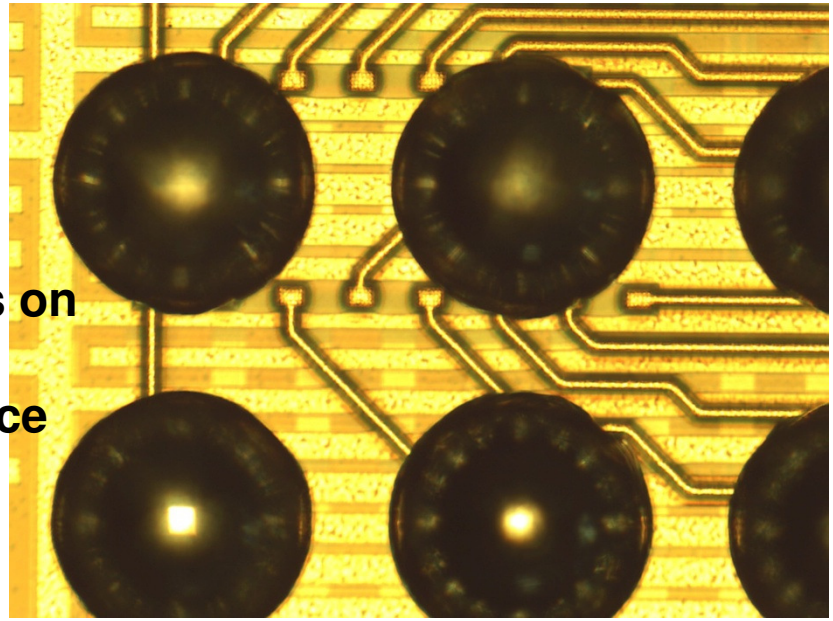

closer view of reticle
CBC2

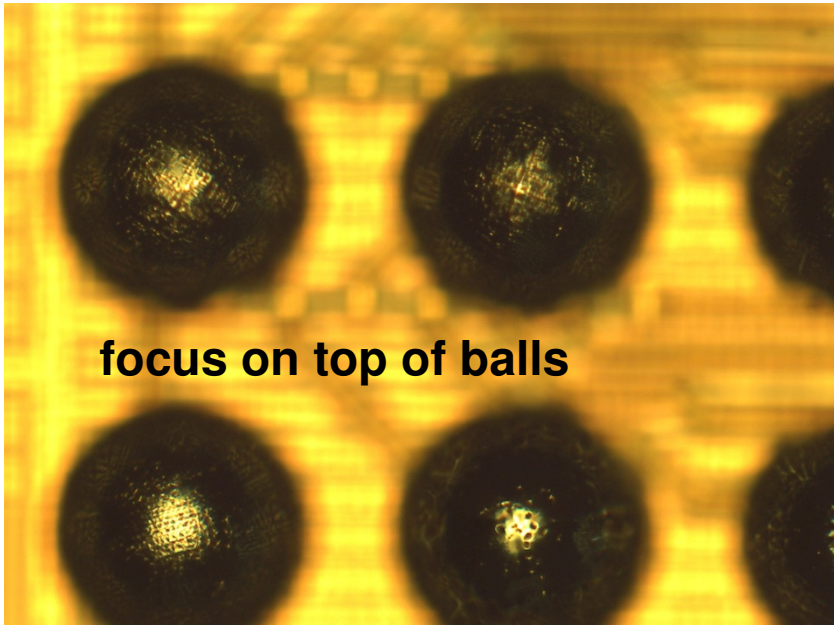

SERIES 2002
DO NOT COVER IT

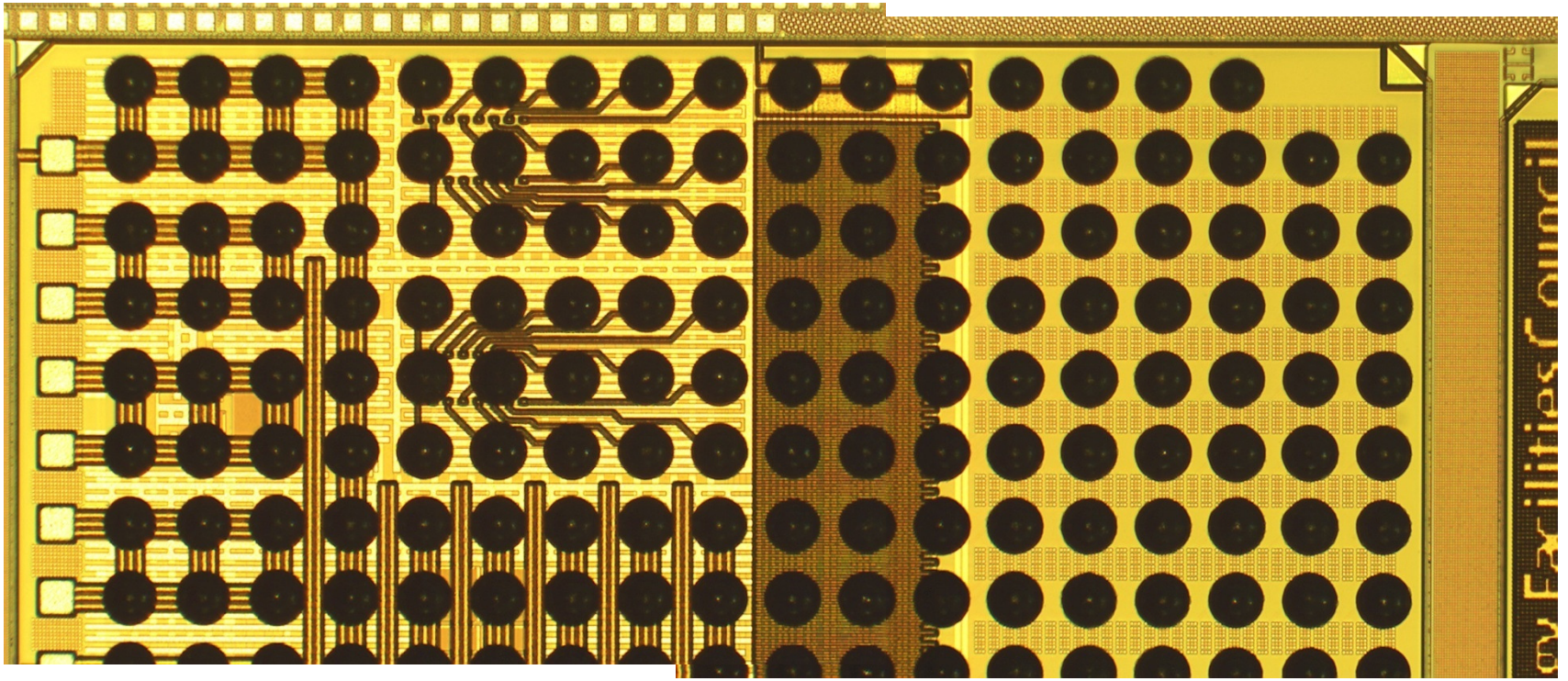

Mitutoyo
MADE IN JAPAN
Wentworth
Laboratories

balls

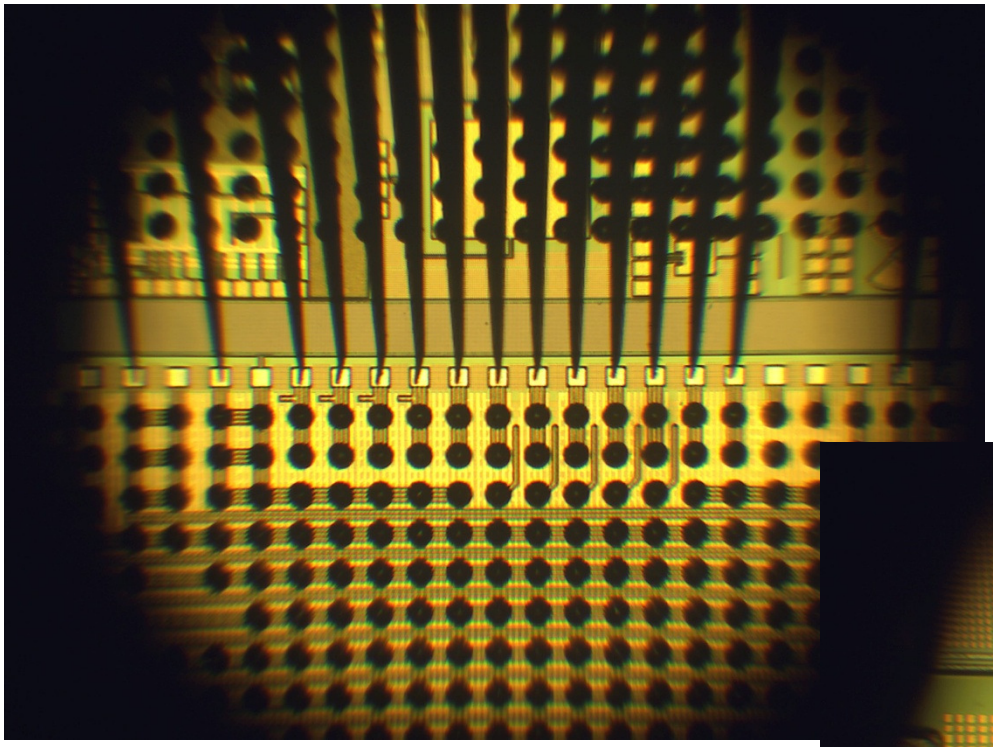
focus on chip surface





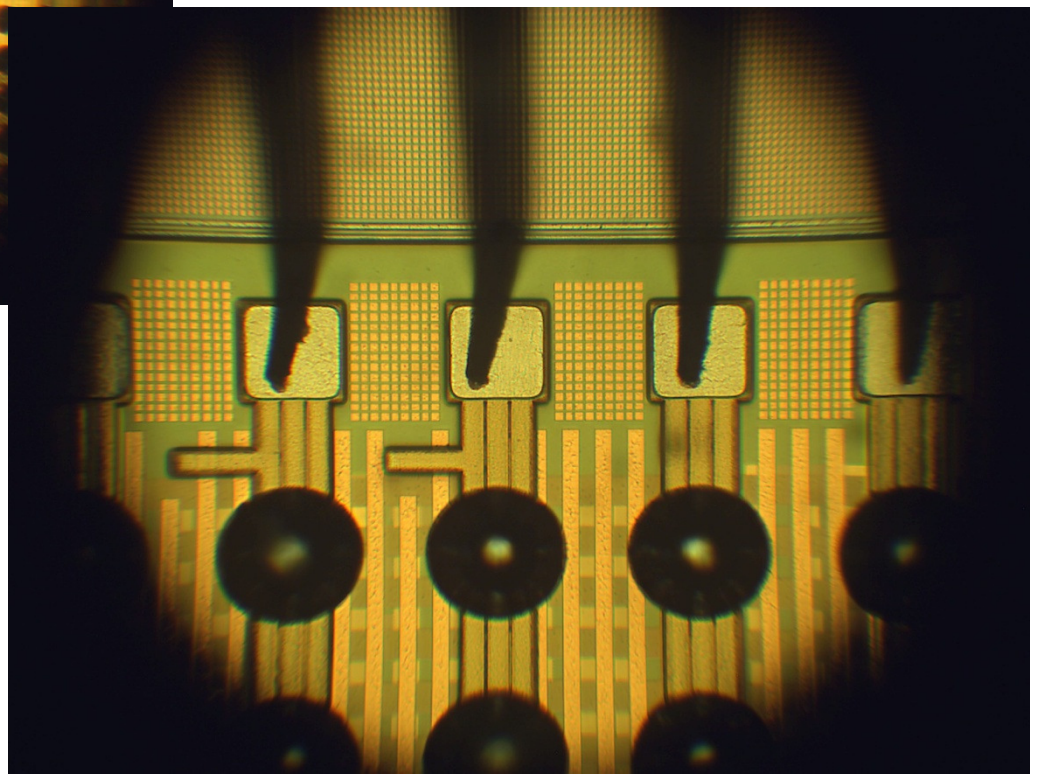


first wafer probed manually



probe station movements under manual control

took ~ 8 hours



bit laborious, but careful setup of automation would have taken longer

wafer test procedure

chip clocked at 40MHz
I2C parameters downloaded

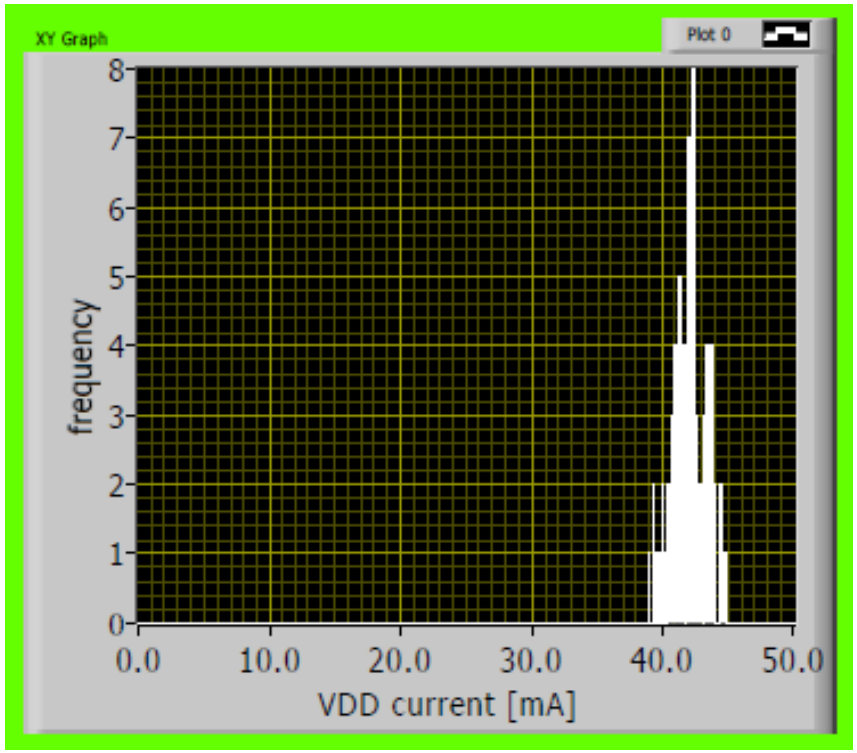
not an exhaustive test - but should be enough to differentiate bump-bond assembly problems from chip problems

power consumption recorded

power consumption dependence on I2C value for some bias currents swept

check all channels respond to test pulse

wafer test results - supply current



chip supplied by single 1.2V rail
LDO supplies 1.1 V for analogue

no significant supply current outliers visible in histogram

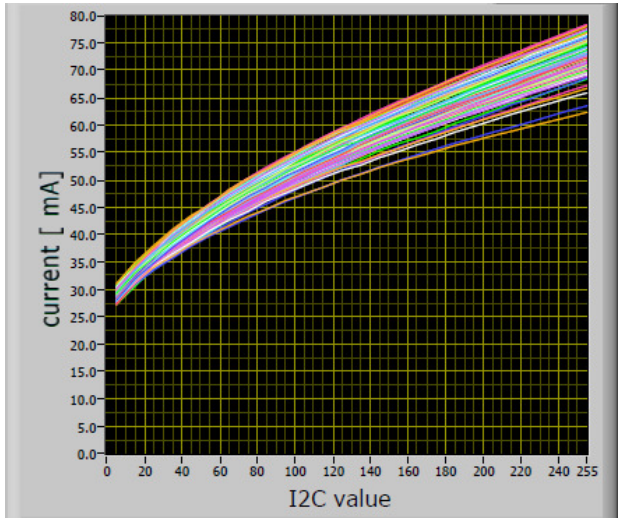
also no defective channel found on any of 112 chips tested on this first wafer

=> 100% yield

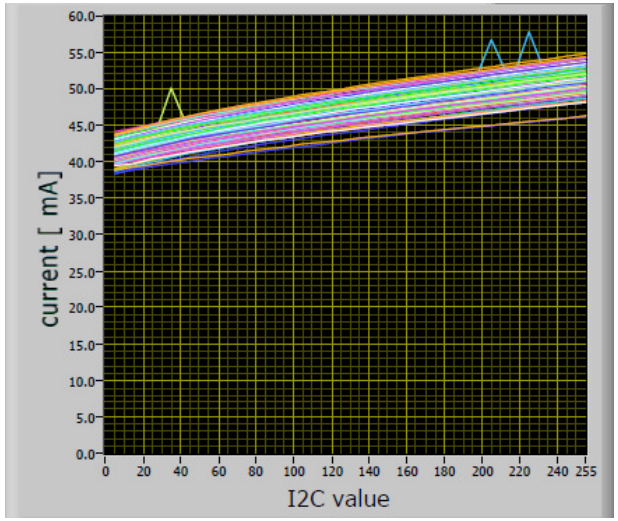
perhaps not too surprising if overall wafer yield high
CBC2 is relatively small area of reticle
& significant fraction of CBC2 area not occupied by active circuitry

wafer test results – bias current sweeps

IPRE1

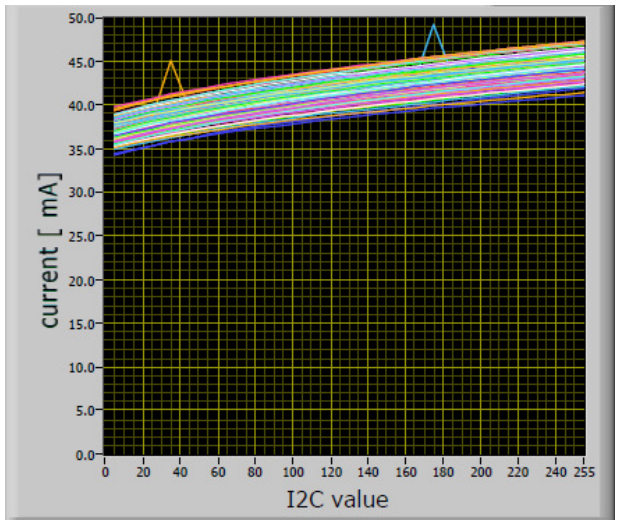


IPRE2

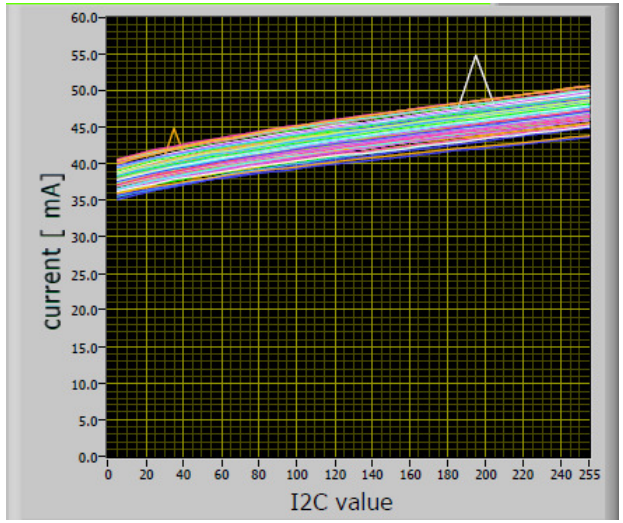


some I2C hiccups

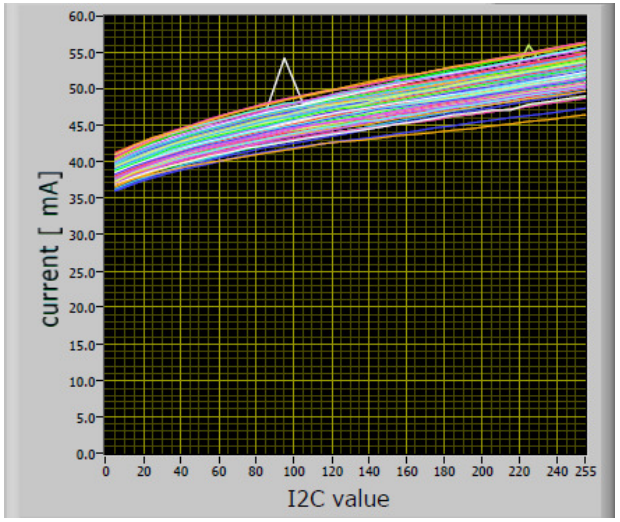
IPSF



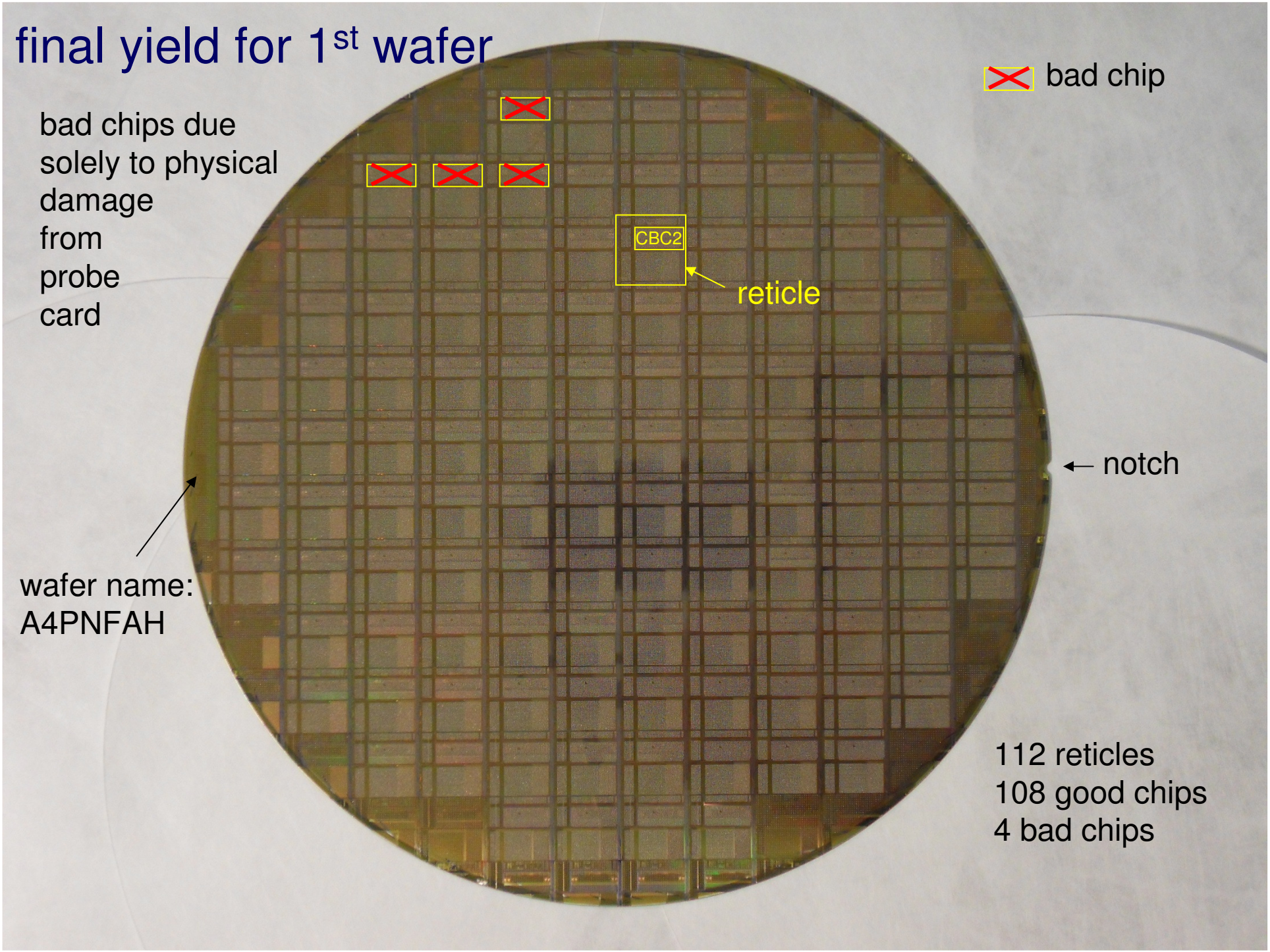
IPA



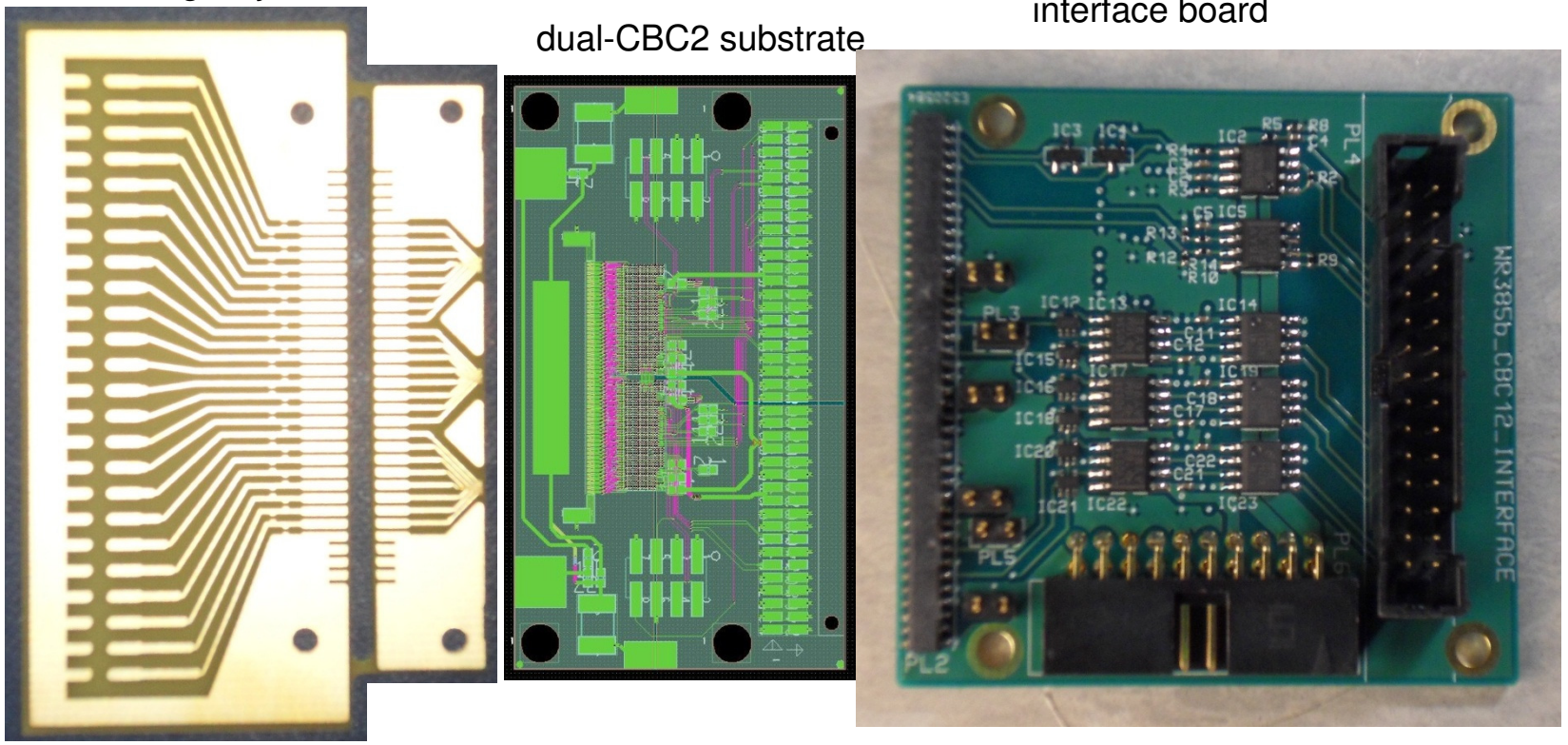
IPAOS

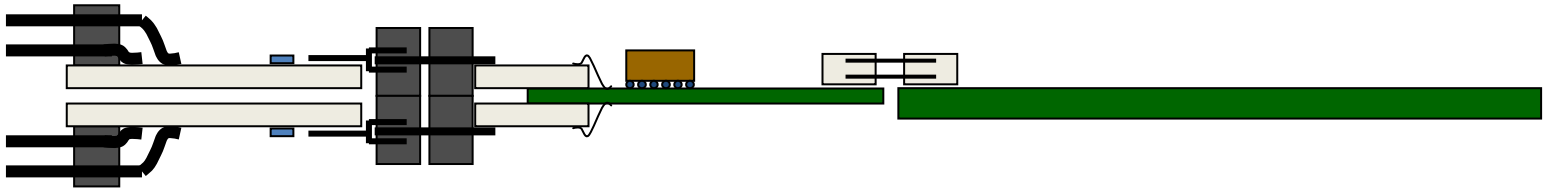


final yield for 1st wafer



dual-CBC2 substrate test setup





2xCBC substrate + PA (both sides) becomes device under test
pluggable charge inject board allows different external capacitance

summary & short term plans

CBC2 finally here

- early test results looks promising
  appears to be working well enough to allow progress with module development

1st March: 1st C4 wafer to cutting company (Novapack, France)

chips will come directly to CERN (Georges)

- company says early next week

further tests with wire-bond setup planned

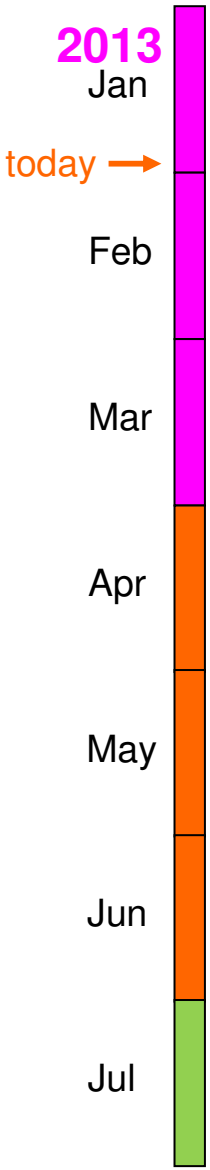
- can be more systematic and detailed now rush to get 1st wafer probed over

need to develop more thorough wafer probe test and automate

- then probe remaining 7 wafers
  - assuming yield remains high can expect > 800 chips total (all 8 wafers)

extra

timeline for next ~ 6 months



17th Jan - 6 wirebond wafers arrived RAL
sent promptly to cutting company
21st Jan - 8 C4 wafers arrived RAL

← 1st Feb - C4 wafers -> Imperial

← ~ week beginning 18th - wirebond CBC2 die available

← target end Feb to have 2 screened C4 wafers ready for cutting

← diced, tested C4 CBC2 chips available for 2xCBC2 substrate assembly

Endicott assembly period - ~ 8 weeks assumed?

← dual chip CBC2 substrates available for test

← target end May to have remaining C4 wafers tested ready for cutting

← target end June to have diced, tested C4 CBC2 chips available for 8xCBC2 substrate

comments

wafer cutting seems to take ~ 3 wks

would prefer to do 1st tests on wire-bonded chips

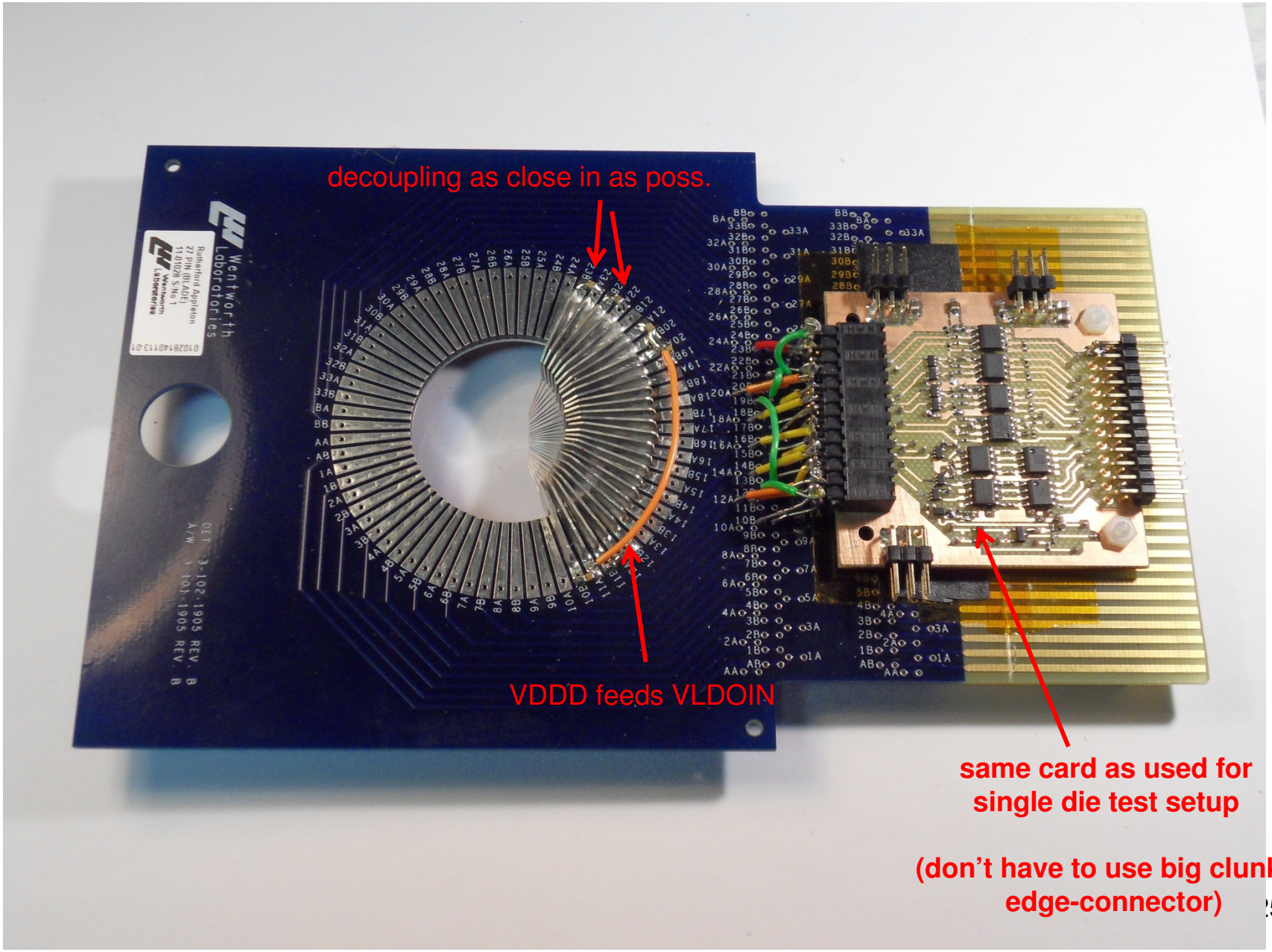
much easier to debug test interfaces and procedures

=> a bit more schedule slippage

learn as much as poss. from wire-bond CBC2 test setup

switch to 2xCBC2 substrate tests

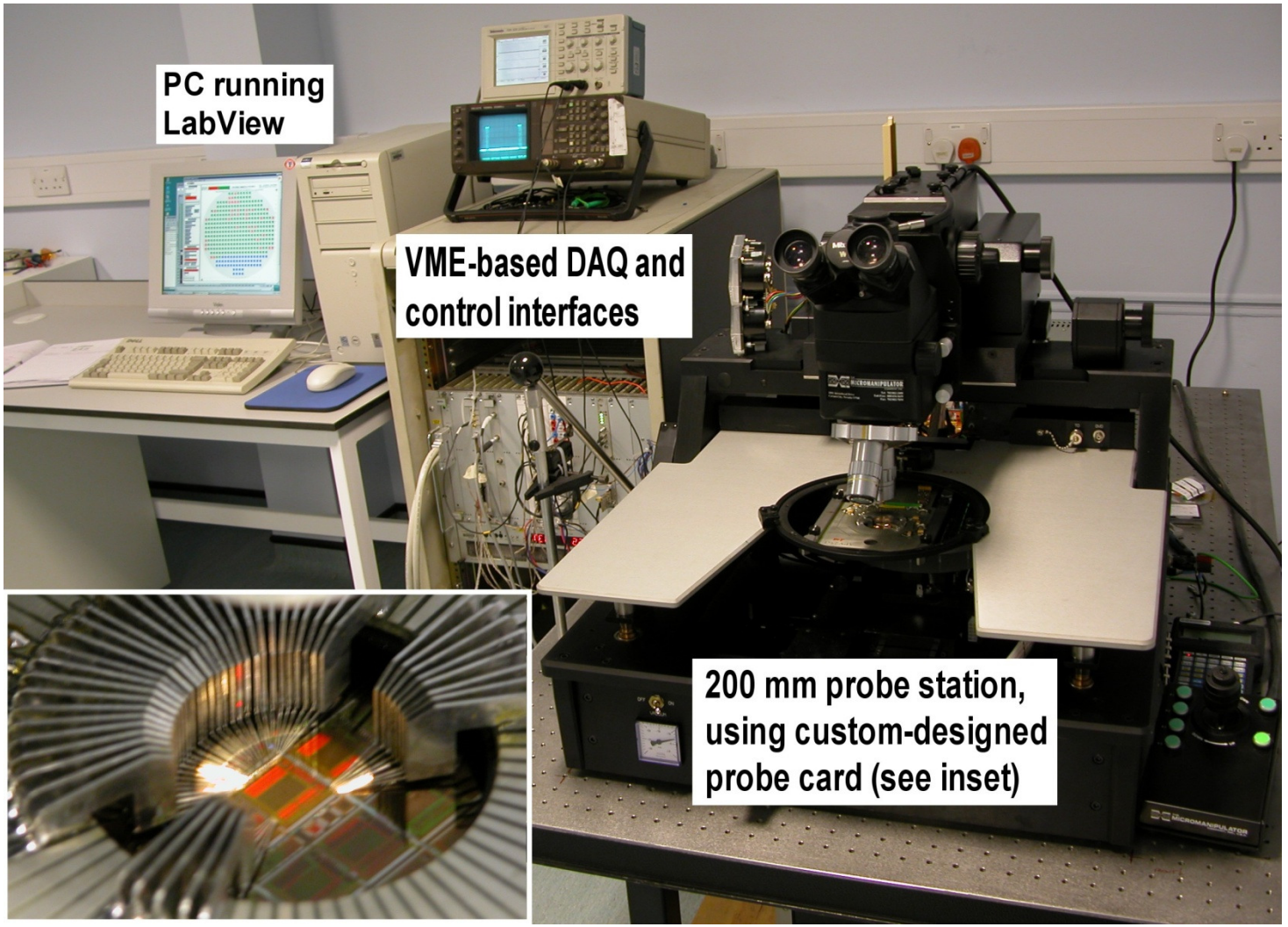
blade probe card for CBC2



Wafer Test Probe Station

will re-use some of APV probe-card interface hardware

ancient PC now replaced and probe-station controlling software checked ok

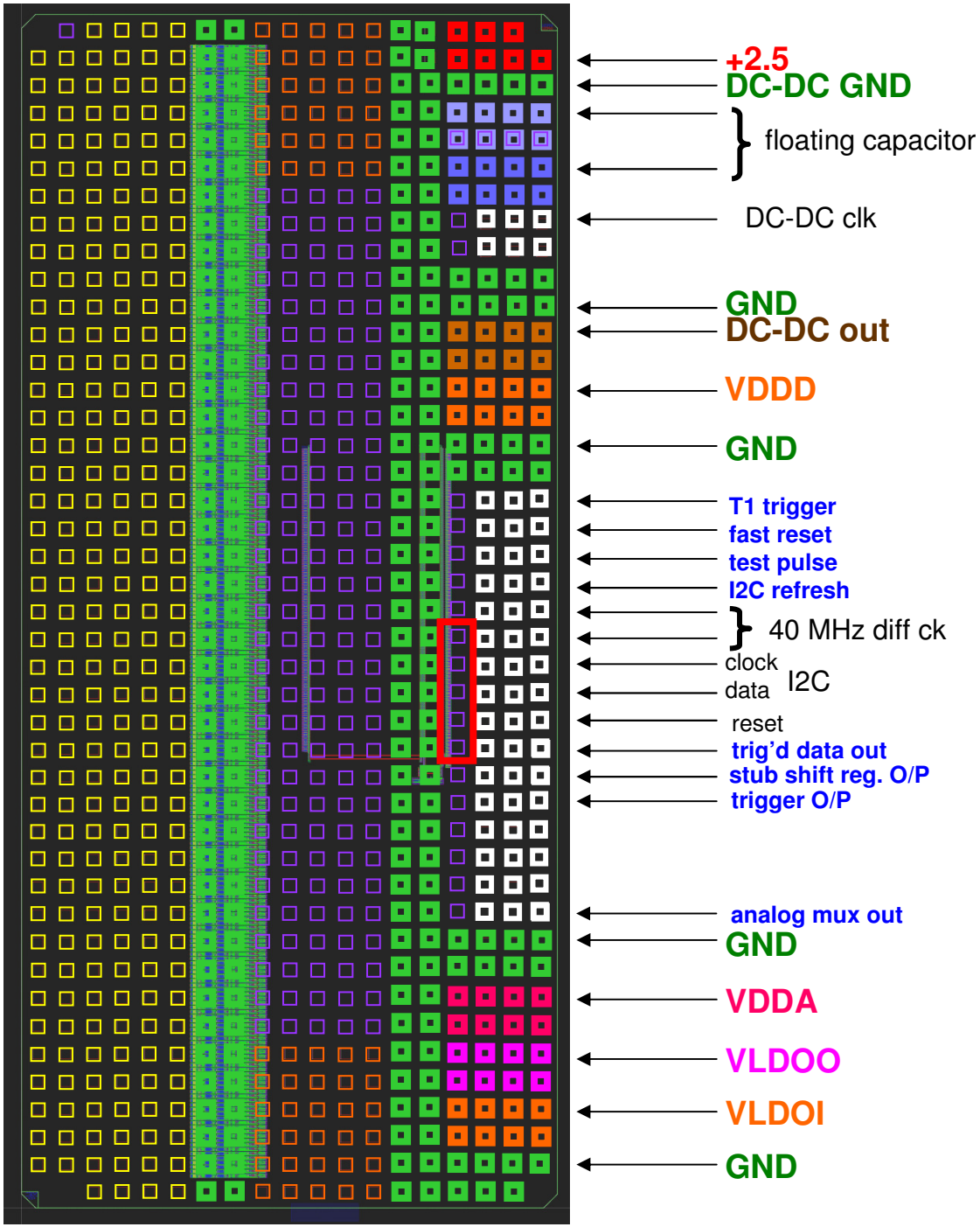


Micromanipulator
8 inch semi–automatic
probe station

VME based
- ADC (8 bits)
- RAL SeqSi
  - 40 MHz CK/T1
- CERN VI2C I/F

PC controls both
DAQ (VME)
& probe-station (RS232)

probe card signals

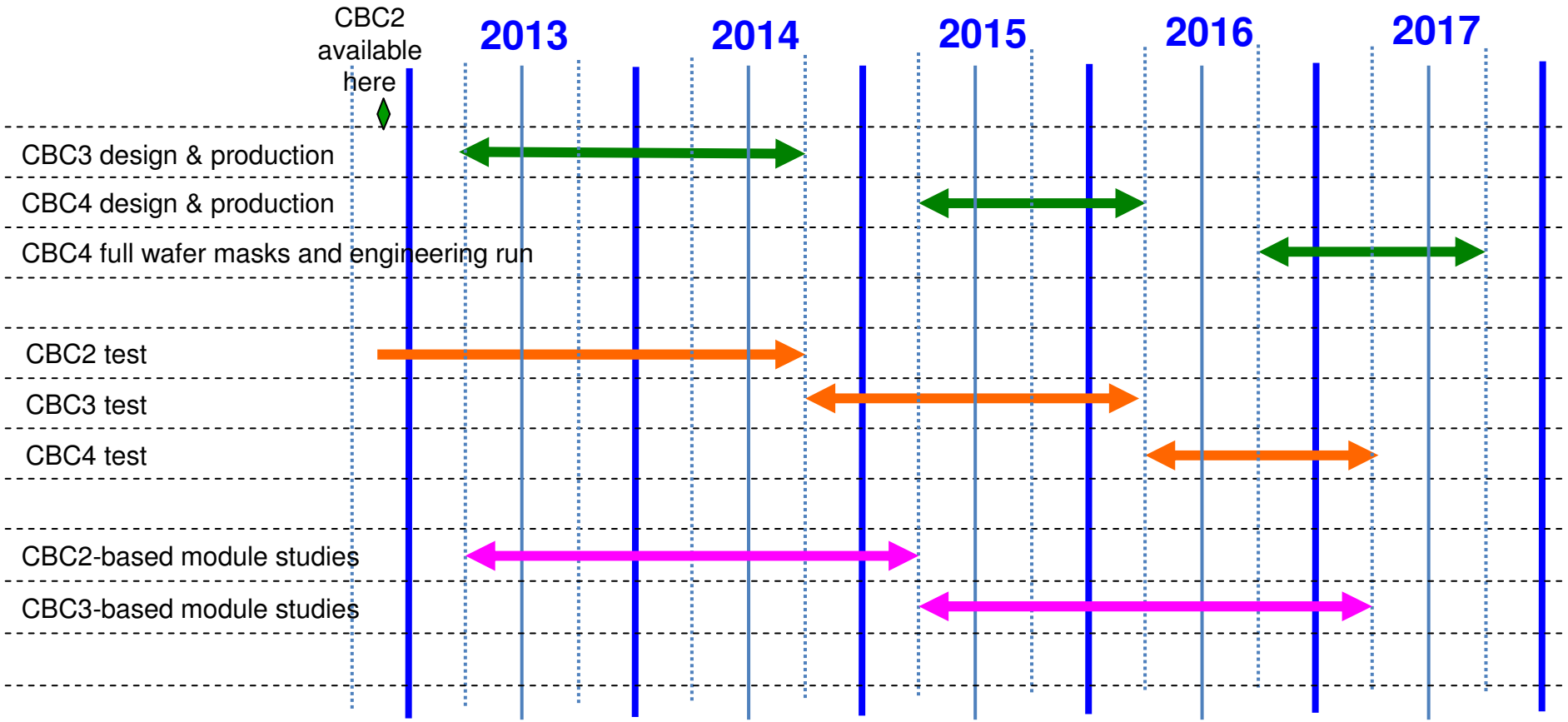


27 altogether

160 MHz signals left out

can try and use DC-DC and LDO
but unlikely to work well
necessary associated capacitors
a long way away from pads

UK Phase II programme



CBC3 should be very close to final chip – available late 2014
- incorporate architecture to transmit stub addresses
- slow ADC for on-chip monitoring
- …

CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017