

CBC2 hybrid & module testing

- update on 2xCBC2 hybrid interface card
- 2xCBC2 hybrid electrical test setup early results
- mini-pT module (Infineon sensors) early results

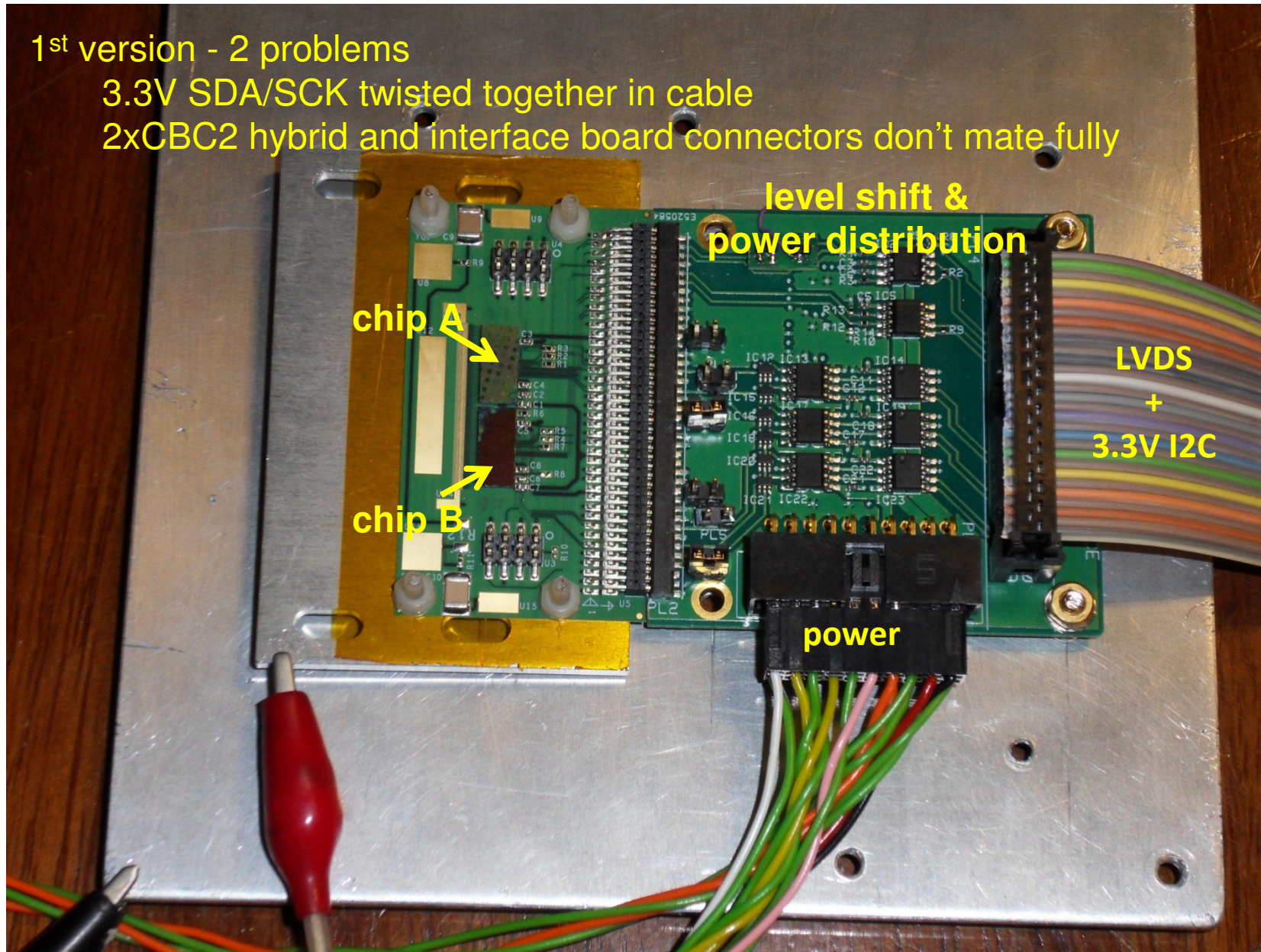
CMS Tk phase II electronics meeting – June 18th, 2013

2xCBC2 hybrid interface card

1st version - 2 problems

3.3V SDA/SCK twisted together in cable

2xCBC2 hybrid and interface board connectors don't mate fully



level shift &
power distribution

chip A

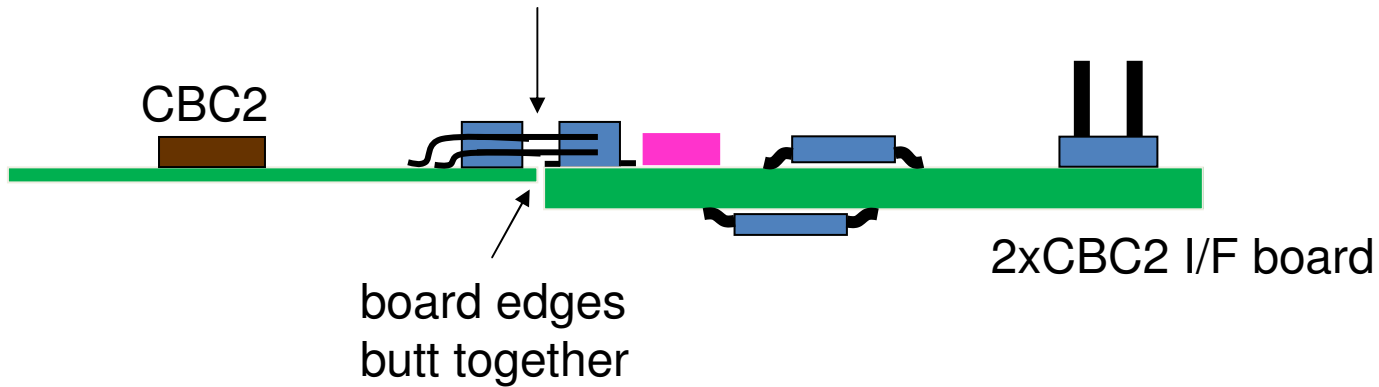
chip B

LVDS
+
3.3V I2C

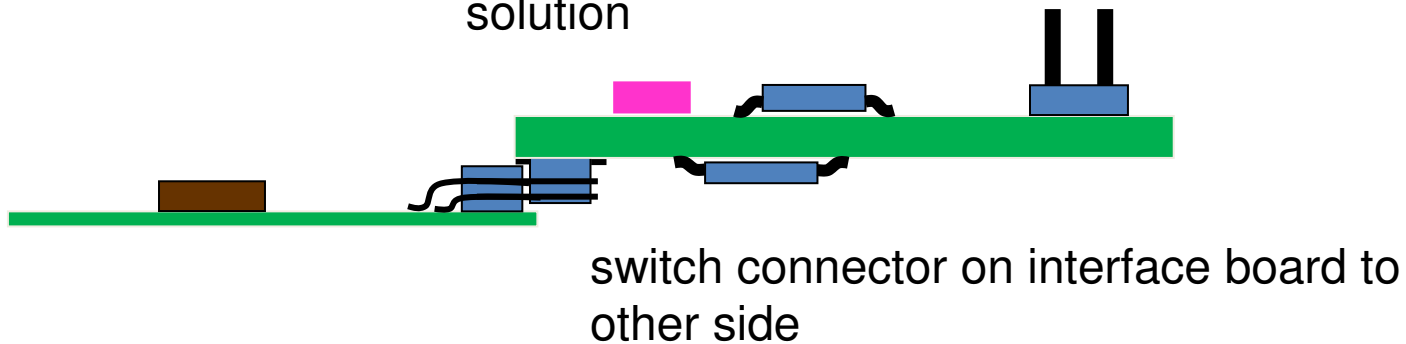
power

2xCBC2 hybrid interface card 1st version problems

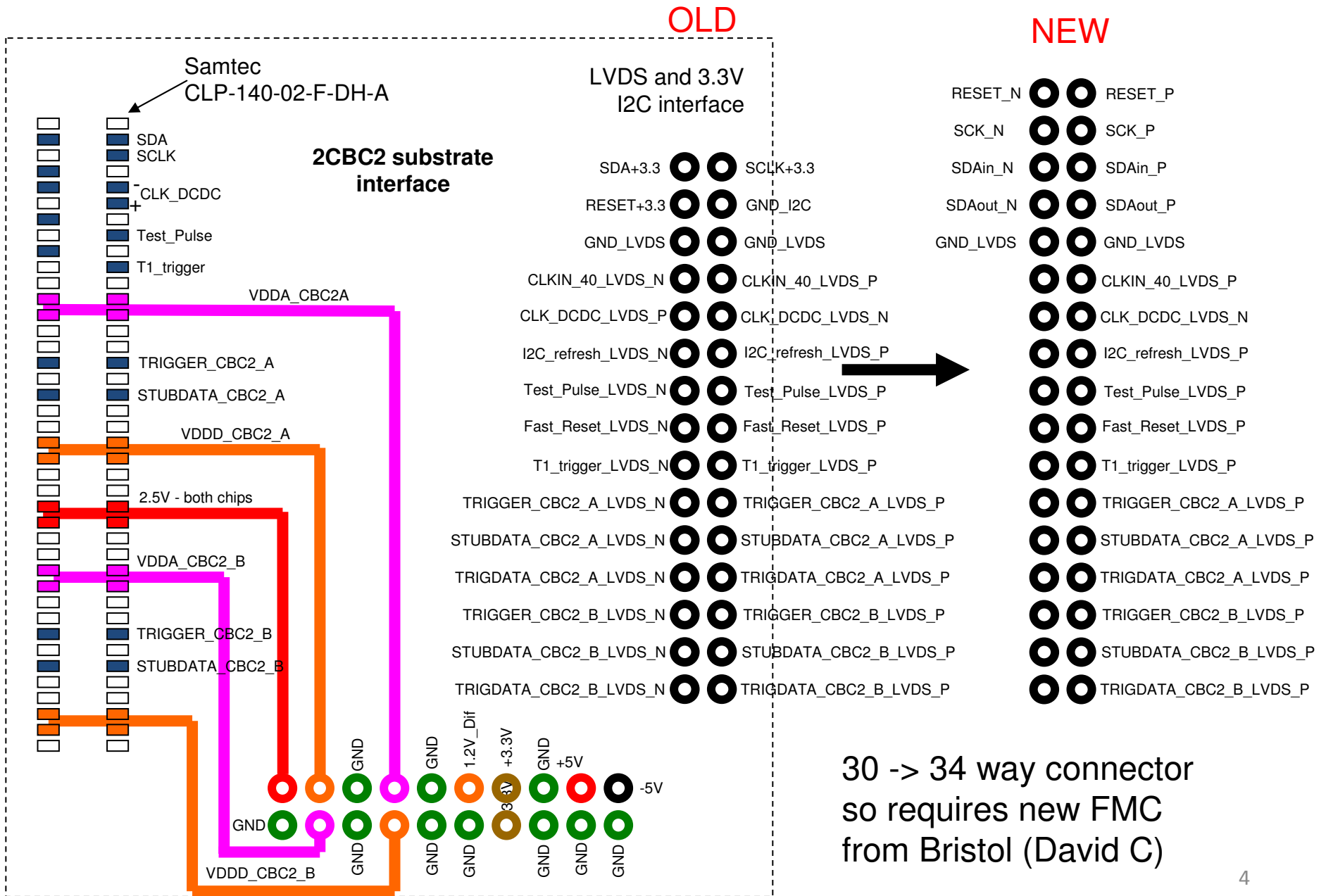
problem is here
connectors don't fully mate
(even if file down edge of board)



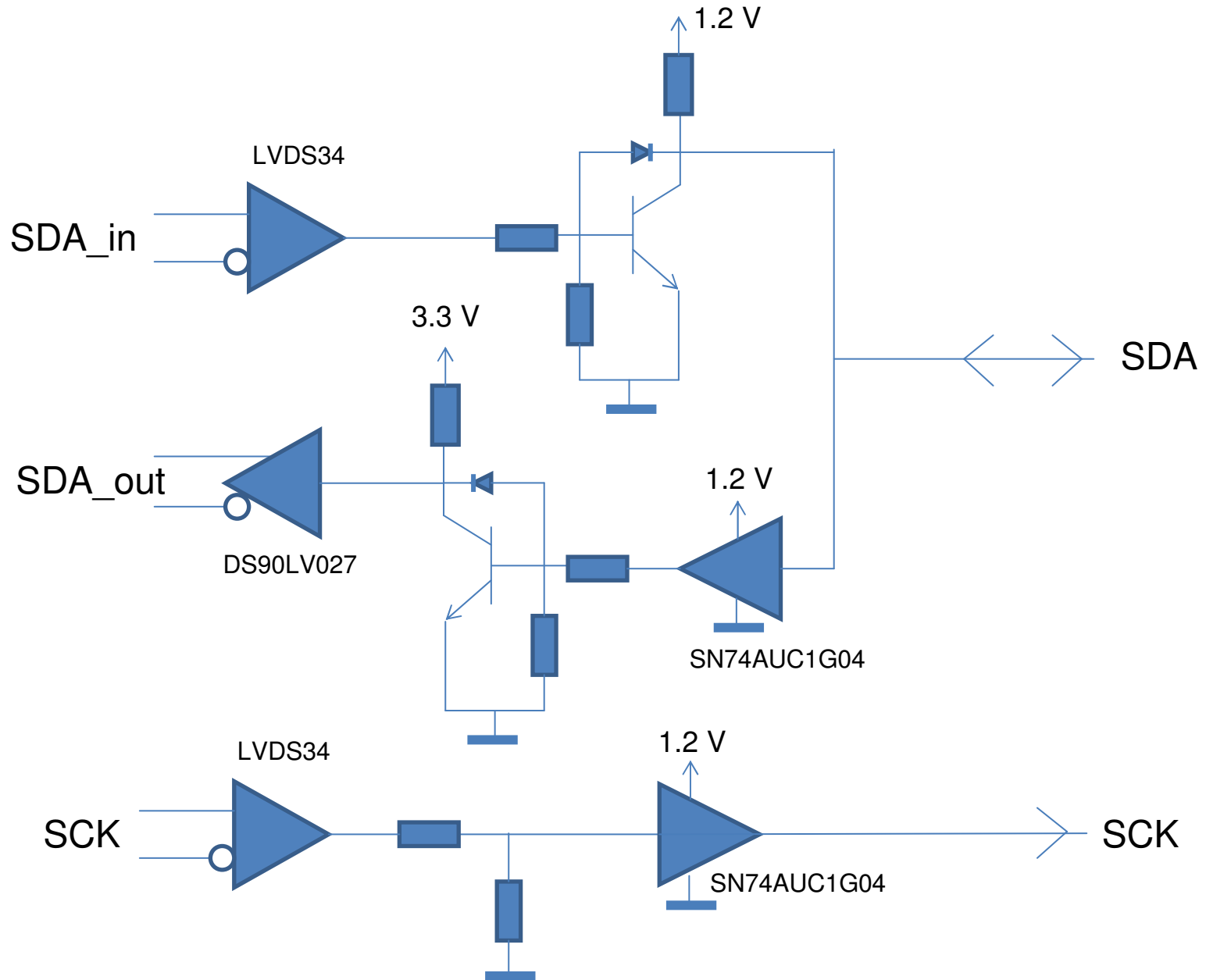
solution

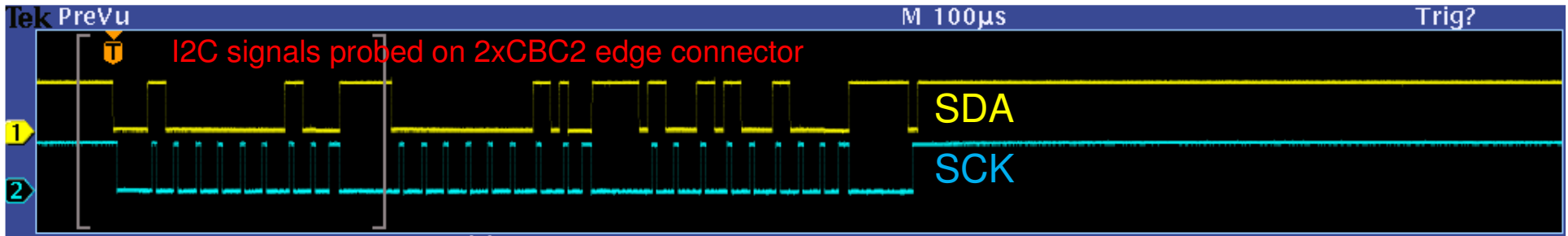


all interface signals now LVDS

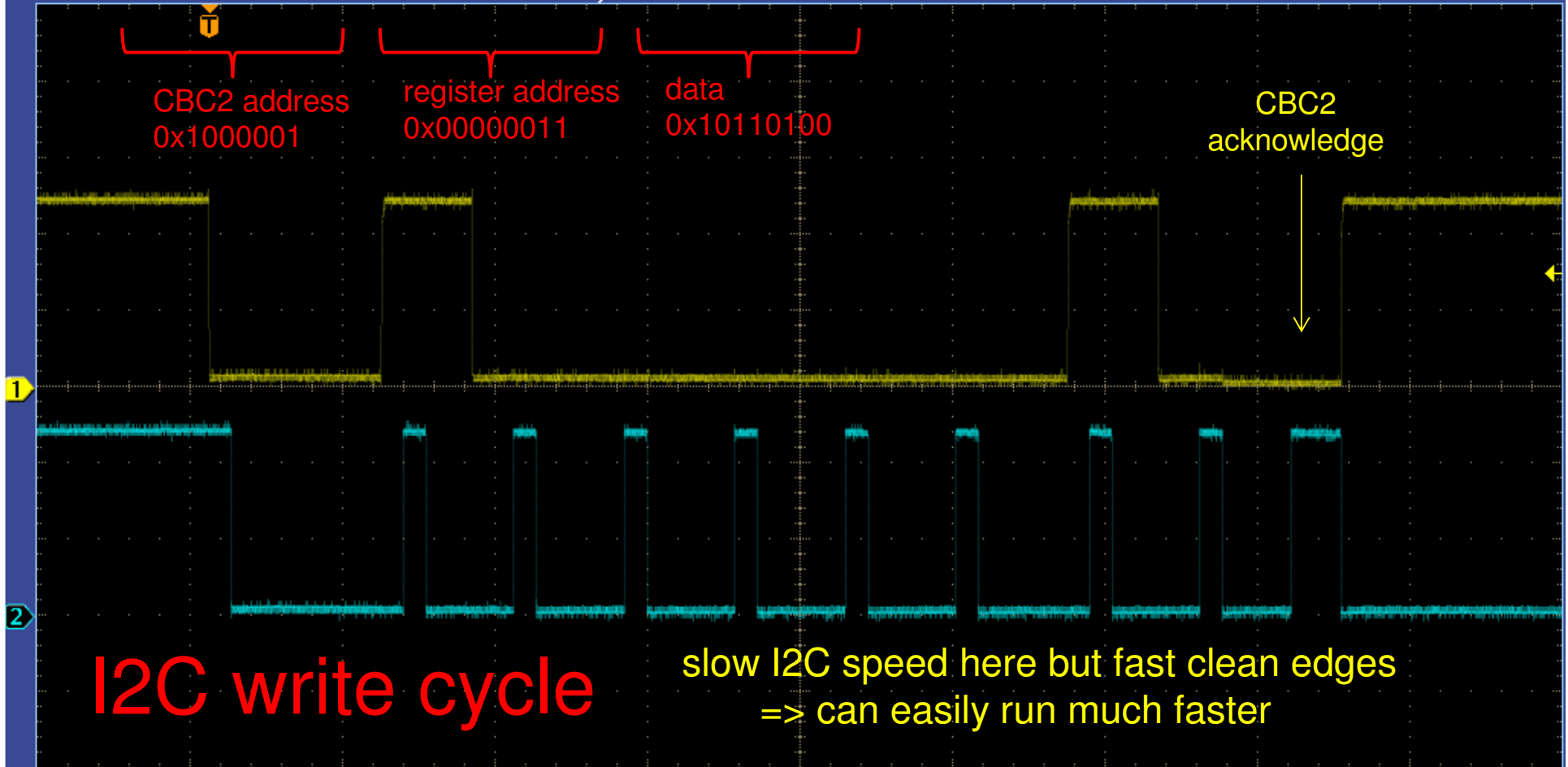


new I2C interface on 2xCBC2 interface card

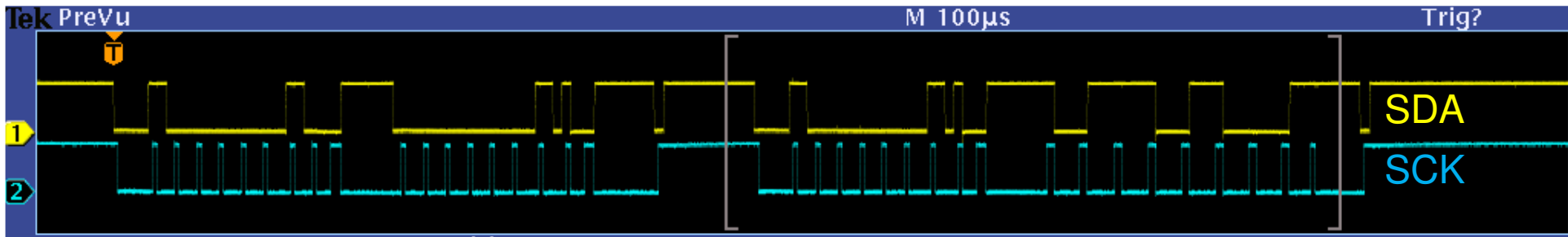




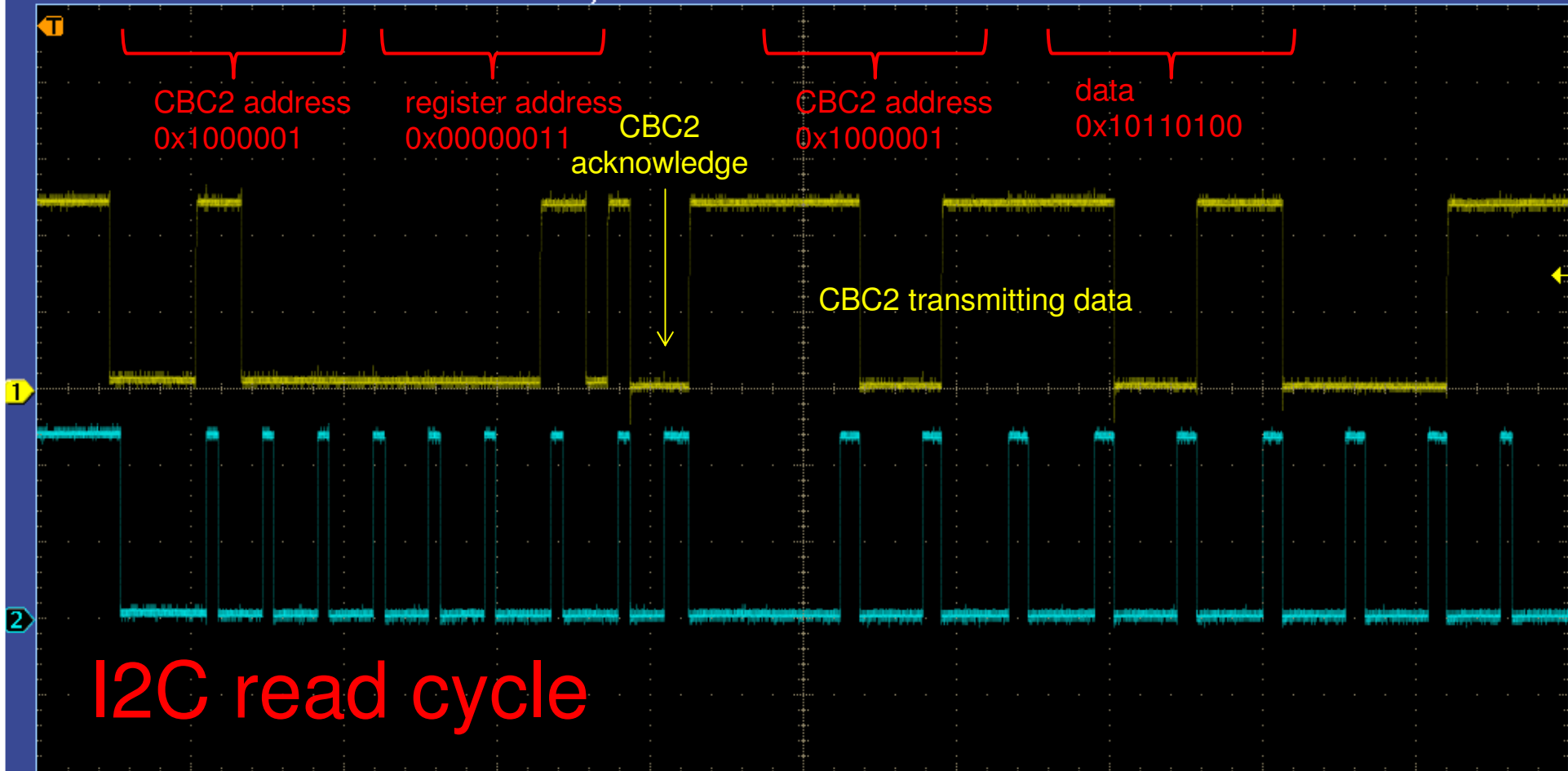
Zoom Factor: 5 X Zoom Position: 77.4µs



1 500mV 2 500mV Z 20.0µs 100MS/s 100k points 1 760mV



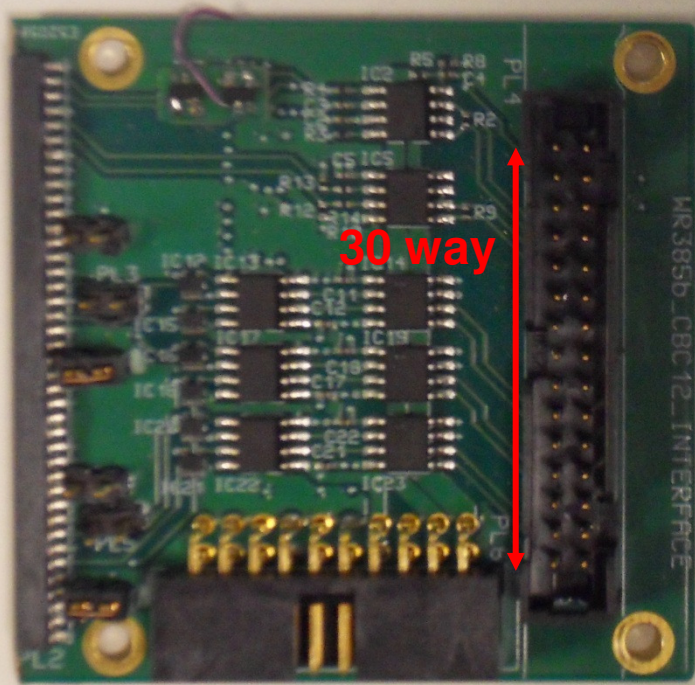
Zoom Factor: 2.5 X Zoom Position: 600µs



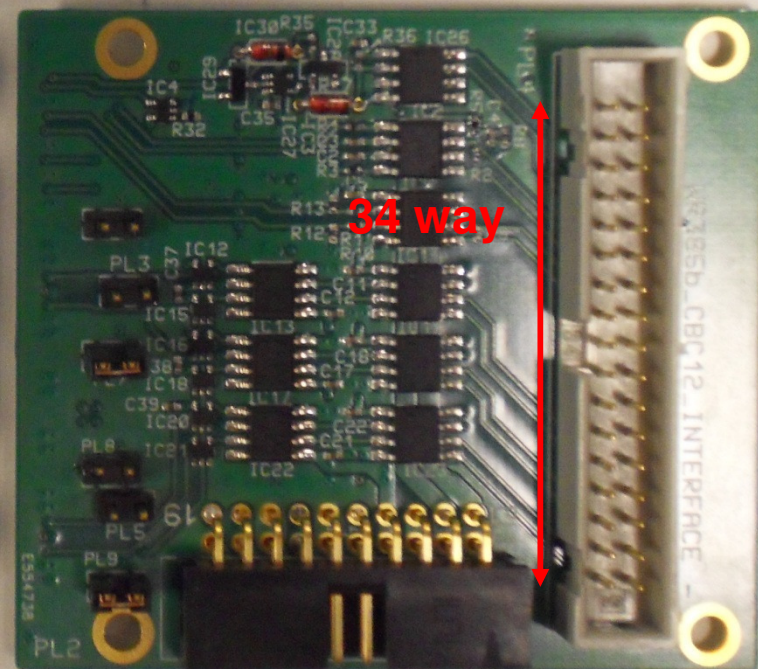
1 500mV 2 500mV Z 40.0µs 100MS/s 1 760mV

5.000 % 100k points

old



new



2xCBC2 hybrid interface card summary

current status

should stop using 1st version 2xCBC2 interface cards

only one outside IC

Bristol (David C) has complete 2xCBC2 hybrid/old interface card system
to verify 1st FMC <-> GLIB system

3 new cards so far populated, more on the way
up to 30 possible

1 for mini-pT module

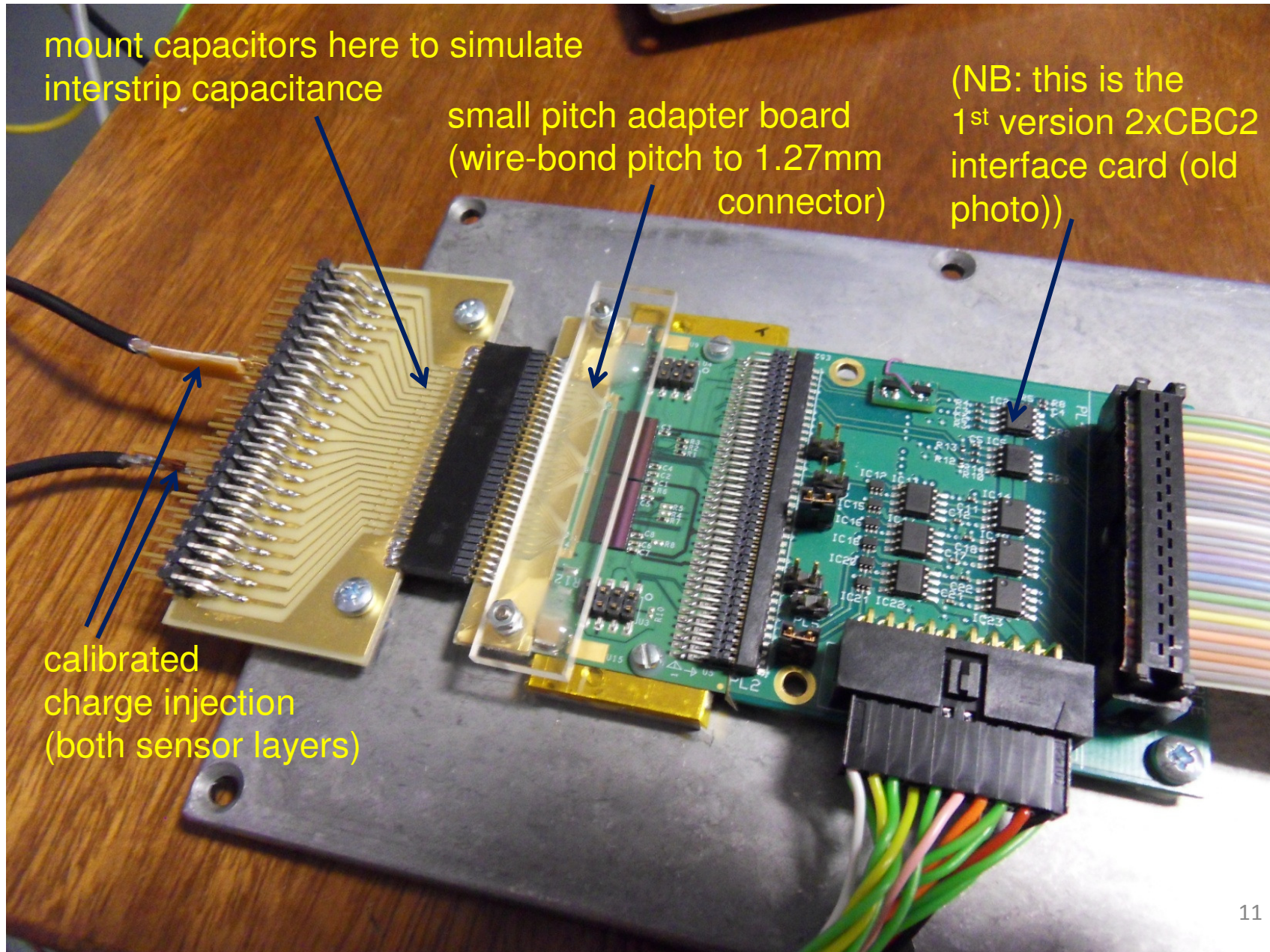
1 for 2xCBC2 electrical test setup

propose to pass 1 to Bristol to verify functionality with 2nd FMC version (available soon)

should develop plans for distributing 2xCBC2/interface card/FMC systems
can we verify full chain functionality before handing over?

2xCBC2 electrical test setup

2xCBC2 electrical test setup



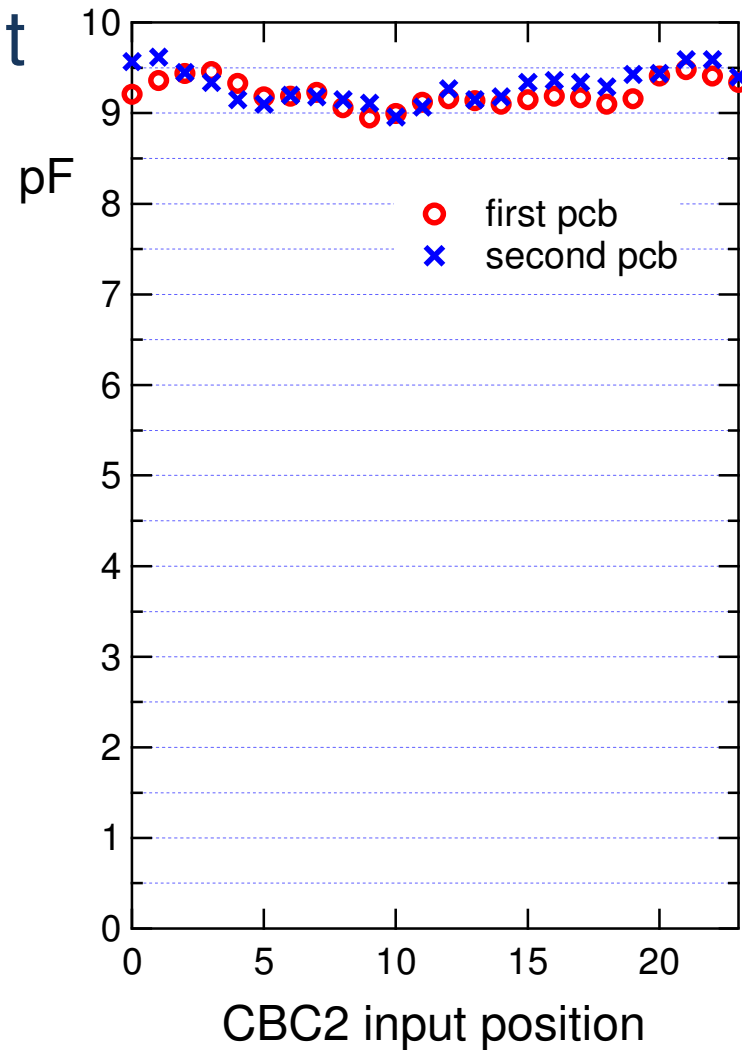
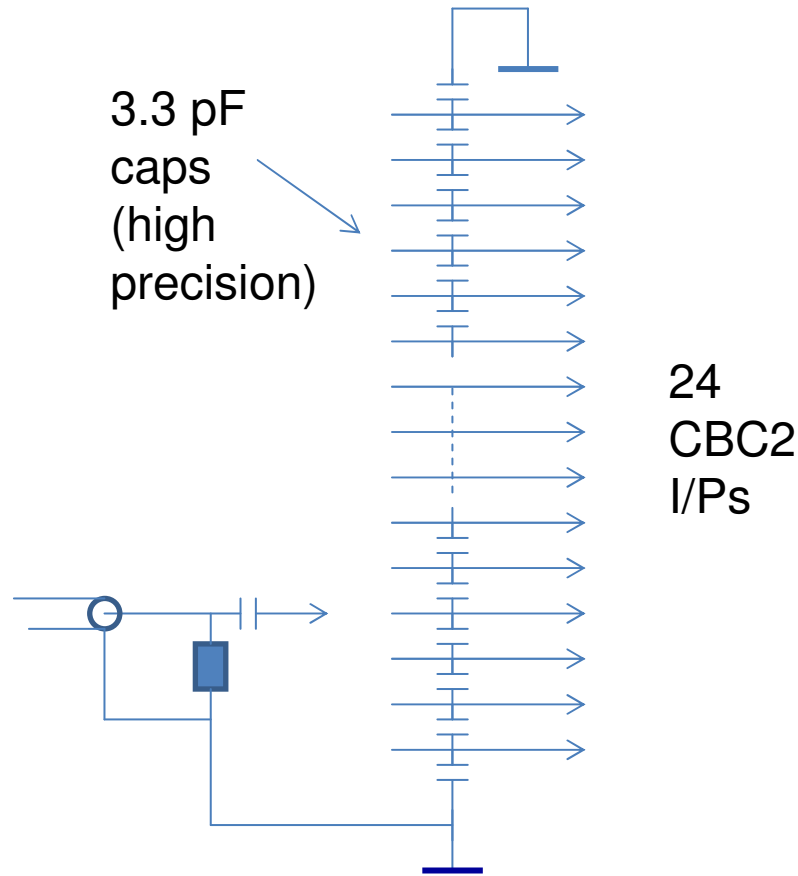
mount capacitors here to simulate interstrip capacitance

small pitch adapter board (wire-bond pitch to 1.27mm connector)

(NB: this is the 1st version 2xCBC2 interface card (old photo))

calibrated charge injection (both sensor layers)

inter-channel cap. measurement



capacitance measured between centre position to 4 nearest neighbours both sides

quite uniform ~ 9.25 pF

(but doesn't include stray capacitance on small pitch adapter board or 2xCBC2 hybrid)

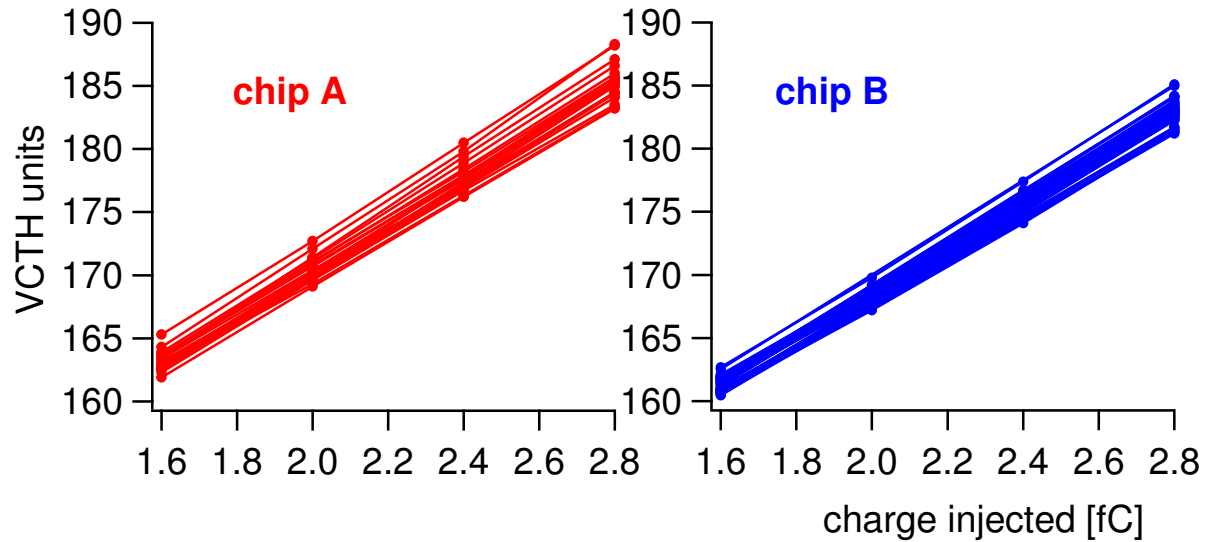
(other boards with different capacitors envisaged, but measurements only with this one at the moment)

gain measurements

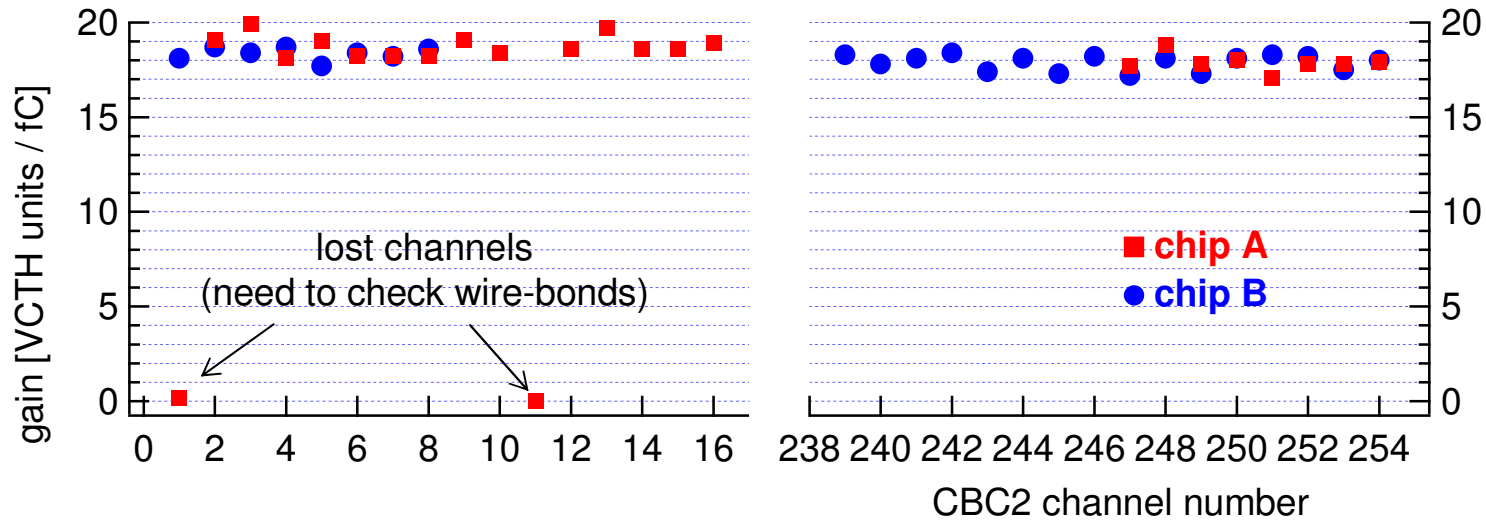
can now measure gain using known input signal

plot s-curve mid-points vs. charge

linear fit gives gain in comparator threshold units / fC



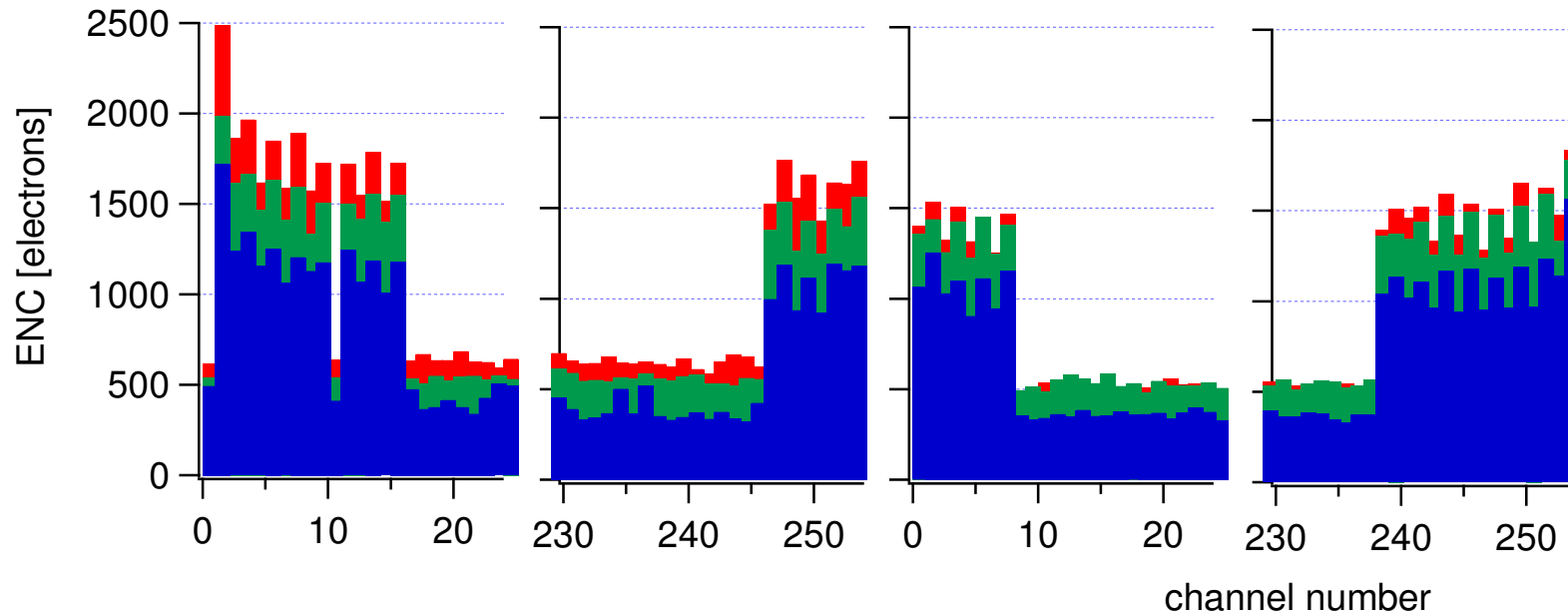
gain uniformity



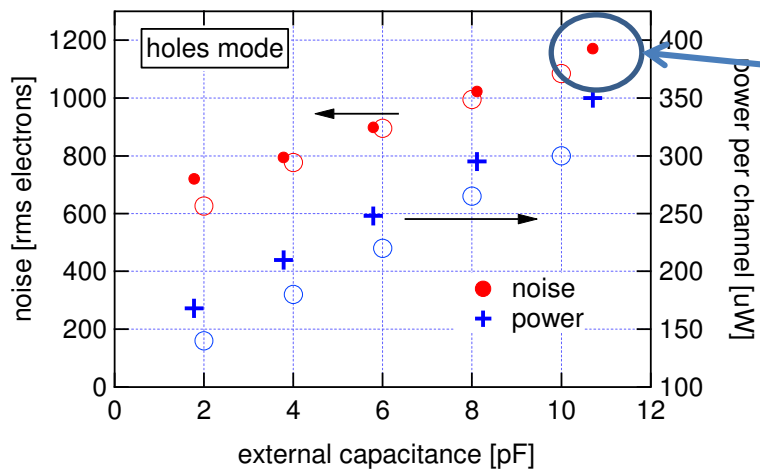
chip	min value	average	max value
A	17.1	18.4	19.9
B	17.2	18.0	18.7

+/- ~ 10% pk-pk spread

noise measurements



CBC1 result



noise measured from s-curves acquired using different test-pulse amplitudes in the right region for measured capacitance

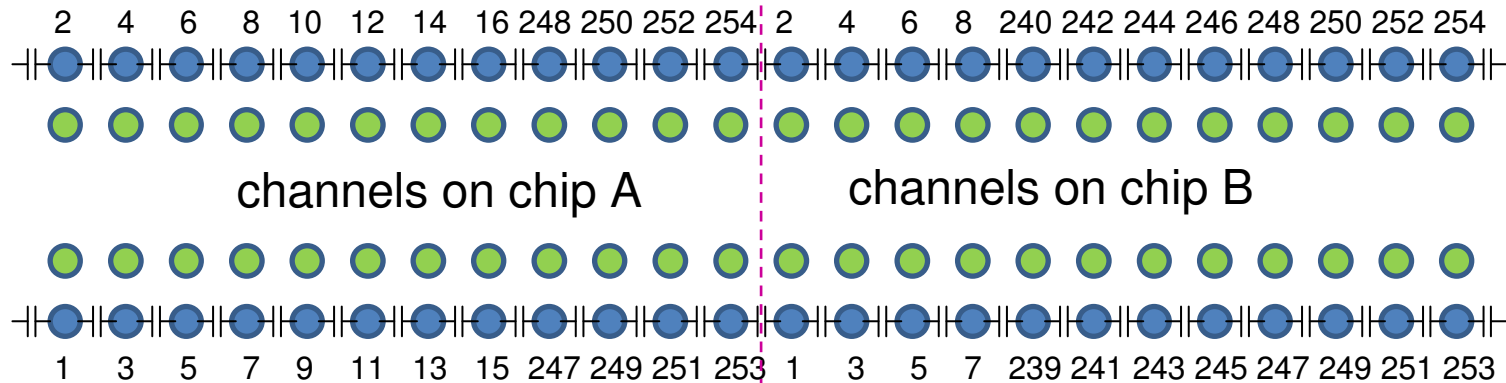
noise higher for larger TP amplitudes needs understanding - appears worse for chip A (probably test pulse generation related?)

systematic difference between upper and lower channels upper channels higher noise

some edge effects visible, but not at chip boundaries

crosstalk measurements

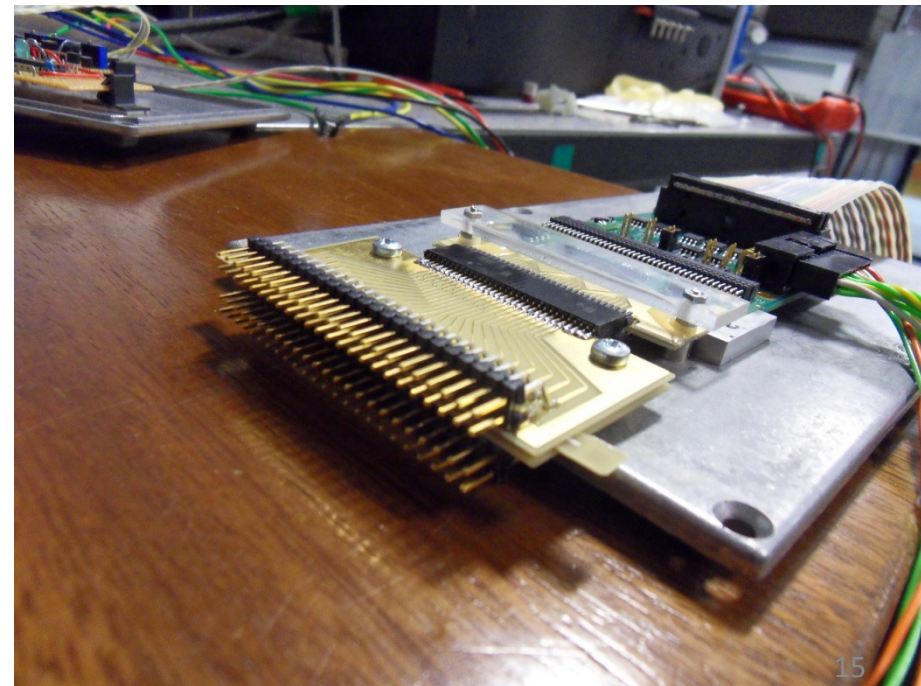
arrangement of channels on charge injection connectors



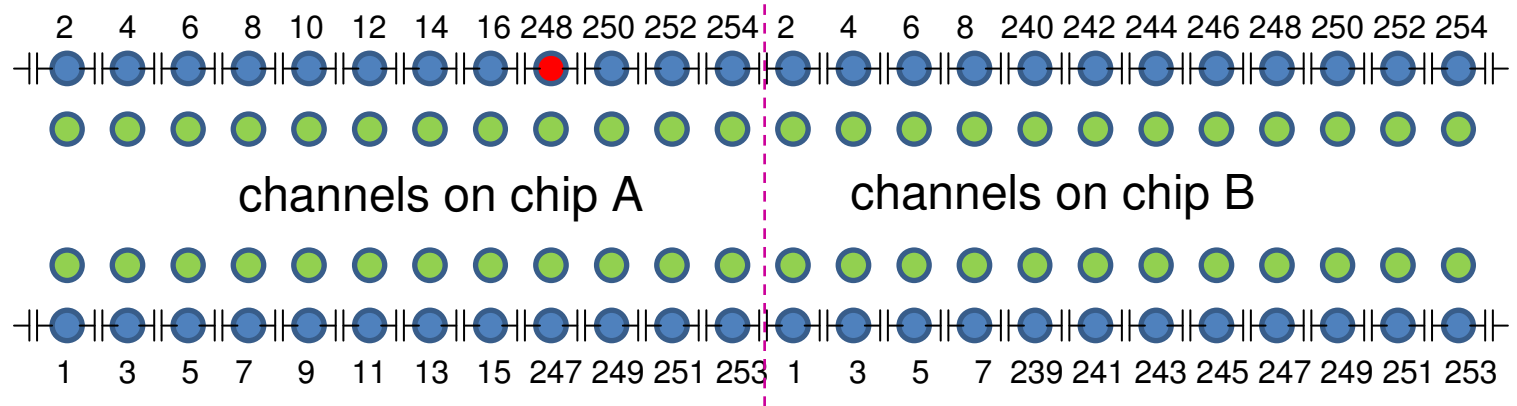
2 possibilities

crosstalk on chip
e.g. channel 7 talks to 6 and 8

crosstalk dominated by interchip C
channel 7 talks to 5 and 9



results(1)

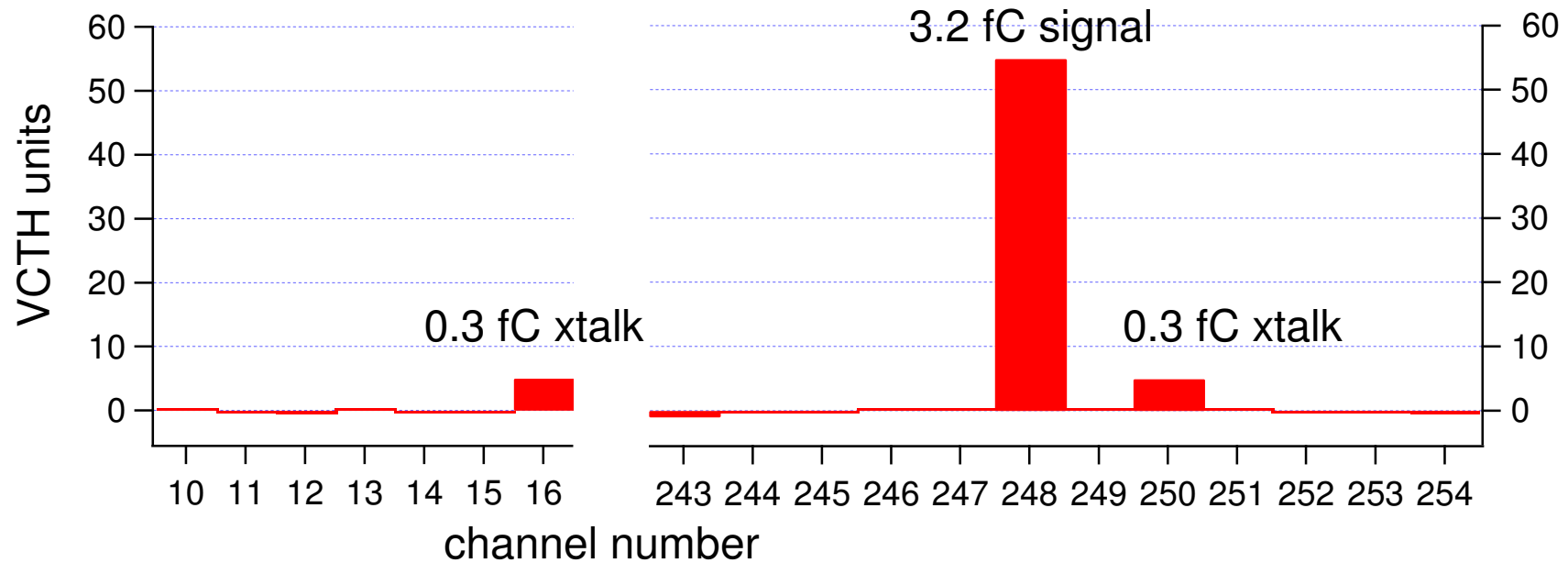


method

inject charge on chosen channel (e.g. chipA/chan248)

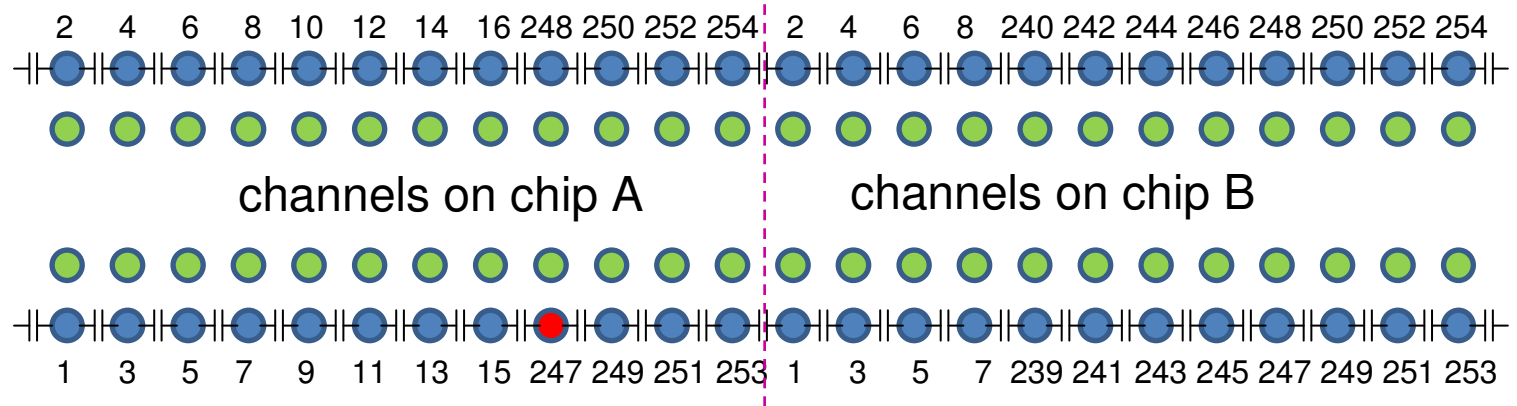
acquire s-curve and find mid-point

remove signal, re-acquire s-curve (mid-point = pedestal), subtract pedestal

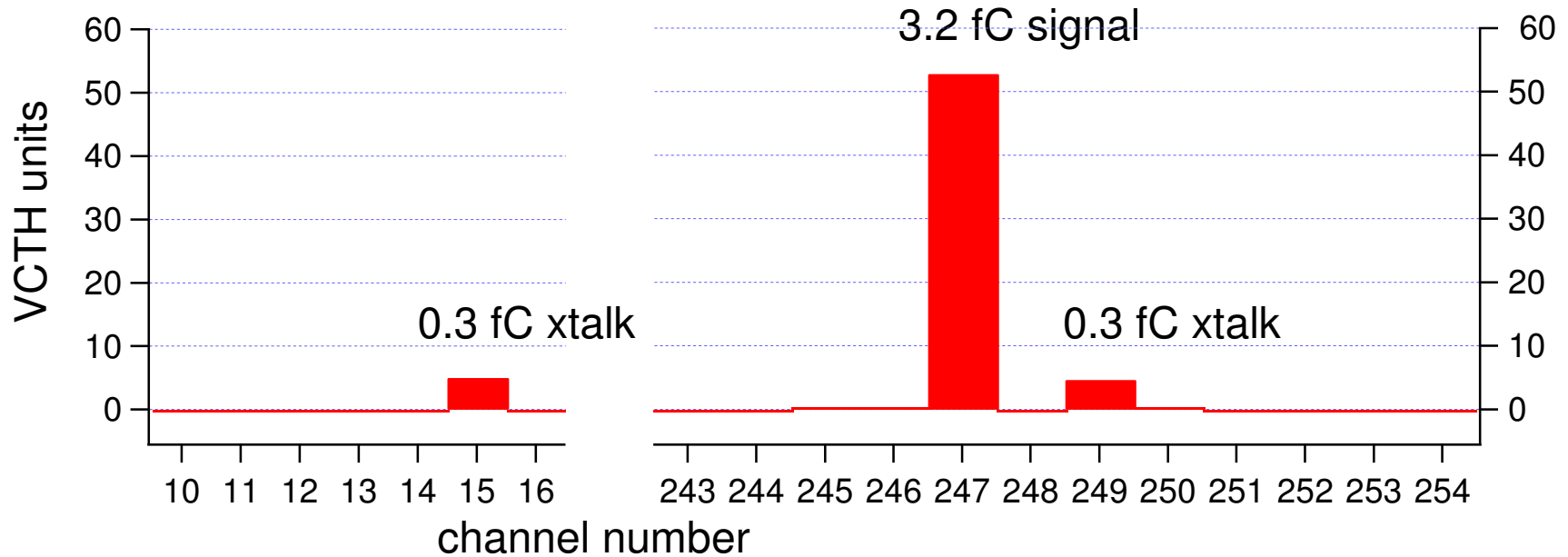


=> all significant crosstalk due to interstrip C, ~9% to nearest neighbour

results(2)

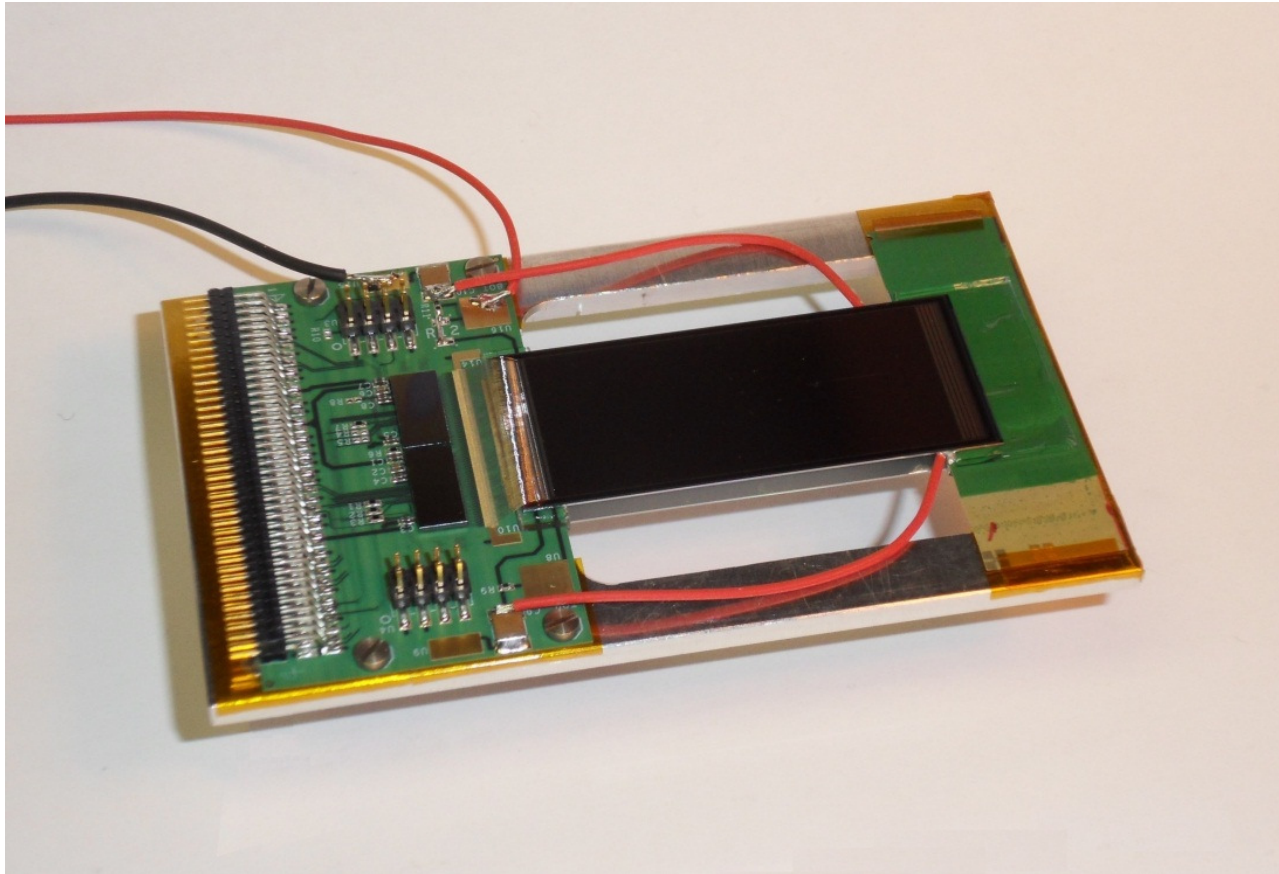


any significant difference if inject signal on lower layer?



=> no

2xCBC2 pT mini-module first results



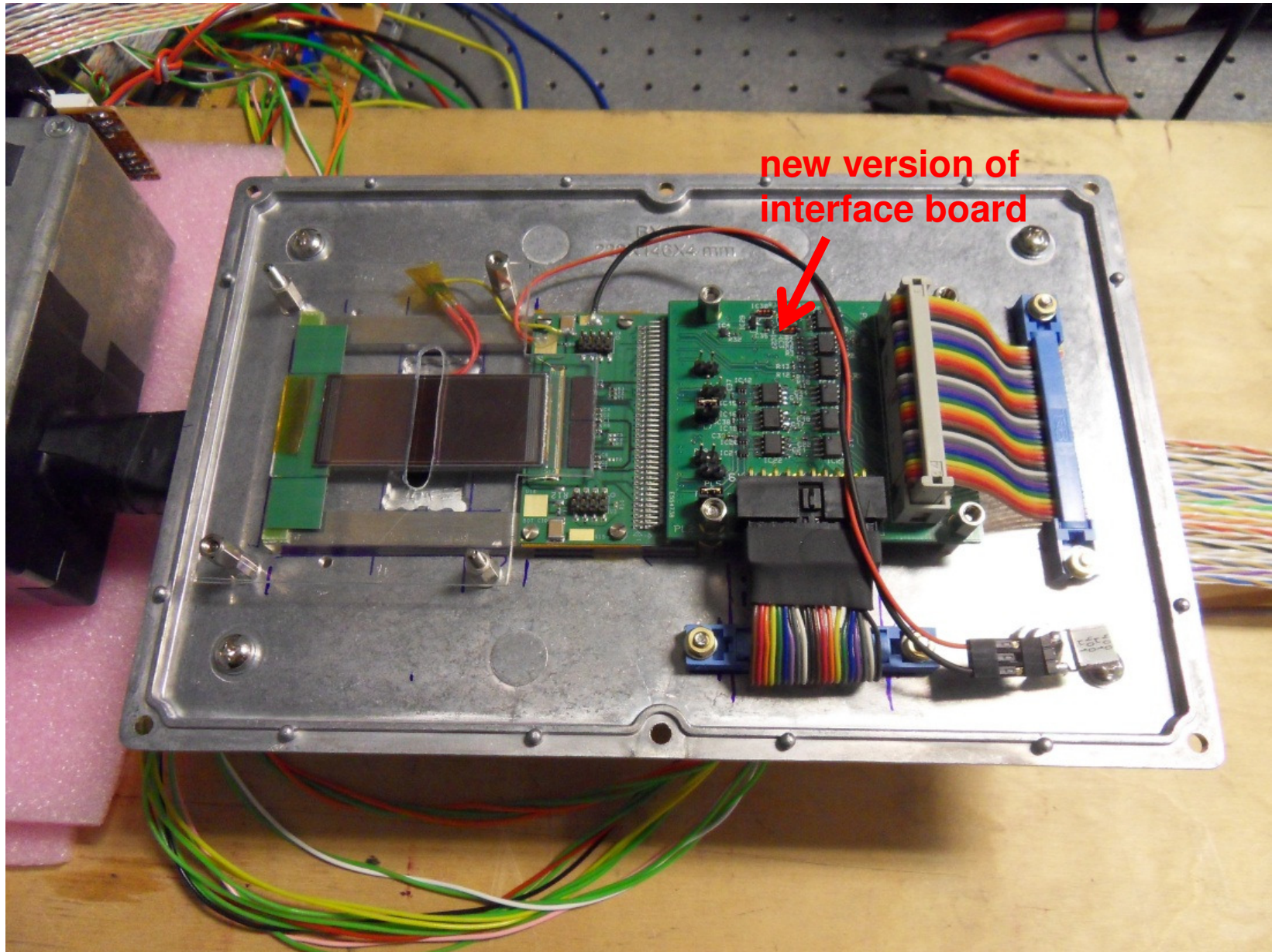
2 modules bonded : small differences in mechanical frame but essentially the same

1st module total leakage ~ 8 μ A

2nd module total leakage ~ 2 μ A (have concentrated on this one)

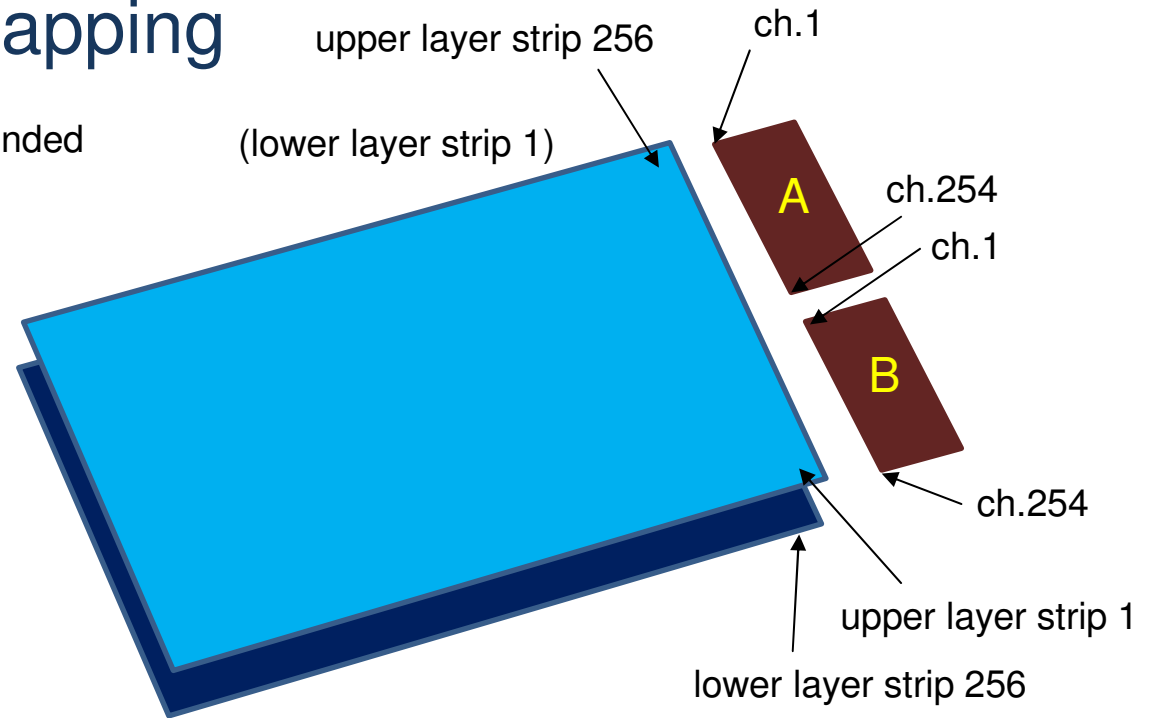
300V bias

mounted for readout

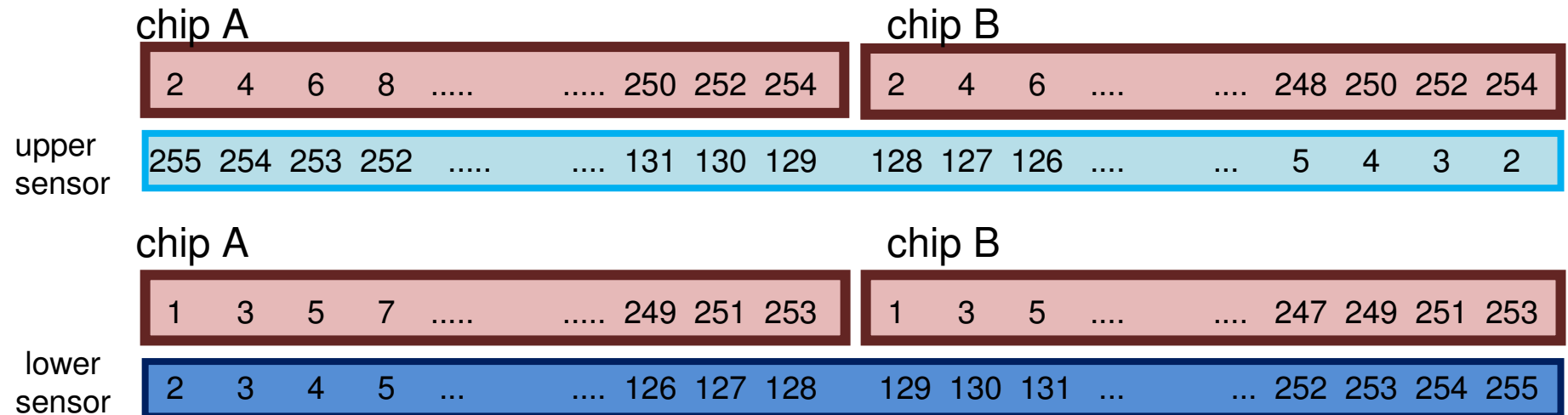


channel to strip no. mapping

2 edge channels on each sensor not bonded
(i.e. strips 2 - 255 inclusive bonded)



chip channel vs. sensor strip



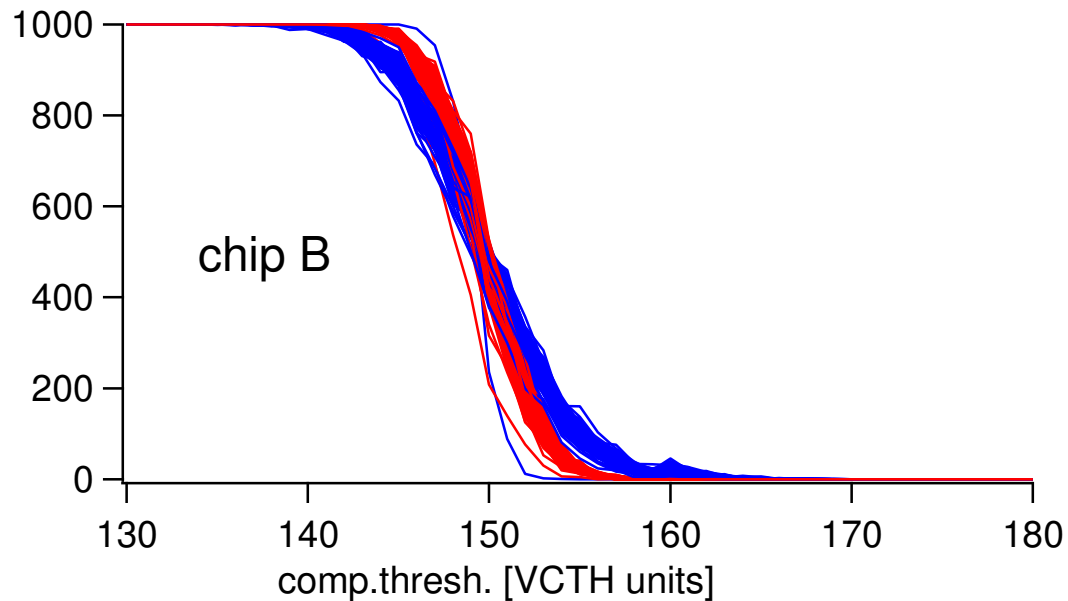
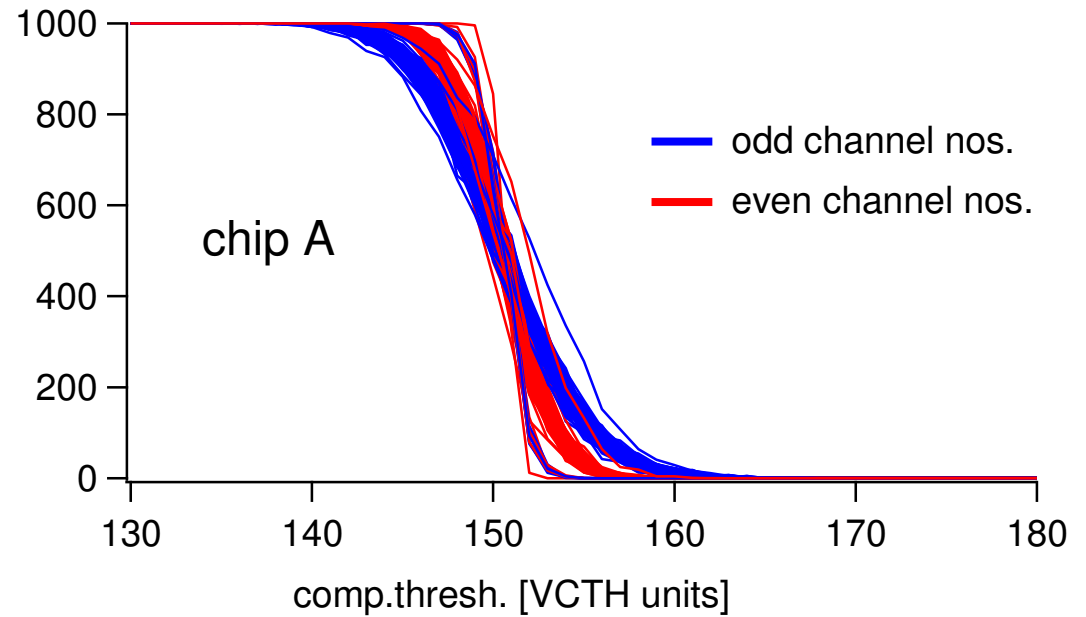
start with s-curves

acquired using on-chip test pulse

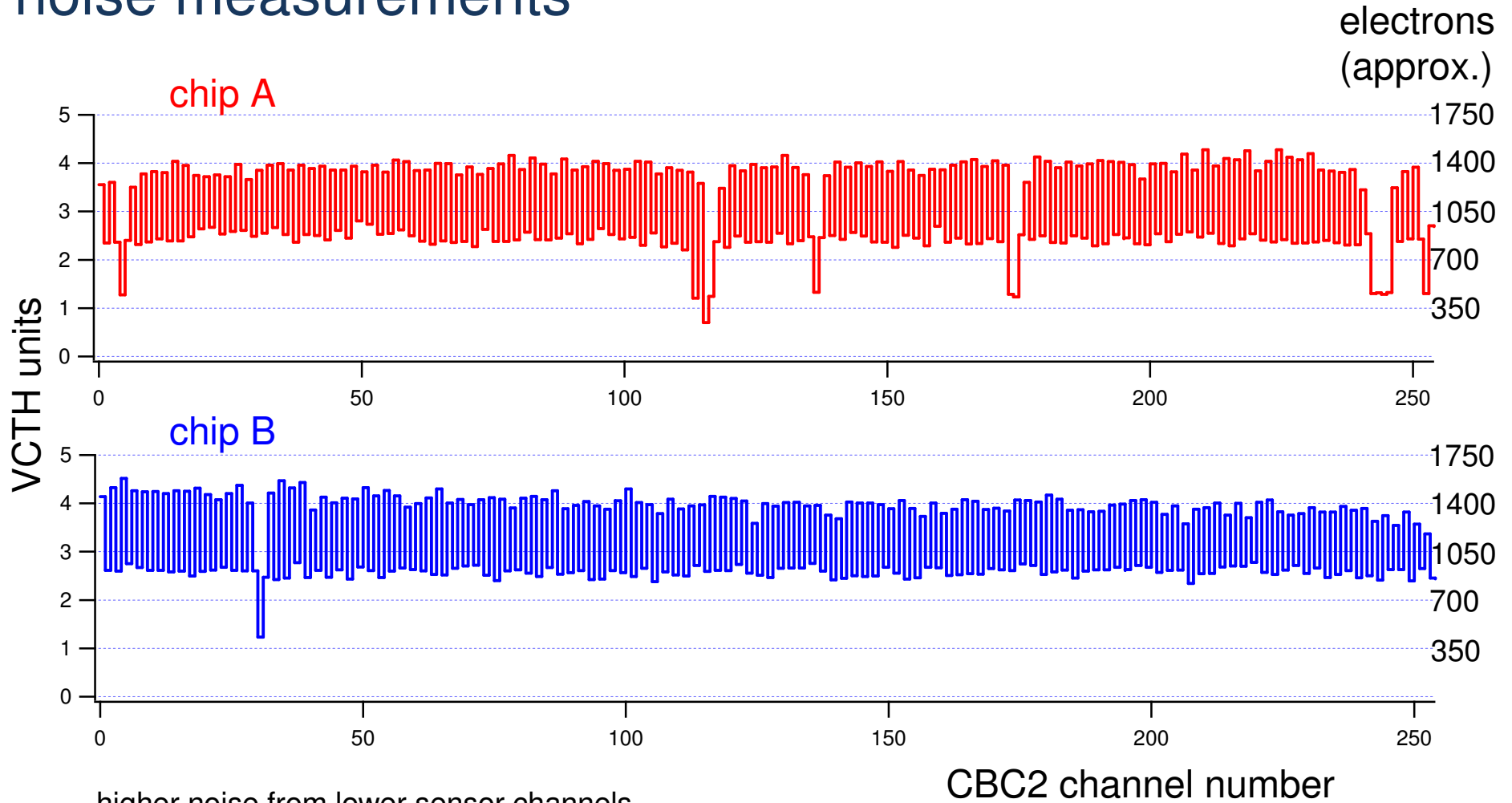
2 clear families corresponding to
odd & even chip channel numbers

odd CBC channels show more “stretched
out” s-curves
=> higher noise

odd channels correspond to lower sensor



noise measurements

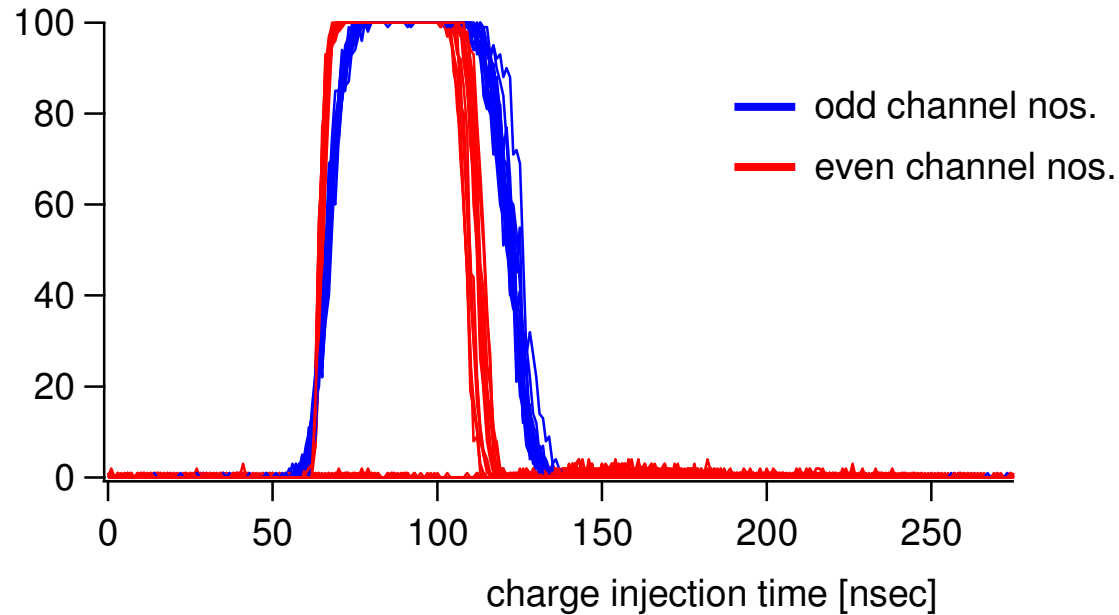


higher noise from lower sensor channels
not clear why

no explanation for anomalously low noise channels either
would seem to indicate no sensor-to-hybrid contact

note: no anomalous edge strip behaviour with sensors

test pulse charge injection time sweep



slower edge times for odd channels (lower sensor) => slower pulse shape => higher capacitance

consistent with higher noise

seems to indicate lower sensor not properly depleted?

note: other module not studied in such depth
but shows broadly similar results
significant?

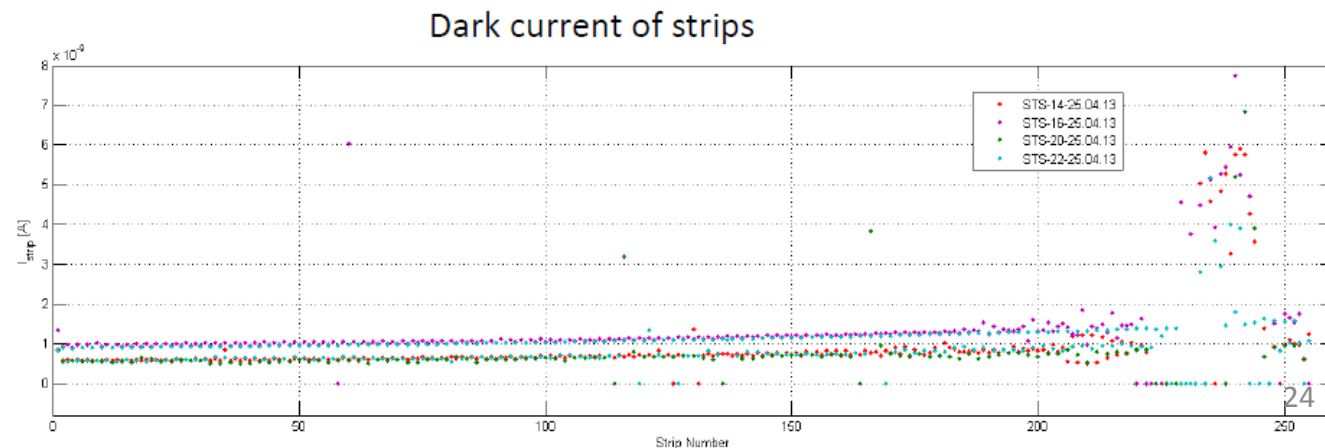
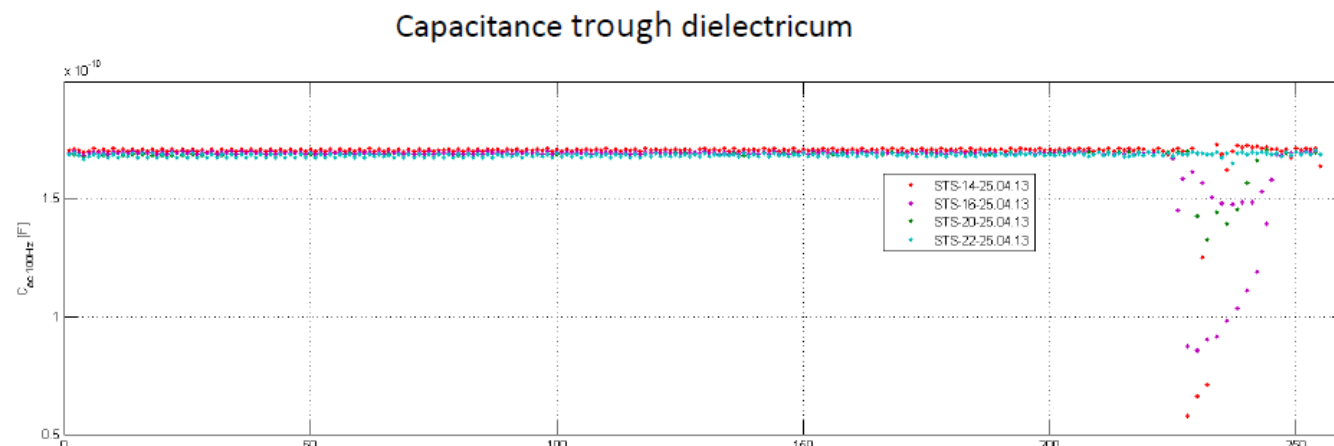
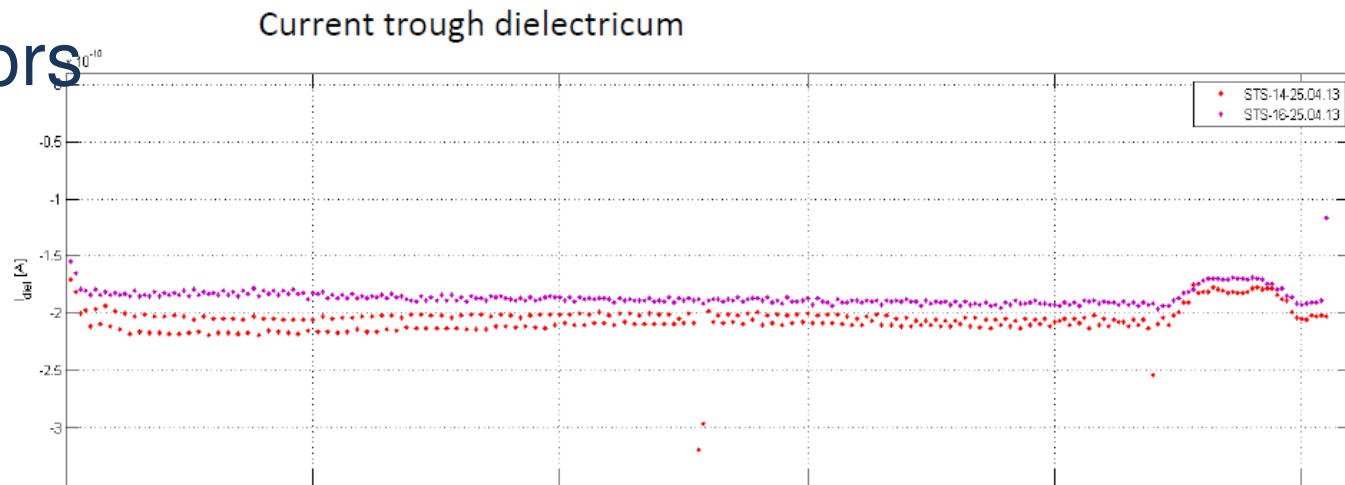
info on sensors from Vienna (Marko)

anomalous
behaviour between
strips 220 - 250

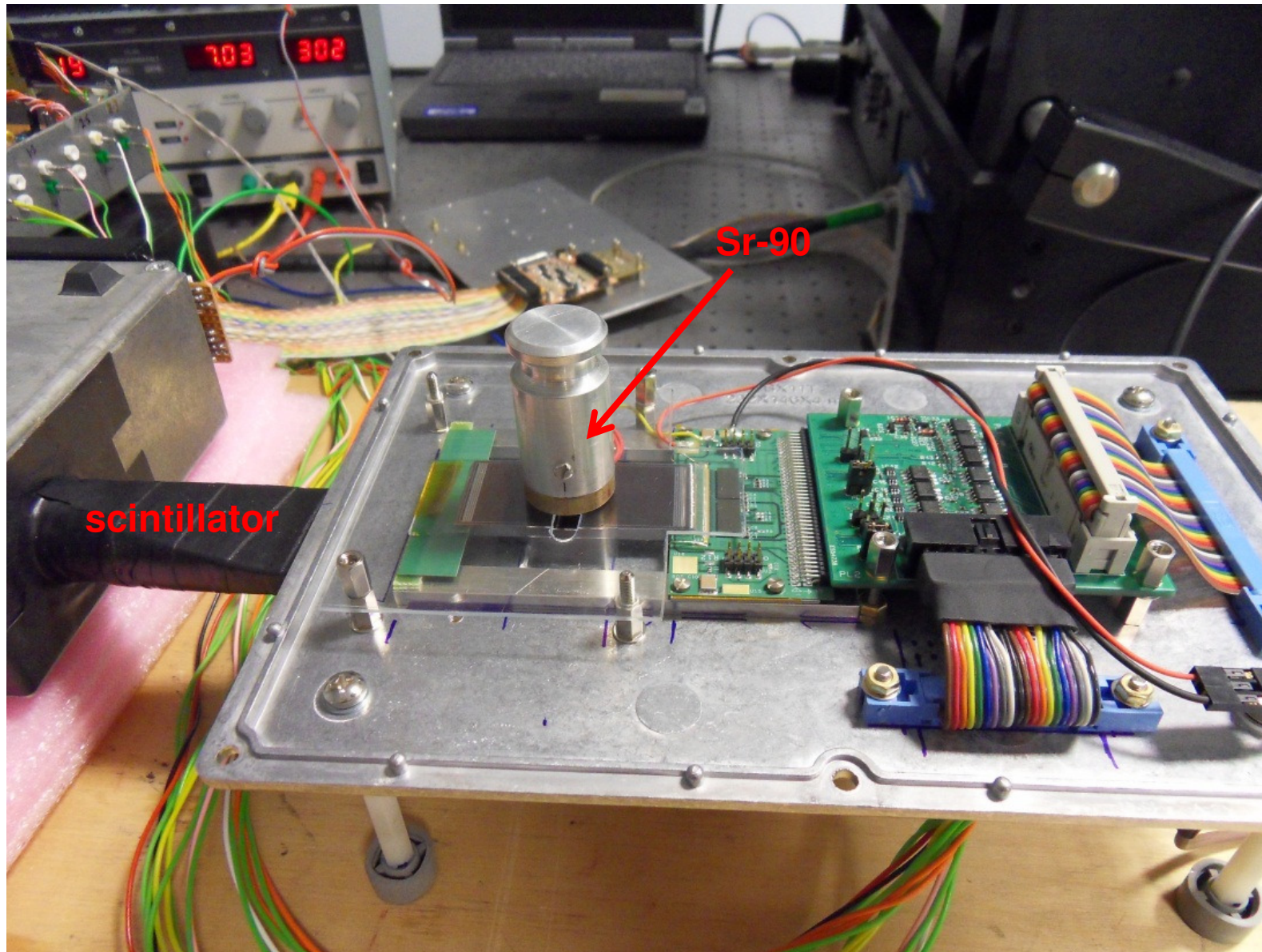
upper sensor
chip A even channels
between 10 - 70

lower sensor
chip B odd channels
between 185 - 245

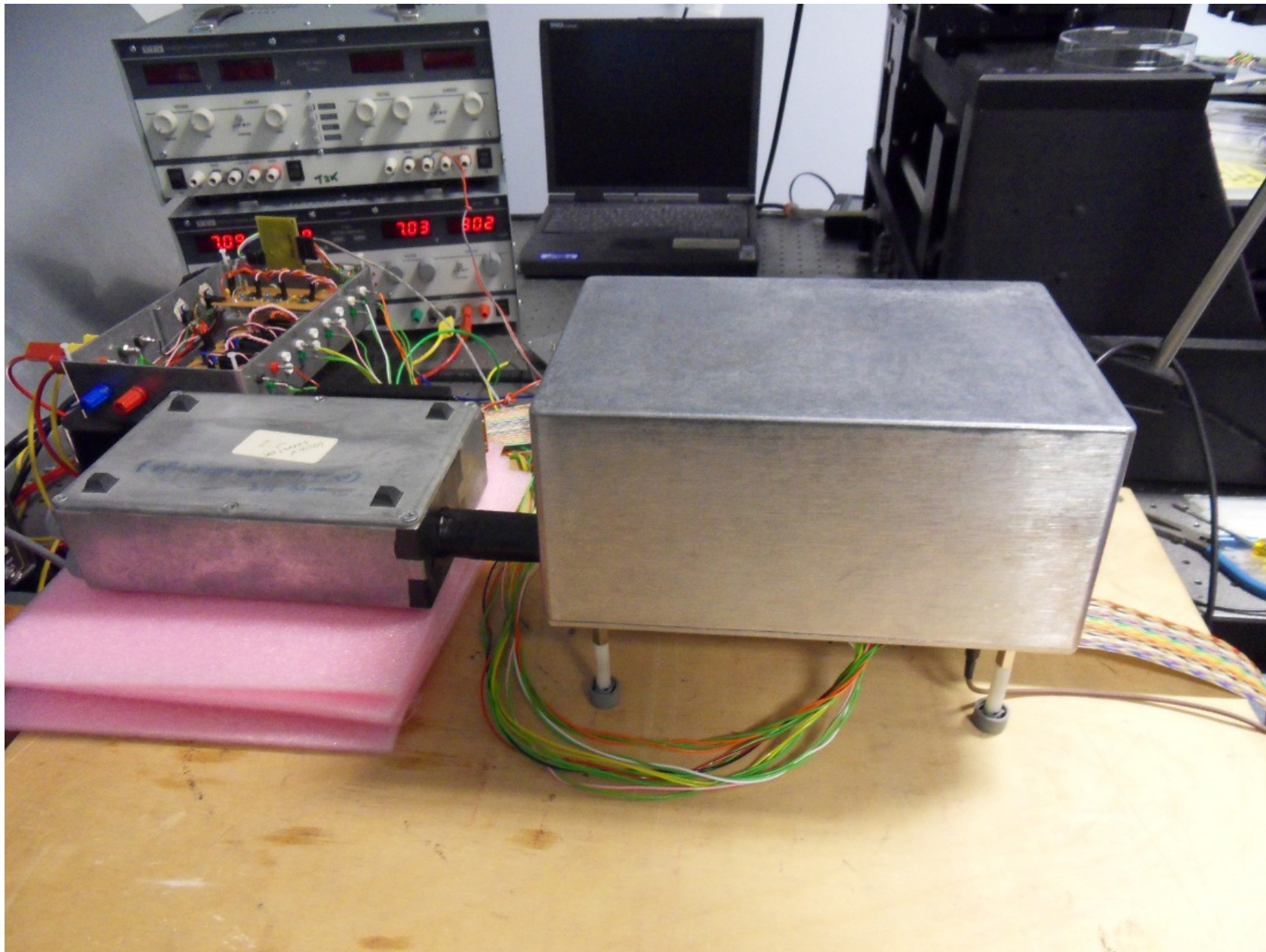
no clear correlation
with any module
measurement so far



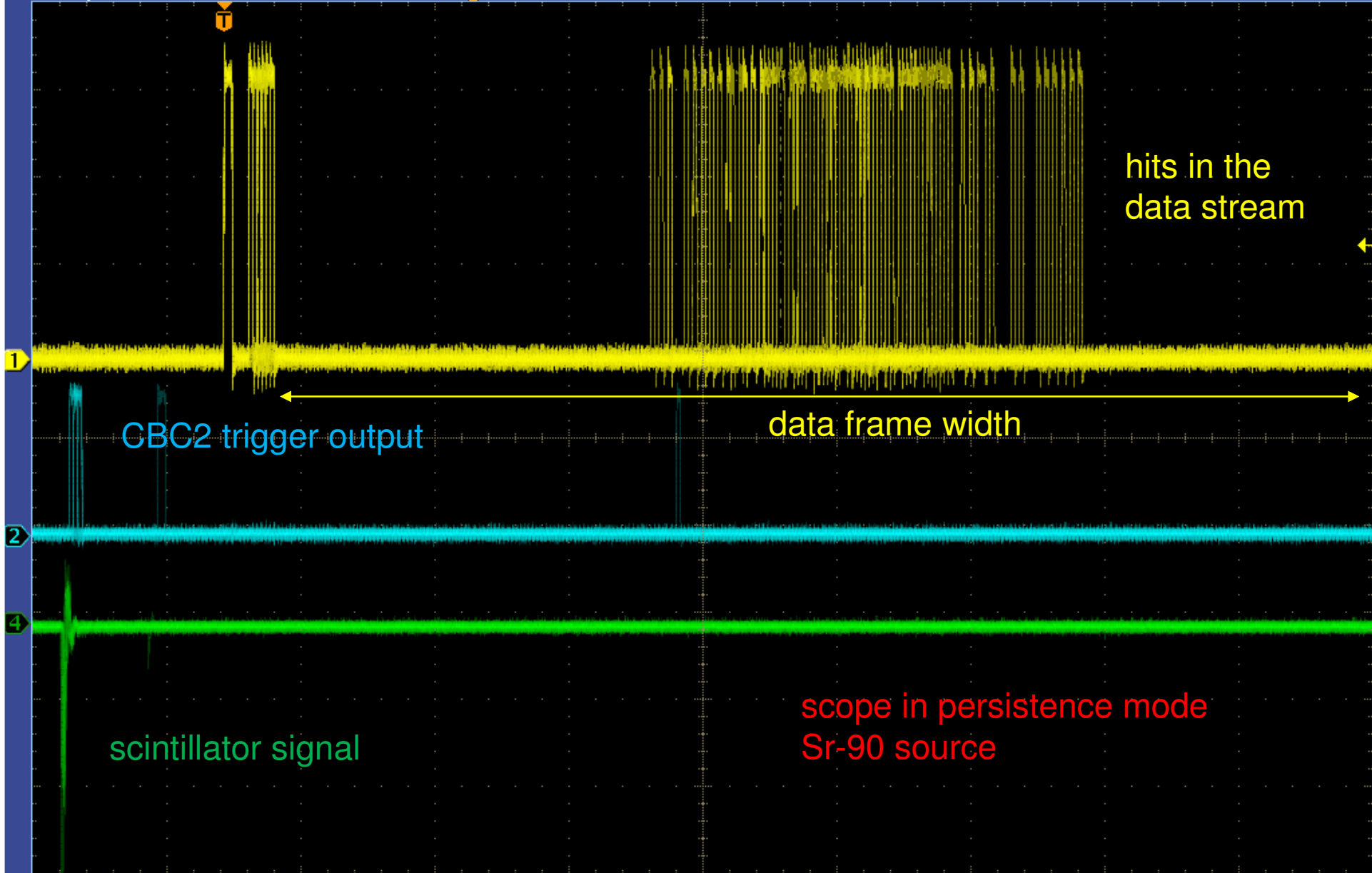
results with source and cosmics



light tight



tek Stop



hits in the data stream

CBC2 trigger output

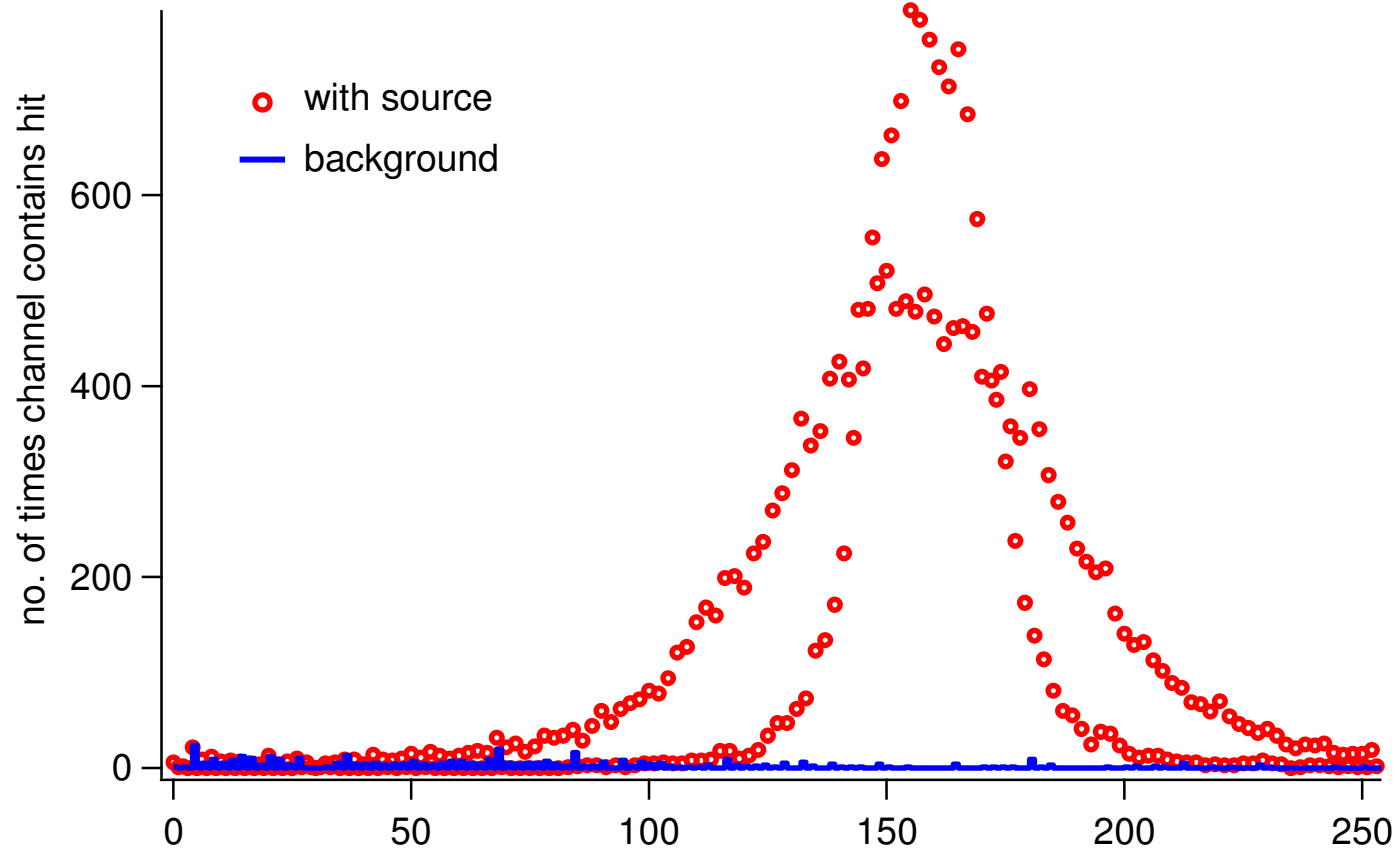
data frame width

scintillator signal

scope in persistence mode
Sr-90 source

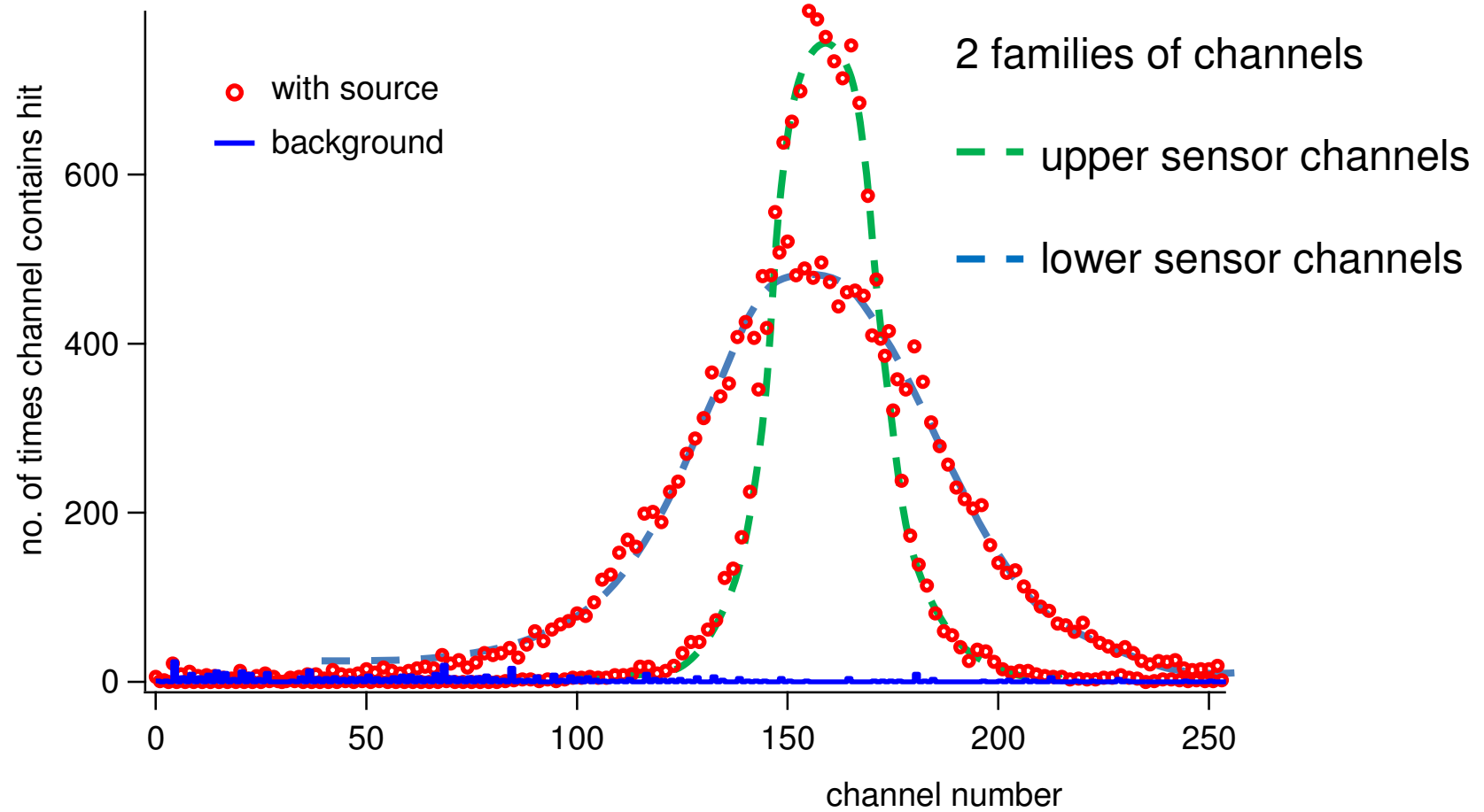
1 1.00 V	2 2.00 V	4 100mV Ω	800ns 14.30 %	1.25GS/s 10k points	1 1.32 V
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Sr-90 beta source profile

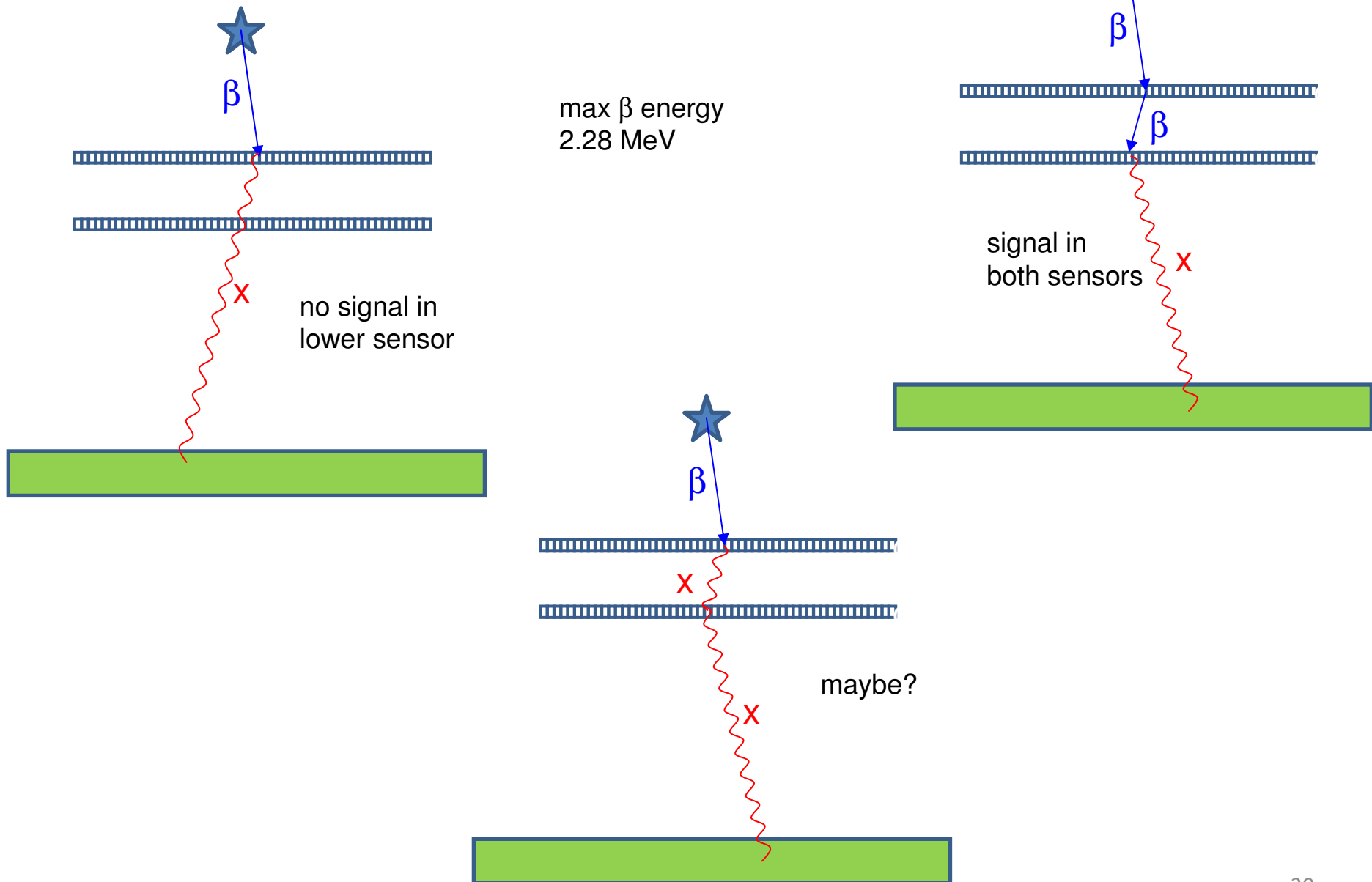


take 10,000 scintillator triggers
count number of times channel contains a hit (not number of clusters)

Sr-90 beta source profile



Sr-90 beta source profile interpretation



cosmic results

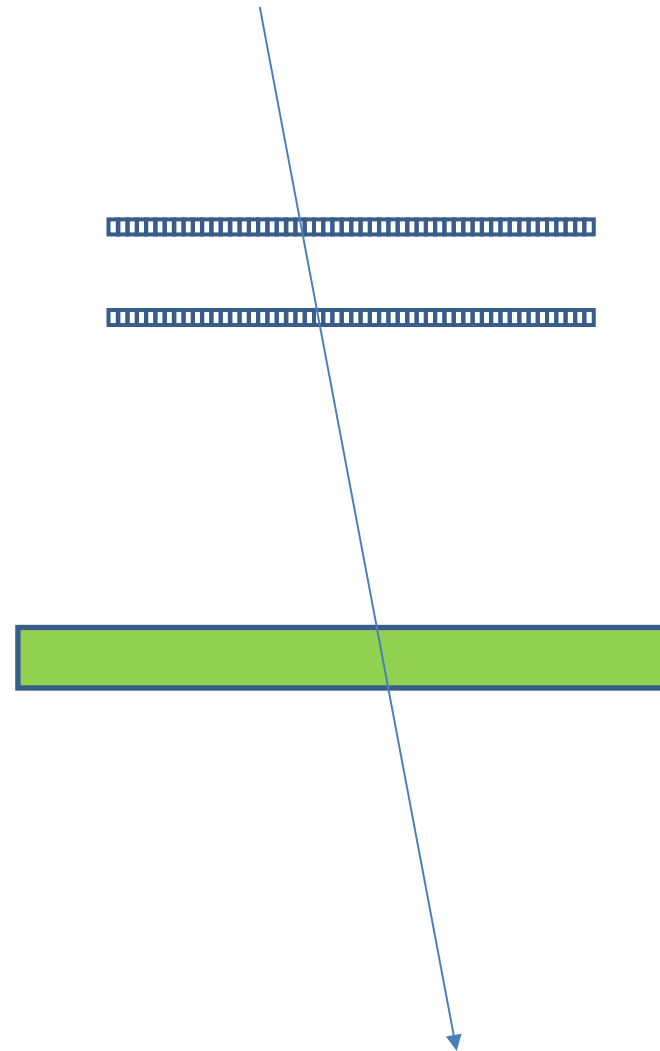
coincidence window set to max in upper sensor
to maximize sensitivity

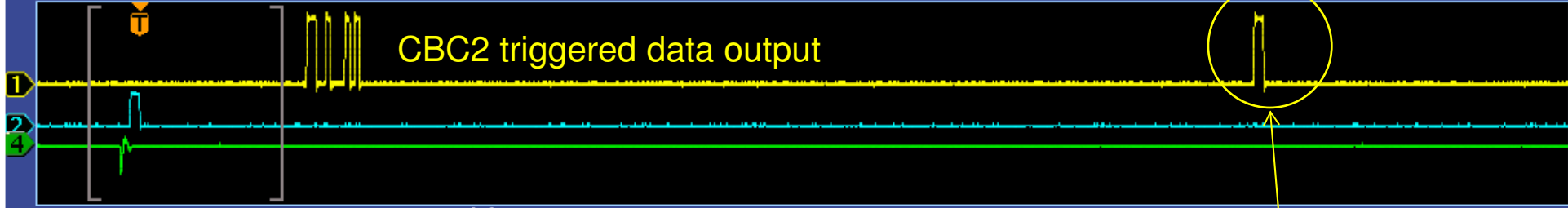
+/- 8 strips

rate still very low

$\ll 1$ Hz

scope pictures of event examples follow

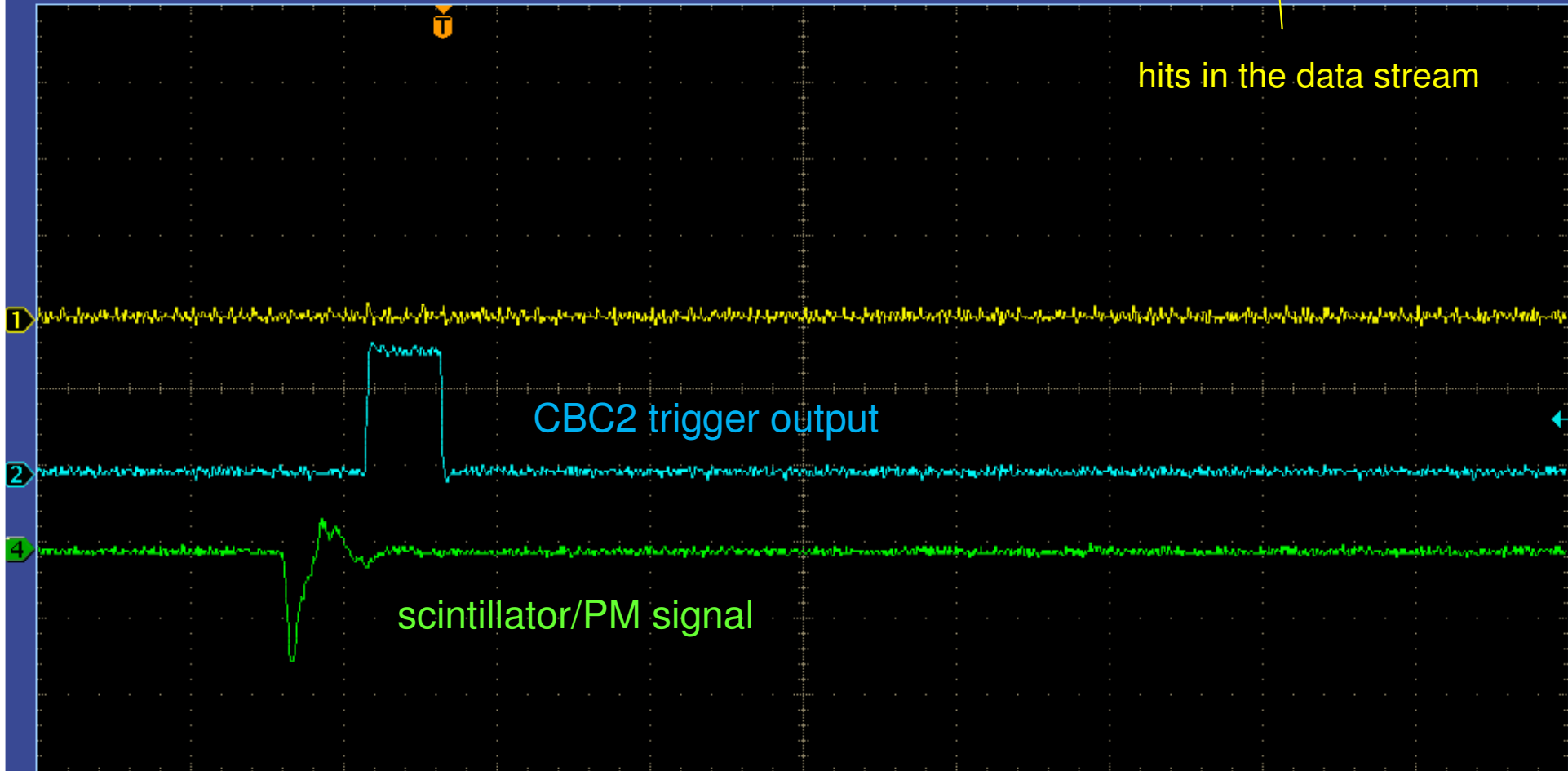




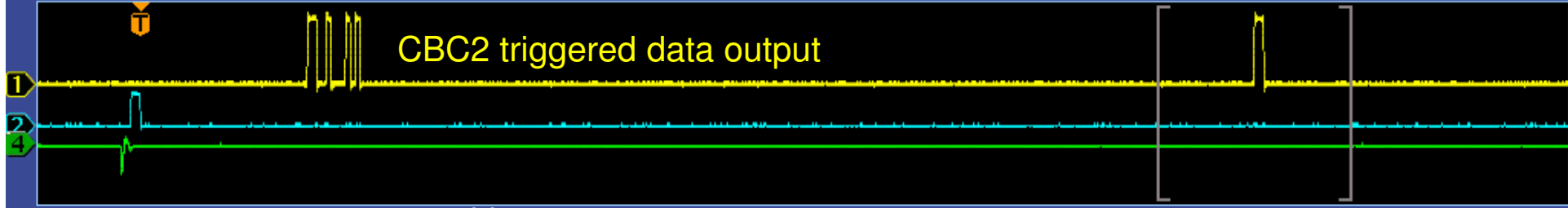
Zoom Factor: 8 X

Zoom Position: 235ns

hits in the data stream

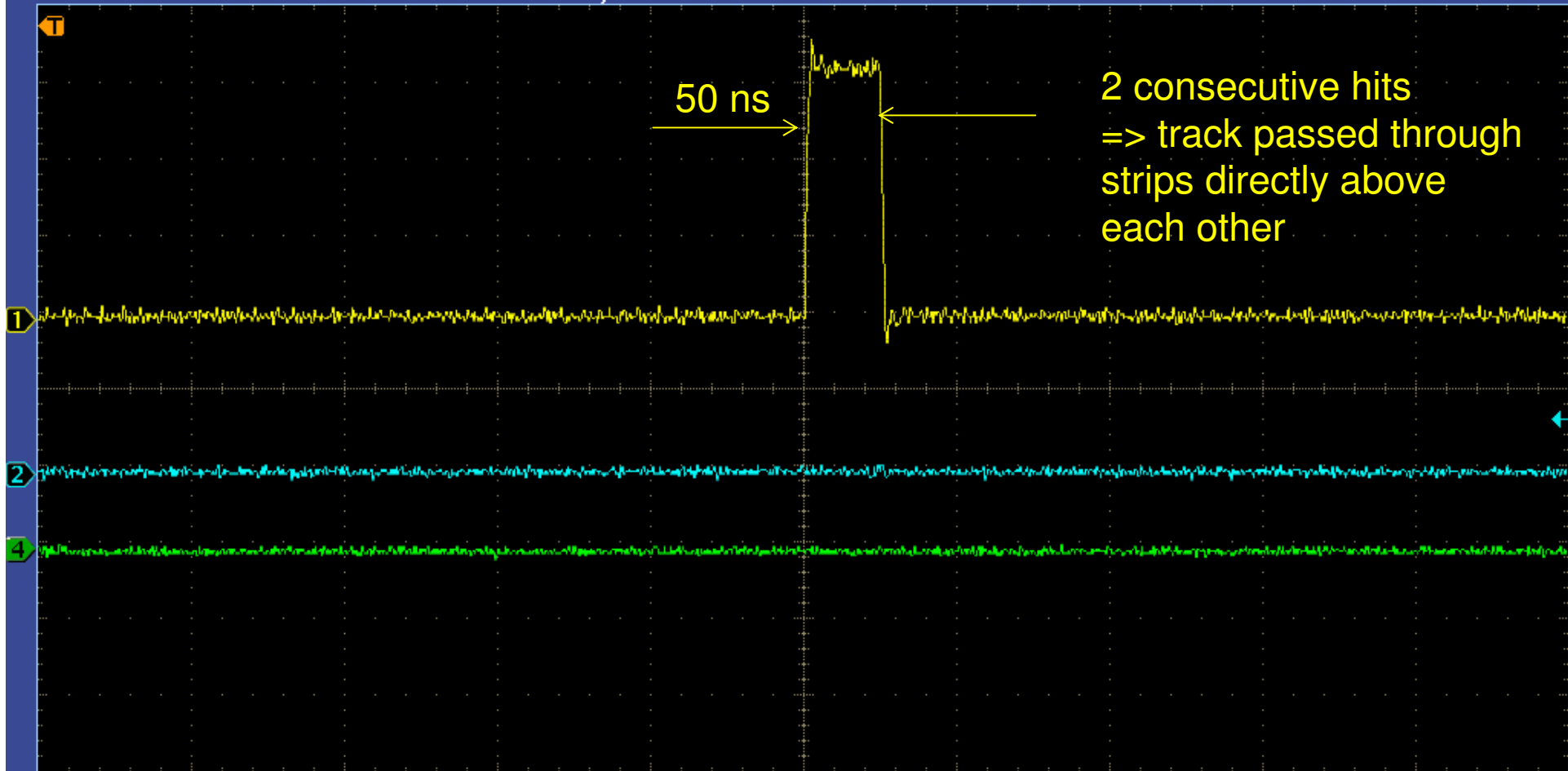


1 1.00 V 2 2.00 V 4 100mV Ω Z 100ns 1.25GS/s 2 ∇ 1.44 V
T 6.700 % 10k points

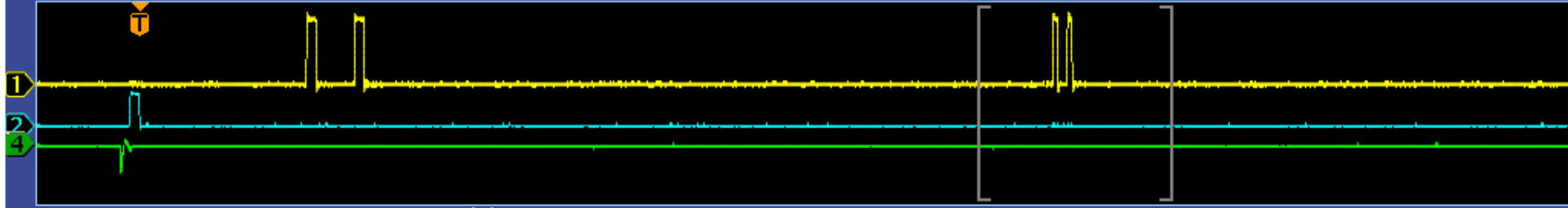


Zoom Factor: 8 X

Zoom Position: 5.82μs

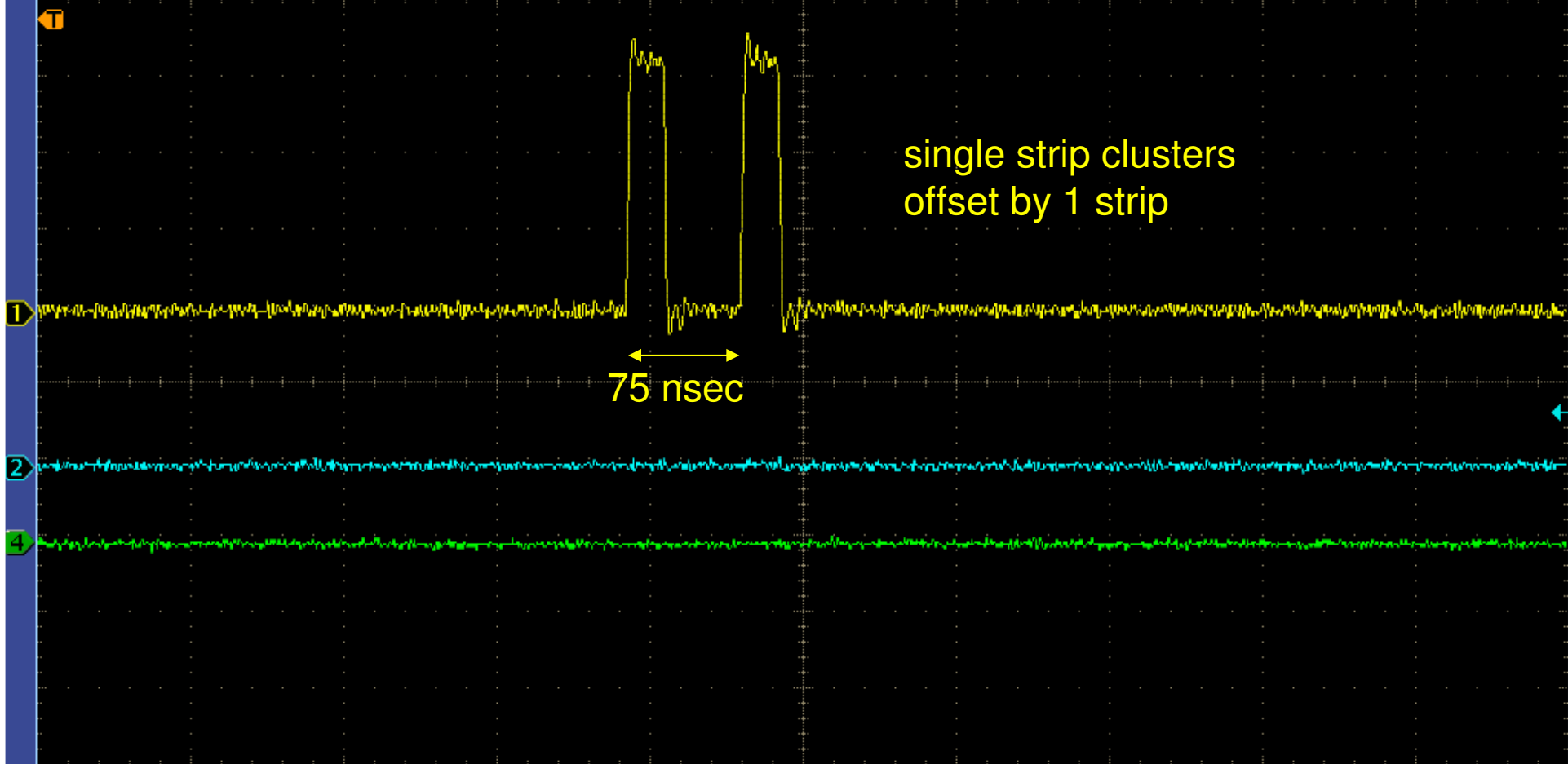


1 1.00 V 2 2.00 V 4 100mV Ω Z 100ns 1.25GS/s 2 1.44 V
T 6.700 % 10k points



Zoom Factor: 8 X

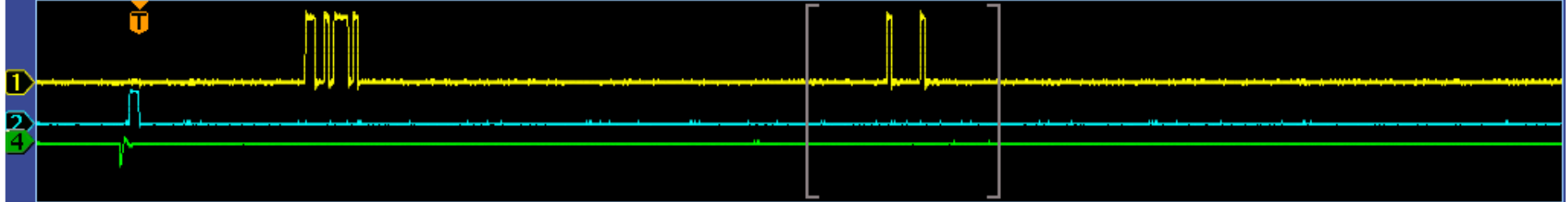
Zoom Position: 4.89µs



single strip clusters
offset by 1 strip

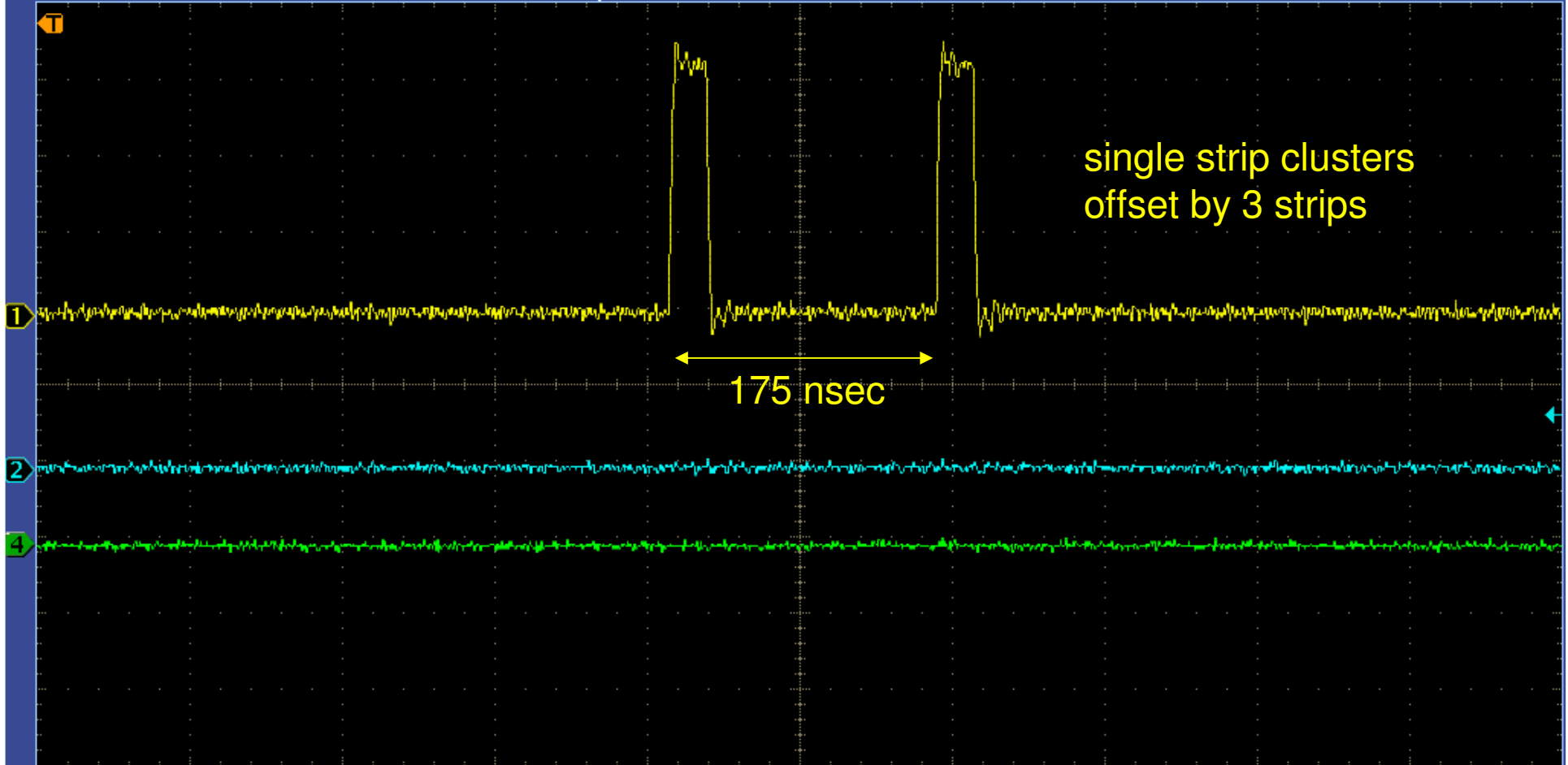
75 nsec

1 1.00 V 2 2.00 V 4 100mV Ω Z 100ns 1.25GS/s 2 1.44 V
T 6.700 % 10k points



Zoom Factor: 8 X

Zoom Position: 4.01 μ s



single strip clusters
offset by 3 strips

175 nsec

1 1.00 V

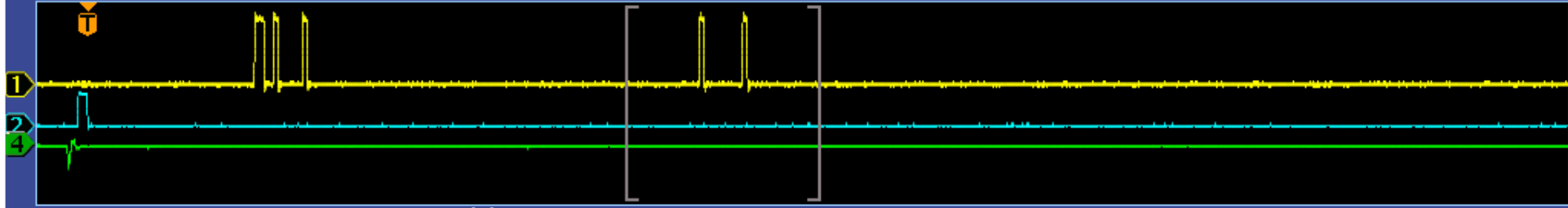
2 2.00 V

4 100mV Ω

Z 100ns
T 6.700 %

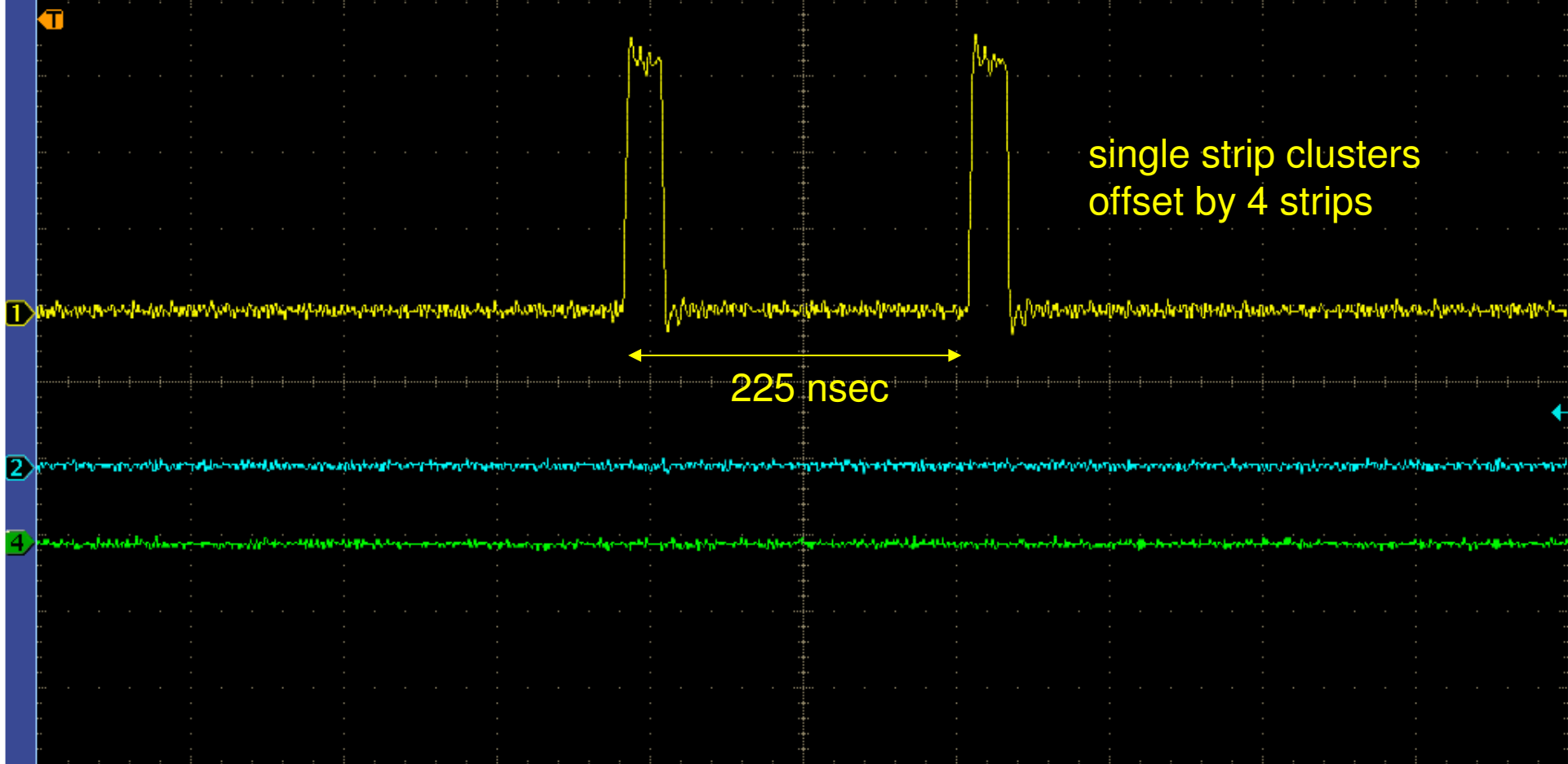
1.25GS/s
10k points

2 1.44 V



Zoom Factor: 8 X

Zoom Position: 3.31 μ s



single strip clusters
offset by 4 strips

225 nsec

1 1.00 V

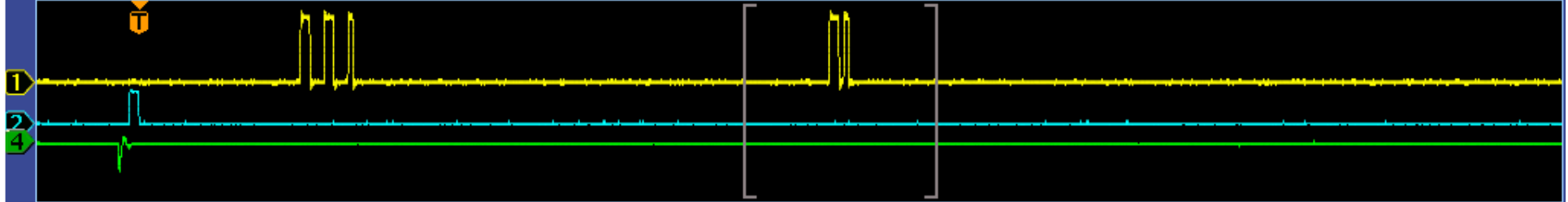
2 2.00 V

4 100mV Ω

Z 100ns
T 3.300 %

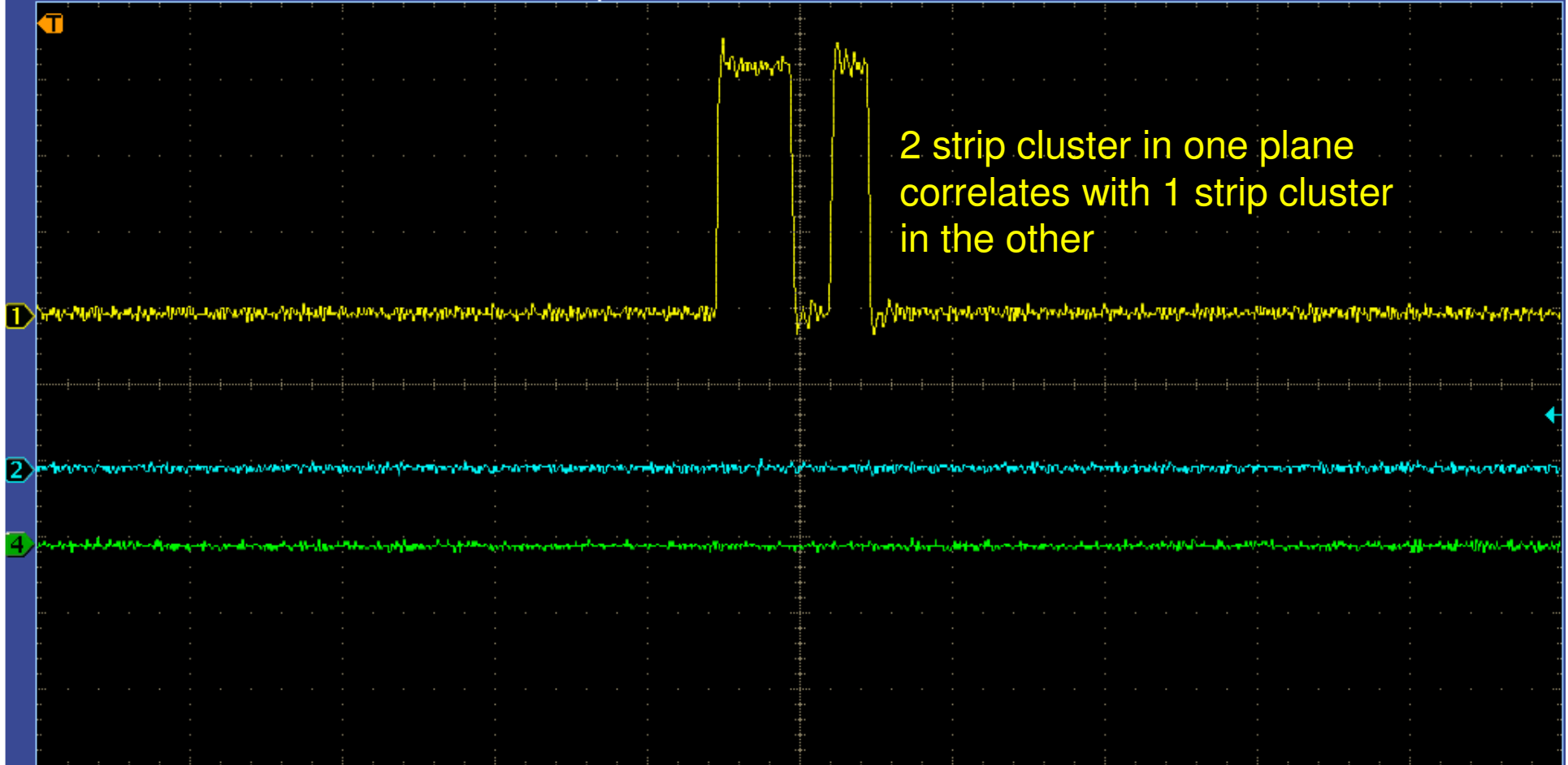
1.25GS/s
10k points

2 1.44 V



Zoom Factor: 8 X

Zoom Position: 3.68μs



1 1.00 V

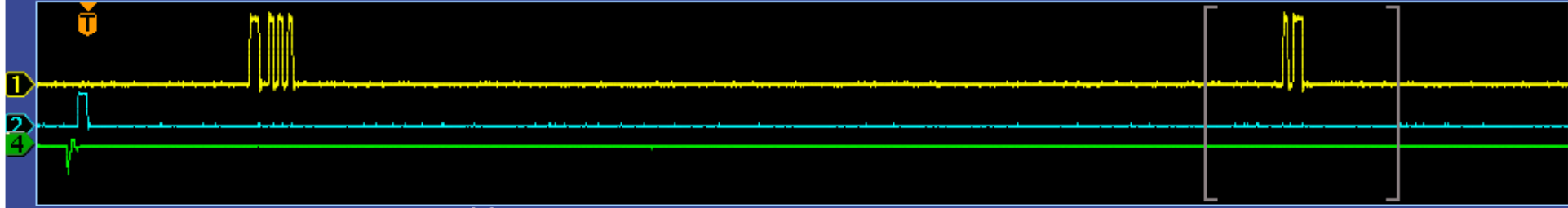
2 2.00 V

4 100mV Ω

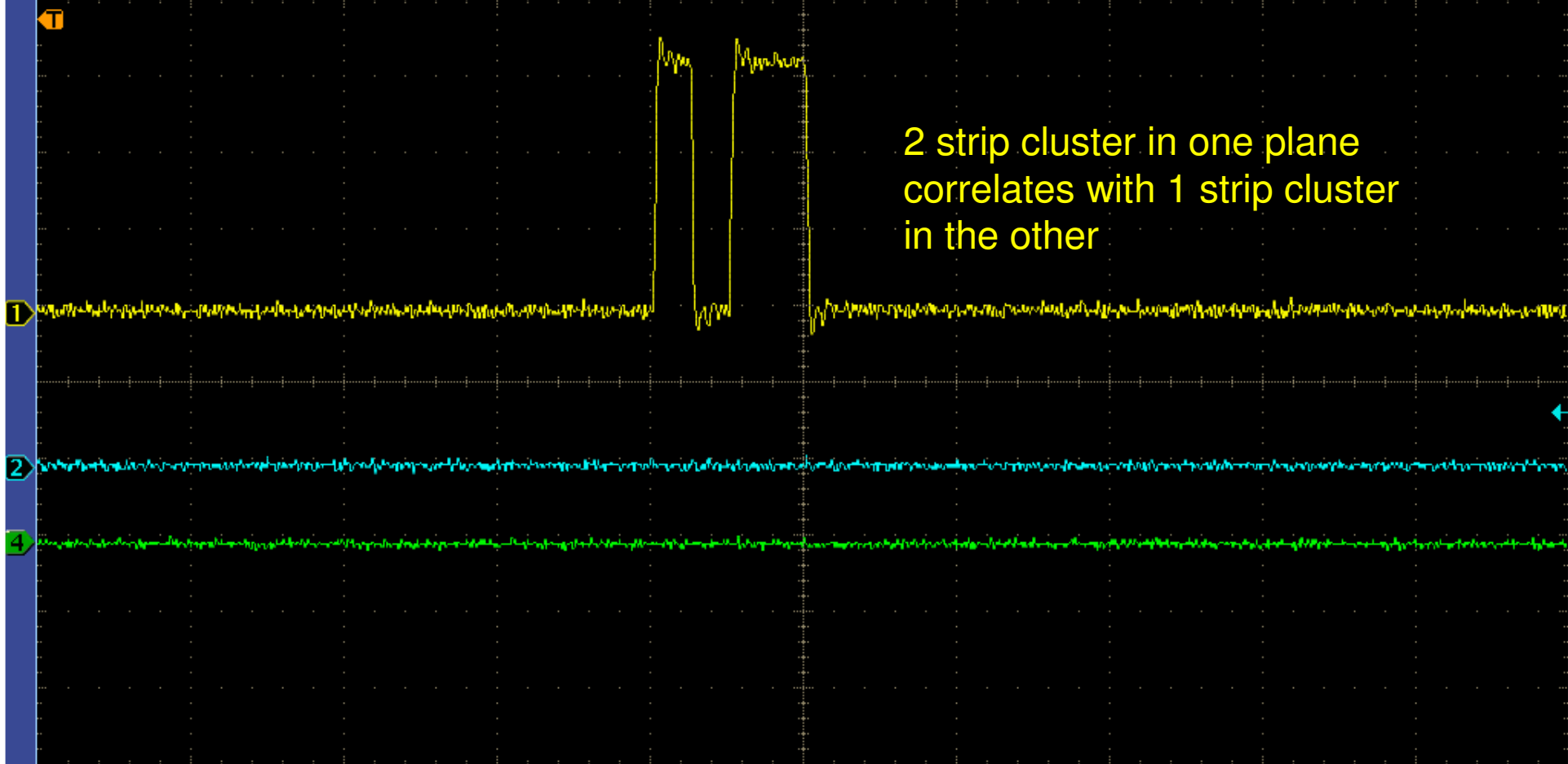
Z 100ns
T 6.700 %

1.25GS/s
10k points

2 1.44 V



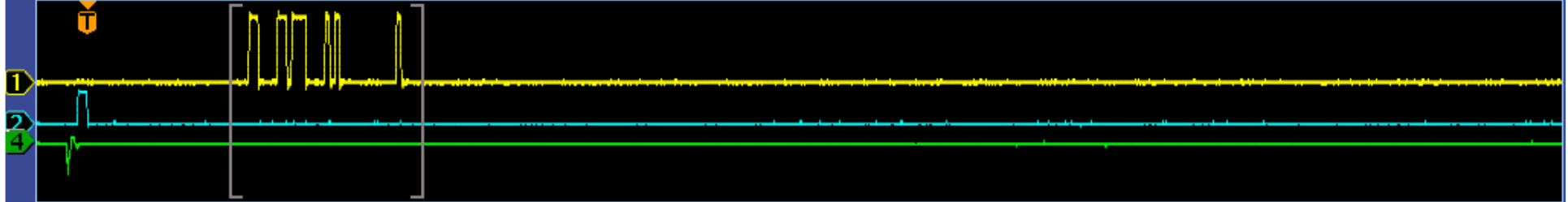
Zoom Factor: 8 X Zoom Position: 6.34μs



2 strip cluster in one plane
correlates with 1 strip cluster
in the other

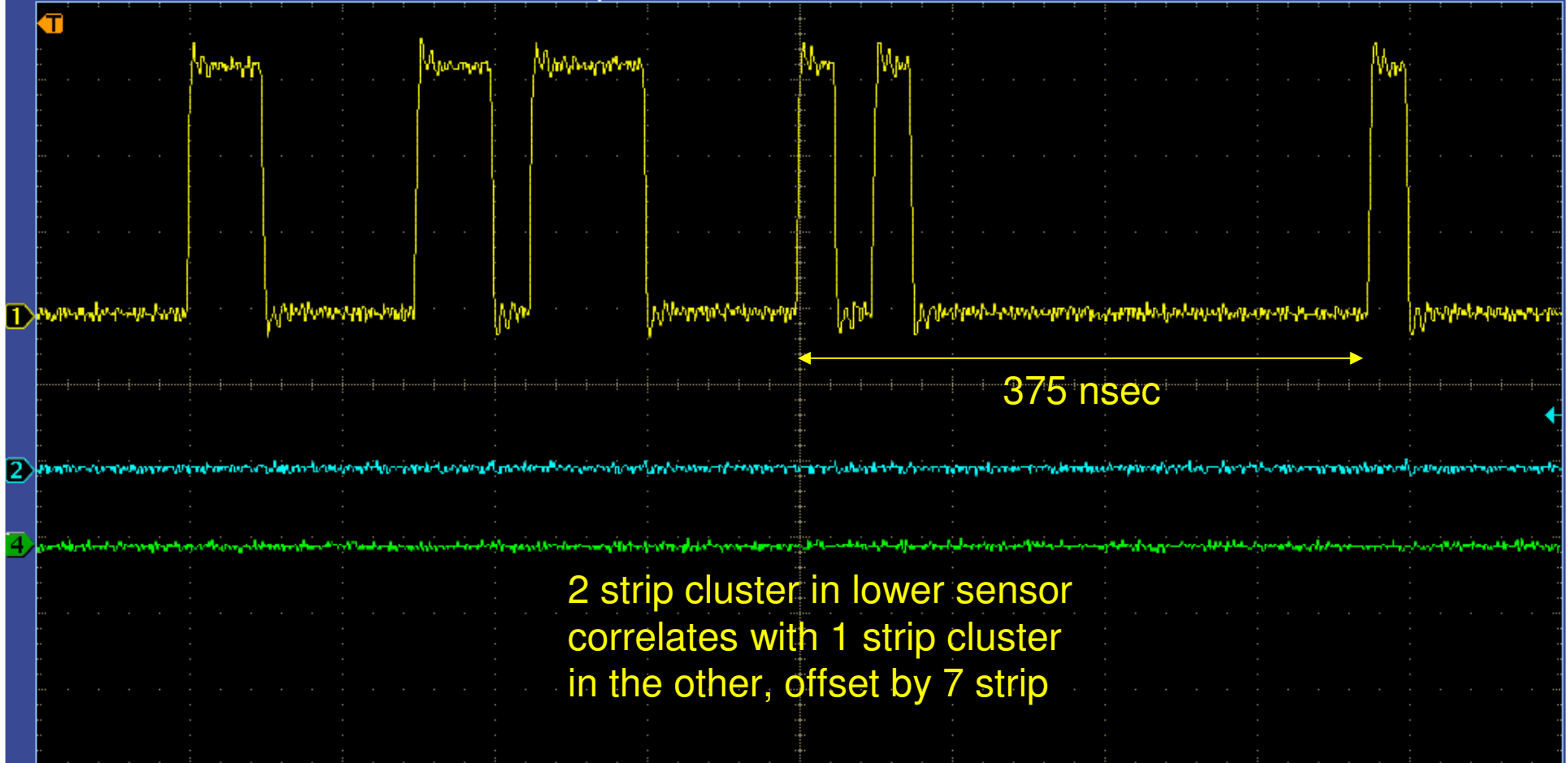
1 1.00 V 2 2.00 V 4 100mV Ω Z 100ns 1.25GS/s 10k points 2 1.44 V

3.300 %



Zoom Factor: 8 X

Zoom Position: 1.25μs



2 strip cluster in lower sensor
correlates with 1 strip cluster
in the other, offset by 7 strip

1 1.00 V

2 2.00 V

4 100mV Ω

Z 100ns
T 3.300 %

1.25GS/s
10k points

2 1.44 V

final remarks

- 2xCBC2 modules with/without sensors

lots of things to study

clearly functional but not everything fully understood at present

would be nice to have module with known good sensors

would help to discriminate between sensor and hybrid issues
doesn't have to be right pitch or length or all channels bonded

- new 2xCBC2 hybrid interface card now available

all differential interface should be much more reliable

- CBC2 wafers

have made some progress with wafer screening software but still some way to go

if diced chips requirement imminent then can scan another wafer by hand (takes ~ 1 day)