CBC2 status update

D.Braga, M.Prydderch (STFC RAL)

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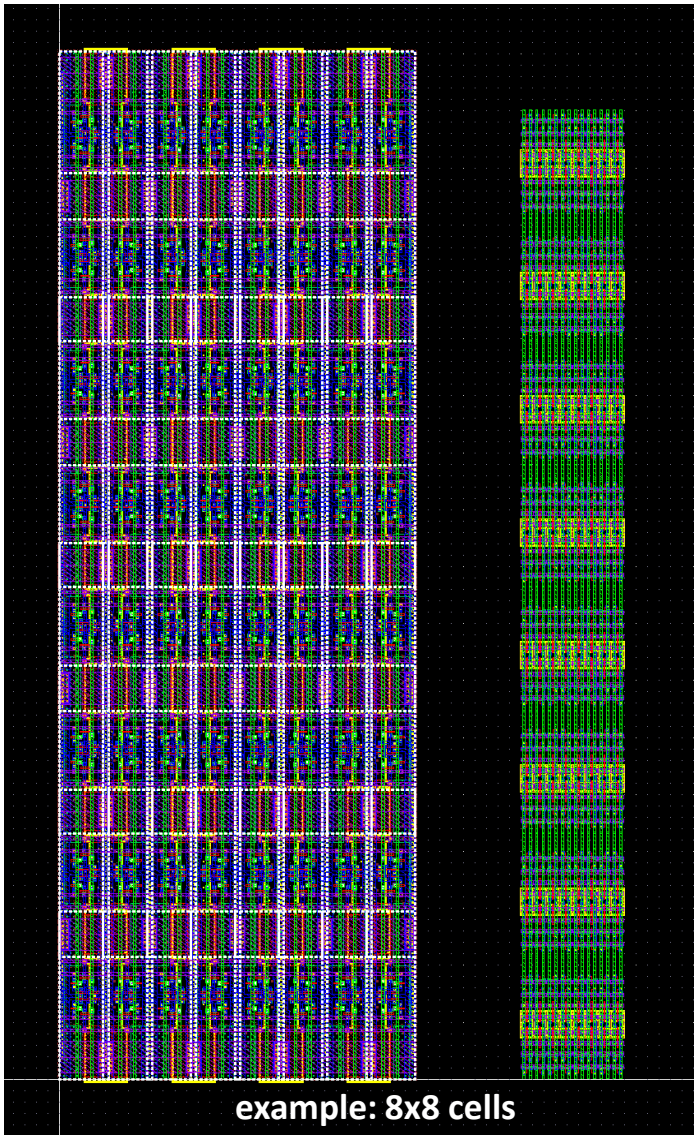
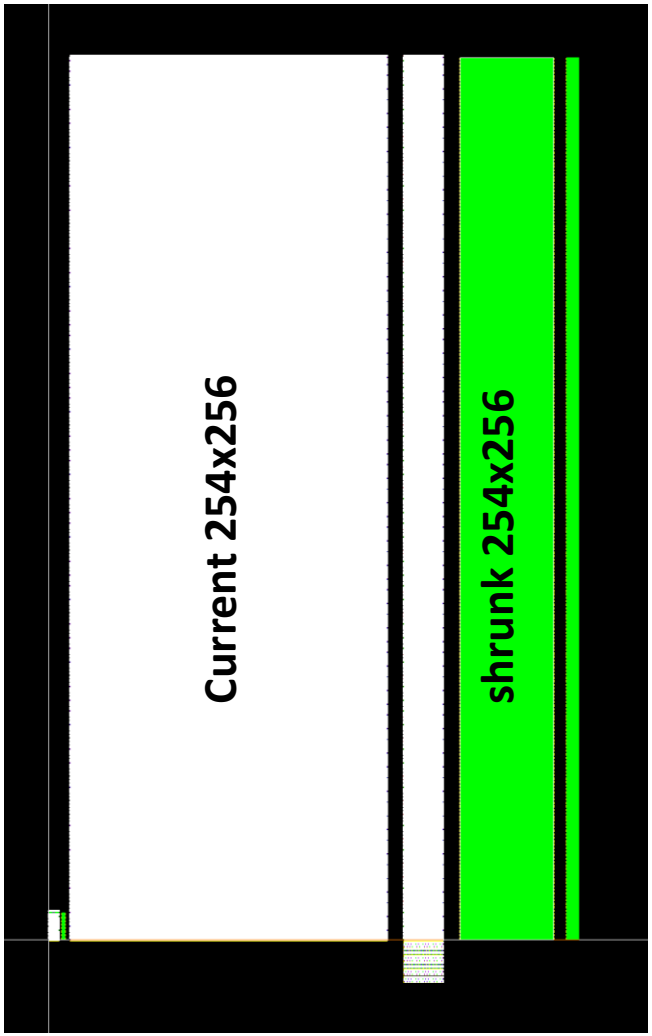
Imperial College London

Science & Technology Facilities Council

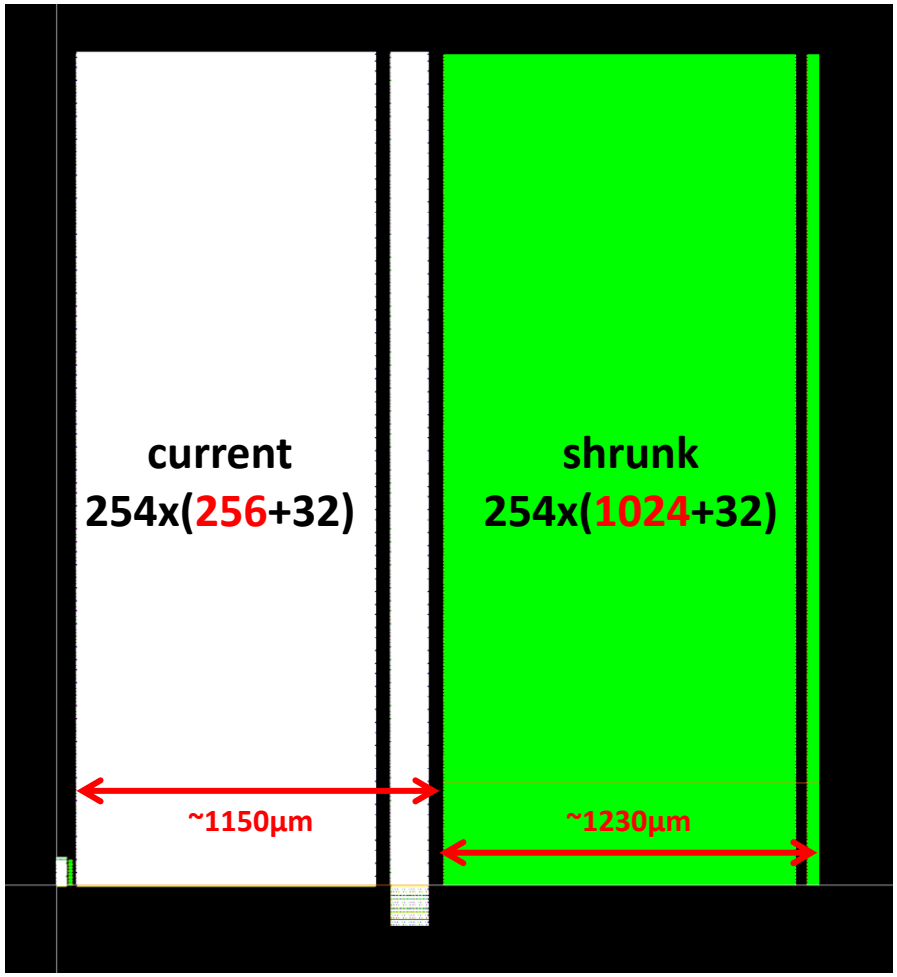
Thin RAM exercise: results



Managed to compress the existing layout by 4



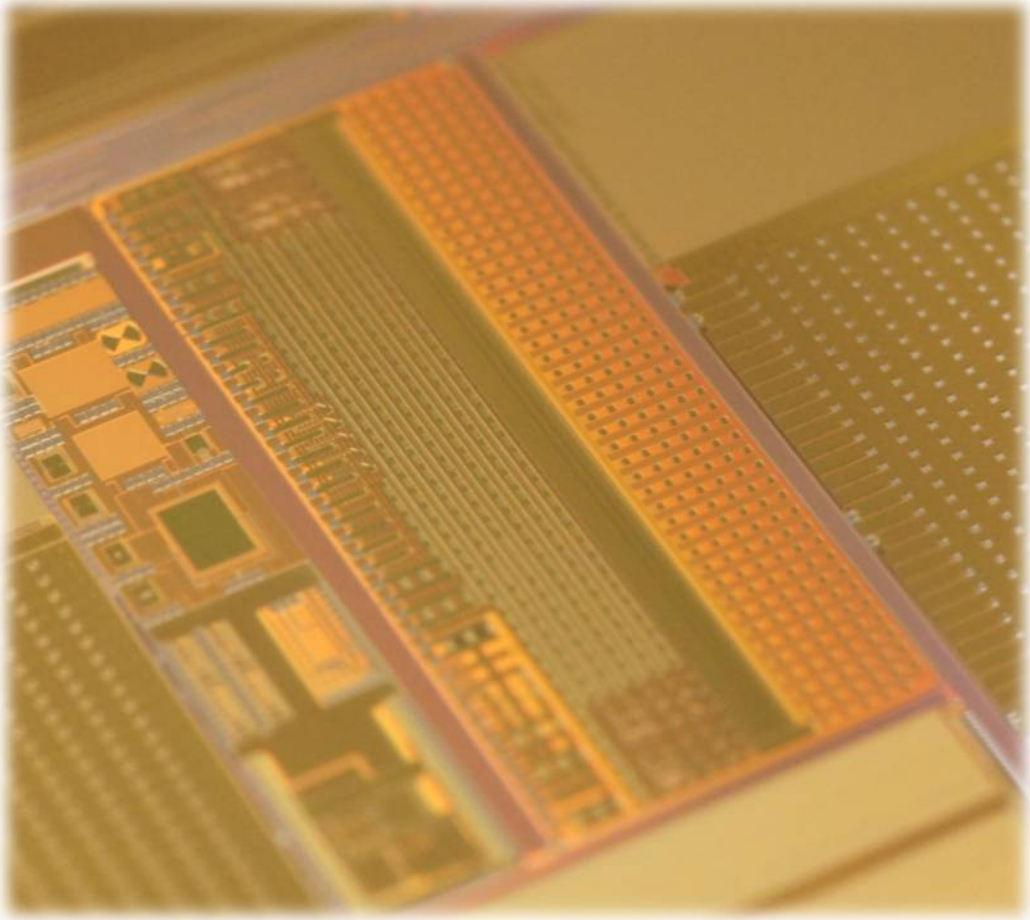
Longer latency: memory pipeline

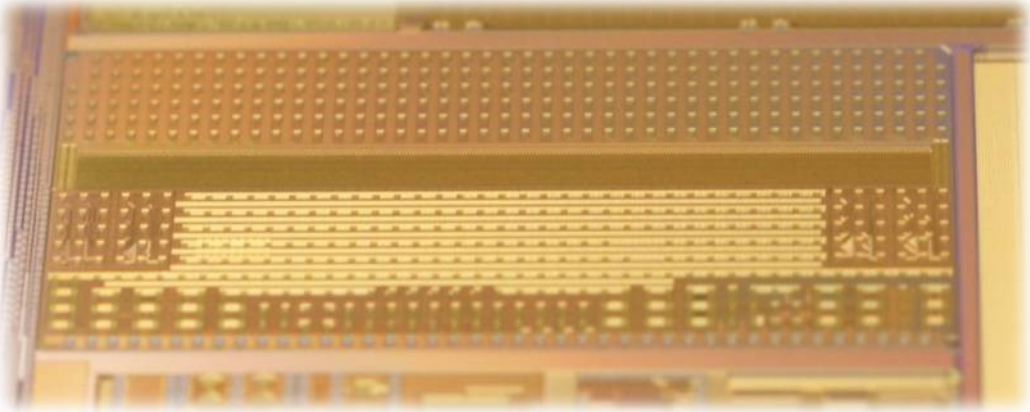


It is possible to have 4 times the memory in the existing area without widening the chip.

However:

- Much increased fringe capacitance between read/write lines → will need to drive these from the middle of the array to reduce line delays
- Might need to include extra area to satisfy local density rules
- Have not altered control circuitry for now (don't foresee any particular problem but premature)
- Test and radiation results from CBC2 memory will not translate to CBC3





Wafer status

Wire-bonded wafers (pictured):

- 6 wafers received on 17/01
- 1 with cutting company since 22/01, will get ½ diced (~50 chips)
- Pressing for fast delivery, but expected in ~3weeks

C4 wafers:

- 8 wafers received on 21/01
- Wafer probes delivered on 15/01
- Wafer probing to start this week at Imperial