CBC powering

can CBC3 be powered from 1.2V +/- 5% ?

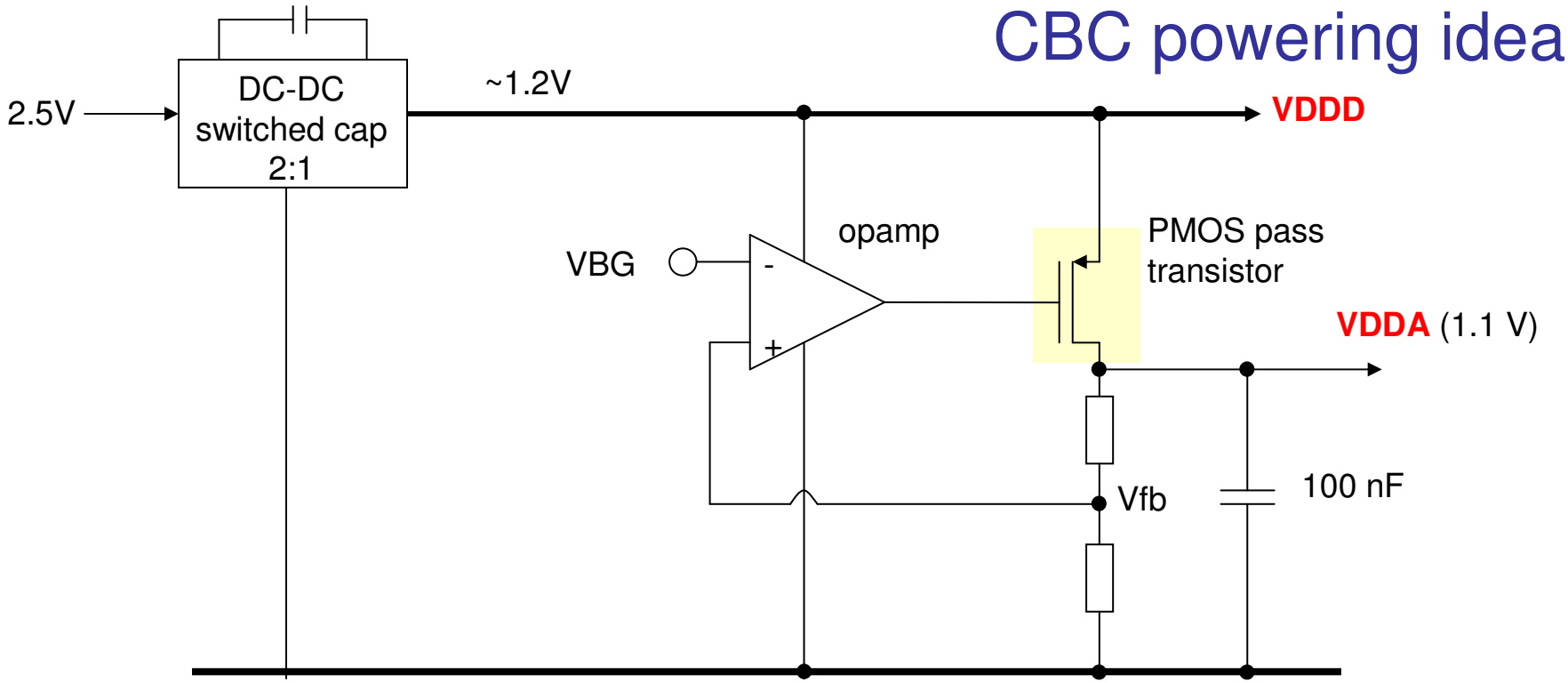
=> 1.14 - 1.26 V

upper limit for CBC

130 nm technology allows VDD up to 1.6 V

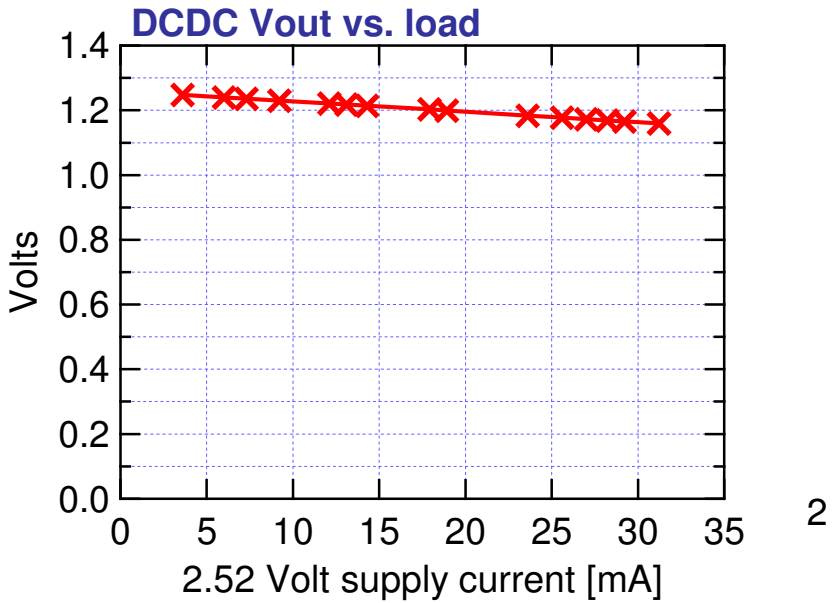
lower limit dictated by correct circuit functionality

CBC powering ideas



switched cap. DC-DC
- does not have to be used
- may well work well in bump-bond layout

in reality needs >2.5V to guarantee
LDO input > 1.2V



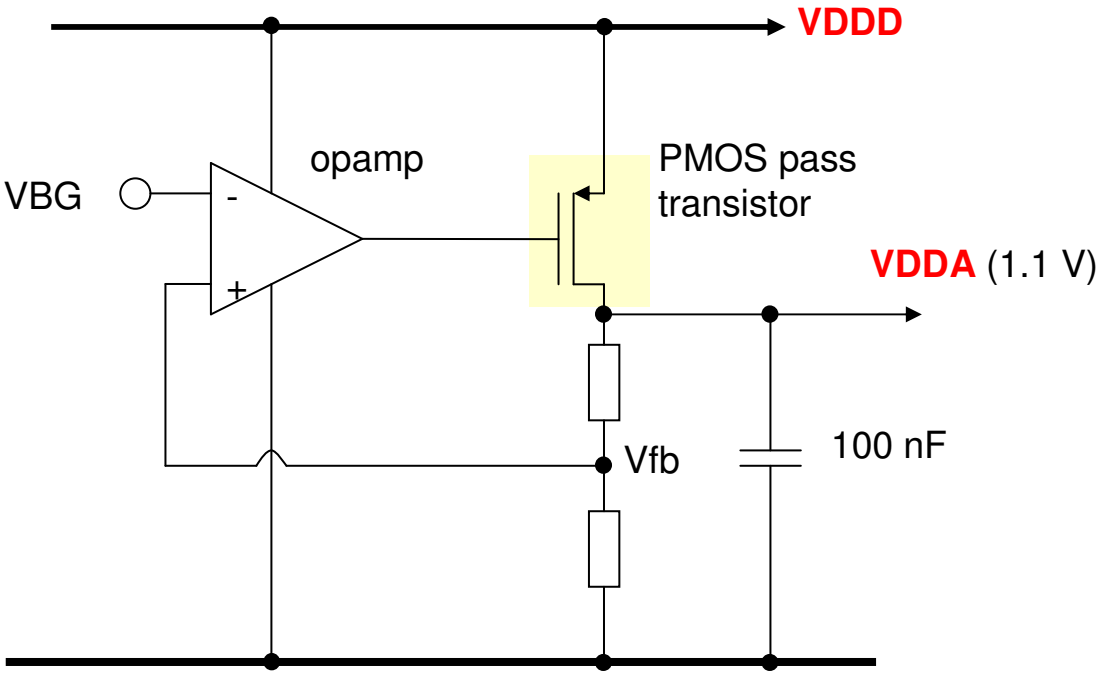
ignoring switched cap DC-DC

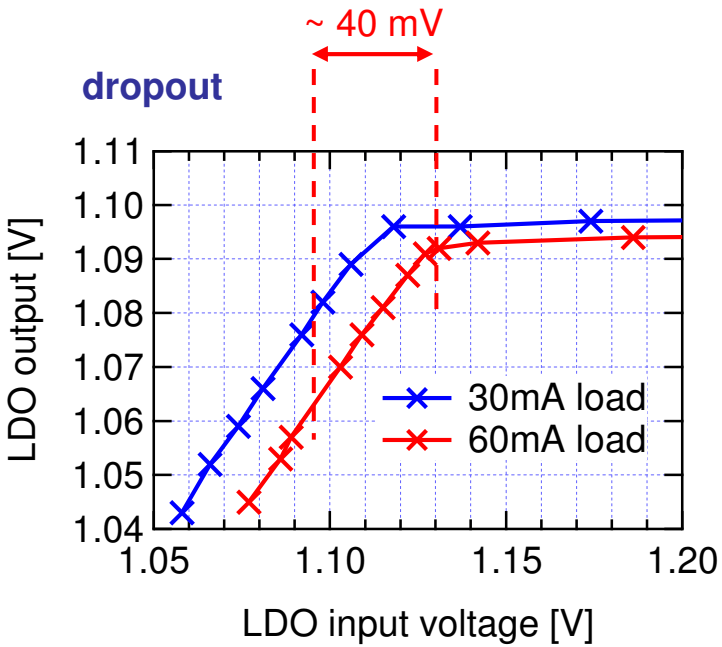
how low can VDDD go?

have to accommodate dropout

have to allow for variations in VBG

have to supply minimum acceptable voltage level for VDDA





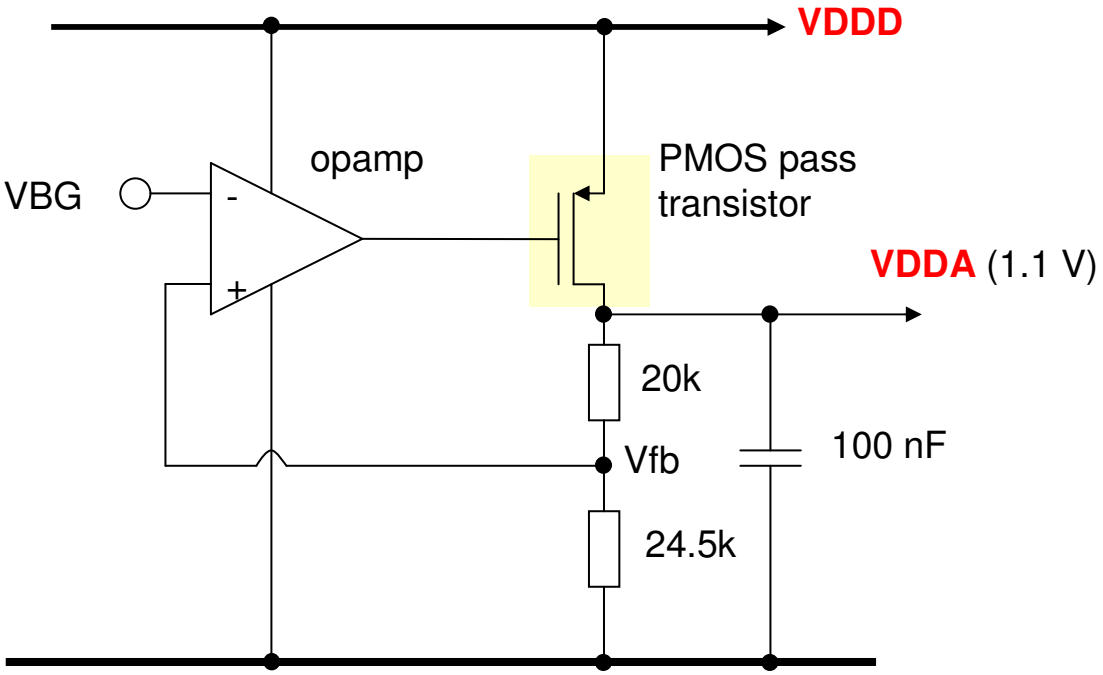
VBG tolerance

VBG measurement data provided

619mV +/- 7.4 mV rms

taking +/- 3 sigma as limits

619 +/- 22 mV (597 - 641)mV

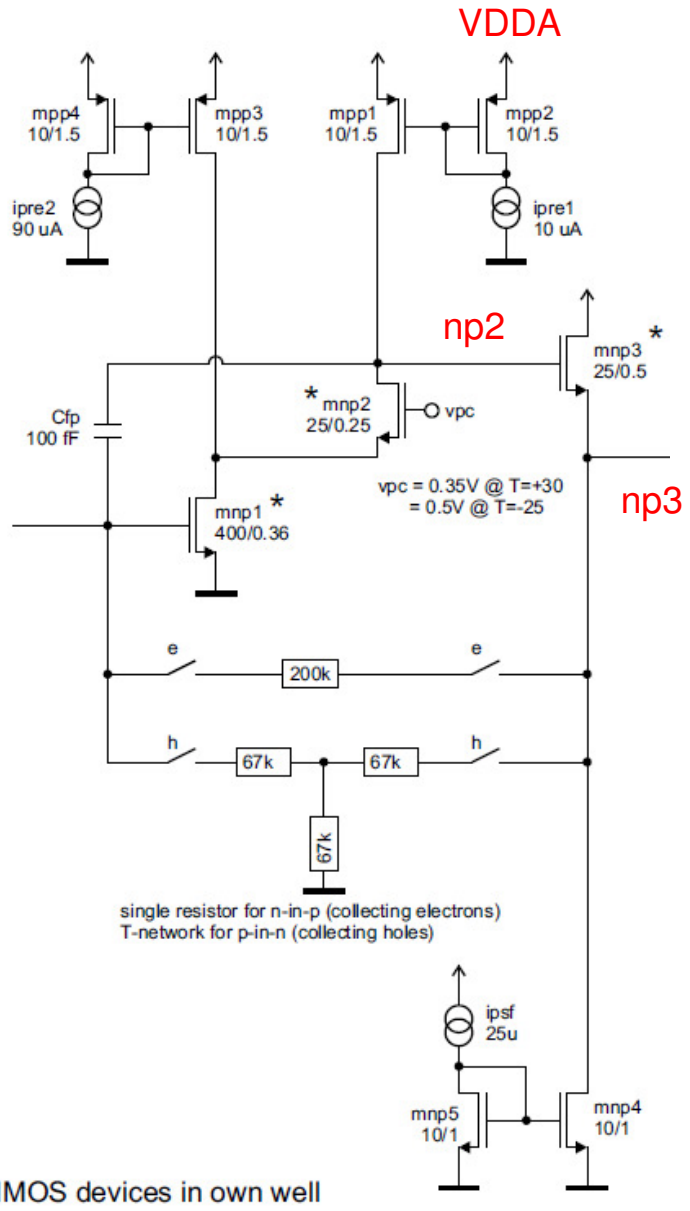


VDDA = 1.82 x VBG
= 1.09 - 1.17 (slightly oversized to allow for series resistance at LDO output)

so VDDD of 1.2V minimum is just about ok (actually a bit marginal)

anything less and LDO will not work correctly

but could analogue stages work at lower VDDA?



design simulation conditions:

+40 -> -40 temperature range

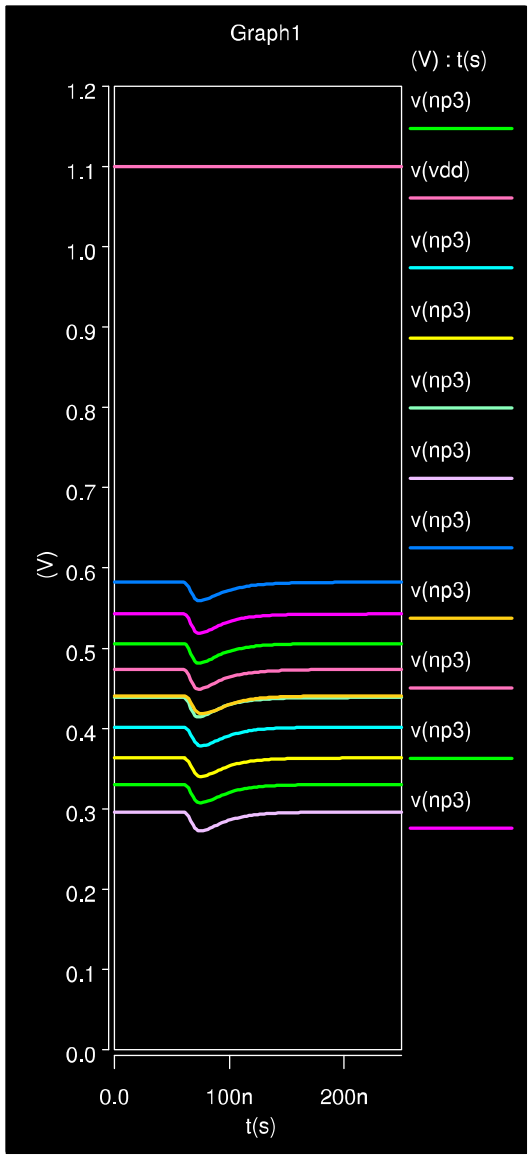
$|I_{LEAK}|$ = 0 -> 1 uA

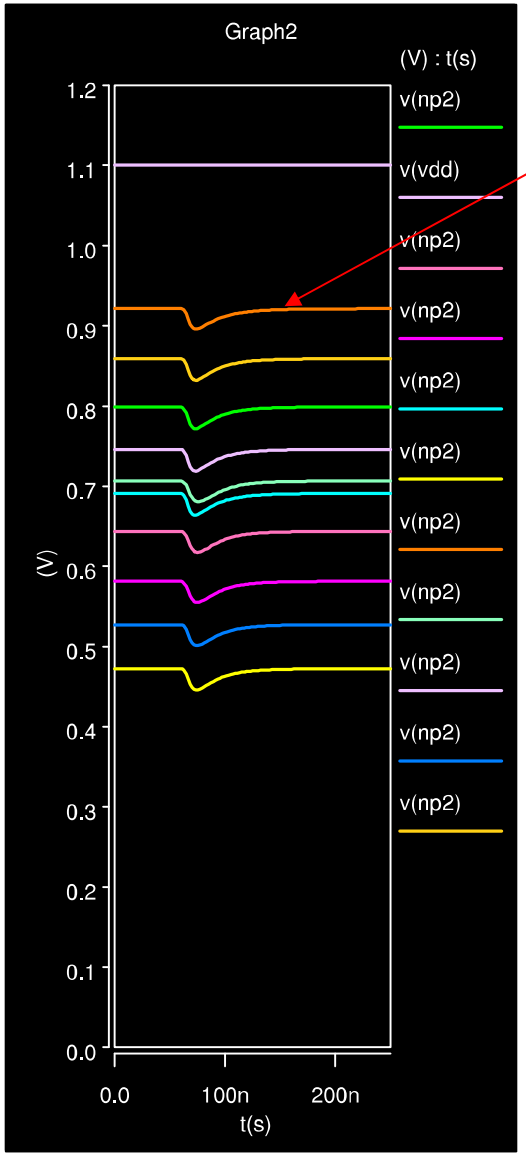
all process corners

TT, FF, SS, FS, SF

goal to achieve a very robust design

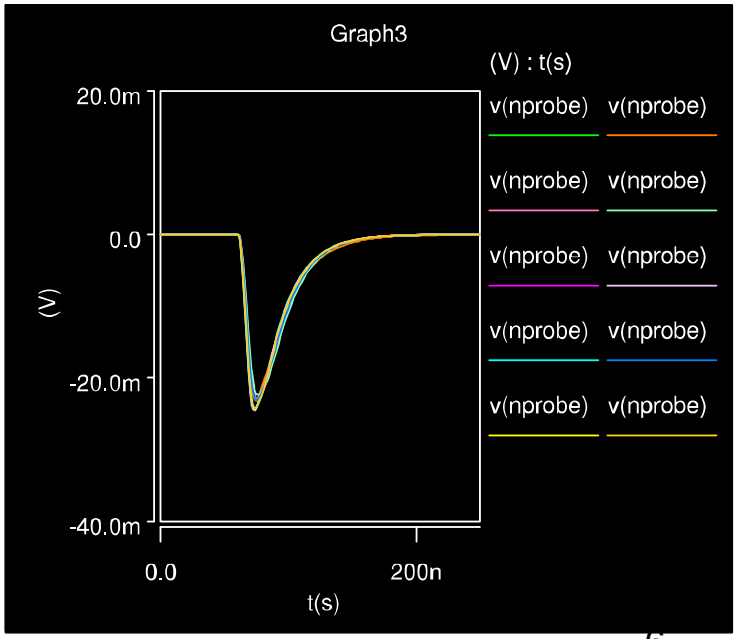
VDDA = 1.1V



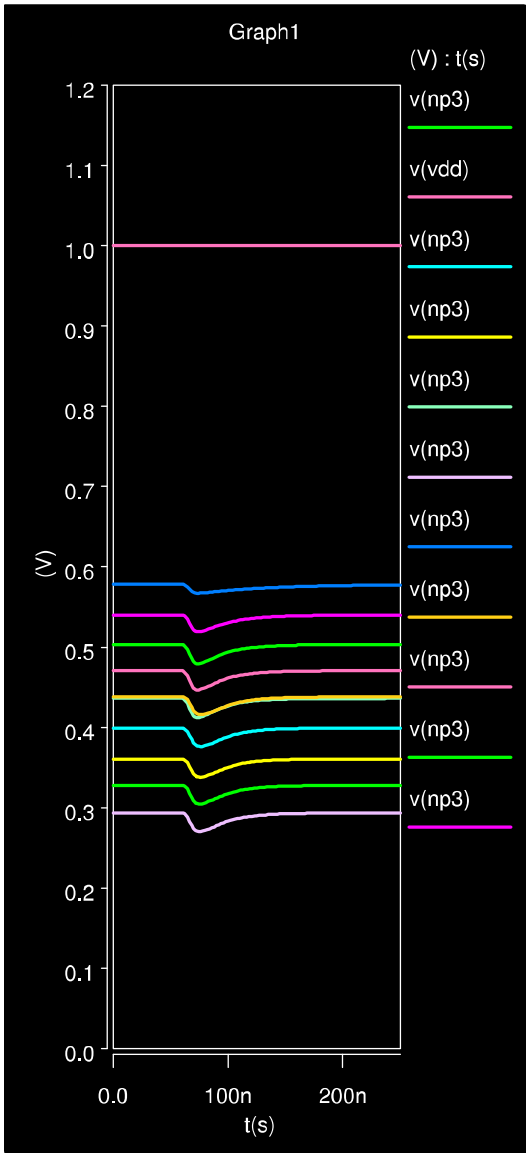


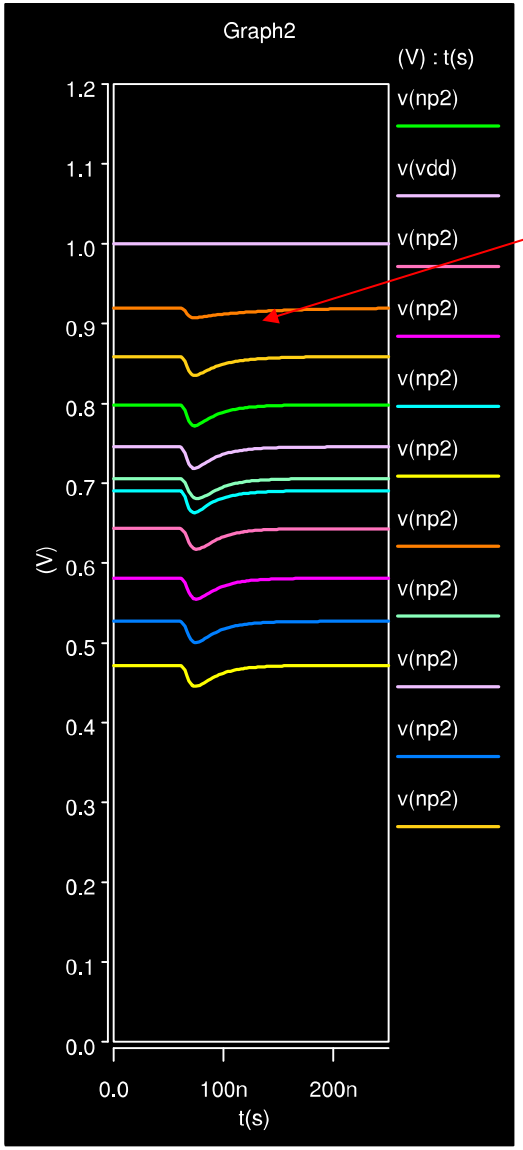
worst case is holes mode
I_{LEAK} = 0
T = -40
SS corner

but OK here for VDDA = 1.1V



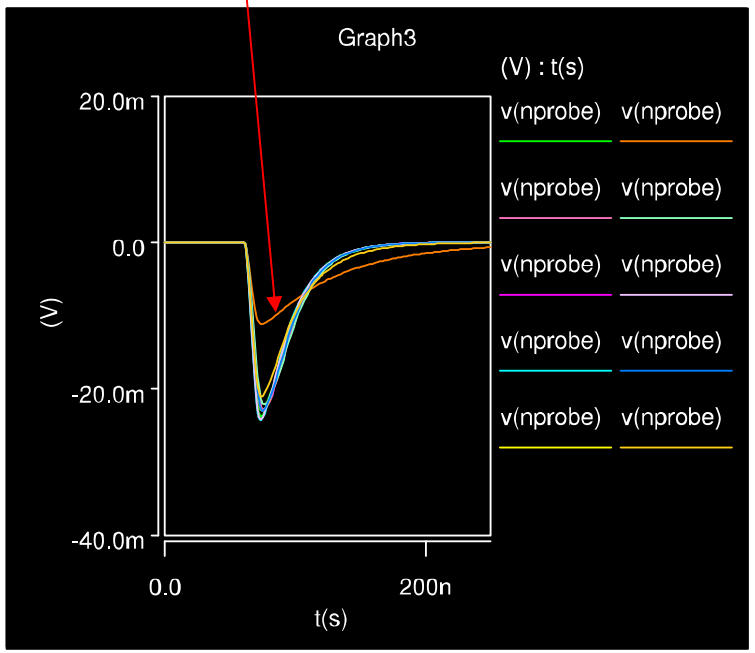
VDDA = 1.0V



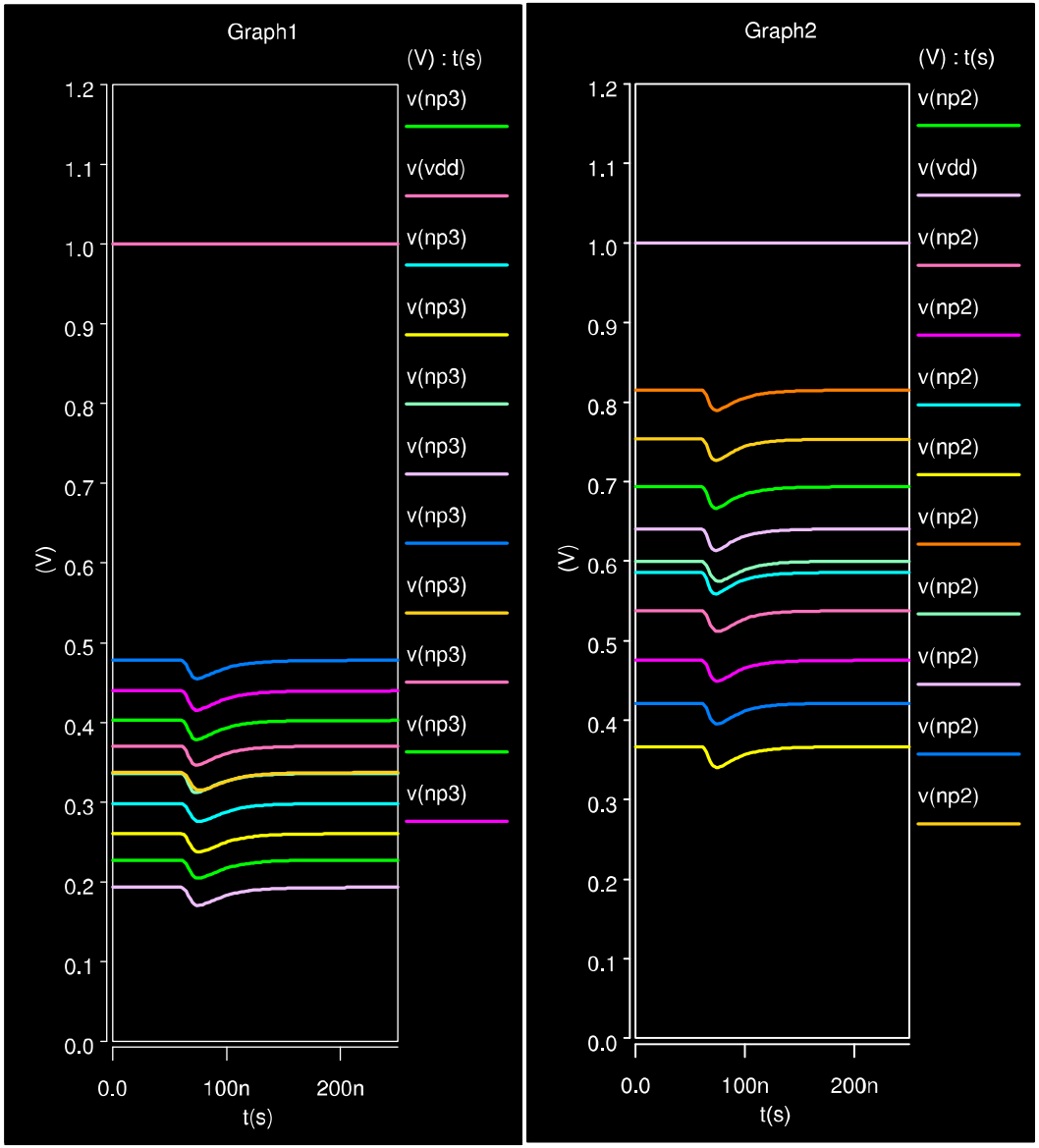


problem arises at node np2
too close to VDDA

holes mode
I_{LEAK} = 0
T=-40
SS corner

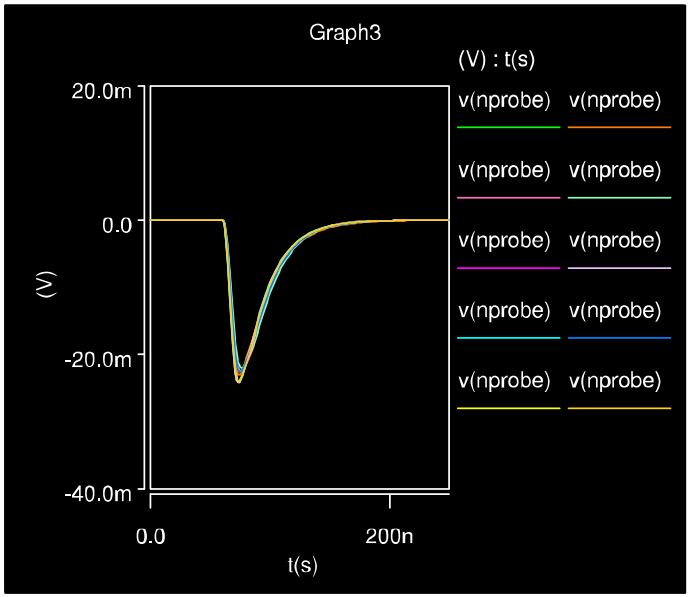


VDDA = 1.0V



goes away with leakage
as DC level decreases

I_{LEAK} = 0.5 uA



what to do?

tweak analogue design to run at 1.0V and adjust LDO?
- can try again, but no guarantee of success
- (spent some time looking at this in original design phase)

would like to avoid major modifications to front end if possible

adjust LDO for 1.0 V and hope we don't see the problem?
- probably unlikely to see this process corner?

impose additional constraints on other parts of system?
- e.g. insist on sensor AC coupling?

some final thoughts

are we doing the right thing trying to force two technologies to the same supply?

forces 65nm chips to high end of operational range

1.2 +/- 5% rather “fine tuned”

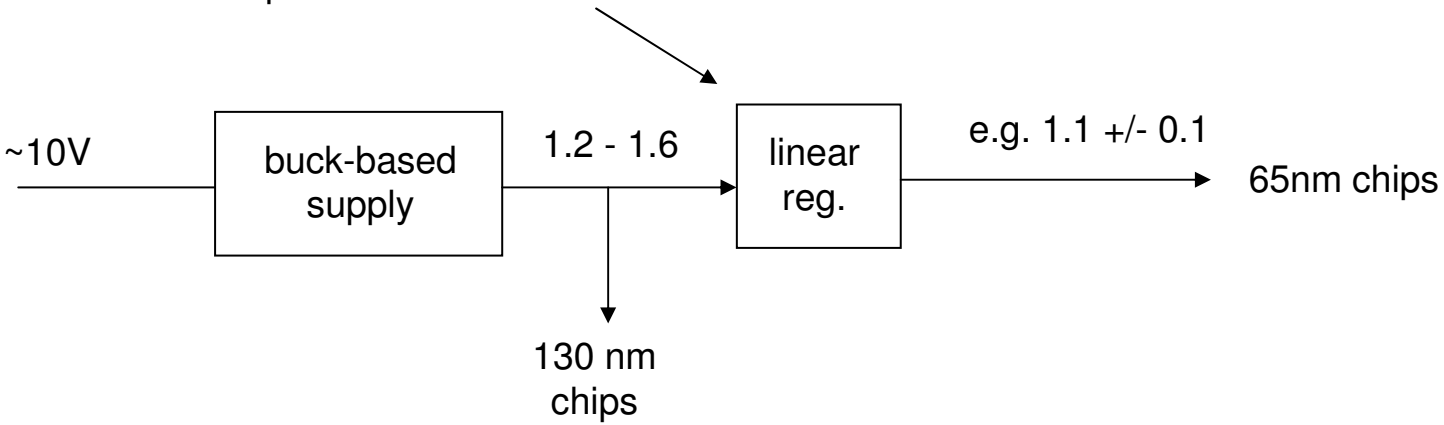
maybe over-constrains power supply design?

could derive 65nm rail from 130nm rail?

removes restriction on 130nm supply & increases tolerances

offers some protection to 65nm chips (& can also increase tolerance)

but have to provide this device



what about ripple on 1.2 +/- 5% ?

i.e. will the lower limit be less than 1.14 (1.14 +/- some level of ripple) ?