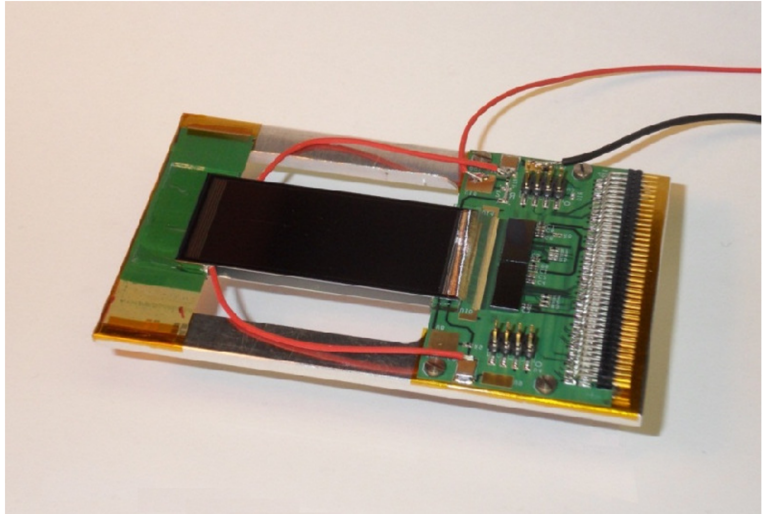
mini-module characterization



2 mini-pT modules exist

results presented last systems meeting (June 18th) showed:

lower noise & faster signals from upper sensor
higher noise, slower signals from lower sensor
=> higher capacitance
results mainly from module #2

since then:

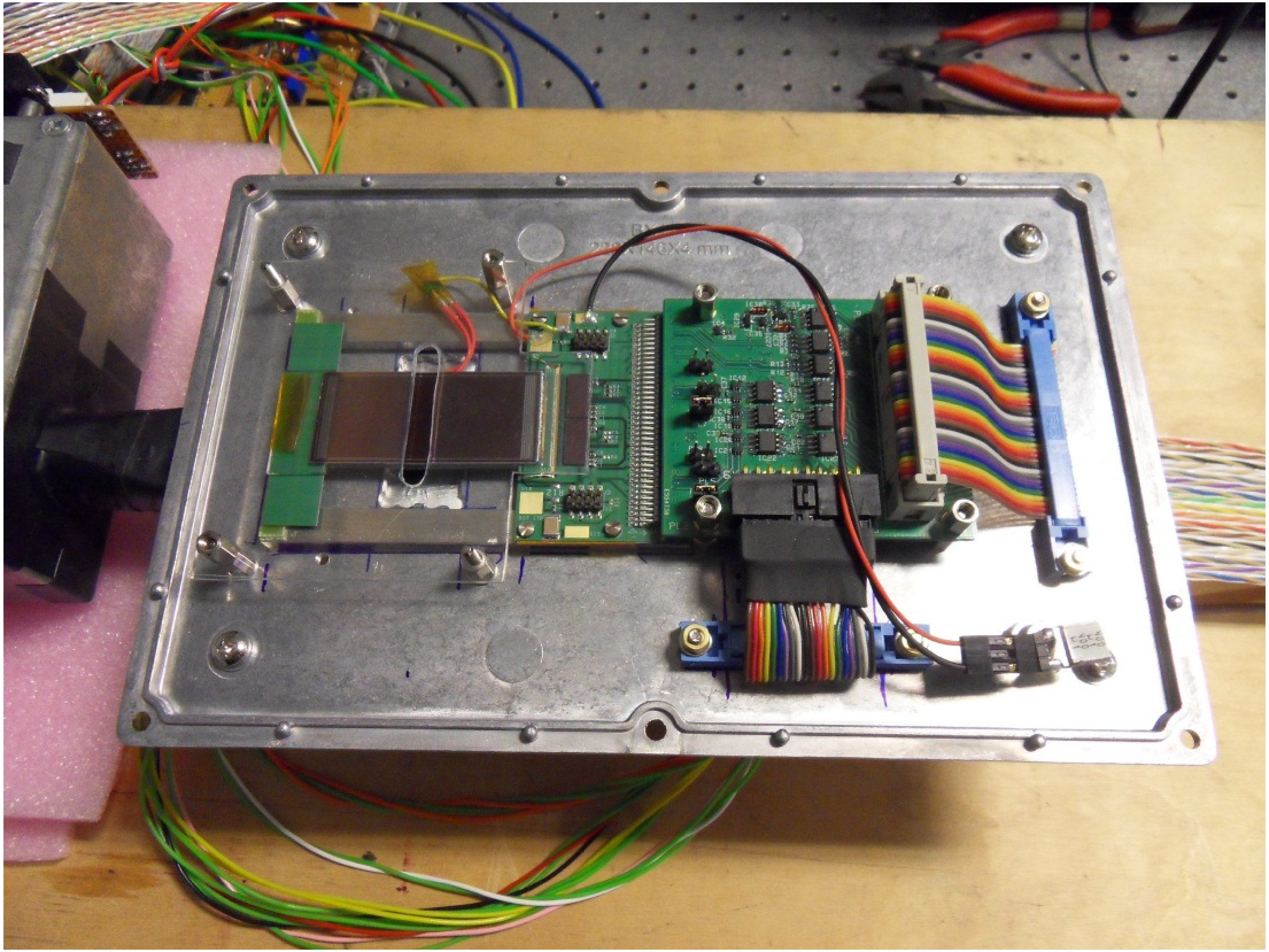
have made a study of both modules looking in more depth at effect of sensor bias
have made some progress in understanding origins of bad channels
have had one interim Vidyo meeting - 26th July
actions (for me) from that meeting now complete
(some results already circulated by e-mail)

not much new today - will use today to draw all information together in one talk
(not everyone participated in interim meeting)

re-cap slides from last time (June 18th)

mini-module test setup

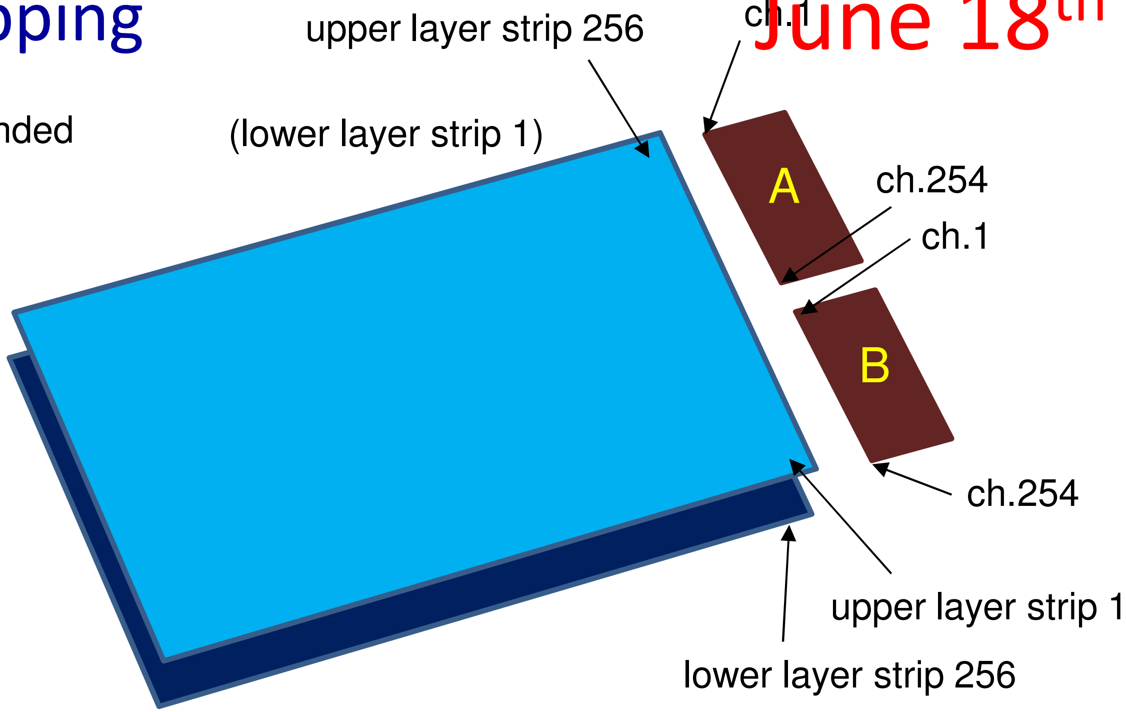
June 18th



channel to strip no. mapping

June 18th

2 edge channels on each sensor not bonded
(i.e. strips 2 - 255 inclusive bonded)



main point to note: lower and upper sensor layer channels feed alternating channels on each chip

chip channel vs. sensor strip #

	chip A									chip B									
	2	4	6	8	.....	.....	250	252	254	2	4	6	....	....	248	250	252	254	
upper sensor	255	254	253	252	.....	....	131	130	129	128	127	126	....	...	5	4	3	2	

	chip A									chip B									
	1	3	5	7	.....	.....	249	251	253	1	3	5	....	....	247	249	251	253	
lower sensor	2	3	4	5	...	....	126	127	128	129	130	131	...	...	252	253	254	255	

s-curves

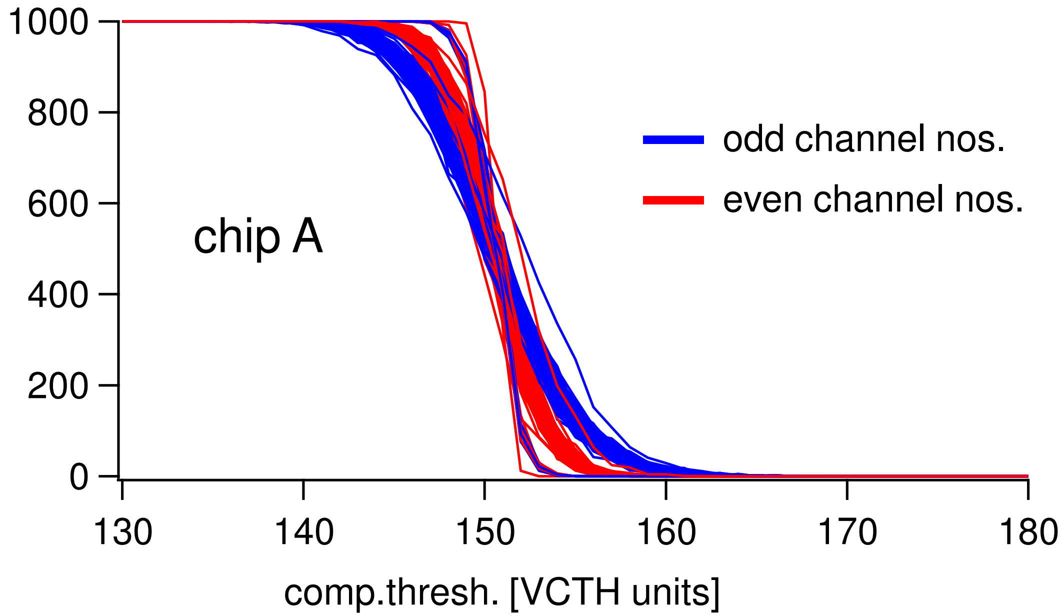
June 18th

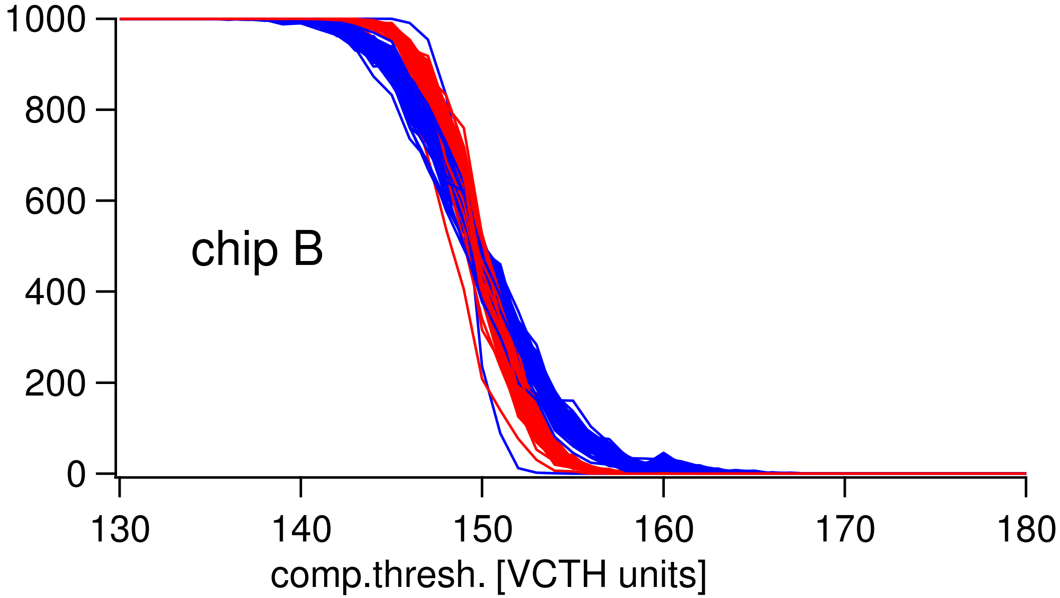
acquired using on-chip test pulse

2 clear families corresponding to odd & even chip channel numbers

odd CBC channels show more "stretched out" s-curves
=> higher noise

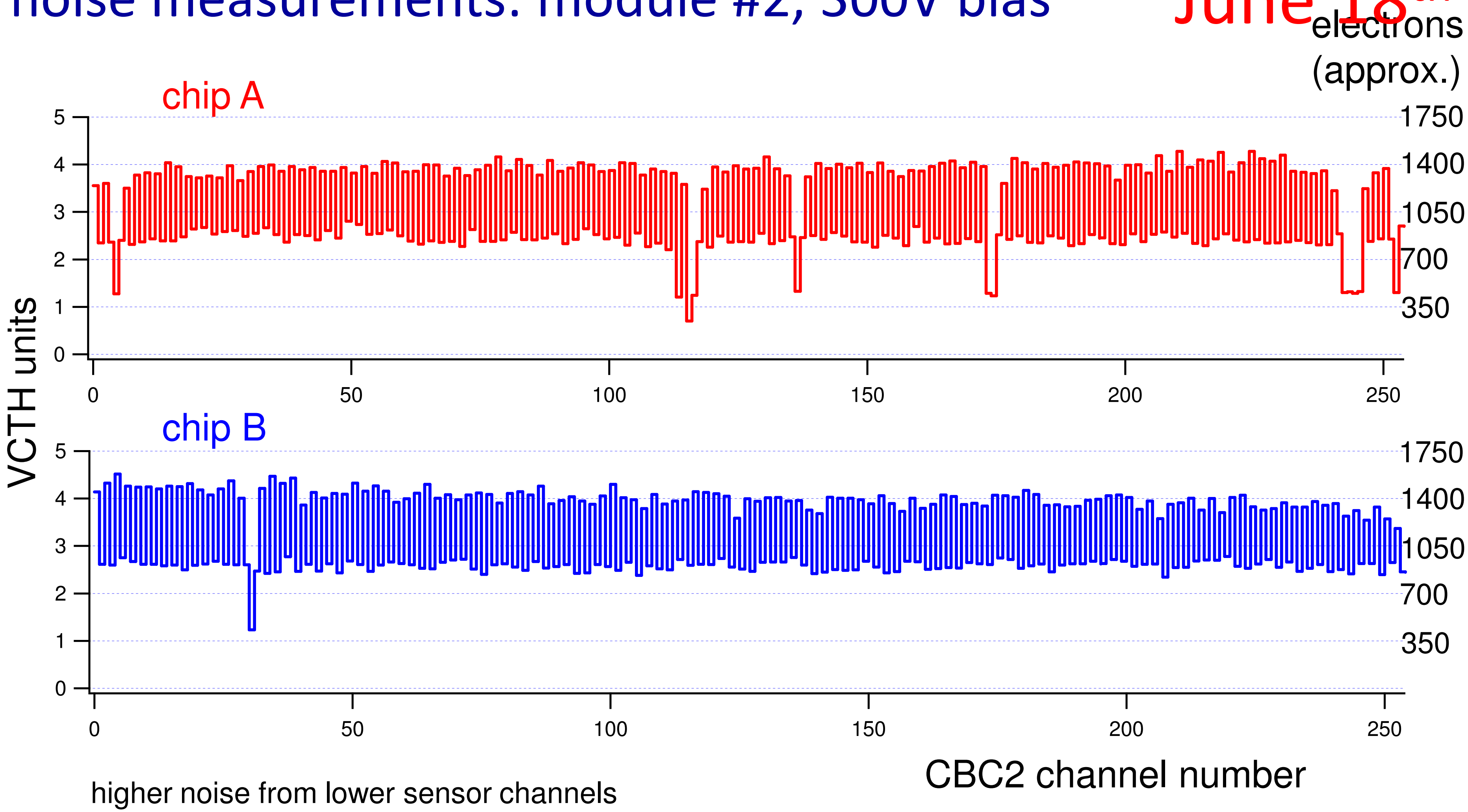
odd channels correspond to lower sensor





noise measurements: module #2, 300V bias

June 18th

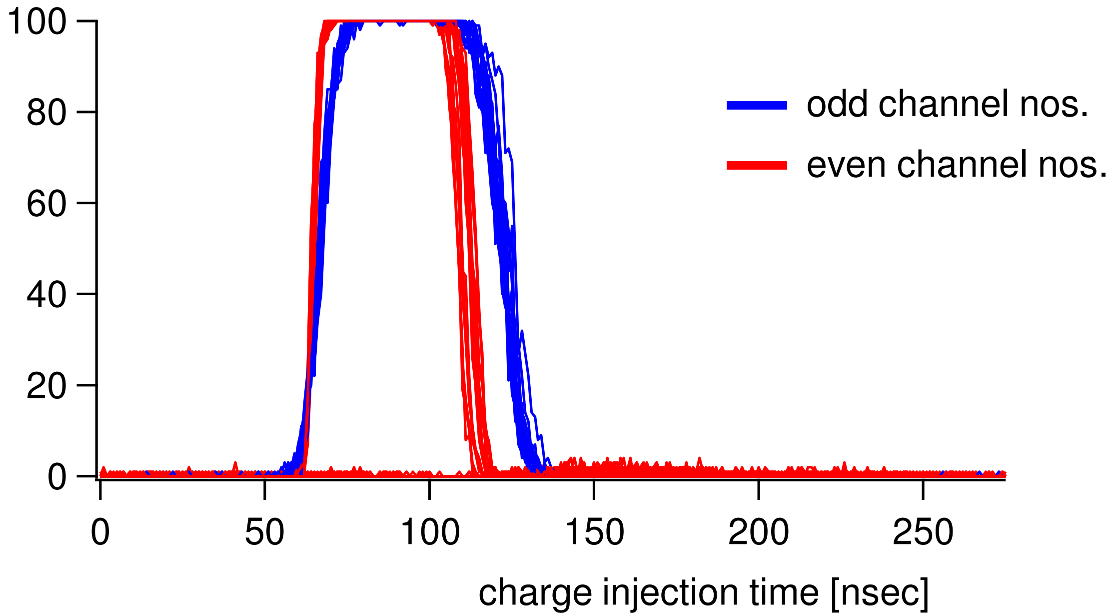


higher noise from lower sensor channels
not clear why

no explanation for anomalously low noise channels either
would seem to indicate no sensor-to-hybrid contact ← NO - see later

test pulse charge injection time sweep

June 18th



slower edge times for odd channels (lower sensor) => slower pulse shape => higher capacitance

consistent with higher noise

seems to indicate lower sensor not properly depleted? ← NO - see later

note: other module not studied in such depth
but shows broadly similar results ← bit different - see later
significant?

conclusions from June 18 meeting

sensor behaviour on modules not clearly understood

results presented for 300V bias

suggestion to vary bias over wider range - might shed some light

recap slides from Vidyo meeting- 26/7/13

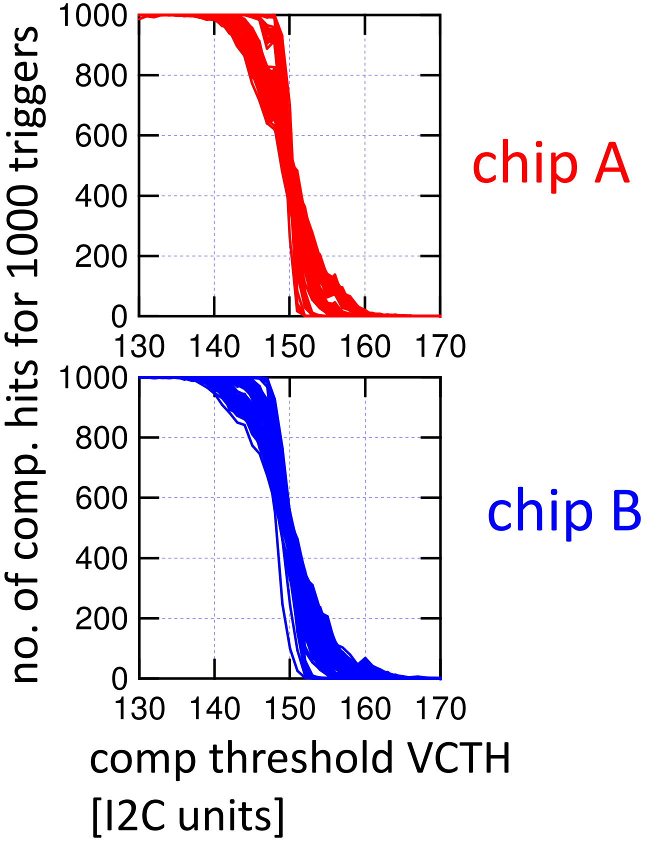
study of both modules looking in more depth at effect of sensor bias

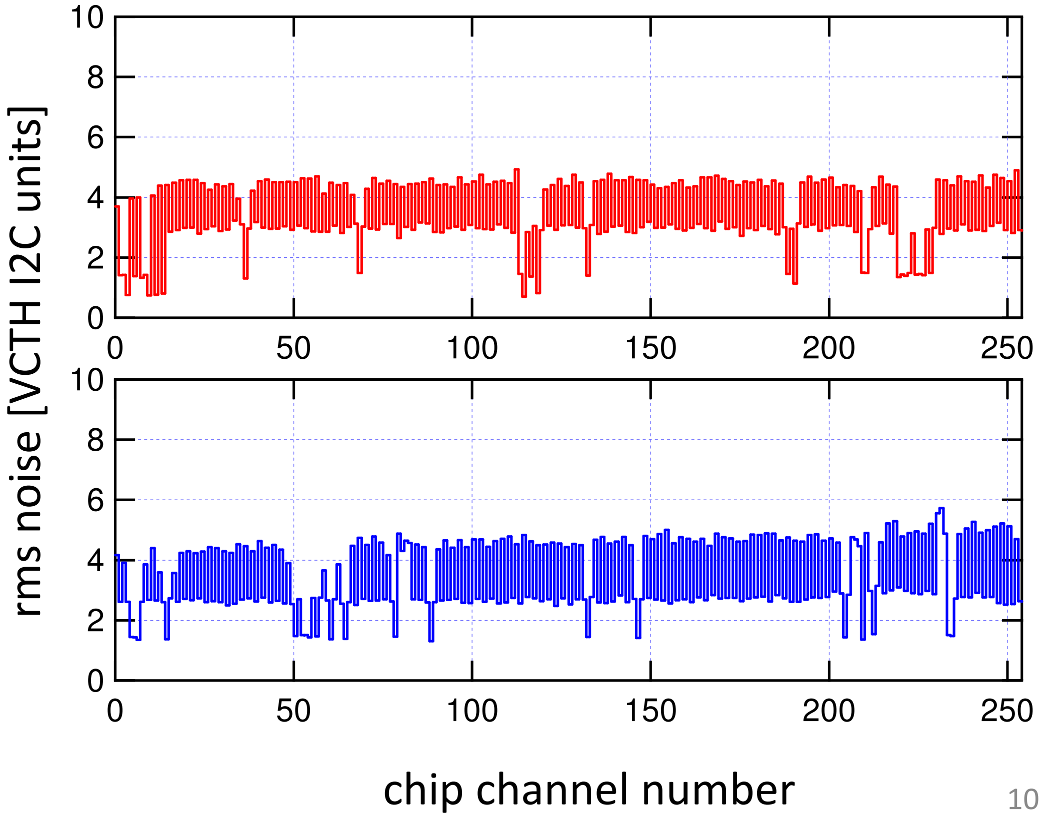
progress in understanding origins of bad channels

noise vs. sensor bias: experimental method

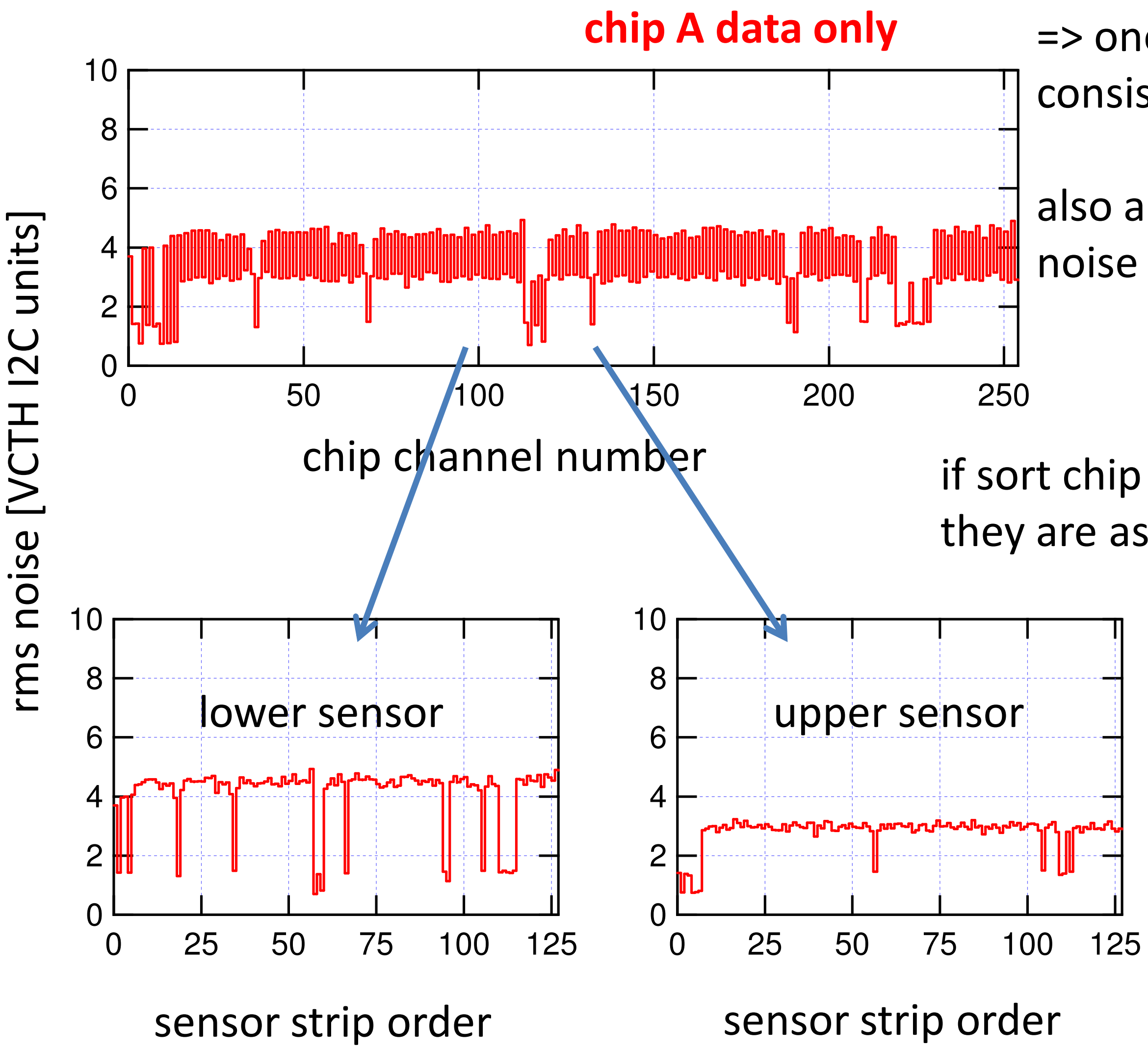
- tune offsets for all channels to centre s-curve mid-points at same value (150) for test pulse amplitude ~ 1 fC
- s-curves acquired by sweeping global comparator threshold parameter VCTH
- fit to s-curve raw data allows noise to be extracted (rms VCTH I2C units)

example result from module #1, 50V bias





sorting the noise



alternating high/low noise values
=> one sensor (lower one) giving consistently higher noise than other

also a significant number of low noise channels

if sort chip channels by sensor with which they are associated, then systematic difference between each sensor becomes clearer

for this module (#1), at **50V** bias, the lower sensor channels show higher noise

leakage behaviour for both modules

mini-module#1

bias [V]	leakage [uA]
20	1.02
50	2.6
100	6.1
200	16.4
300	35
400	60

mini-module#2

bias [V]	leakage [uA]
50	0.28
100	0.56
200	1.3
300	2.5
400	5.6
500	13.8
600	39.3

tables show leakage (both sensors) dependence on bias

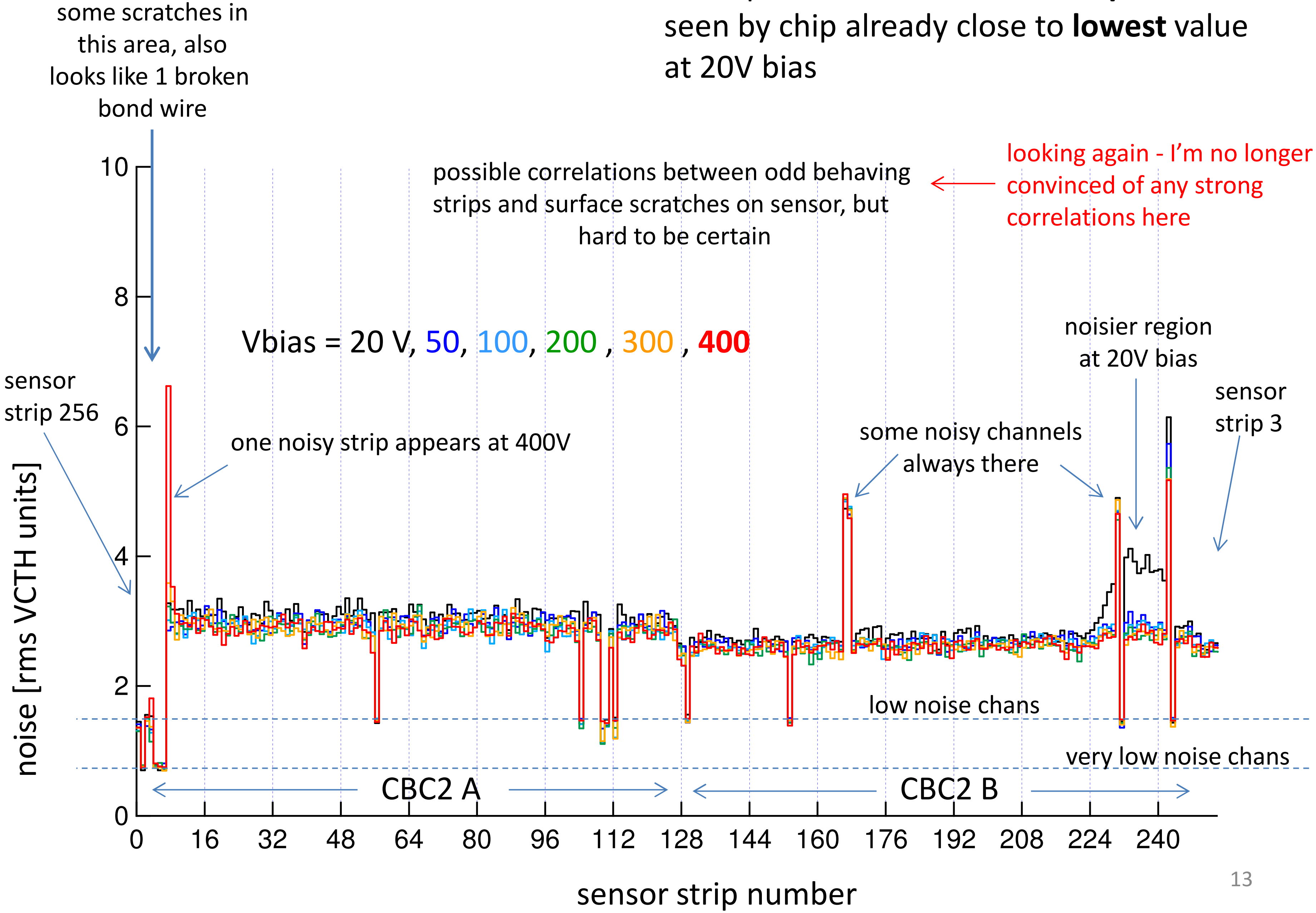
bias voltage taken to a level where noisy channels start to appear

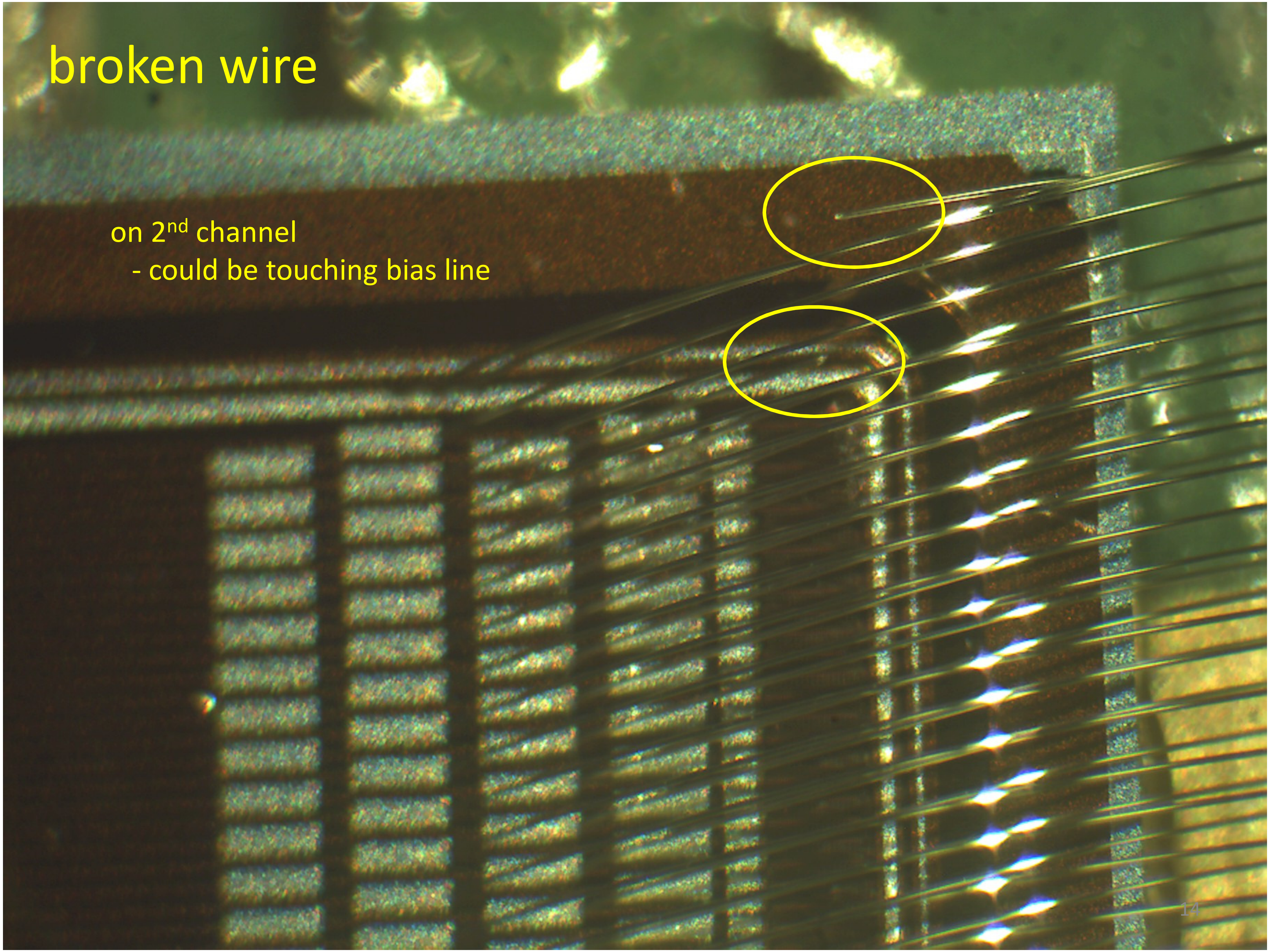
will only show noise sorted by sensor , for each module

note: one chip only now working on module#2. CBC2B got damaged when probing sensor to verify bias voltage getting through to strips (not sure how it happened)

mini-module#1: upper sensor

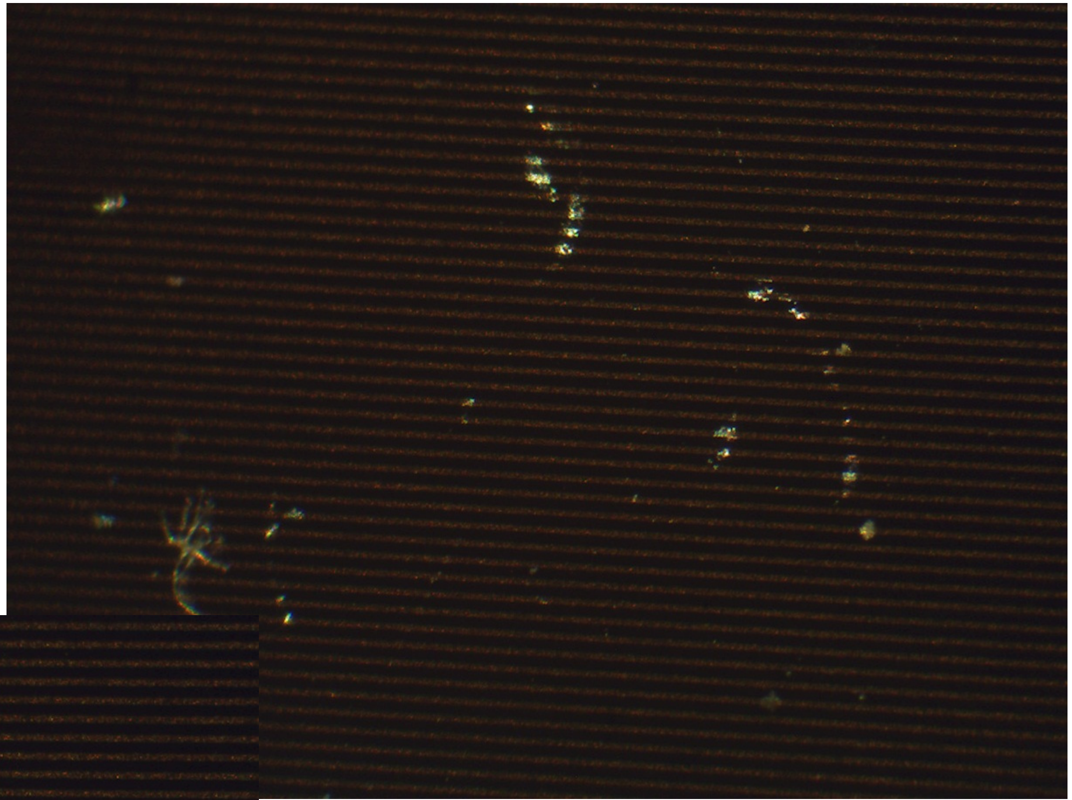
noise performance vs bias => **capacitance** seen by chip already close to **lowest** value at 20V bias

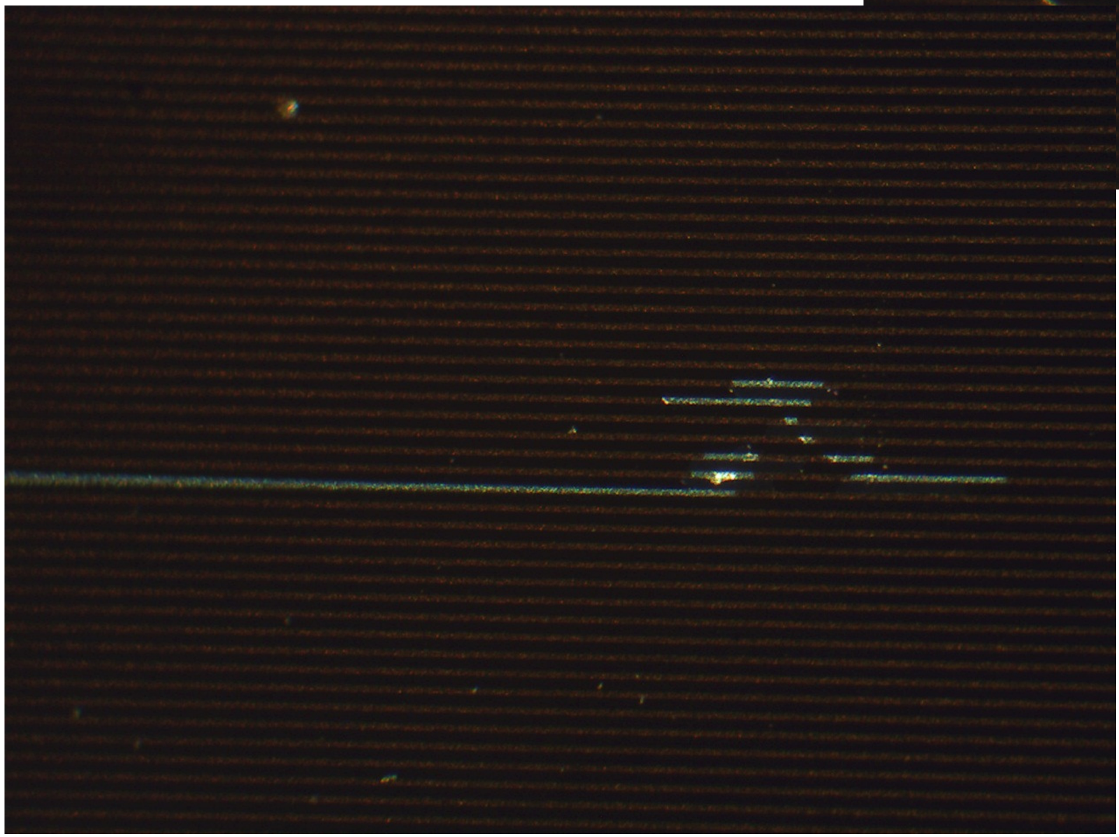



broken wire
on 2nd channel
- could be touching bias line
14

surface scratches

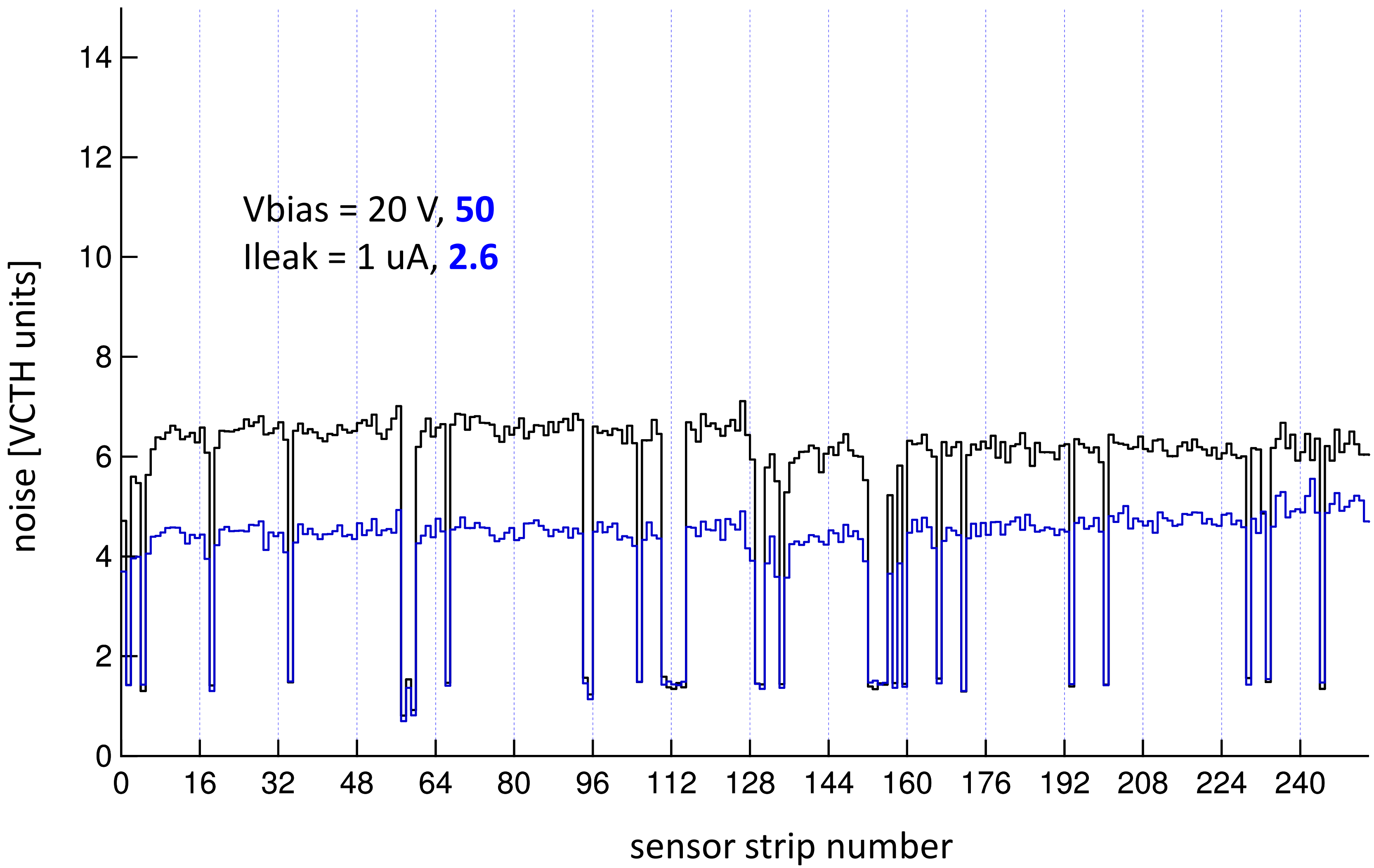
but **not** so obvious correlation with problem channels
(previously thought there was)



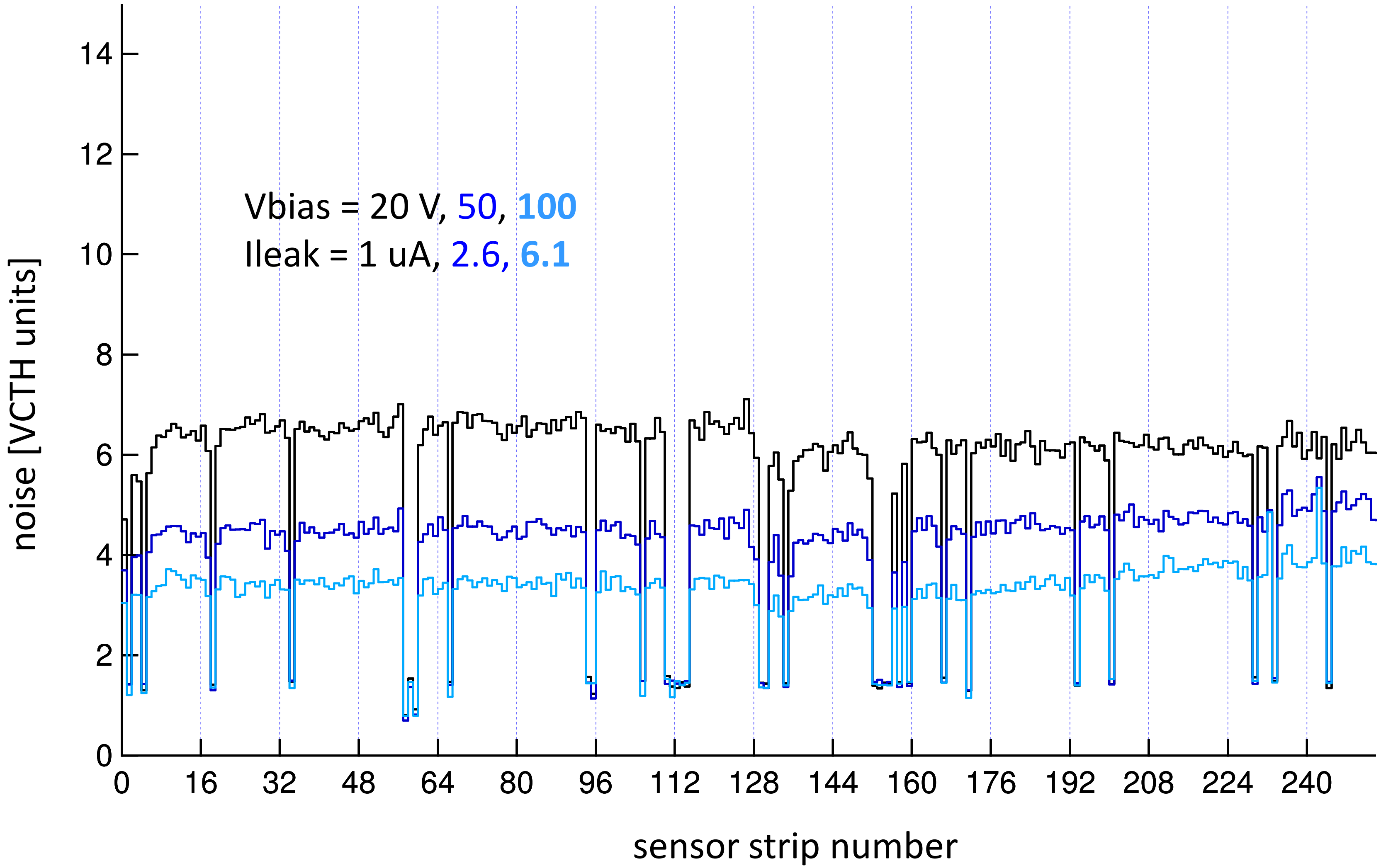


mini-module#1: **lower** sensor

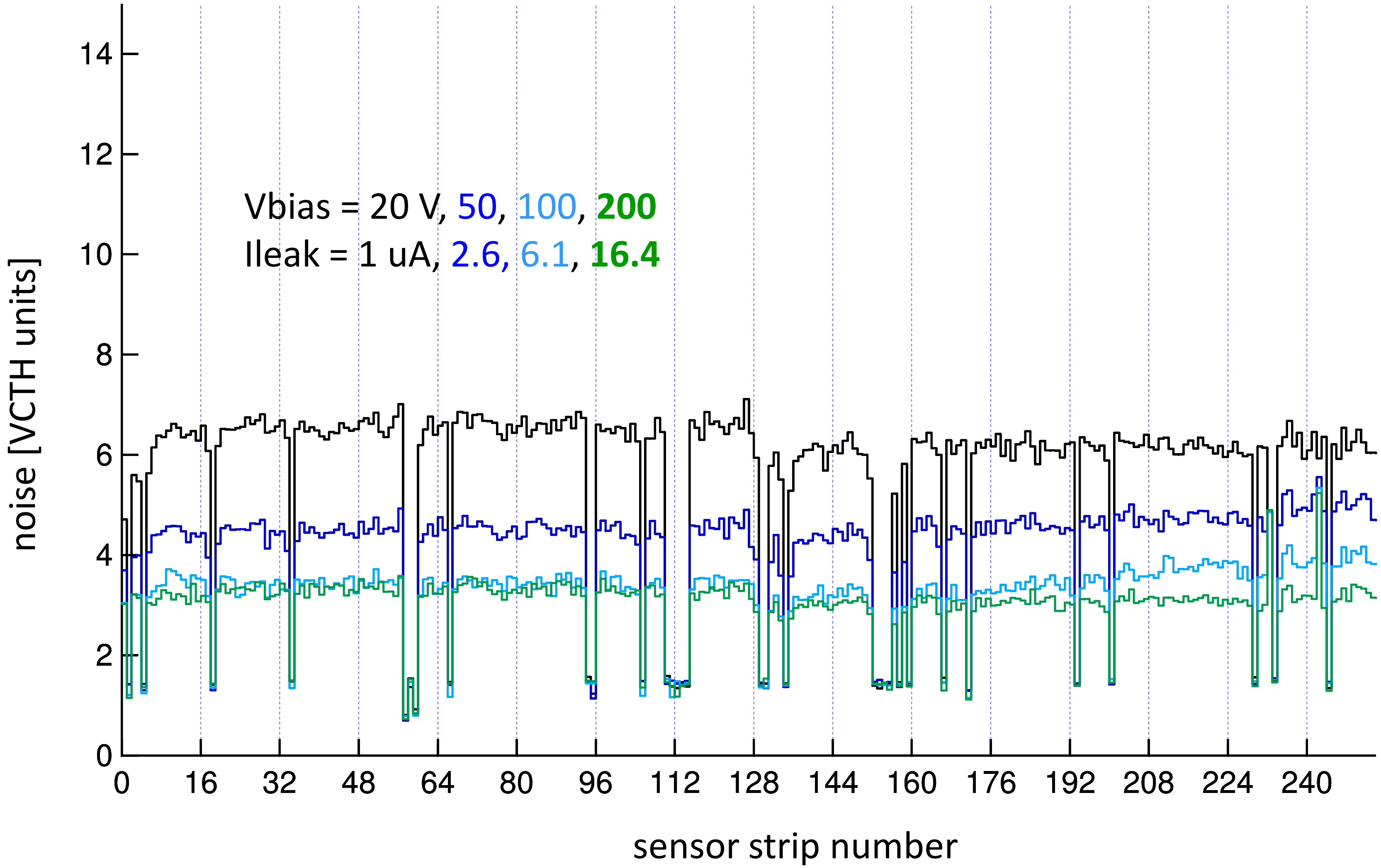
sorting noise data by sensor strip number: lower sensor, 20 & 50V



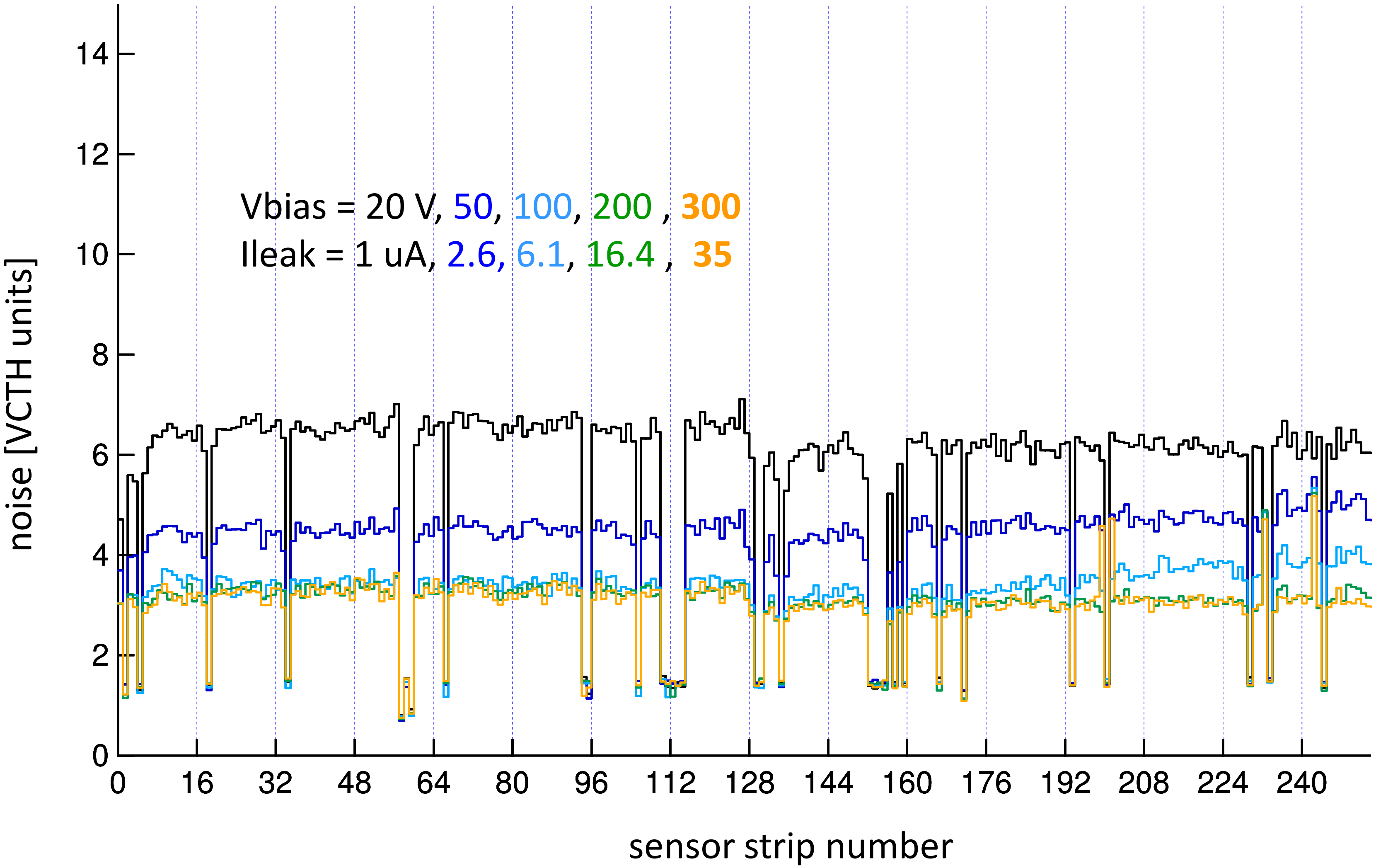
mini-module#1: **lower** sensor



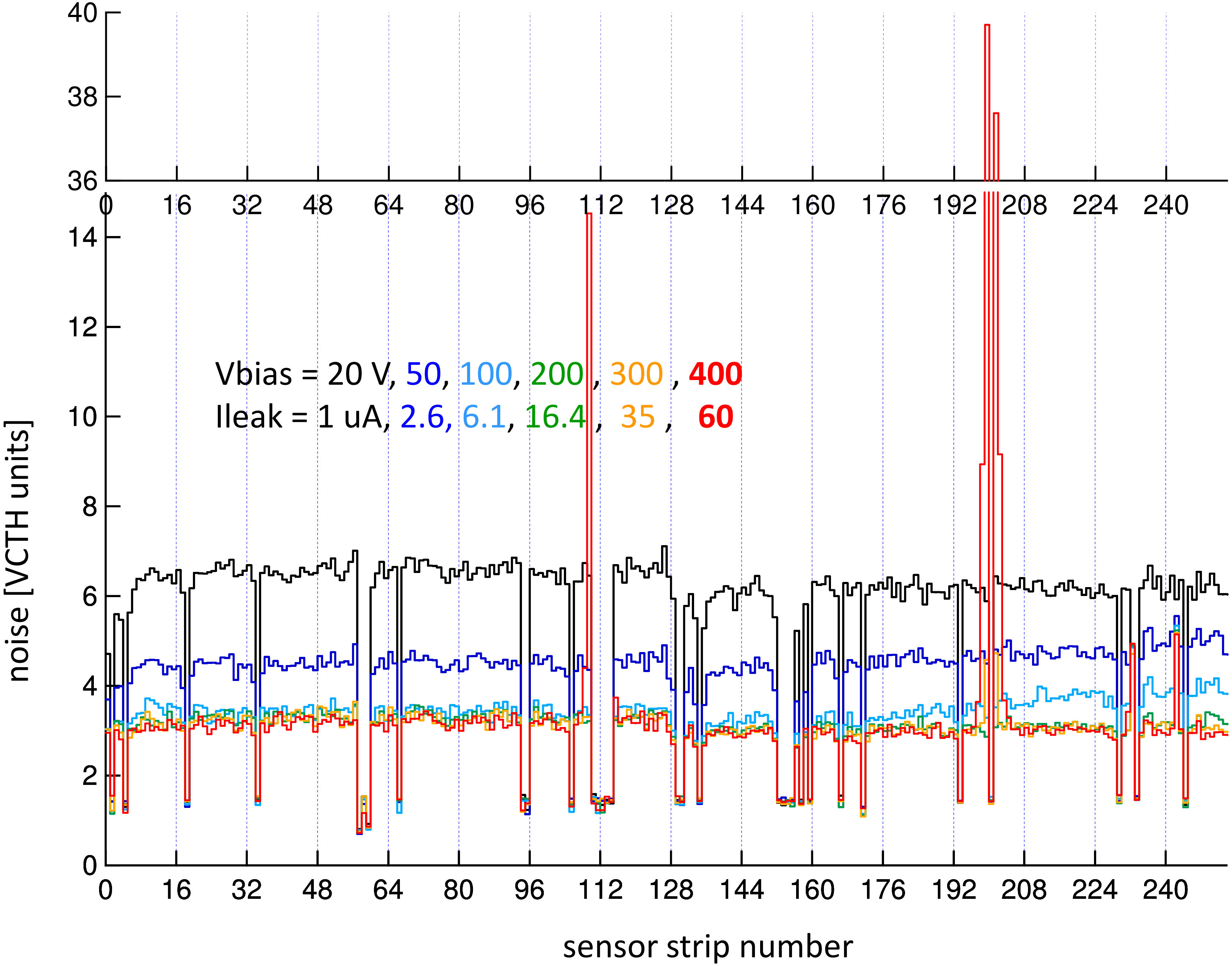
mini-module#1: **lower** sensor



mini-module#1: **lower** sensor

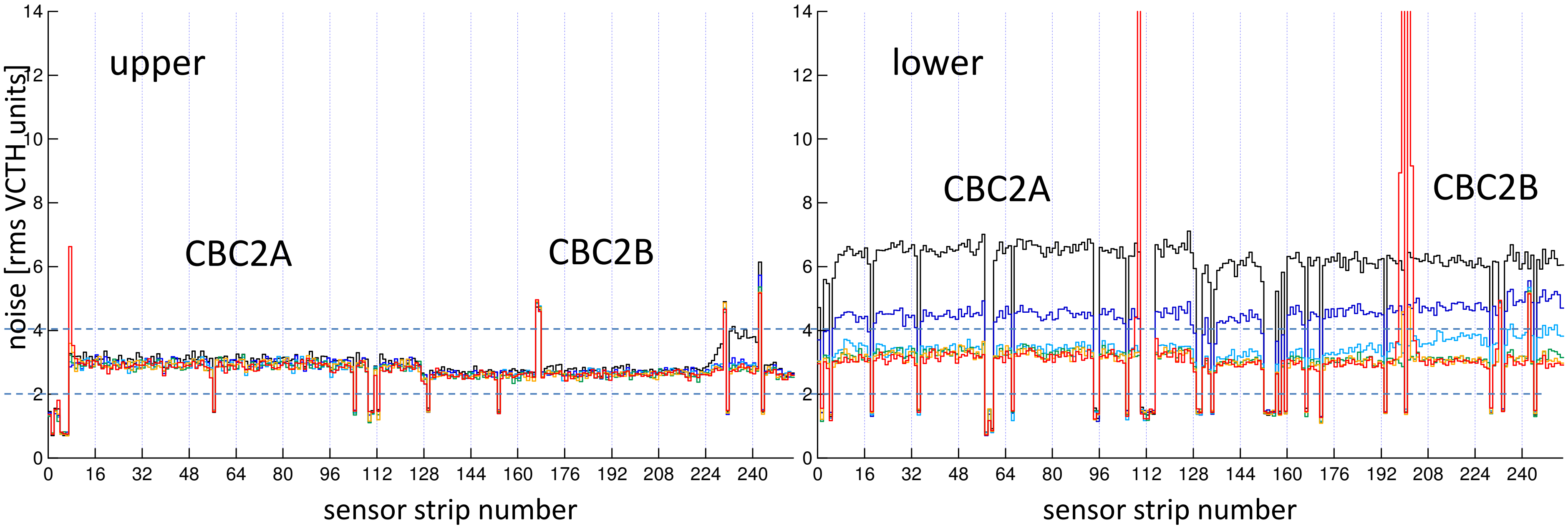


mini-module#1: lower sensor



comparison of two sensors on mini-module#1

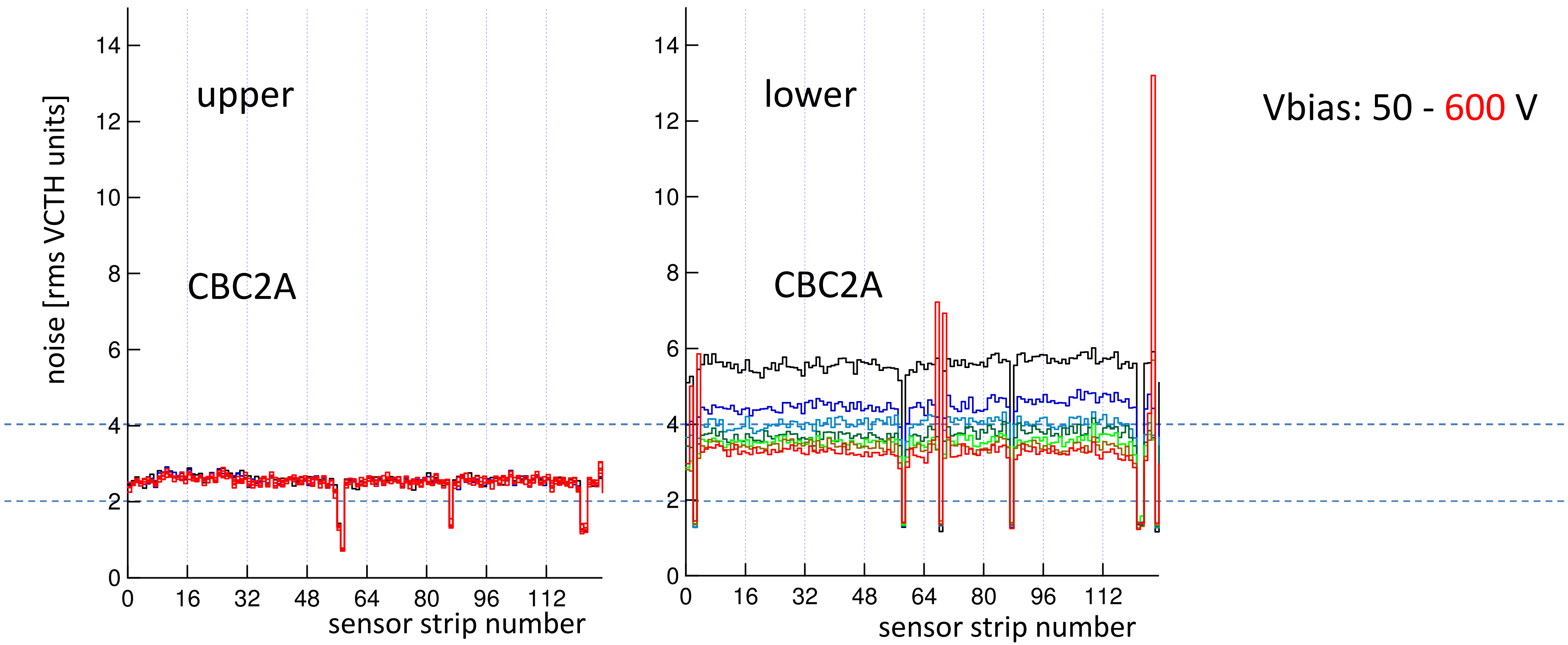
Vbias: 20 - 400 V



lower sensor noise needs higher bias (>100V) before reaching minimum value

but final levels ~same - lower and upper (slightly higher on lower)

comparison of two sensors on mini-module#**2**



similar behaviour, but lower sensor doesn’t get to as low levels as upper before noisy strips start to develop

summary so far
observations from bias studies - both modules

different dependence of noise on bias

  for both modules the lower sensor needs higher bias

  is this is just a coincidence? ← my preference

    (i.e. not related to some kind of effect of the hybrid)

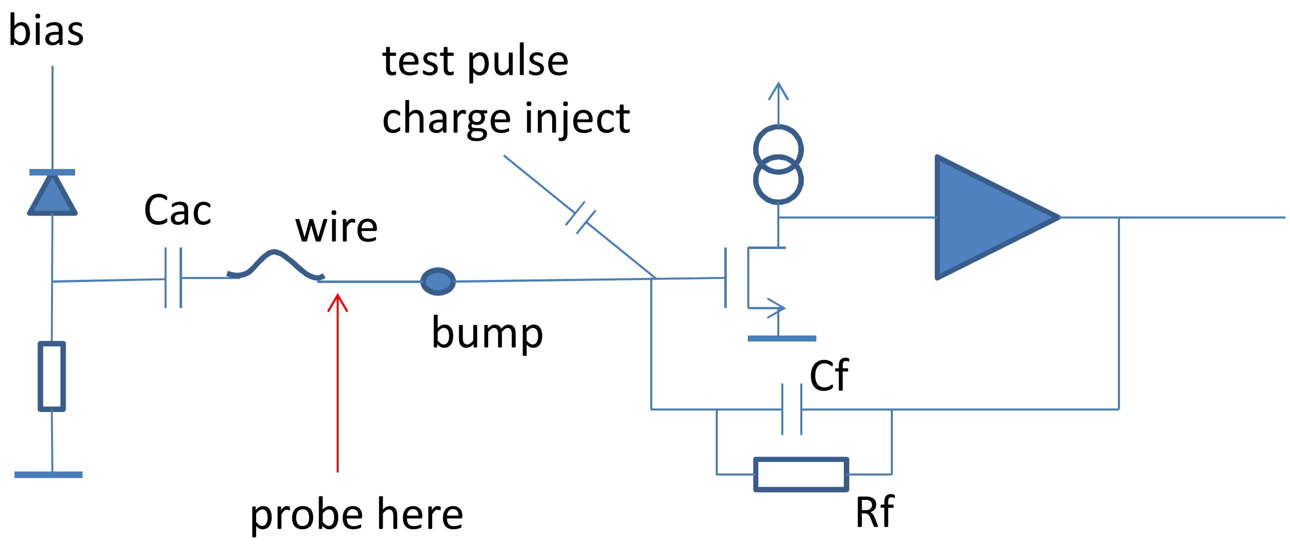
  or something related to the hybrid

    cannot see what this could be

low-noise channels are not affected by the sensor bias - would seem to indicate that they are not connected - but where?

  next few slides will show evidence that failure looks to be at the bump-bond level

investigating low-noise module channels



behaviour observed consistent with failure of connection between strip and amplifier

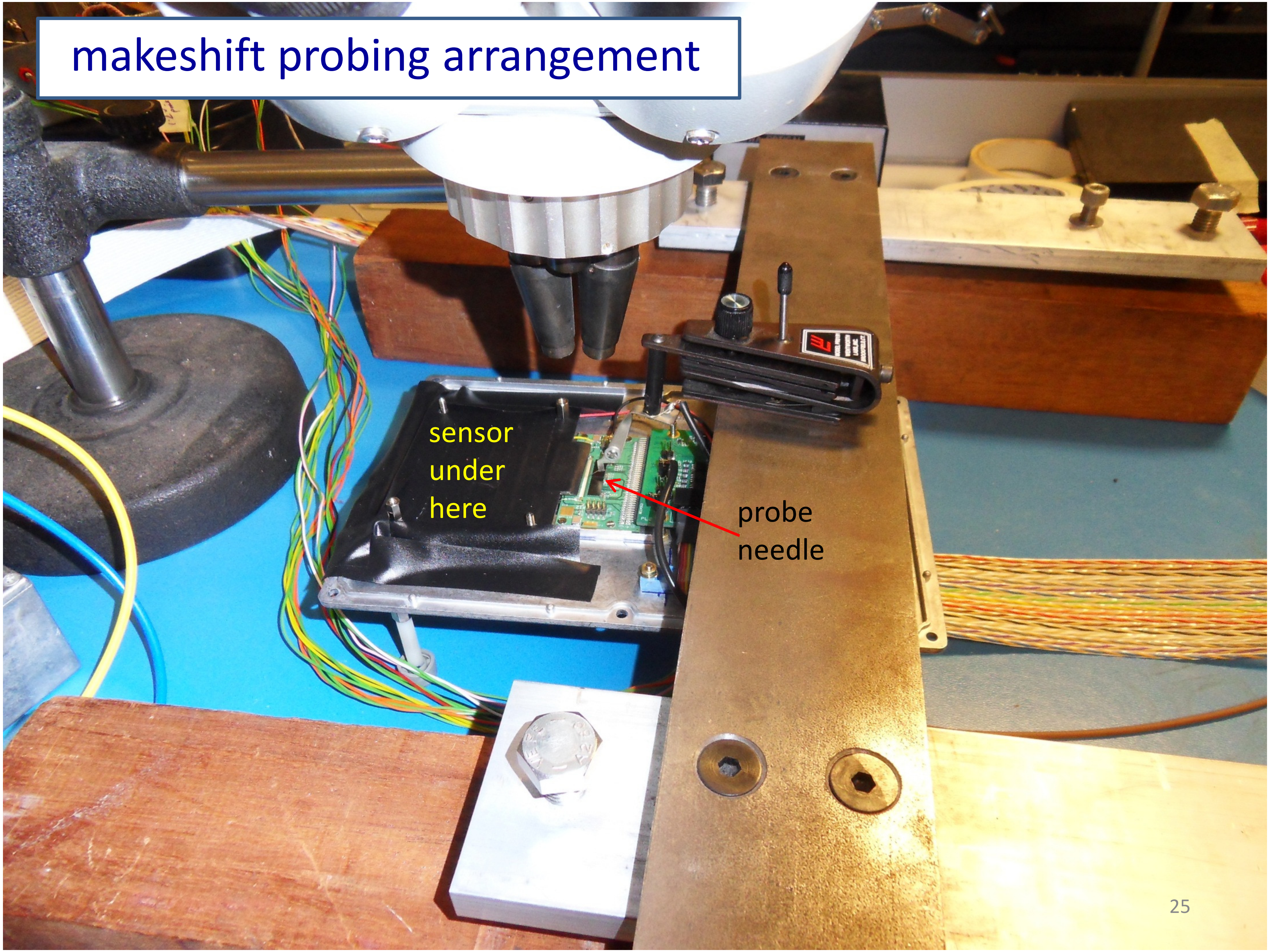
poor wire contact? something wrong with sensor?

failed bump-bond seems the most likely?

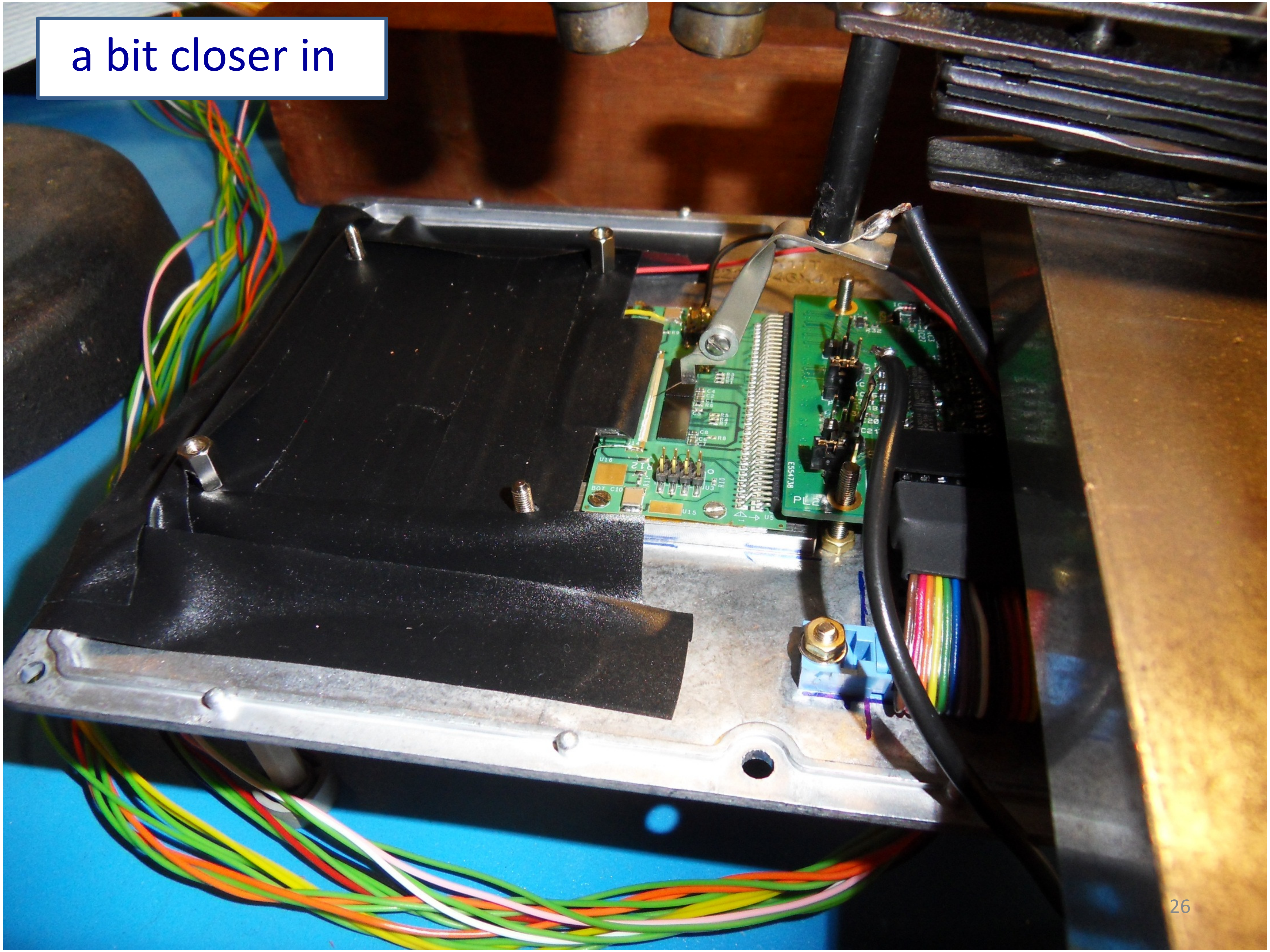
if can place grounded probe on wire-bond pad on hybrid then can switch off input transistor and channel will no longer respond to test pulse

if bump-bond has failed then channel will still respond to test pulse

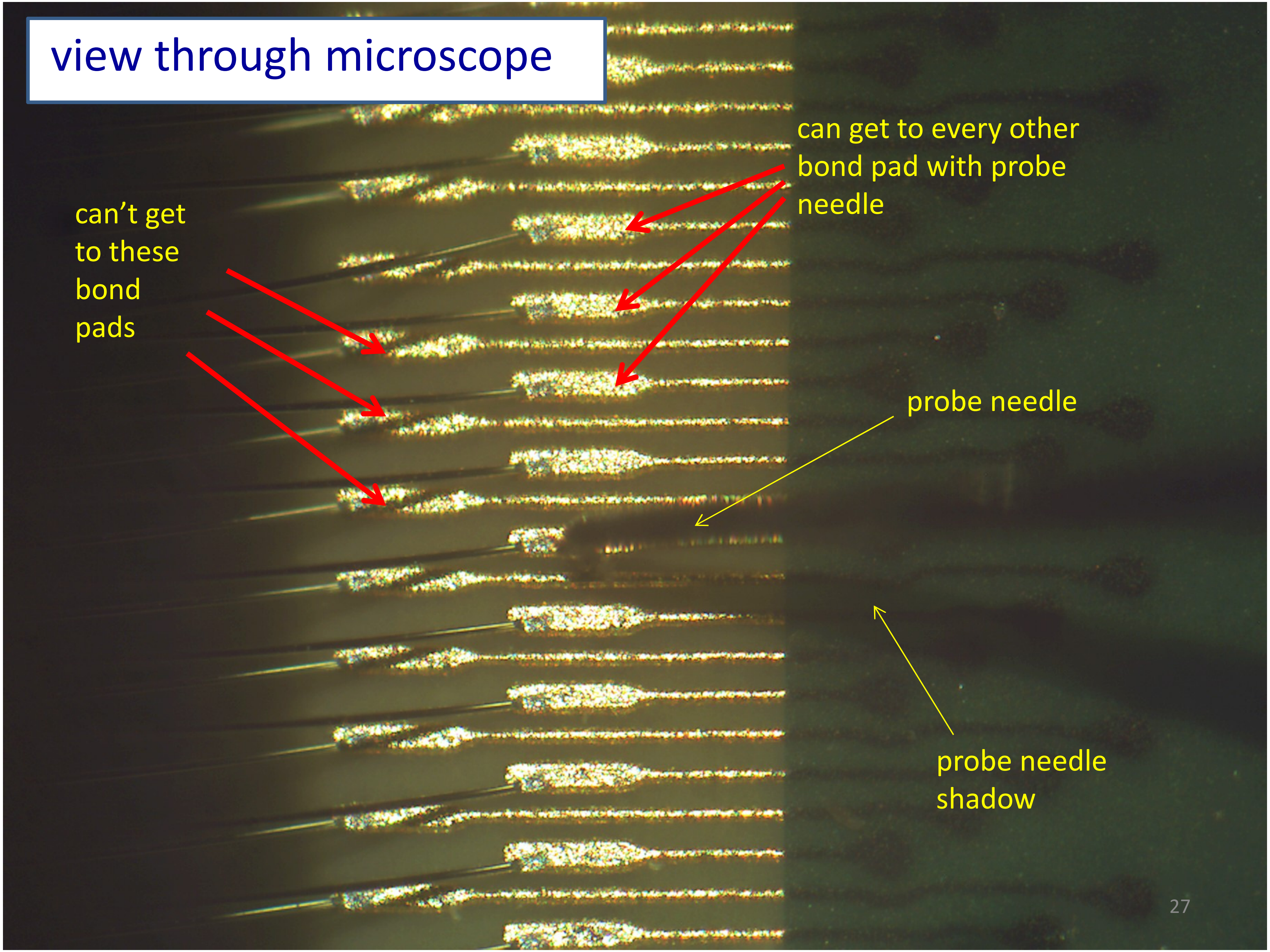
makeshift probing arrangement



a bit closer in

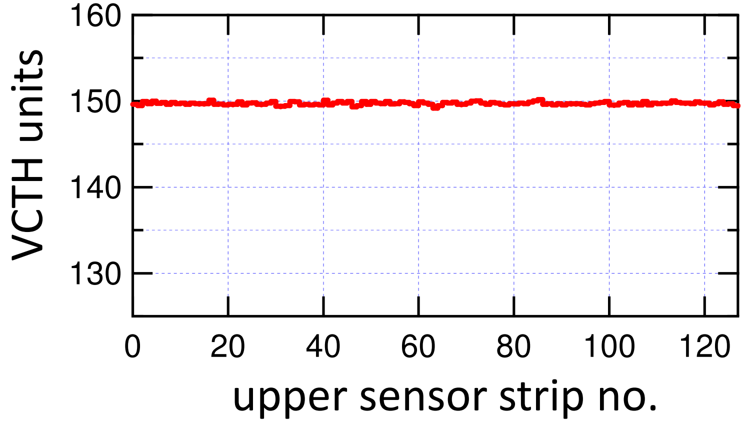


view through microscope

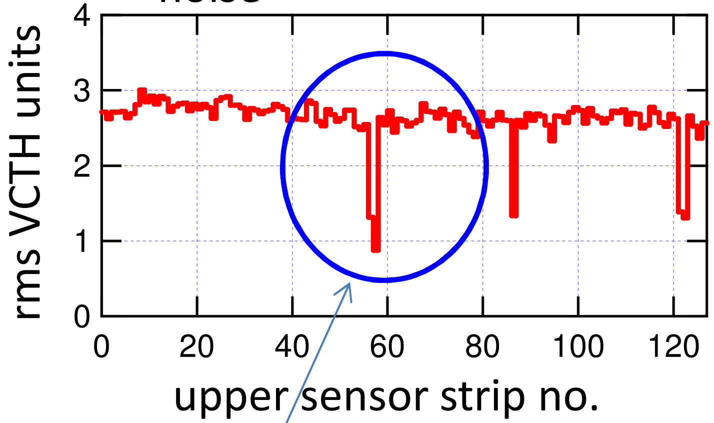


module under study: module#2(chip A only)

gain (s-curve mid-point)

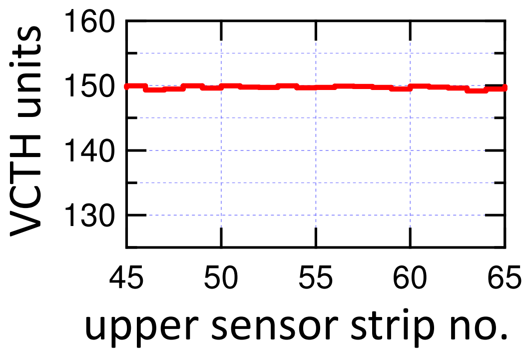


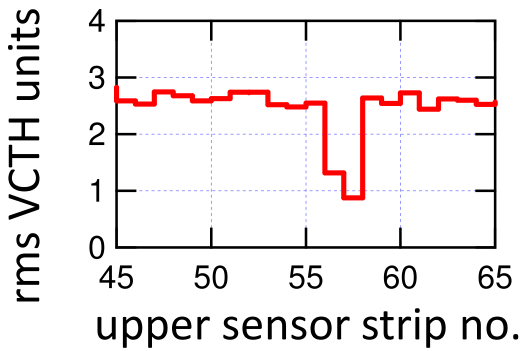
noise



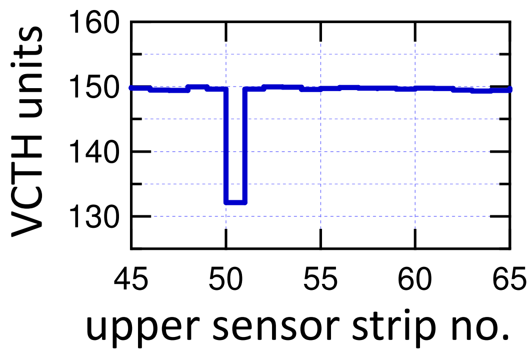
gain plot shows s-curve mid-points resulting from ~1fC test pulse
(after tuning comparator offsets to value of 150)

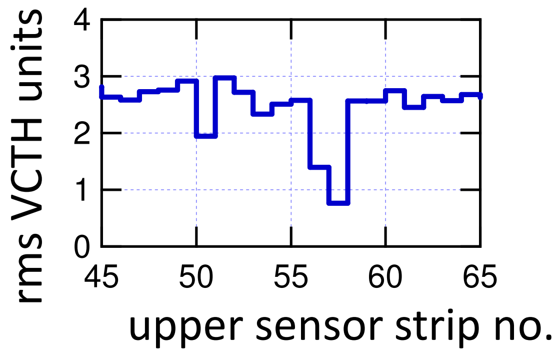
will concentrate on region around these two “bad” strips





now place grounded probe on strip 50 wire-bond pad





for a normally behaving channel (strip 50), grounding the wire-bond pad which is connected (via bump-bond) to CBC input, means that that channel no longer responds to the test-pulse

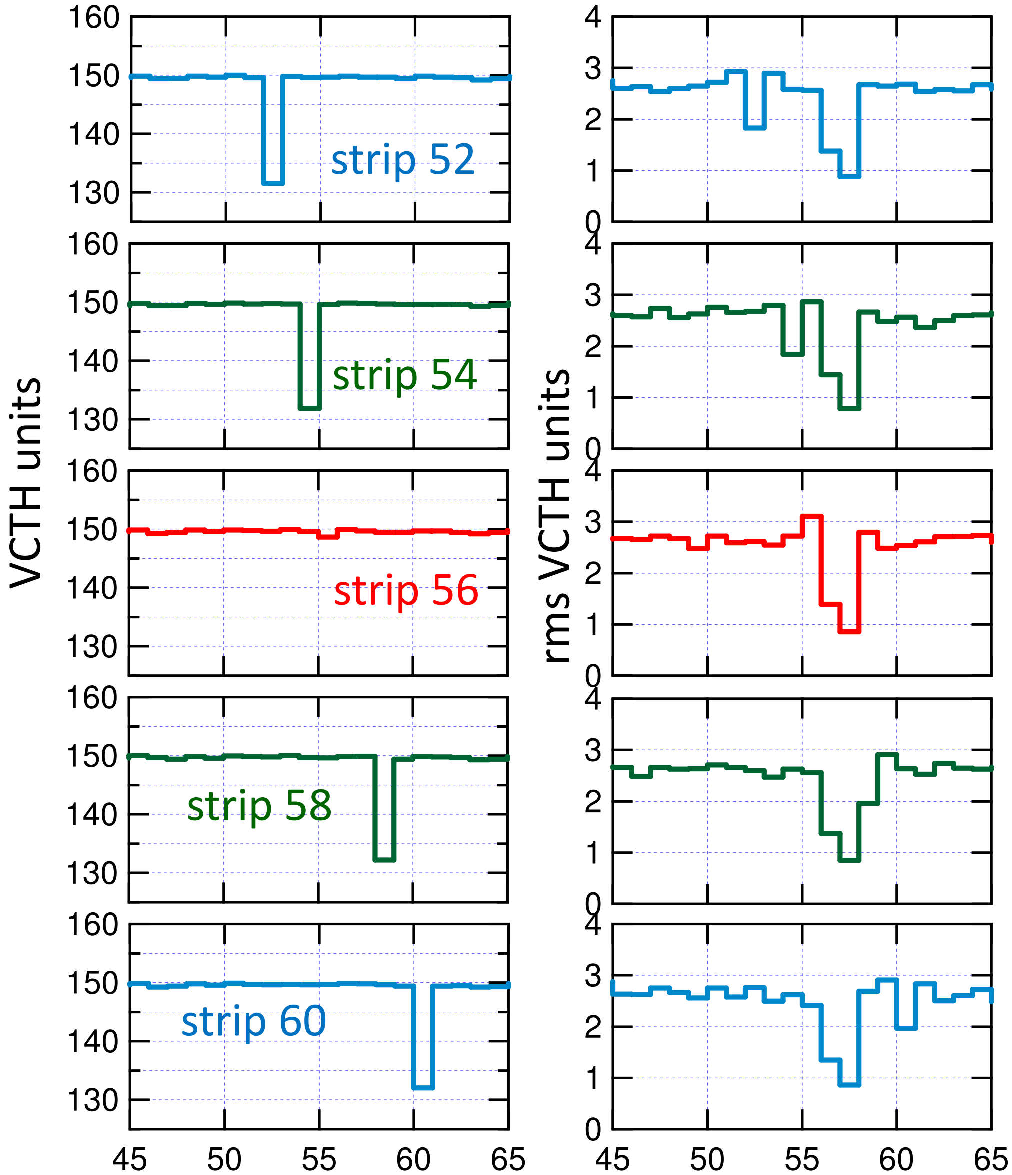
amplitude (strip 50) drops to pedestal level ~ 130

noise of that channel also drops

not to zero, but possibly noise introduced by the probe passes through the preamp feedback capacitor Cf

now proceed to “walk” grounded probe along the strips - remember can only safely probe every other strip

grounding every other strip - one at a time



upper sensor strip no.

strip 56 still responds to the test pulse

implication is that strip 56 (one of the two “bad” channels) is disconnected from the wire-bond pad

presumably the bump-bond has failed?

further investigations

results up-to-here discussed during Vidyo meeting (26th July)

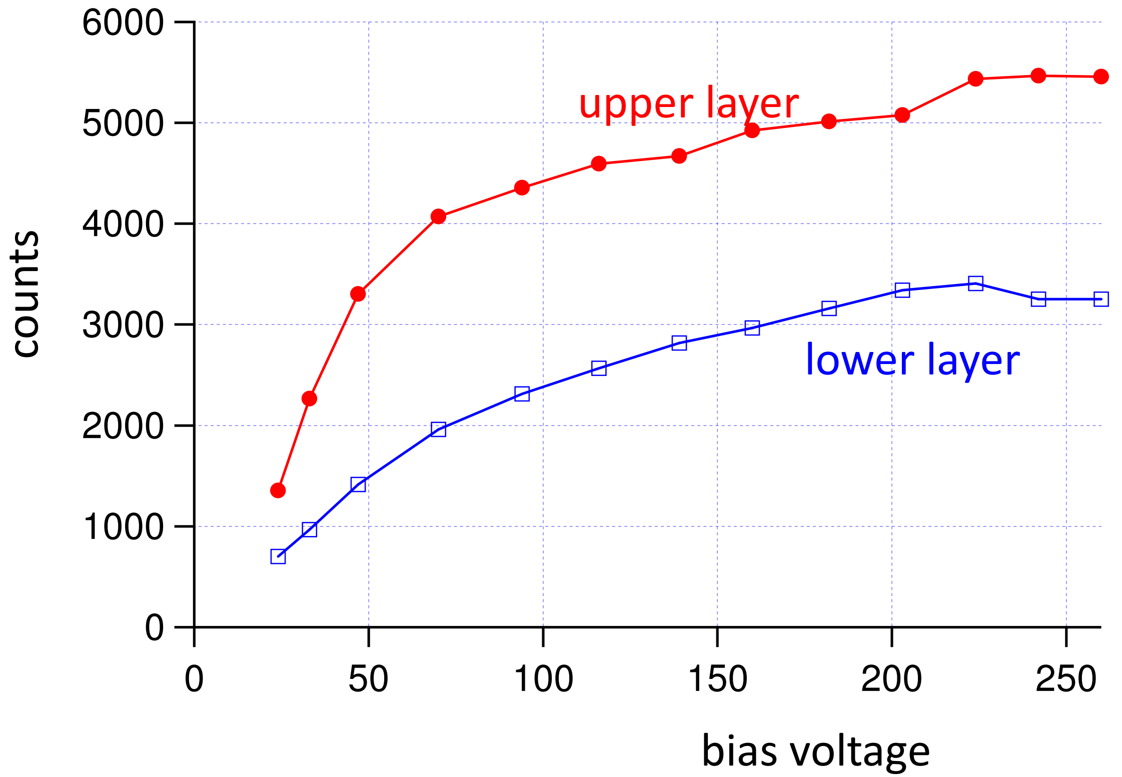
• noise measurements for lower sensors on both modules still a puzzle -
  are they depleting as expected from previous measurements on sensors?
  (before module assembly)

  => check signal amplitude vs. bias - not just noise

• can we be sure low noise channels due to bump-bond failure?
  could be due to cracked track (metallization for bonding makes tracks more brittle)

  => probe faulty channel closer to chip after scraping off solder mask

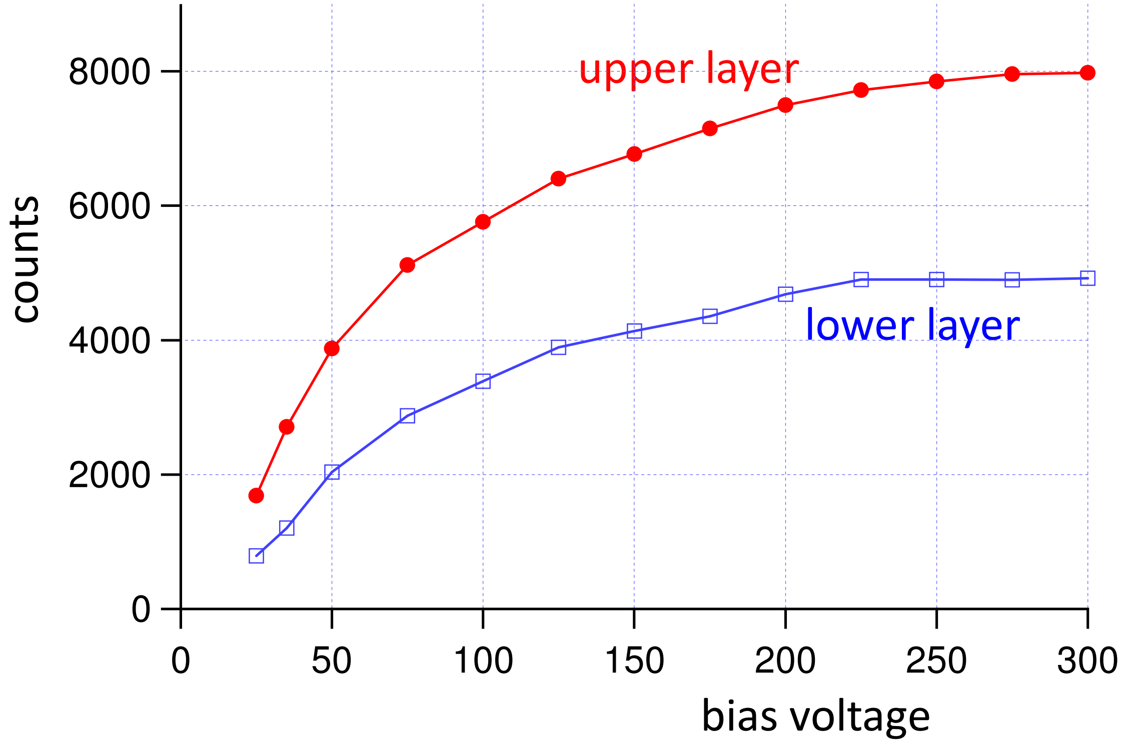
signal vs. bias - mini-module#1



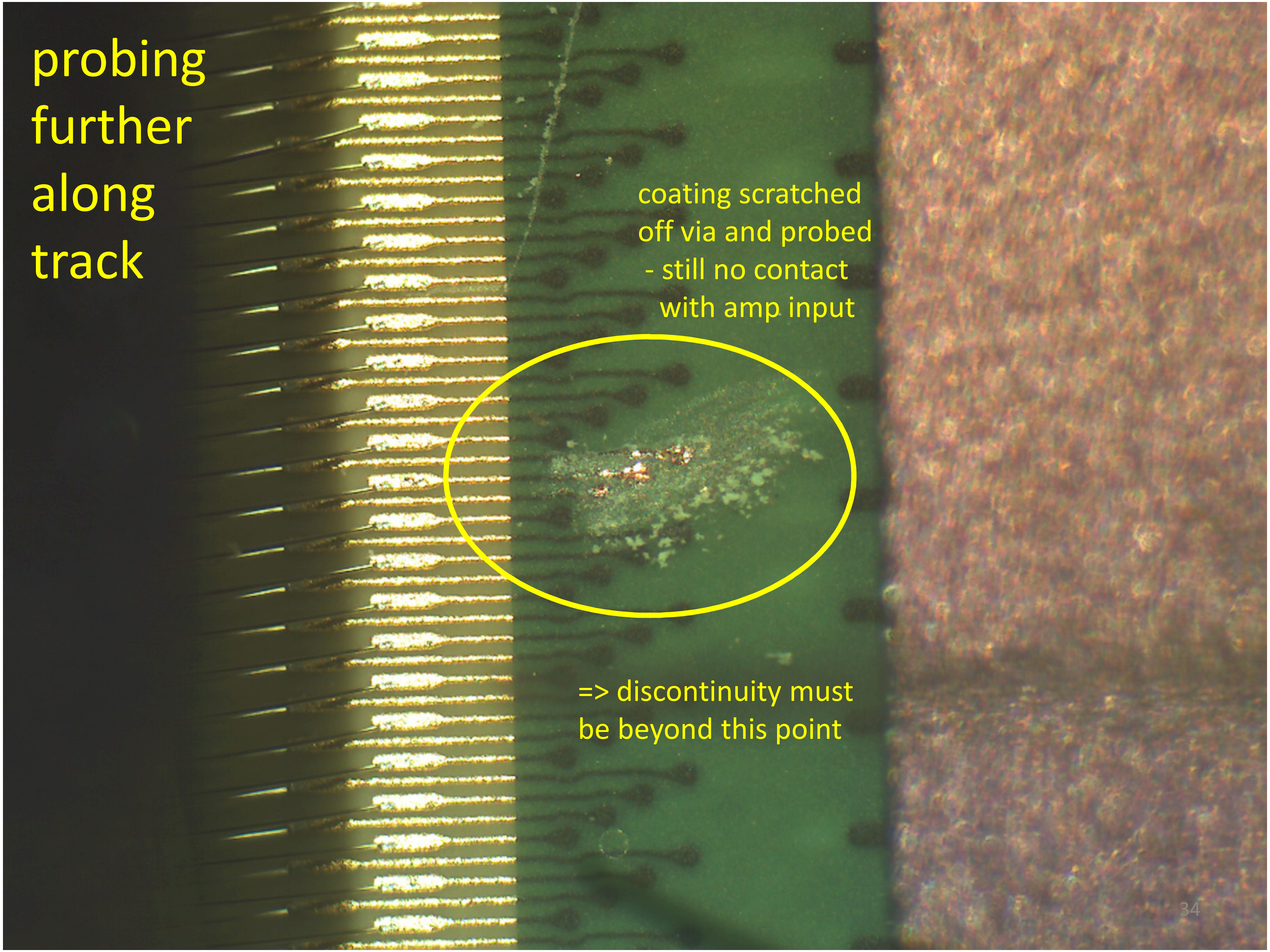
method:
threshold set at ~ 1 fC, Sr-90 source
look at one channel from each layer in middle of area “illuminated” by source
count number of times comparator fires for 100,000 scintillator triggers

counts saturate as bias voltage approaches 250 Volts

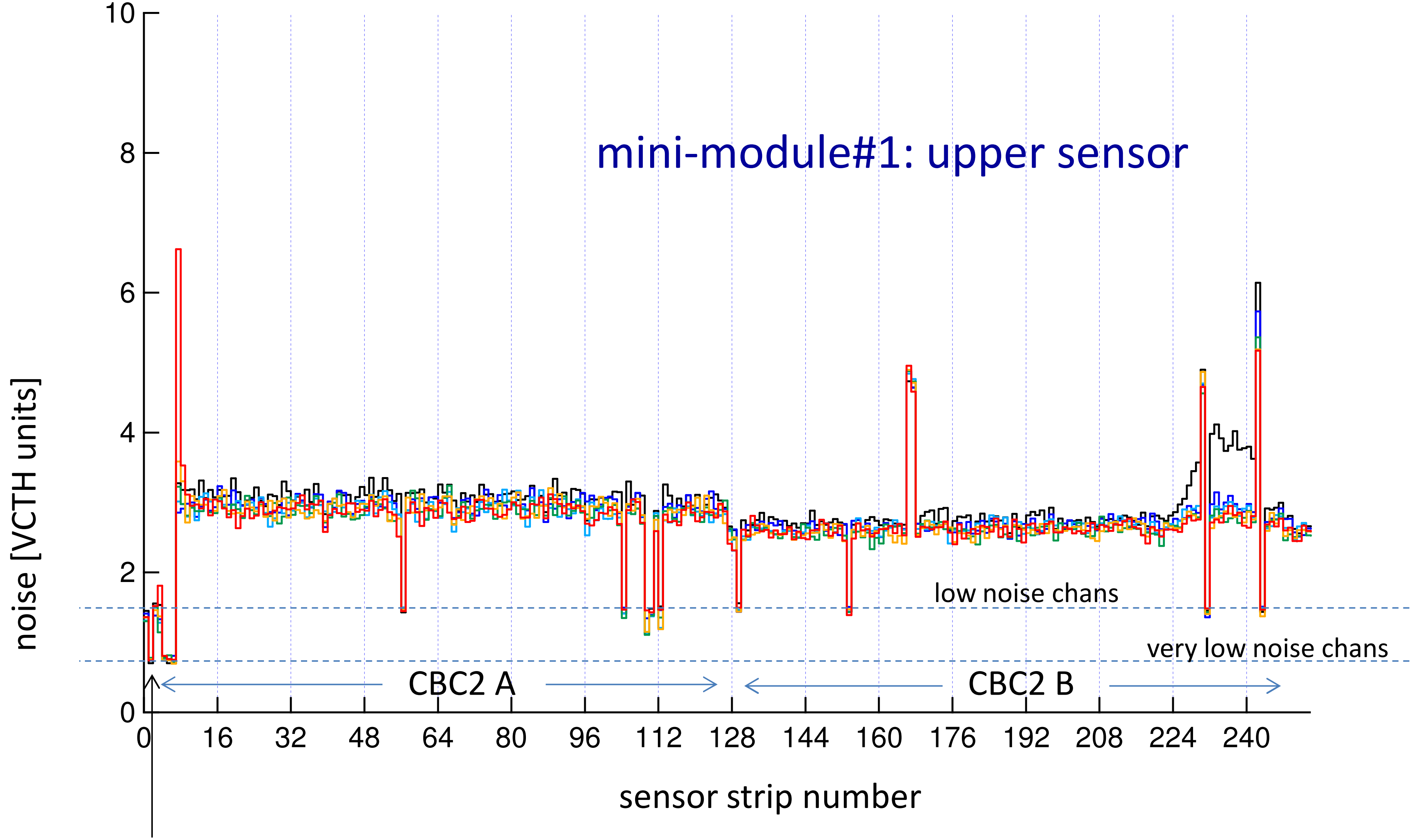
signal vs. bias - mini-module#**2**



similar result

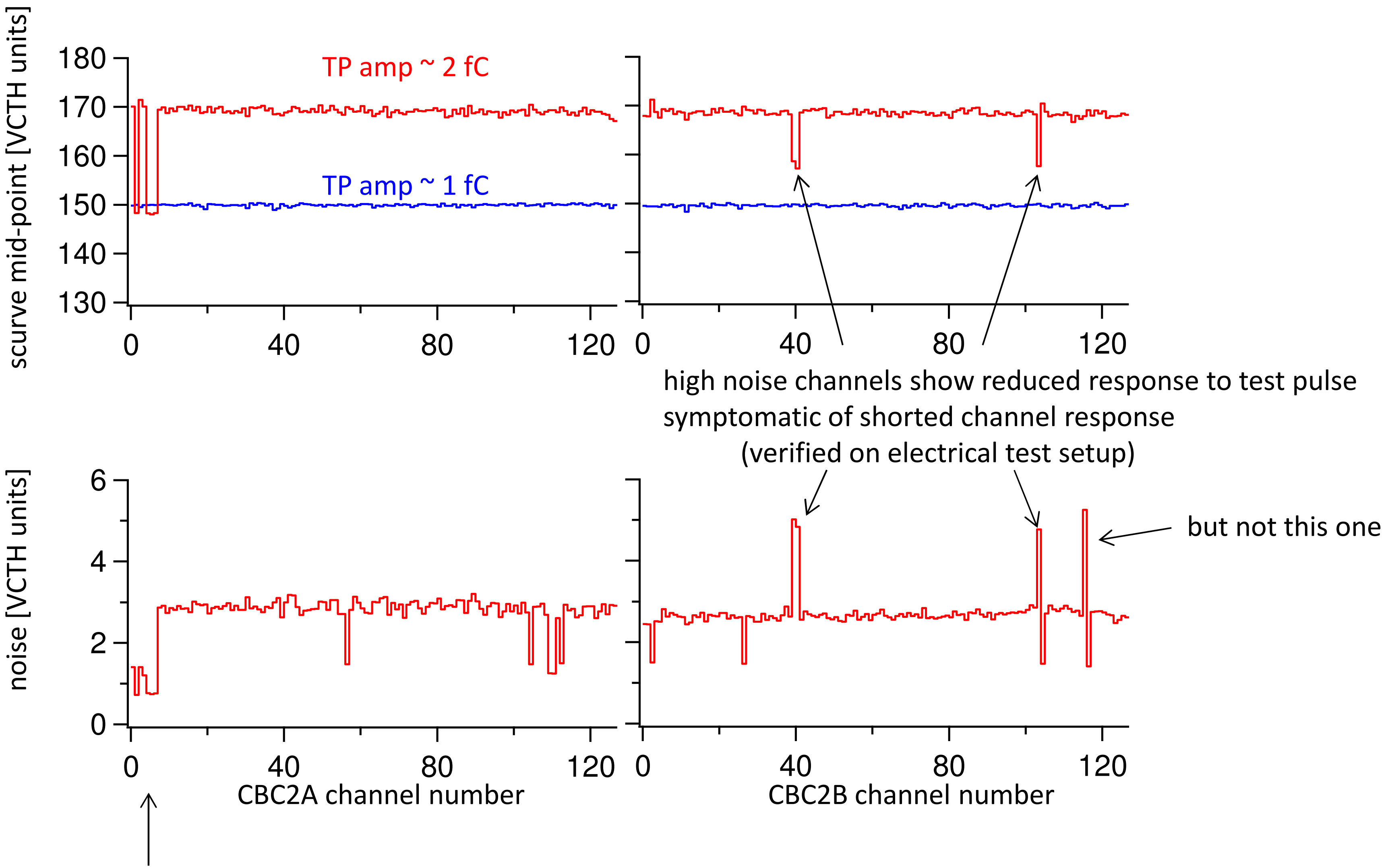

probing further along track
coating scratched off via and probed - still no contact with amp input
=> discontinuity must be beyond this point

what about very low noise channels?



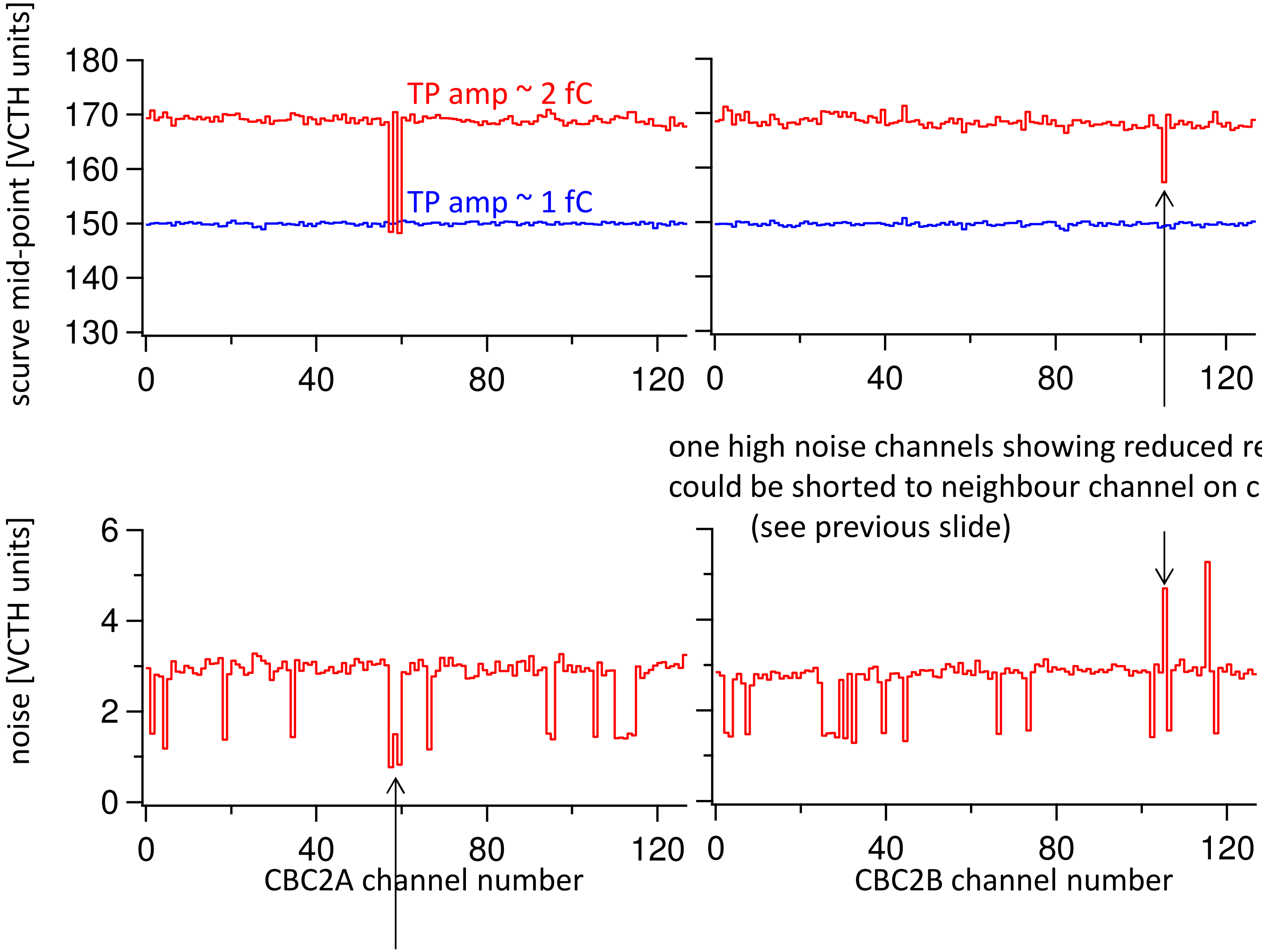
this one corresponds to the broken wire - what about the others?
to diagnose look at test pulse response behaviour

varying test pulse amplitude: **UPPER** sensor



very low noise channels show no response to test pulse
damaged amplifiers? or shorted to something?

varying test pulse amplitude: LOWER sensor



one high noise channels showing reduced response to test pulse
could be shorted to neighbour channel on chip but other sensors
(see previous slide)

pair of very low noise channels on this sensor also showing no response to test pulse

overall summary

- signal measurements show sensor appears to be depleting as expected
- still no explanation for noise dependence on bias for lower layer sensors

  different inter-strip capacitance dependence on bias for these sensors?

  (note: both sensors don't behave in quite the same way)

  or some effect due to the hybrid?
- low noise channels are disconnected from amplifiers - evidence points to the bump-bonds

  disconnection during the module assembly/wire-bonding process?
- very low noise channels show no response to test pulse

  damaged or shorted somewhere/somehow?
- high noise (low-gain) channels (not those bias related) appear to be shorted

  but weren't there prior to module assembly (gain measured for all channels)

next step

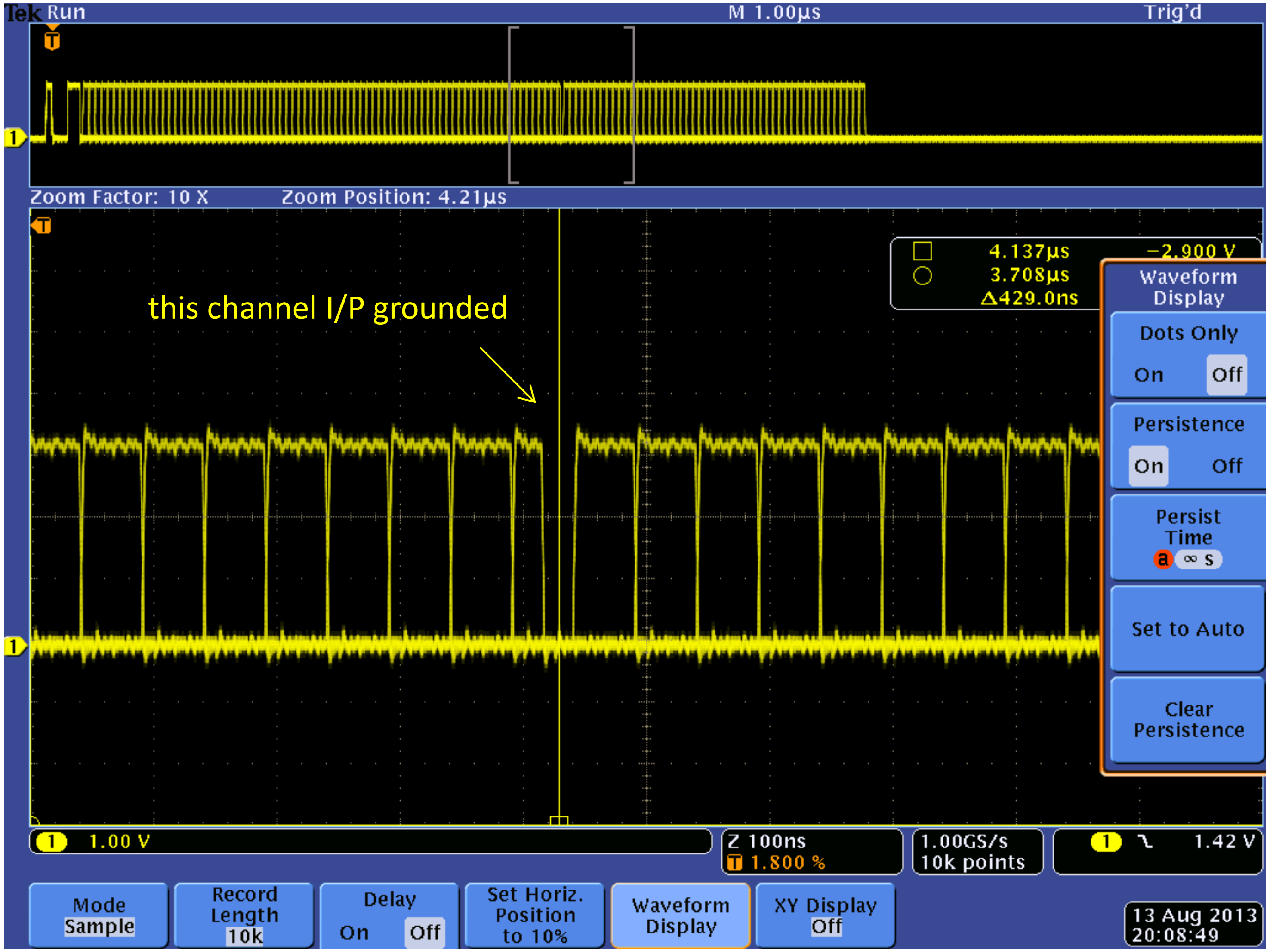
make another module - use hybrid with under-filled chips

should not be possible to disturb bump-bonds

use hybrid where wire-pad to amplifier connectivity has been verified for all channels

testing all channels on a hybrid

cycle test pulse continuously through all chip channels
view chip output frames on scope - infinite persistence
lower grounded probe tip on wire-bond pad - signal should disappear for that channel
repeat for all channels



underfilled hybrid #U03

all channels verifed connected

both chips

top **and** bottom
side wire bond pads
arrays

hybrid status summary

(those that have passed through Imp. College)

1st batch of 5 (all not under-filled)

- #1 in electrical test setup at IC
- #2 to Bristol for first tests with FMC, now passed on to Strasbourg
- #3 problem with I2C lines disconnected at connector - repaired - keep at IC
- #4 -> mini-module #1
- #5 -> mini-module #2

2nd batch: 4 under-filled, 2 not

- N01 at IC
- N02 at IC
- U01 at IC
- U03 at IC
- U04 -> Bristol for FMC development (will come back with FMC to IC)
- U06 all channels probed, to CERN for another mini-module