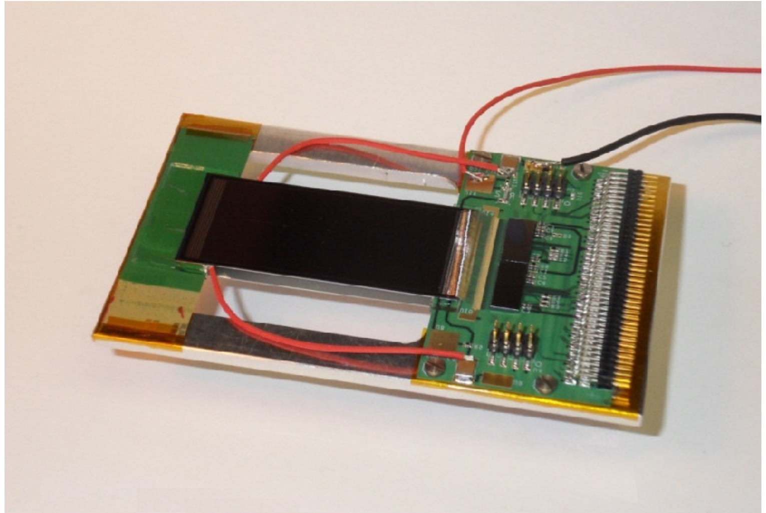
mini-module#3 characterization

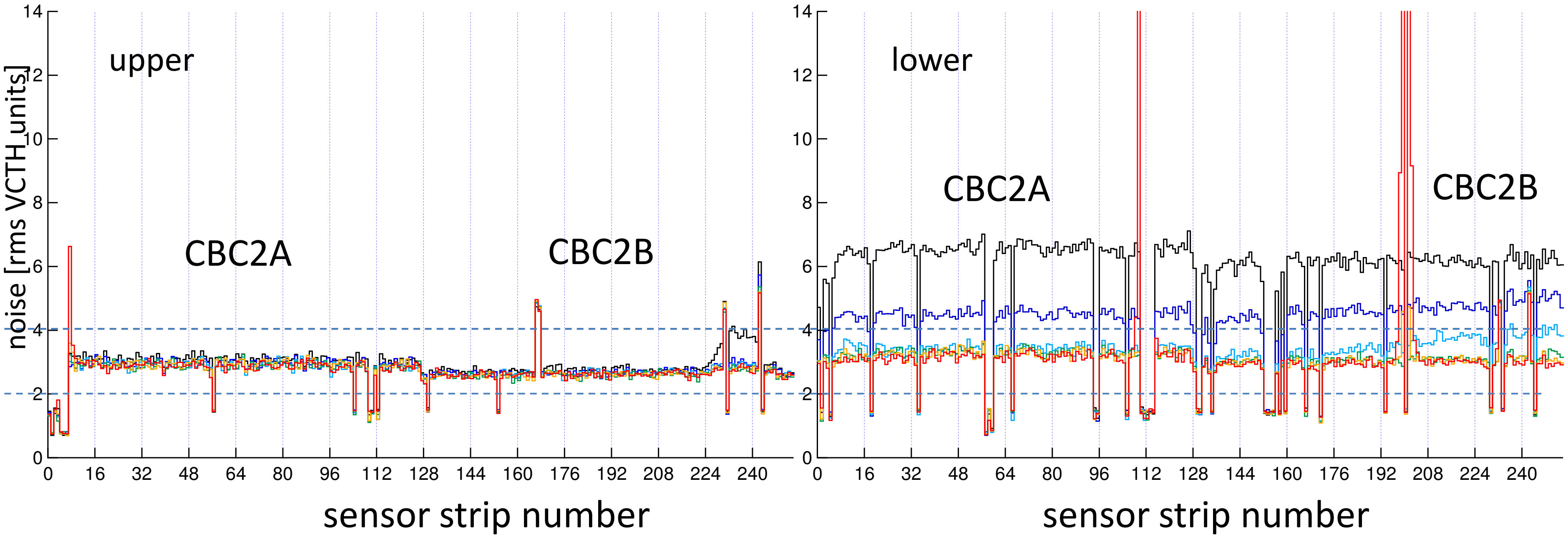


brief recap on modules 1 and 2
results for module 3
some slides on ESD protection in CBC2 from Davide
CBC2 self-triggering results

systems meeting, 17/10/13

mini-module#**1**: noise vs bias, both sensors

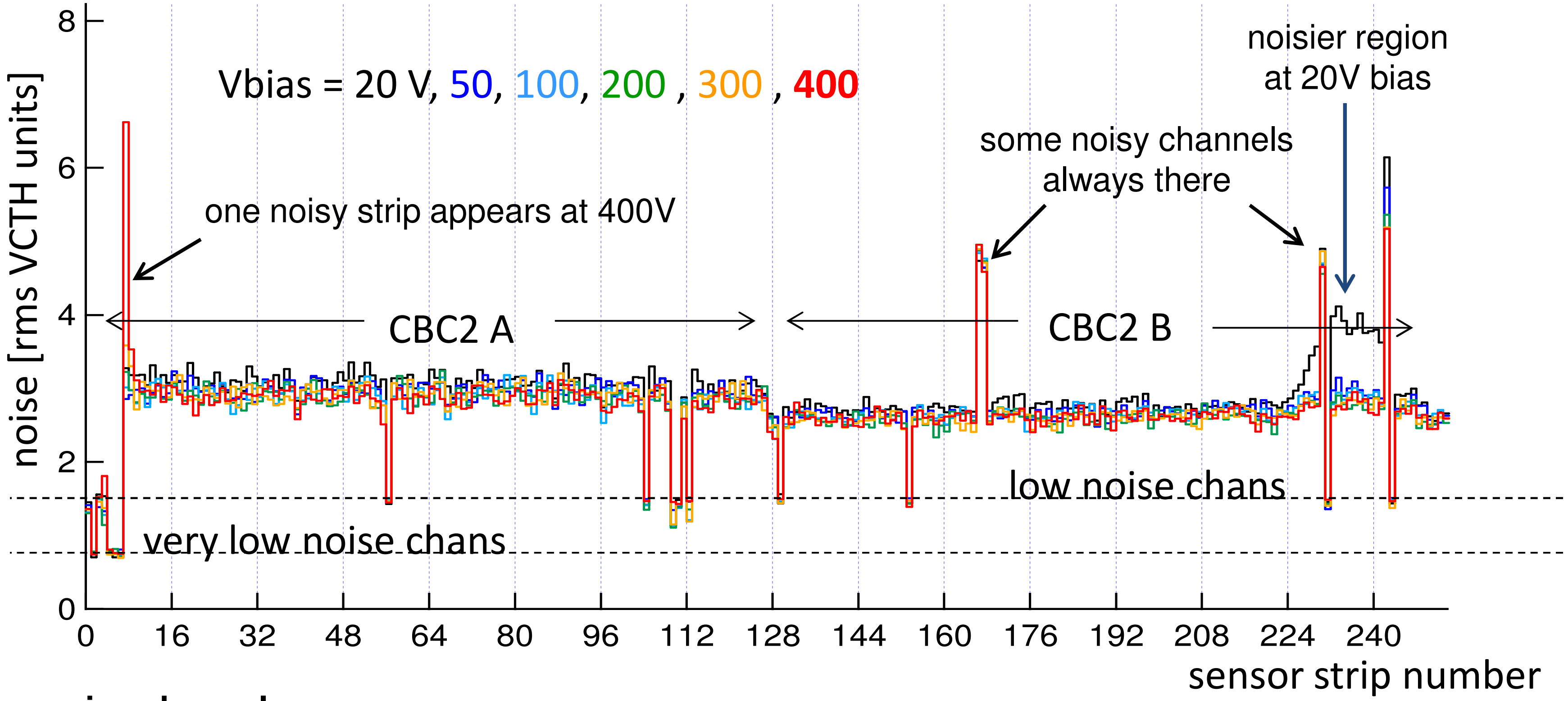
Vbias: 20 - 400 V



lower sensor needs higher bias (>100V) before noise reaches minimum value

final levels ~same - lower and upper
behaviour suggests different capacitance dependence on bias for lower sensor

mini-module#1: low noise channels, upper sensor example



low noise channels

these channels have somehow become disconnected at bump-bond level

they still respond to the test pulse

presumably during module assembly and bonding (the hybrid is very flexible)?

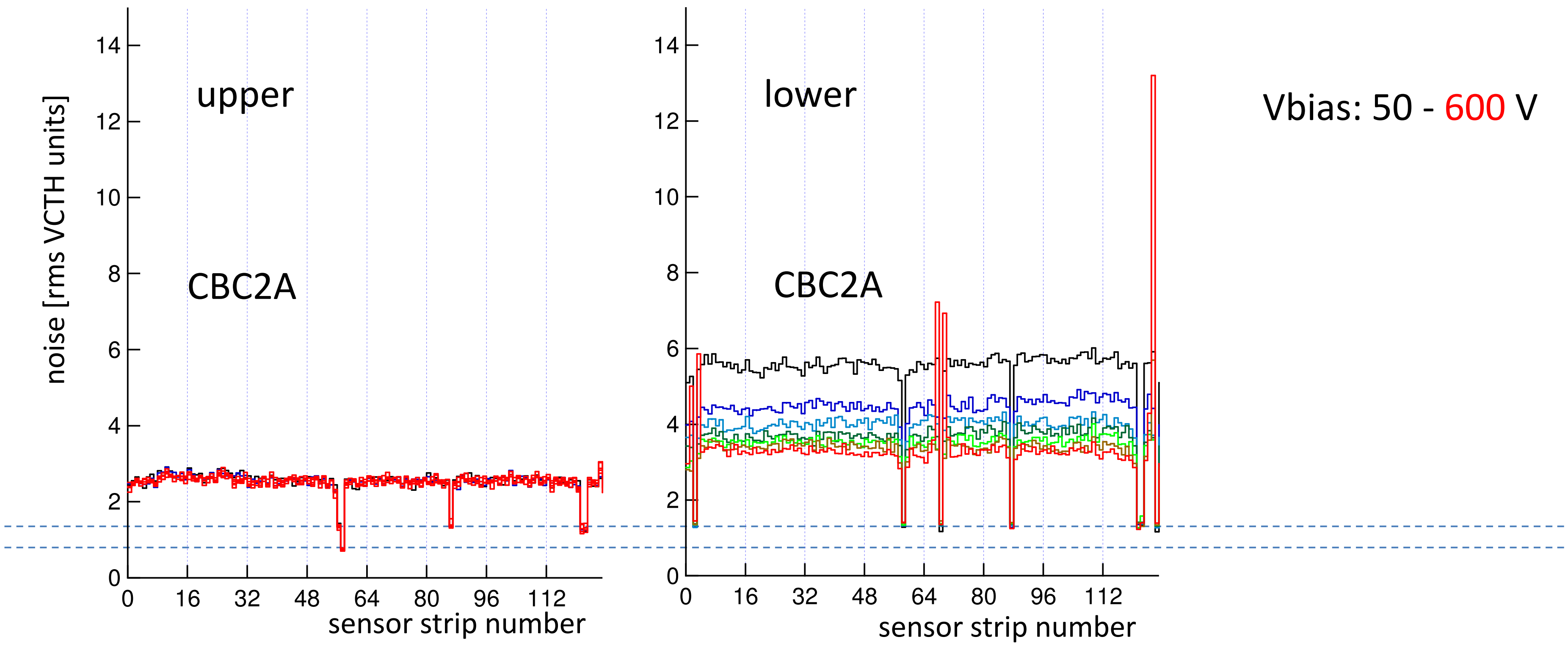
very low noise channels

these channels damaged - no test pulse response

higher noise channels

behaviour ~consistent with two channels shorted together

mini-module#2



results only from CBC2 A (other chip damaged - so not powered)

similar behaviour to module#1

lower sensor needs higher bias before reaching minimum noise

low and very low noise channels exist and respond in the same way

where we left it last time

- anomalous behaviour found in the noise dependence on bias for lower layer sensors - both modules

    different inter-strip capacitance dependence on bias for these sensors?

    or some effect due to the hybrid?

- low noise channels are disconnected from amplifiers - both modules, both sensor layers

    evidence points to the bump-bonds

    disconnection during the module assembly/wire-bonding process?

- very low noise channels show no response to test pulse

    damaged or shorted somewhere/somehow?

- high noise (low-gain) channels (not those bias related) appear to be shorted together

    but weren't there prior to module assembly (would have shown up in acceptance tests)

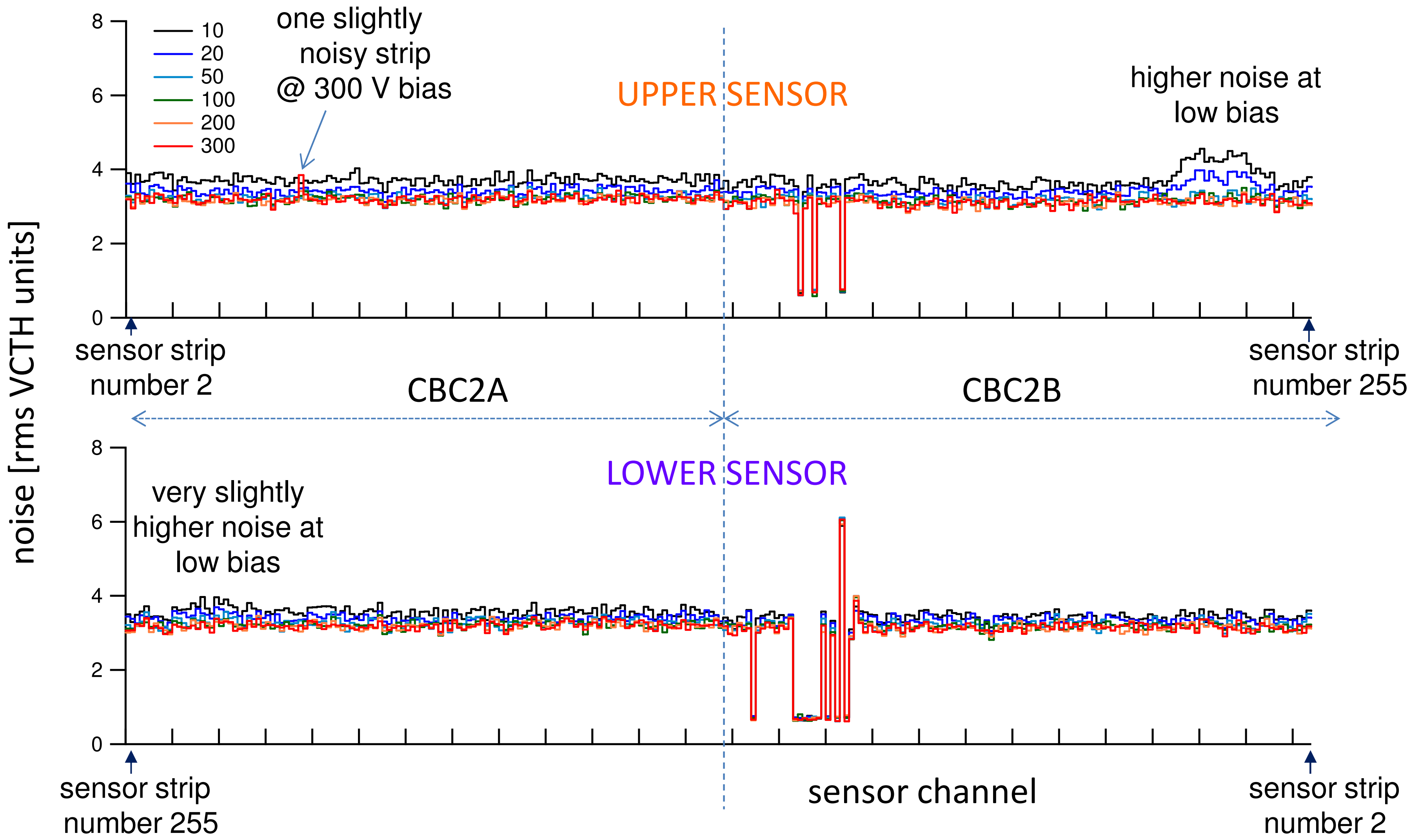
since then

another module made - using hybrid with under-filled chips (bonds encapsulated)

should not be possible to disturb bump-bonds
using hybrid where wire-pad to amplifier connectivity verified for all channels
Infineon sensors carefully selected

results from mini-module#**3**

mini-module#3: noise vs. bias, both sensors

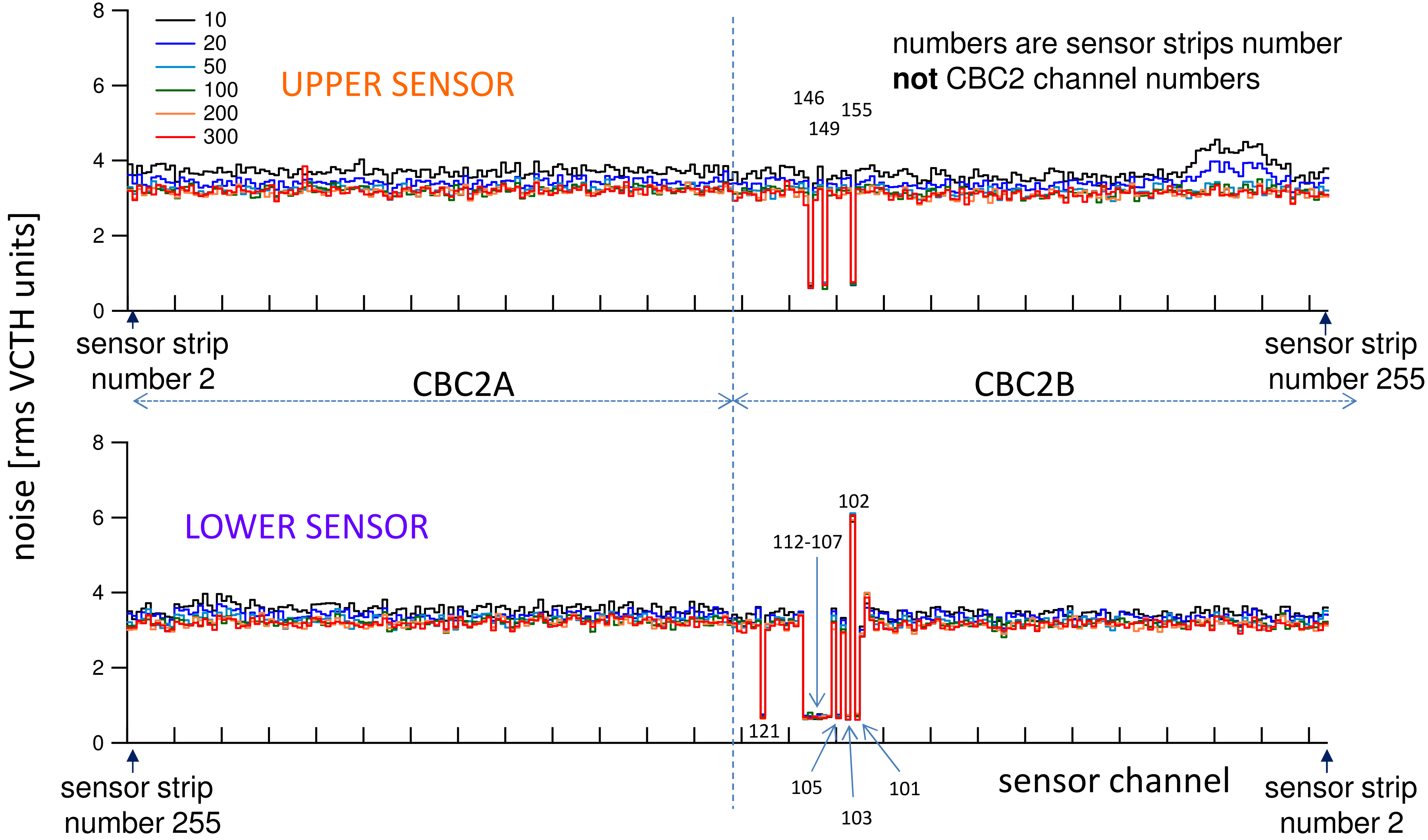


from these results can conclude:

=> previous upper/lower noise behaviour differences **not** due to hybrid

must be characteristic behaviour of the particular sensors used on modules 1 & 2

mini-module#3: odd behaving strips region



all low noise channels are **very** low noise channels - not responsive to test pulse
all associated with CBC2B - both layers (but more associated with lower layer)
high noise channel 102 does respond to test pulse

module 3 odd behaving channels
strip no. correspondence to CBC2B channel number

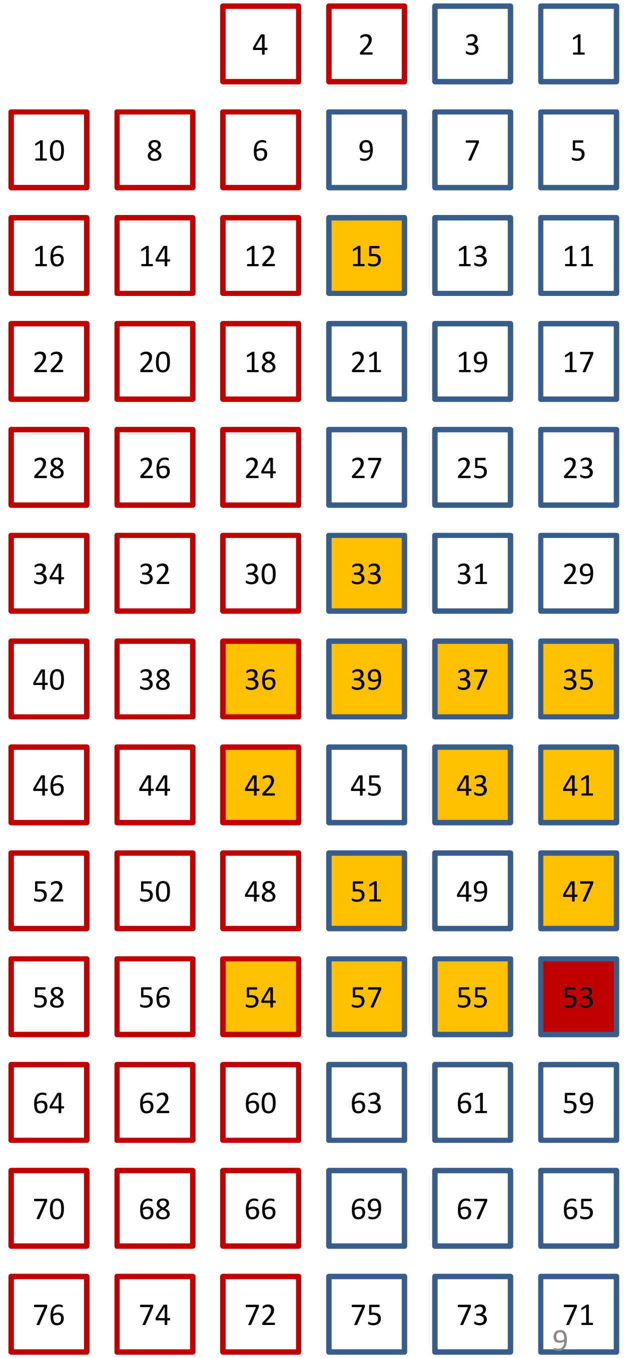
upper sensor strip number	**CBC2B chan. no.**
146	36
149	42
155	54

lower sensor strip number	**CBC2B chan.no.**
100	57
101	55
102	**53**
103	51
105	47
107	43
108	41
109	39
110	37
111	35
112	33
121	15

this one included for reason on next slide

this is the higher noise channel

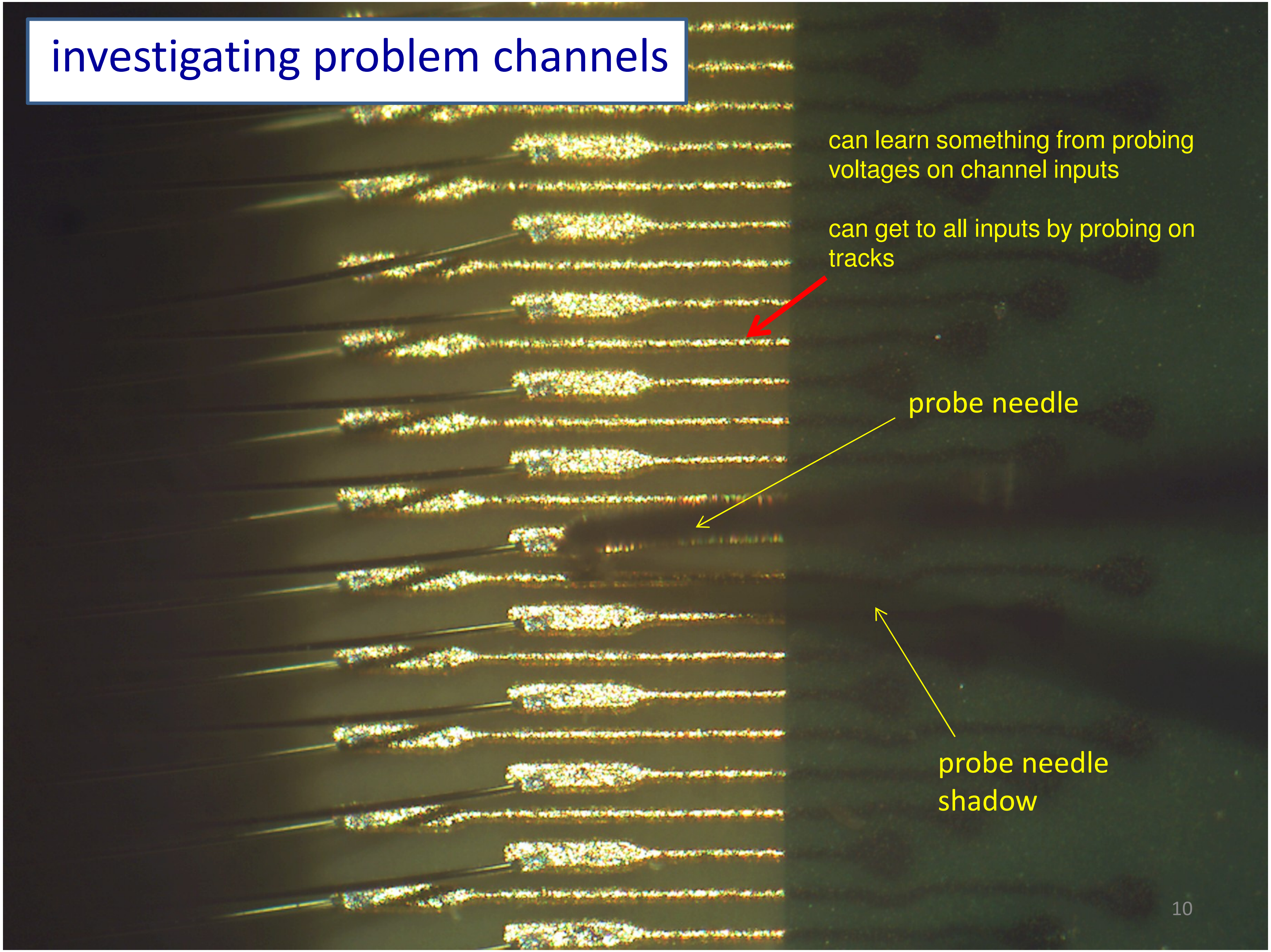
CBC2B pad pattern on hybrid showing location of problem channels



upper sensor layer pad

lower sensor layer pad

investigating problem channels



module 3 odd behaving channels:
voltages measured on wire-bond tracks

upper sensor strip number	**CBC2B chan. no.**	
146	36	floating
149	42	16 mV
155	54	16 mV

lower sensor strip number	**CBC2B chan.no.**	
100	57	130 mV
101	55	2 mV
102	**53**	**normal**
103	51	floating
105	47	floating
107	43	floating
108	41	4 mV
109	39	floating
110	37	23 mV
111	35	floating
112	33	31 mV
121	15	floating

probe lowered on to tracks adjacent to wire-bond pads on hybrid. probe connected to DVM and scope

good (normal) channels show a voltage ~ 245 mV which corresponds to the input FET gate voltage

some of the bad channels appear floating
 scope just shows pickup - same as when not in contact with anything

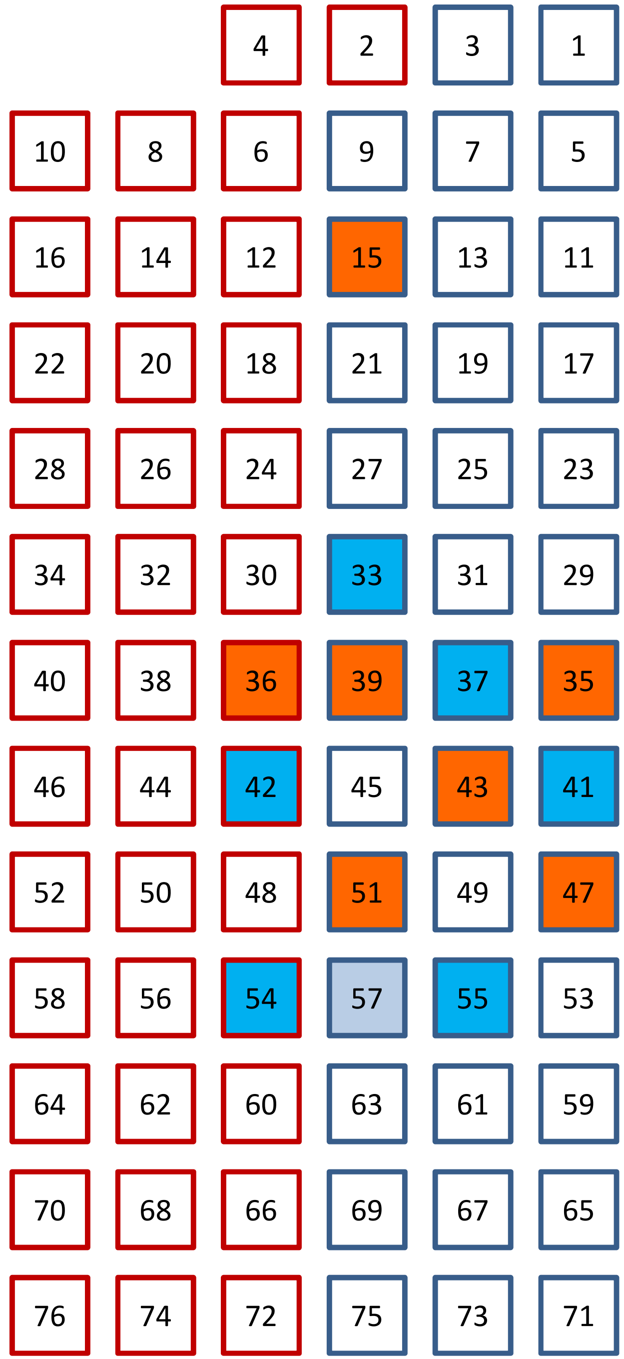
some of the bad channels have abnormally low voltages
 appear to be being pulled down

strip channel 100 (CBC2B channel 57) shows lower than normal voltage (but not as low as others)

none of the bad channels respond to test pulse, **including** strip channel 100 (CBC2 channel 57)

channel 102 is “just a noisy channel”

module 3 odd behaving channels:
pattern of floating and low voltage channels



floating

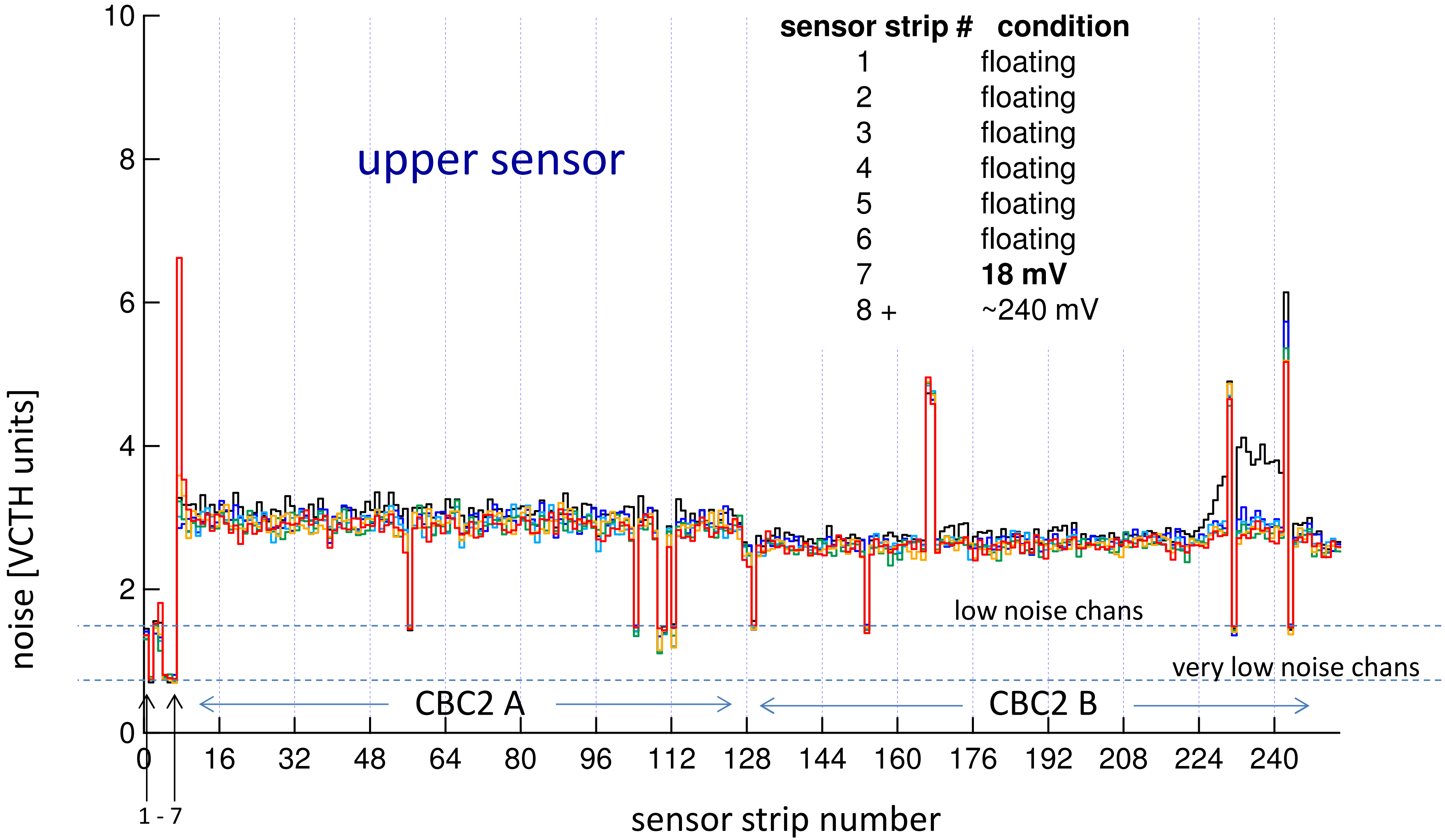
low (few mV - few 10's mV)

quite low (130 mV)

[normal level ~ 250 mV]

note: no bad channels in two columns furthest from amplifier inputs
significant?

probing channel voltages on mini-module#1

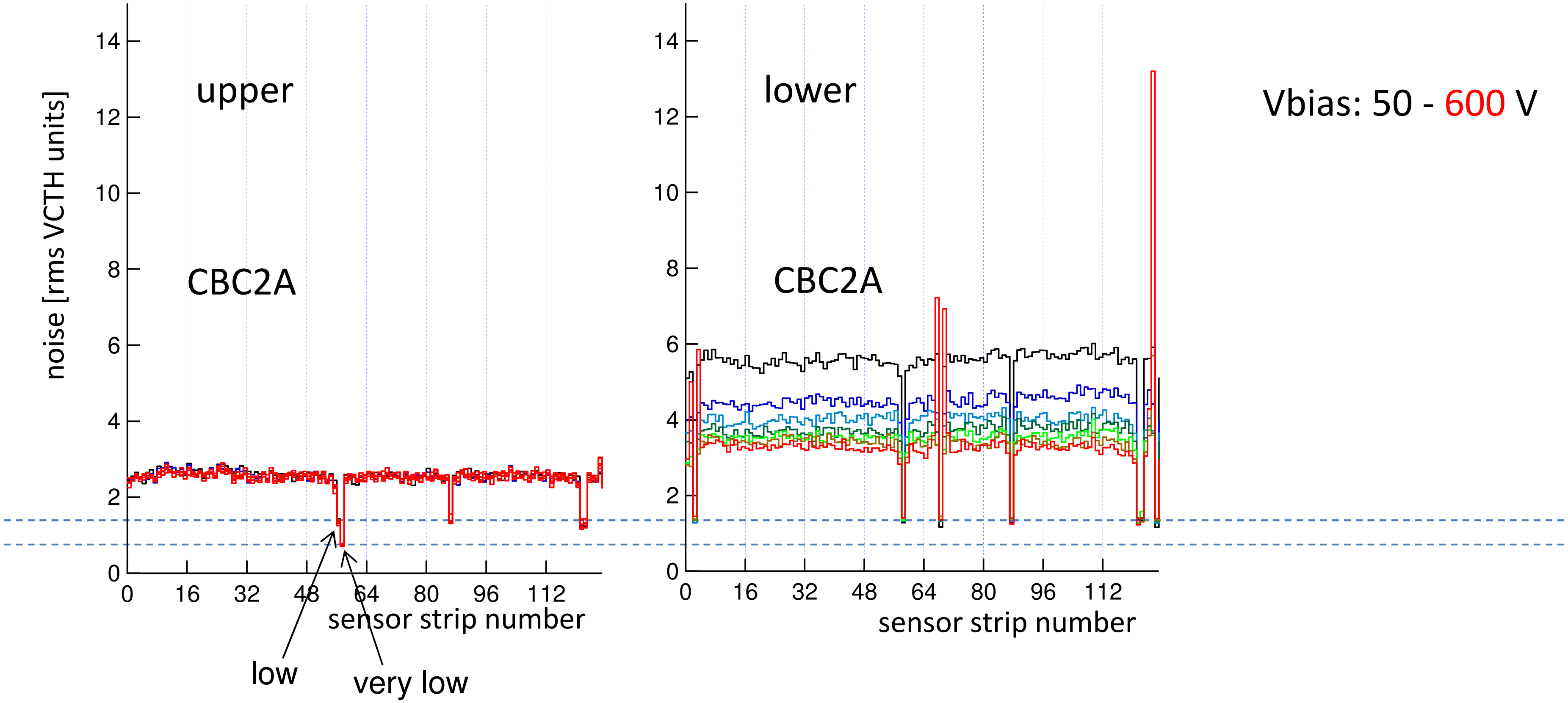


very low-noise channels don't respond to test pulse

low noise channels do

all bad channels floating - except channel 7

probing channel voltages on mini-module#2



Vbias: 50 - 600 V

both of these channels (low & very low) appear floating

only very low noise channel does not respond to test pulse on this chip

ON ESD IN CBC

ESD models

	HBM (Human Body Model)	MM (Machine Model)	CDM (Charge Device Model)
Simulates	Human discharge through chip	Metal tool discharging through chip	Charged chip discharging through ground
Characteristics	I: lowest V: lowest Duration: longest	I: medium V: medium Duration: medium	I: highest V: highest Duration: shortest

NB: ESD diodes are kept small on the input pads to limit the capacitance on the node

1. Human Discharge = mishandling → not appropriate to design for this
2. Other possible mechanisms:
    1. Bump bonding: CDM? no indication that this is a risky process for ESD (many hybrid-pixels readout have 100s of pads with no ESD protection)
    2. Wire bonding: MM. (charge from friction during the soldering on the pad?)
    3. …?

ESD protection

CBC2 uses the same ESD input protection of CBC1, since those have shown no failure (but few CBC1s tested and no bump bonding!)

Two factors to consider:
- **failure current**
- **series resistance**

for both **wiring** and **devices**

Wiring:
ESD via rules in 250um process (APV25):
- minimum contact area >3.90um2 → much bigger in CBC2 but could be made even bigger
- wiring width >6.4um (recommended >12.8um) (but metal resistance in 250um process about twice the one of the 130um process)

NB: design manual says that resistance <16 Ohm is considered short
Input tracks on CBC2 up to ~25 Ohm → can be reduced in next version

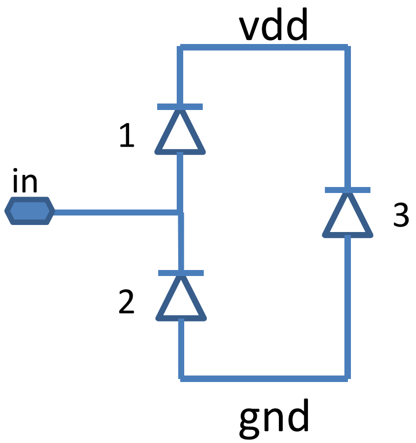
Devices:
- See table

130um rules for double diode	min.	recommended	CBC2
HBM down diode perimeter (ESD01a)	110um	200um	114um
HBM up diode perimeter (ESD01b)	220um	350um	229um

NB: esdvpnp device used as up-diode:
- Advantages
  - Low capacitive loading
  - Competitive area consumption
  - Low on-resistance due to NWell Rs remaining low, leads to improved clamping of pad voltages during ESD event
- Disadvantages
  - Device also operates as a vertical PNP, injects holes into SX.
  - → radiation hardness issue? CERN should provide a ESD library soon so we'll be able to compare it with what they have

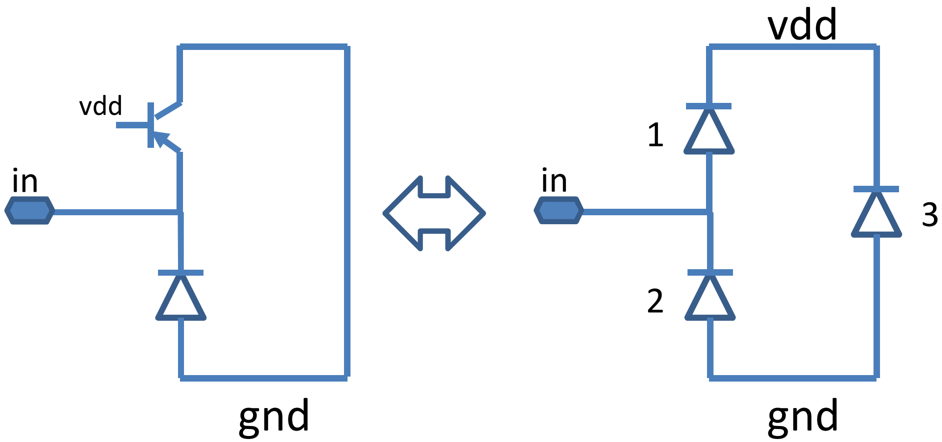
CBC vs APV

APV25



Diode	Type	Area	perimeter
1	diodep	$2.9*10^{-10}$	340um
2	diodew	$1.4*10^{-10}$	180um
3	diodew	$4.0*10^{-10}$	501um

CBC2



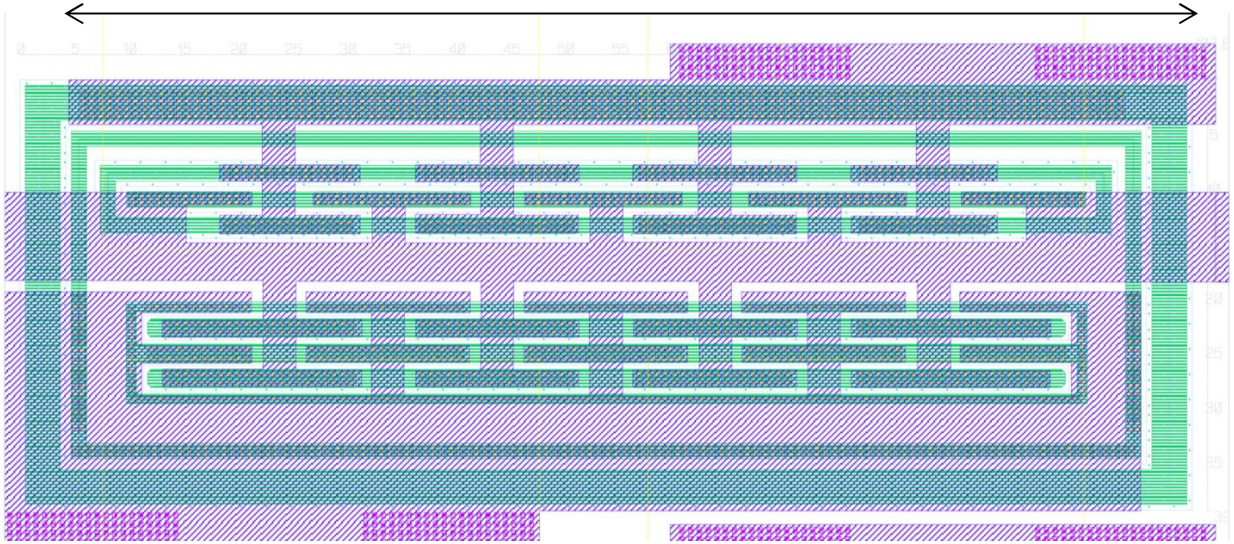
Diode	Type	Area	perimeter	CBC/APV area	CBC/APV perimeter
1	esdvpnp P+/NW ESD diode (dual well)	$0.8*10^{-10}$	229um	0.28	0.67
2	esdndsx N+/PW ESD diode (dual well)	$0.4*10^{-10}$	114um	0.29	0.63
3					

Layouts

APV25

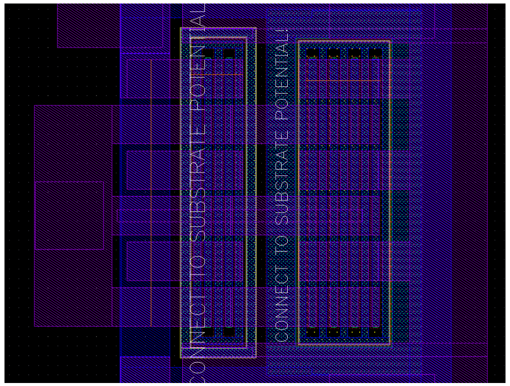
Input ESD protection

~100um



~30um

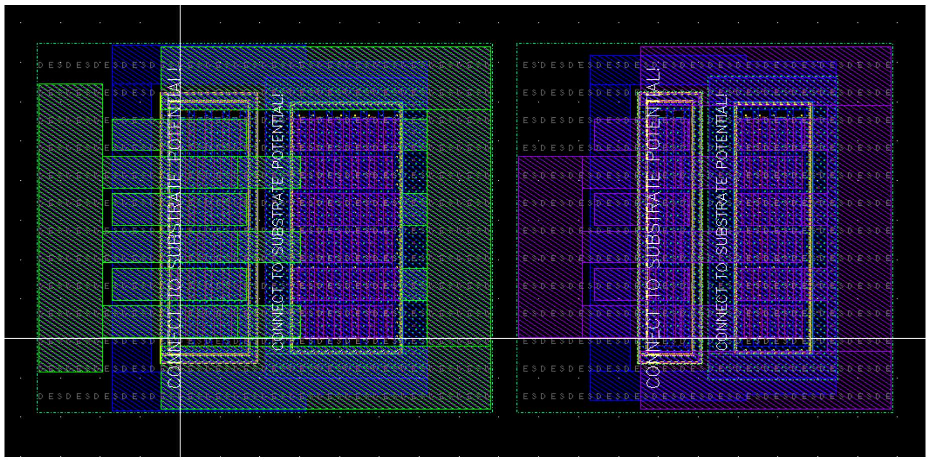
CBC2

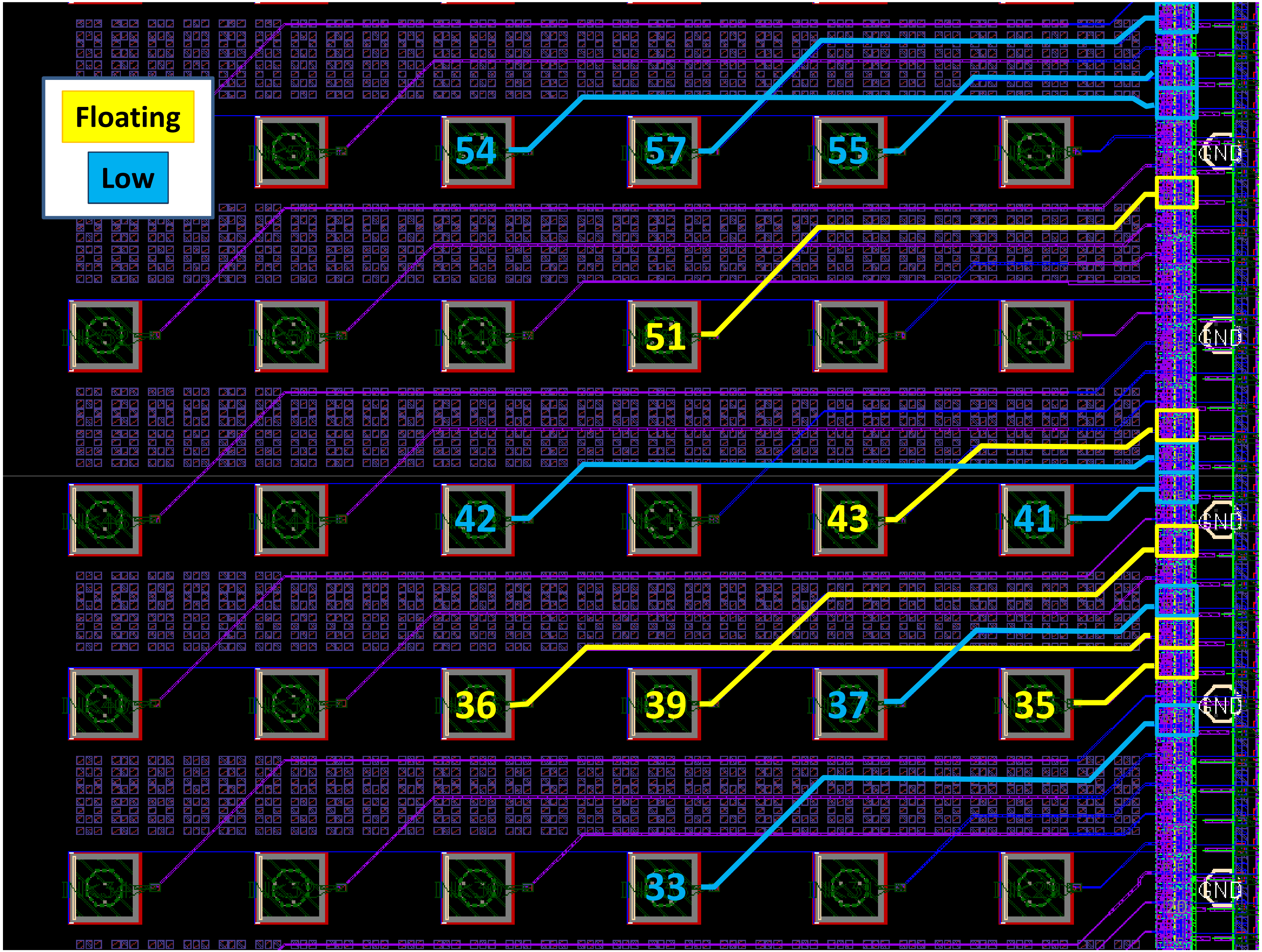


~30um

ESD with recommended dimensions next to CBC2 ESD

→ Can easily fit in existing layout





Floating
Low
54
57
55
51
42
43
41
36
39
37
35
33
GND
GND
GND
GND
GND

- NB: the VDD/GND straps for the ESD input array are fairly long (~250squares of MG → ~8.5 Ohms)

Reduce that in CBC3 by running in parallel with E1 (which is ~5.5 times less resistive → down to ~1 Ohm level)
Also M3 is not used at the moment, comes as default in the ESD pcell

- NB: finger length >50um in the diodes helps reduce the resistance (not sure how, to me it seems the opposite): could tilt the diodes by 90degrees (APV –style) and keep them on the same pitch, but then the power and gnd straps will take much more area, so not a preferred option.

- NB: no indication in the manual that bump-bonding is a significant factor for ESD

summary

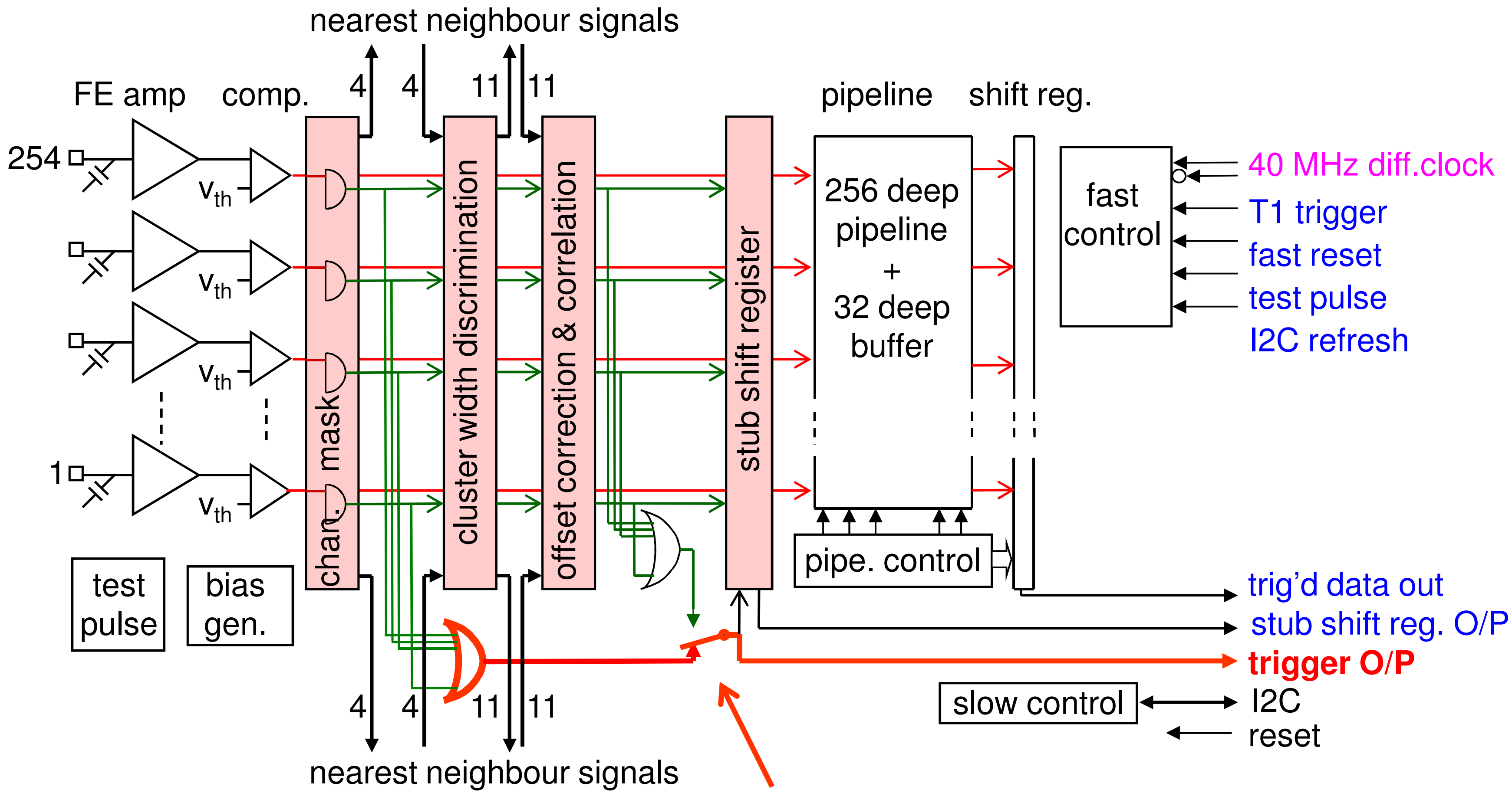
mini-module#3 is working well - will go into November test beam

noise vs. bias shows previous anomalous capacitance vs. bias behavious for lower sensor attributable to sensors - not to some kind of hybrid effect

a small region of channels in module#3 have got damaged somehow

characteristics of behaviour and damage mechanism not yet understood

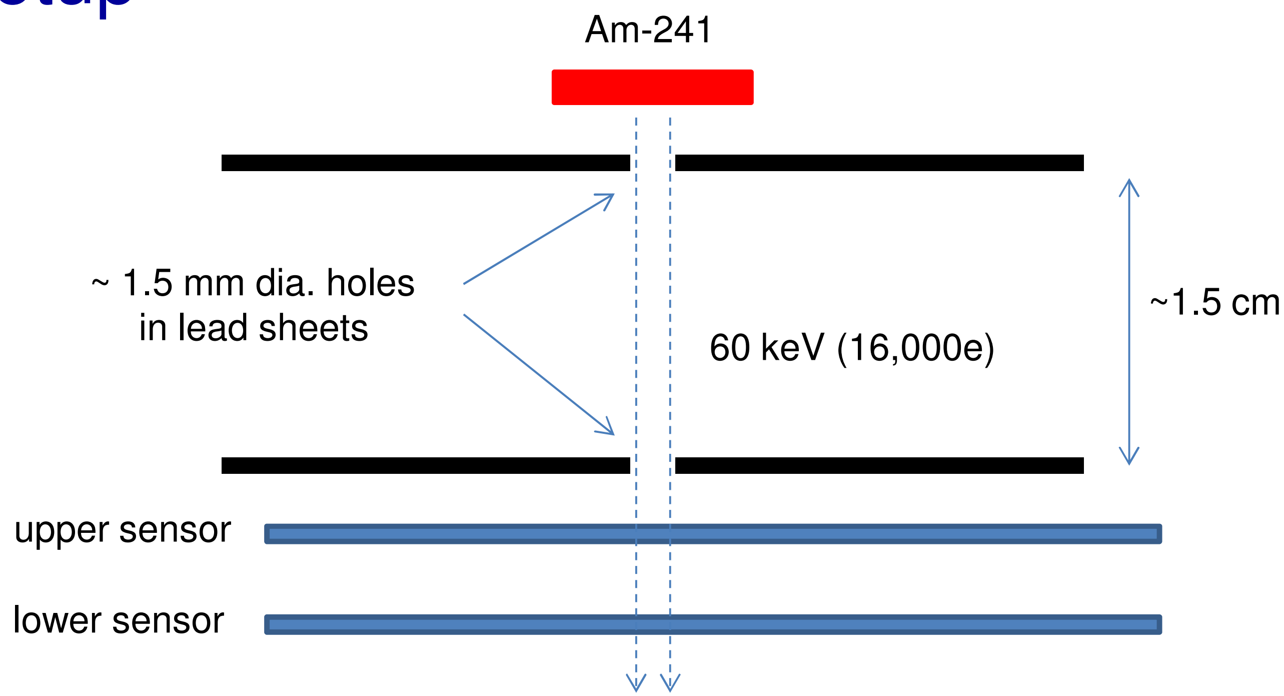
CBC2 self triggering



can operate CBC2 in mode where any unmasked comparator output will generate trigger
-> bypasses CWD and correlation logic

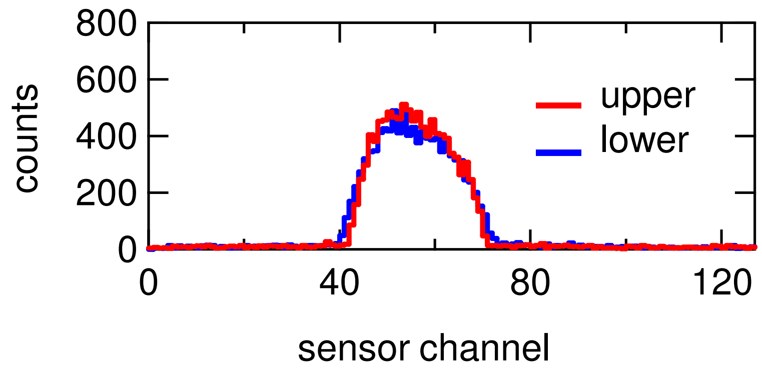
=> can sense and trigger on ~low energy γ's interacting in either sensor layer

self triggering setup

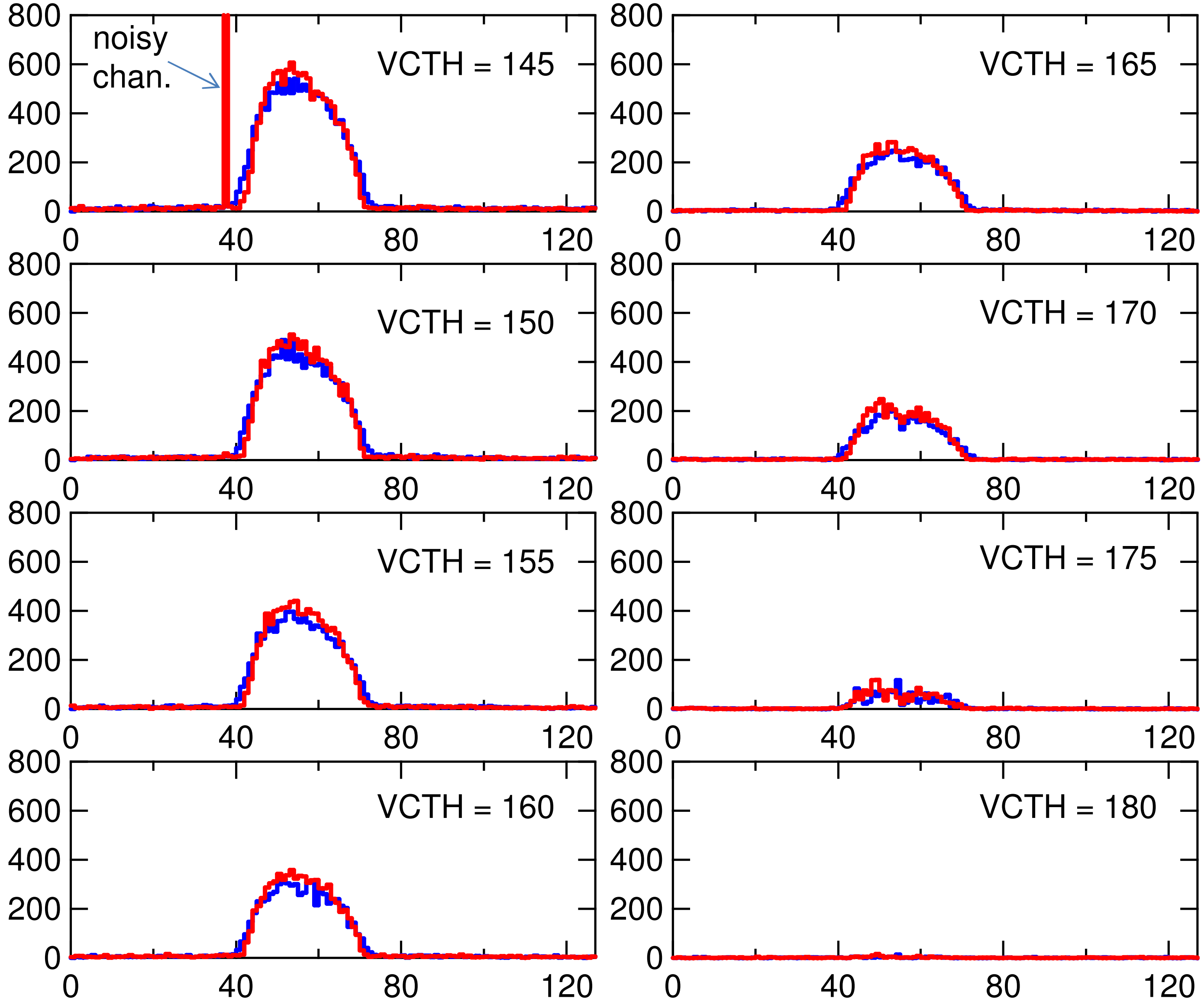


acquire data for fixed time interval
e.g. 100 seconds

histogram counts detected in each sensor



self triggering results vs. comparator threshold



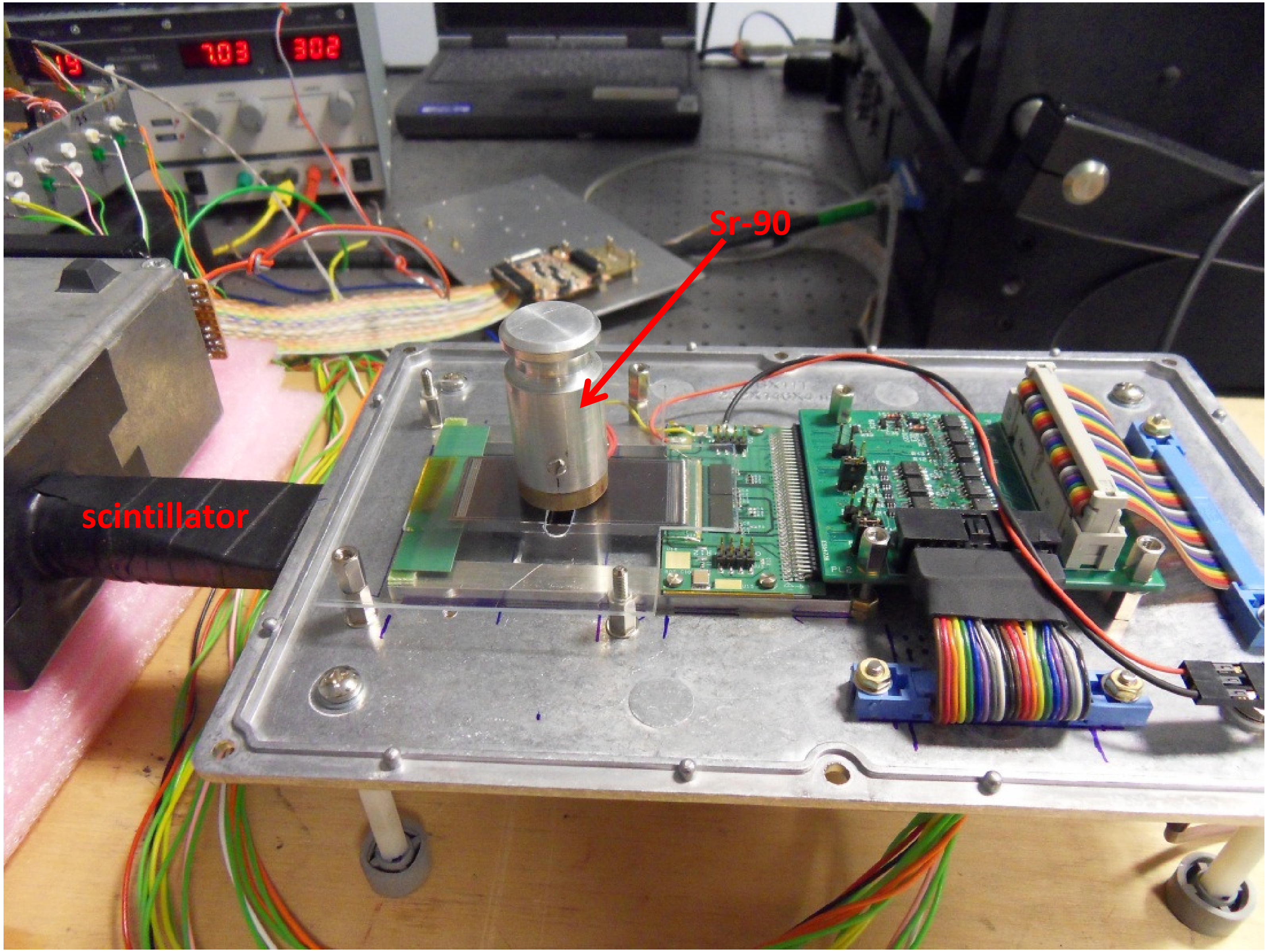
significance

might be useful for verifying sensor alignment if can achieve much finer collimation

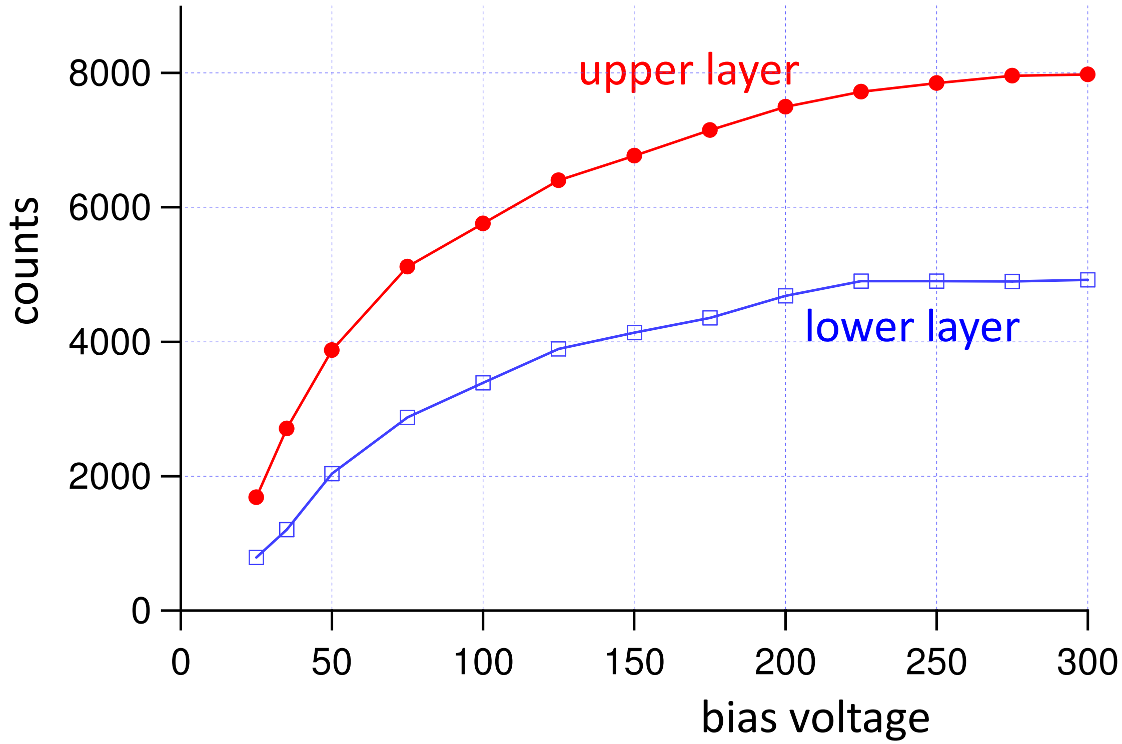
also quick and easy way of verifying functionality - don't need scintillator trigger

extra

mini-module in test setup



signal vs. bias - mini-module#**1**



method:
threshold set at ~ 1 fC, Sr-90 source
look at one channel from each layer in middle of area “illuminated” by source
count number of times comparator fires for 100,000 scintillator triggers

counts saturate as bias voltage approaches 250 Volts

consistent with depletion behaviour measured in Vienna

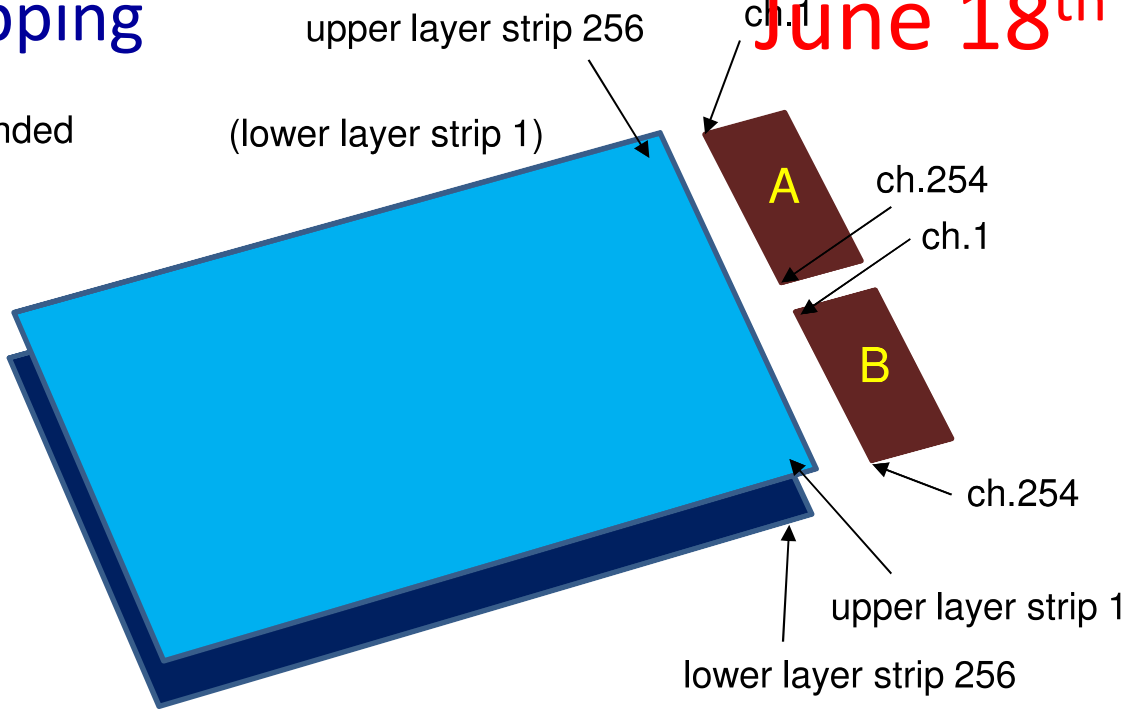
(other module behaves similarly)

channel to strip no. mapping

June 18th

2 edge channels on each sensor not bonded
(i.e. strips 2 - 255 inclusive bonded)

main point to note: lower and upper sensor layer channels feed alternating channels on each chip



chip channel vs. sensor strip #

	chip A									chip B								
	2	4	6	8	.....	.....	250	252	254	2	4	6	....	....	248	250	252	254
upper sensor	255	254	253	252	.....	....	131	130	129	128	127	126	....	...	5	4	3	2

	chip A									chip B								
	1	3	5	7	.....	.....	249	251	253	1	3	5	....	....	247	249	251	253
lower sensor	2	3	4	5	...	....	126	127	128	129	130	131	...	...	252	253	254	255

leakage behaviour for both modules

mini-module#1

bias [V]	leakage [uA]
20	1.02
50	2.6
100	6.1
200	16.4
300	35
400	60

mini-module#2

bias [V]	leakage [uA]
50	0.28
100	0.56
200	1.3
300	2.5
400	5.6
500	13.8
600	39.3

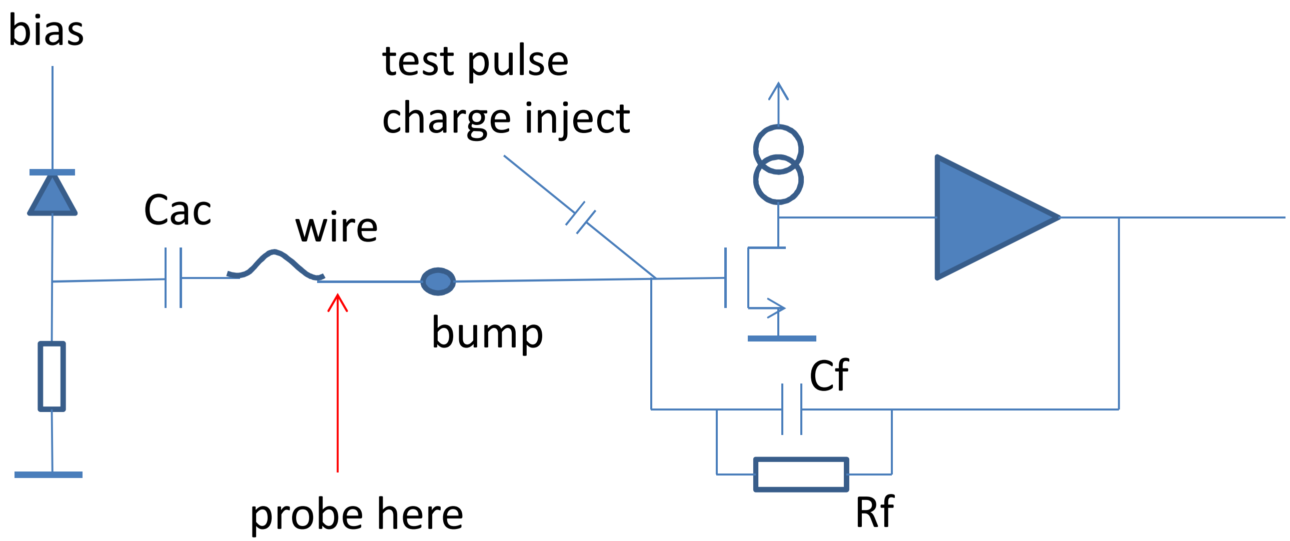
tables show leakage (both sensors) dependence on bias

bias voltage taken to a level where noisy channels start to appear

will only show noise sorted by sensor , for each module

note: one chip only now working on module#2. CBC2B got damaged when probing sensor to verify bias voltage getting through to strips (not sure how it happened)

investigating low-noise module channels



behaviour observed consistent with failure of connection between strip and amplifier

poor wire contact? something wrong with sensor?

failed bump-bond seems the most likely?

if can place grounded probe on wire-bond pad on hybrid then can switch off input transistor and channel will no longer respond to test pulse

if bump-bond has failed then channel will still respond to test pulse

hybrid status summary

(those that have passed through Imp. College)

1st batch of 5 (all not under-filled)

- #1 in electrical test setup at IC
- #2 to Bristol for first tests with FMC, now passed on to Strasbourg
- #3 problem with I2C lines disconnected at connector - repaired - keep at IC
- #4 -> mini-module #1
- #5 -> mini-module #2

2nd batch: 4 under-filled, 2 not

- N01 at IC
- N02 at IC
- U01 at IC
- U03 at IC
- U04 -> Bristol for FMC development (will come back with FMC to IC)
- U06 all channels probed, to CERN for mini-module#3
- U25 all channels checked (10/13), to CERN for another mini-module
- U26 all channels checked (10/13), to CERN for another mini-module