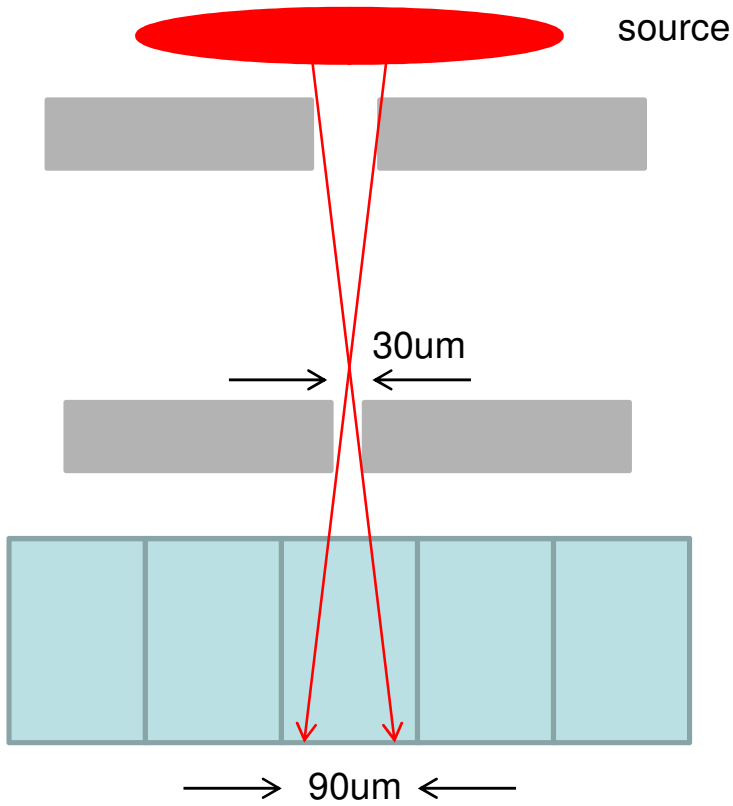
CBC2 and CBC3 news

CNM module with Am-241
CBC3 design progress

M.Raymond/M.Prydderch, Electronics for 2S and PS-Pt modules, 11/11/14

CBC2: work in progress



Am-241 studies - 59.5 keV (16.5k electron signal)

If can make sufficiently narrow collimator can capture all signal in single strip => useful calibration point

need a narrow collimator slit ~30 um

need to take care with positioning

- collimator exit slit has to be close to silicon surface and aligned with some precision
- range of 60 keV photoelectron ~ 25 um so need all interactions to be >25um away from edge of strip

need a high activity source

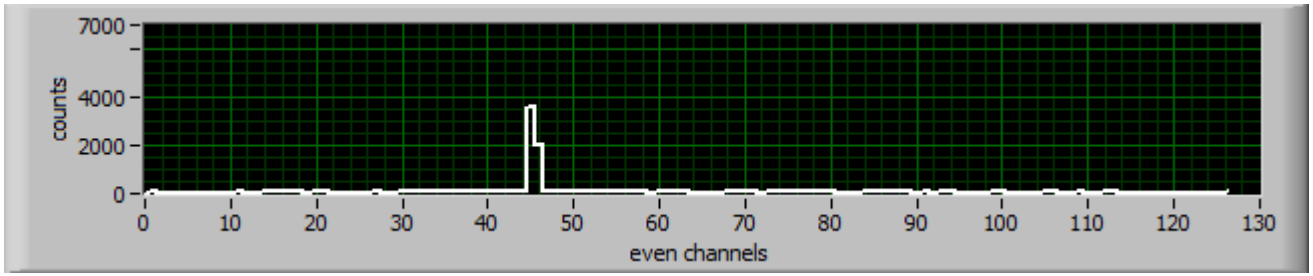
- ~500MBq -> single strip count-rate ~5 Hz
- => takes many hours to sweep VCTH and acquire a spectrum with good statistics

programme CBC2 in OR254 mode -> self-triggering

- any signal in any channel above threshold will fire trigger output

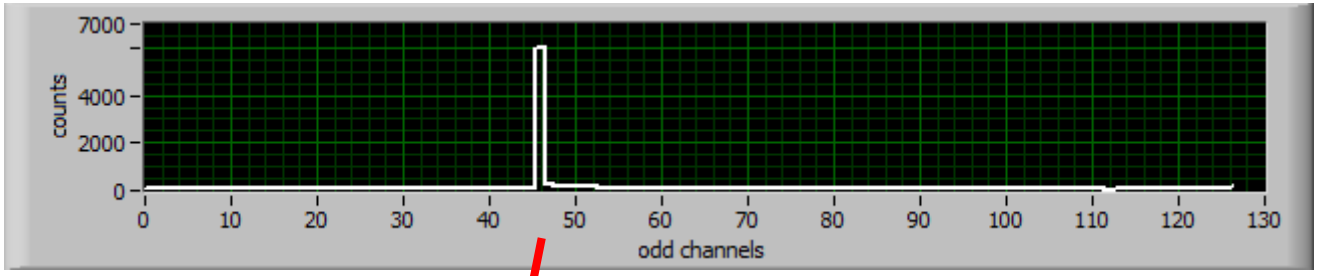
have started to make measurements on CNM module

Am-241 measurements - CNM module

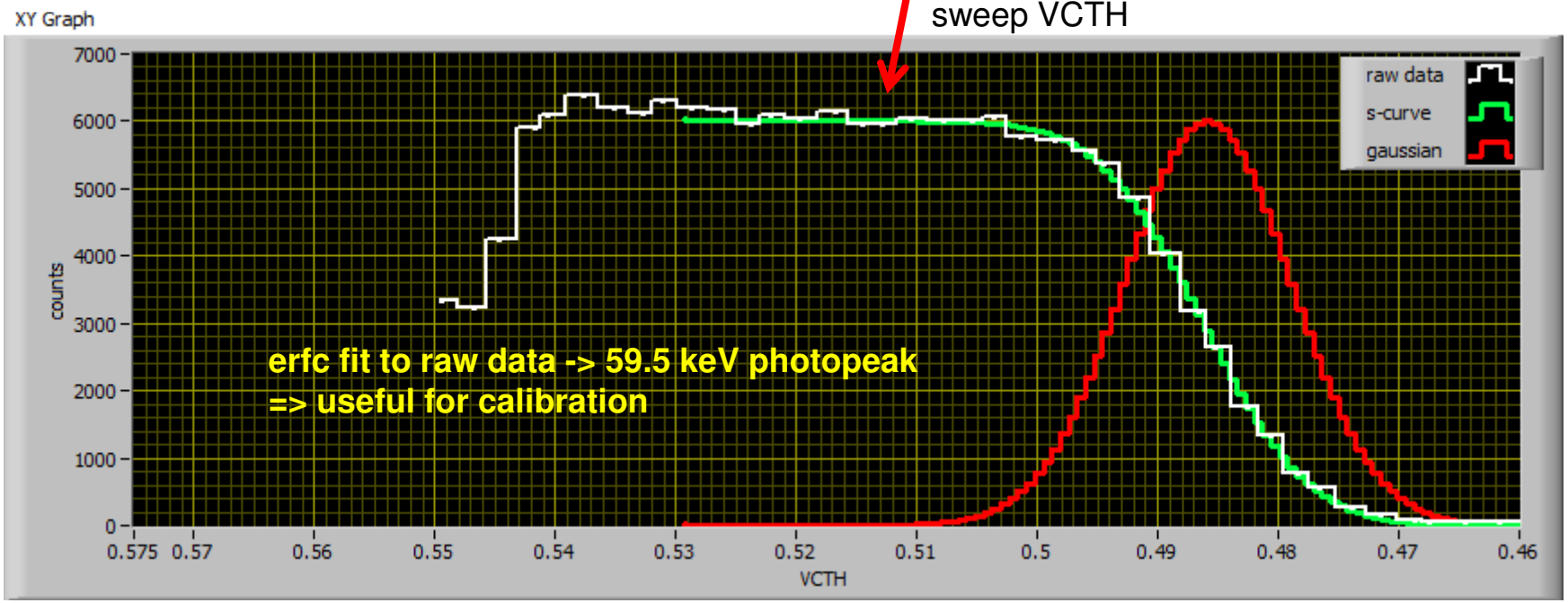


signal in one sensor layer
split between 2 channels

signal in other sensor layer
confined to 1 channel
=> successful alignment

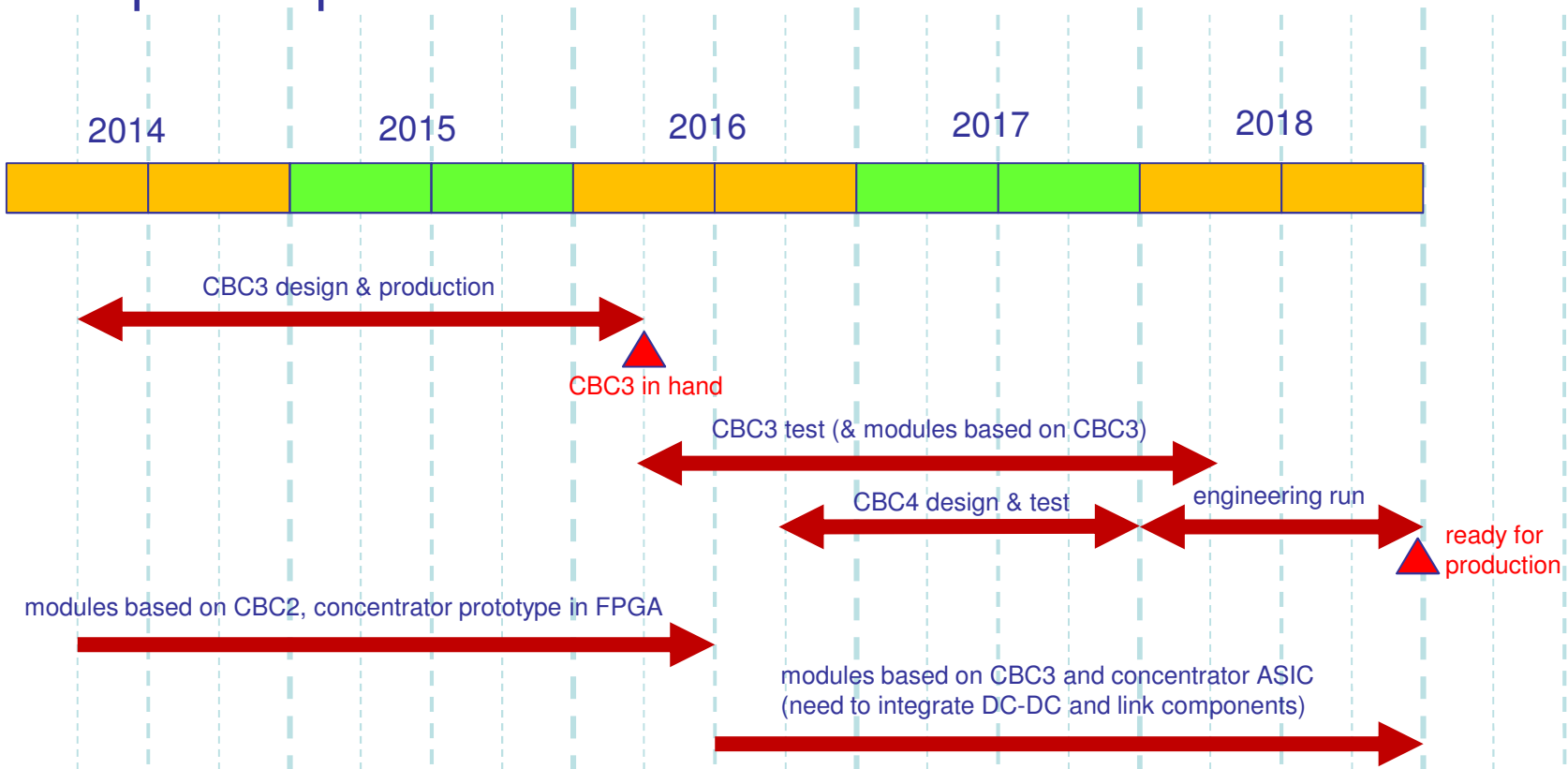


sweep VCTH



VCTH in Volts (measured using analogue MUX)

CBC development plan reminder



CBC3 is intended to be the final version of the chip
should appear ~ 1st half 2016
CBC4 is an “insurance iteration” if something has to be fixed

CBC3 design progress at RAL

Mark Prydderch, Michelle Key-Charriere, Davide Braga

- SRAM cell status
  SRAM cell has been re-designed - PMOS switches and enclosed NMOS

- I2C cell SEU sensitivity

  improving hardness of triplicated logic means increased size to keep storage cells further apart
  SEU resistant Whitaker cell used in pipeline not much larger
  currently propose to look at replacing I2C storage cells with this

- correlation/stub finding logic with ½ strip resolution

  completed at coding and circuit level for 5 bit bend info generation
  awaiting decision on bend info changes before proceeding to layout

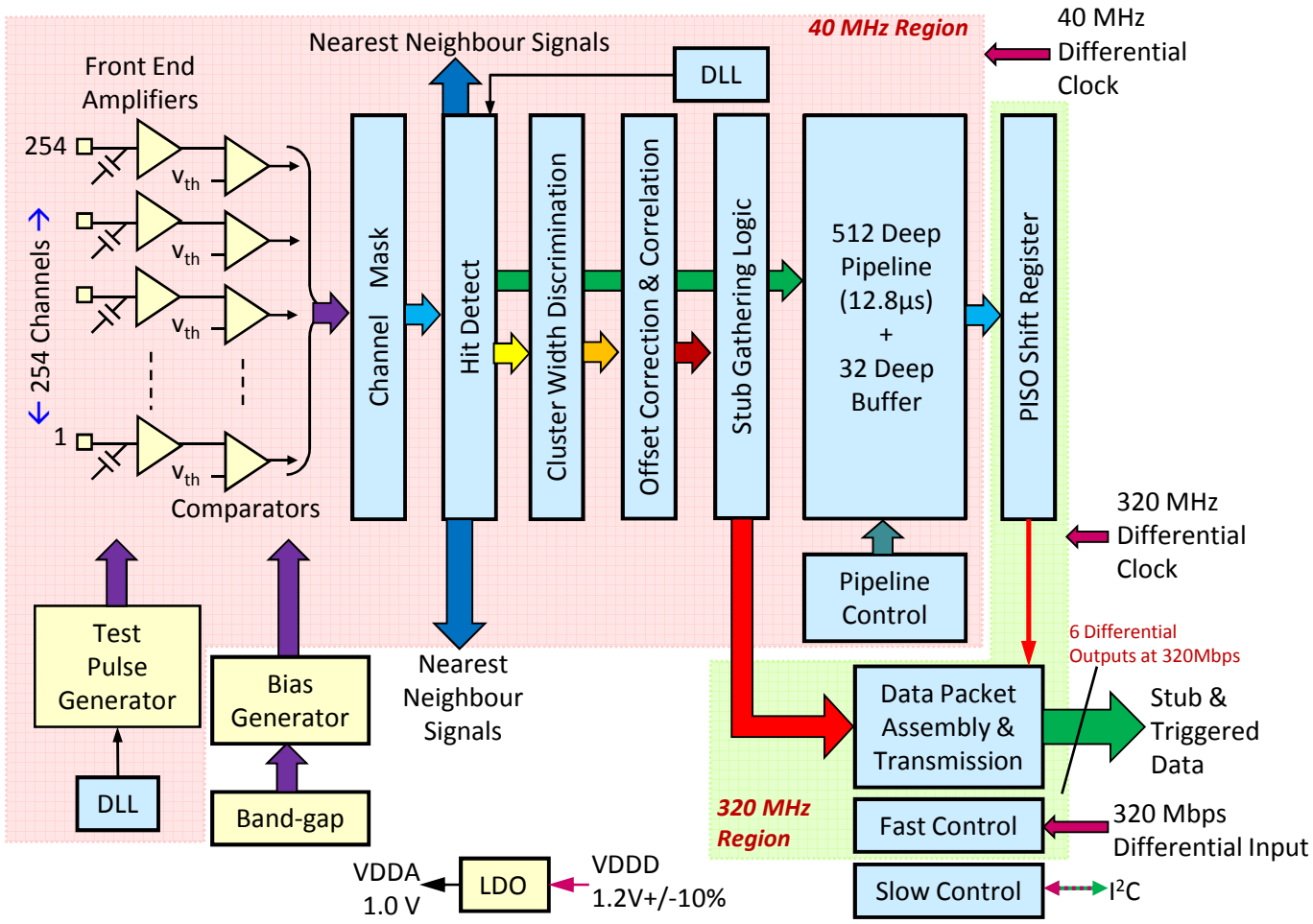
- logic for transfering 3 stub addresses to data assembly circuitry completed to layout stage

- data assembly circuitry currently under design

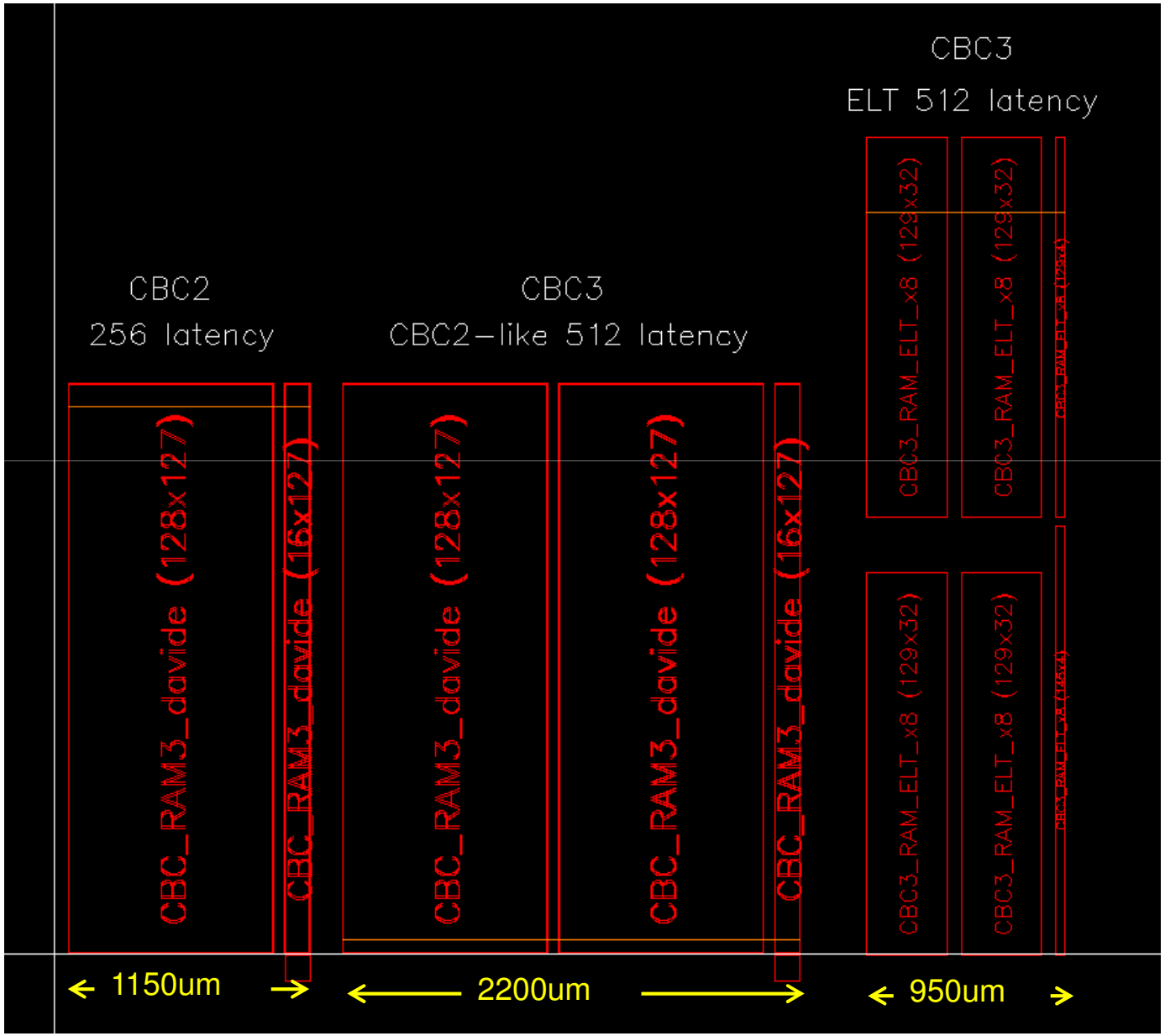
- CBC3 specification document almost complete - needs choice of bend info

- top level simulation constructed to verify synchronization of data from different time domains

CBC3 architecture



CBC3: Options for extended pipeline



next 2 slides from Mark Prydderch following discussions of options for CBC3 submissions

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CBC development options

Full Size CBC3 (current plan) – Size estimate ~66mm^2

- MOSIS Submission: Cost estimate = $212,360 (+ 7% CERN DK levy?)
  Number of Devices = 40 (Possible to buy more at a cost?)
- Engineering Run: Cost estimate = $450,000 for 2 wafers (extra wafer costs $4000). Number of Devices = ~420/Wafer
- Shared Engineering Run: Cost estimate = *Unkown* – What will our share be? Who will share?

Mini CBC3 – Size estimate ~33mm^2 for ½ size or ~17mm^2 for ¼ size.

- MOSIS Submission:
  - ½ size Cost estimate = $106,430; Number of Devices = 40
  - ¼ size Cost estimate = $55,070; Number of Devices = 40

Test Structures

- Which circuits?:
  - Pipeline? – Could test radiation hardness.
  - Pre-amp? Discriminator?
- Cost estimate = *Unkown* (No minimum die size imposed)

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CBC development options

Full Size CBC3 (current plan) →

- PRO: Can be useful to community; Closer to final chip
- CON: Cost
- MOSIS Submission:
  - PRO: ½ price of full run
  - CON: Only 40 devices; Restricted run schedule
- Engineering Run:
  - PRO: Possibly no more NRE; Lots of devices; Flexible submission
  - CON: Full price
- Shared Engineering Run:
  - PRO: Lots of devices; Semi-flexible submission; Shared cost
  - CON: Unpredictable

Mini CBC3 →

- PRO: Scalable to final chip; Tests all functions; Uses same test hardware(?)
- CON: Almost the same effort as full chip; Would it be used by community?

Test Structures →

- PRO: Low manufacturing cost; Low risk
- CON: Diverts resource (effort & money) away from progress to final full chip; Additional circuits required that aren't useful to final chip; Requires new test hardware; Requires additional effort for testing; Of no use to community