CBC2 ionizing irradiation results

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recap of results from 1st irradiation

new results from cold irradiation

progress in understanding what's going on

new results from irradiation to higher dose levels

systems meeting, 29th July, 2014.

recap from last time

1 chip irradiated to ~ 12 Mrads
X-rays (Mo tube)
(see * for dose calculations)
room temp. ~ 30°

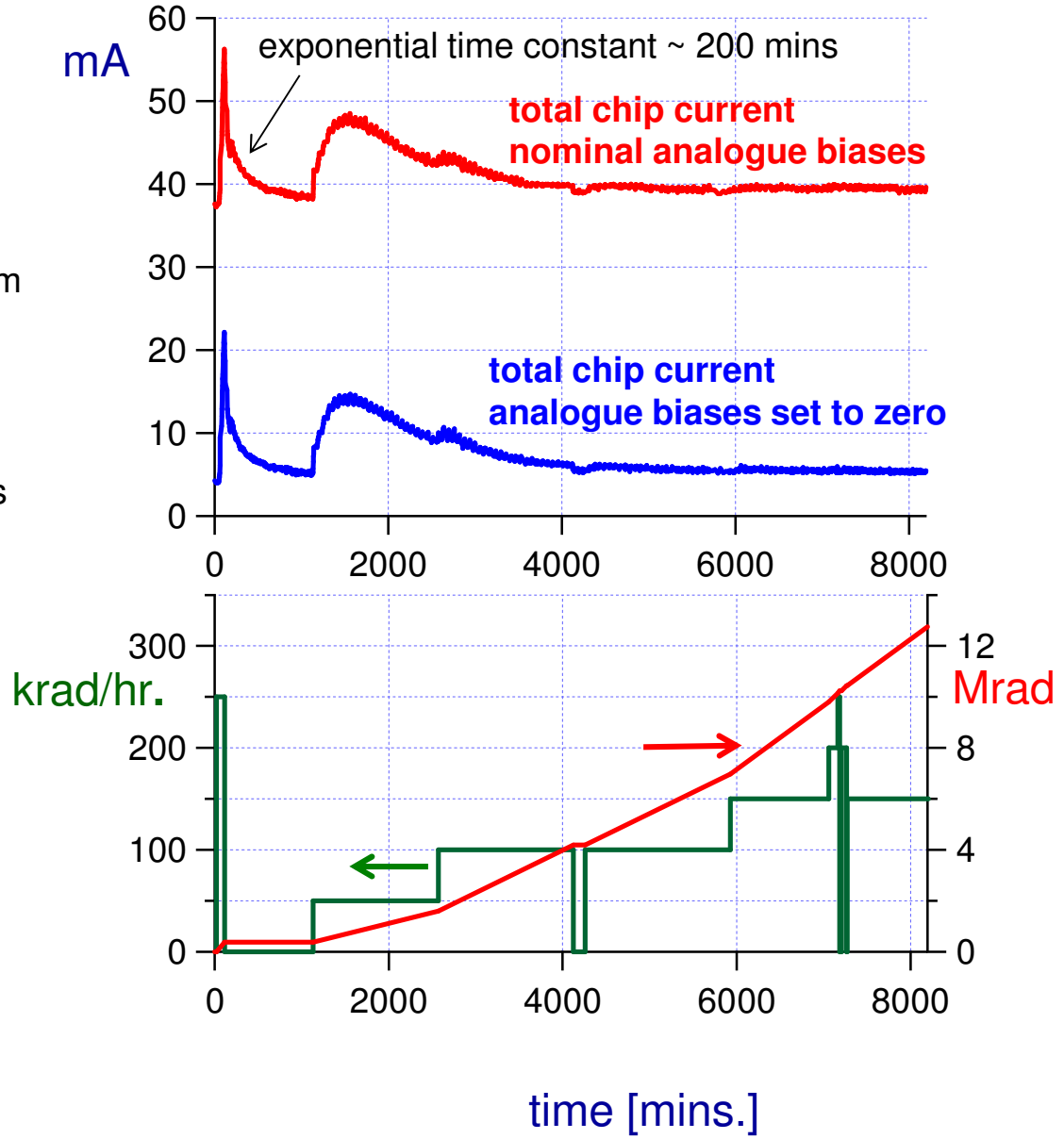
no significant change to behaviour apart from

current increase during early stages
of irradiation ~ 1 Mrad
decays away if stop irradiation
effect disappears at higher dose levels

so not necessarily a problem, but

chips in HL-LHC will be cold
- does that affect the behaviour?
(the rate current decays away)

not clear what is going on and in
what part of the chip
(no separation between
analogue/digital supplies)



*Davide's presentationfrom last time;
https://indico.cern.ch/event/312869/session/1/contribution/7/material/slides/0.pdf

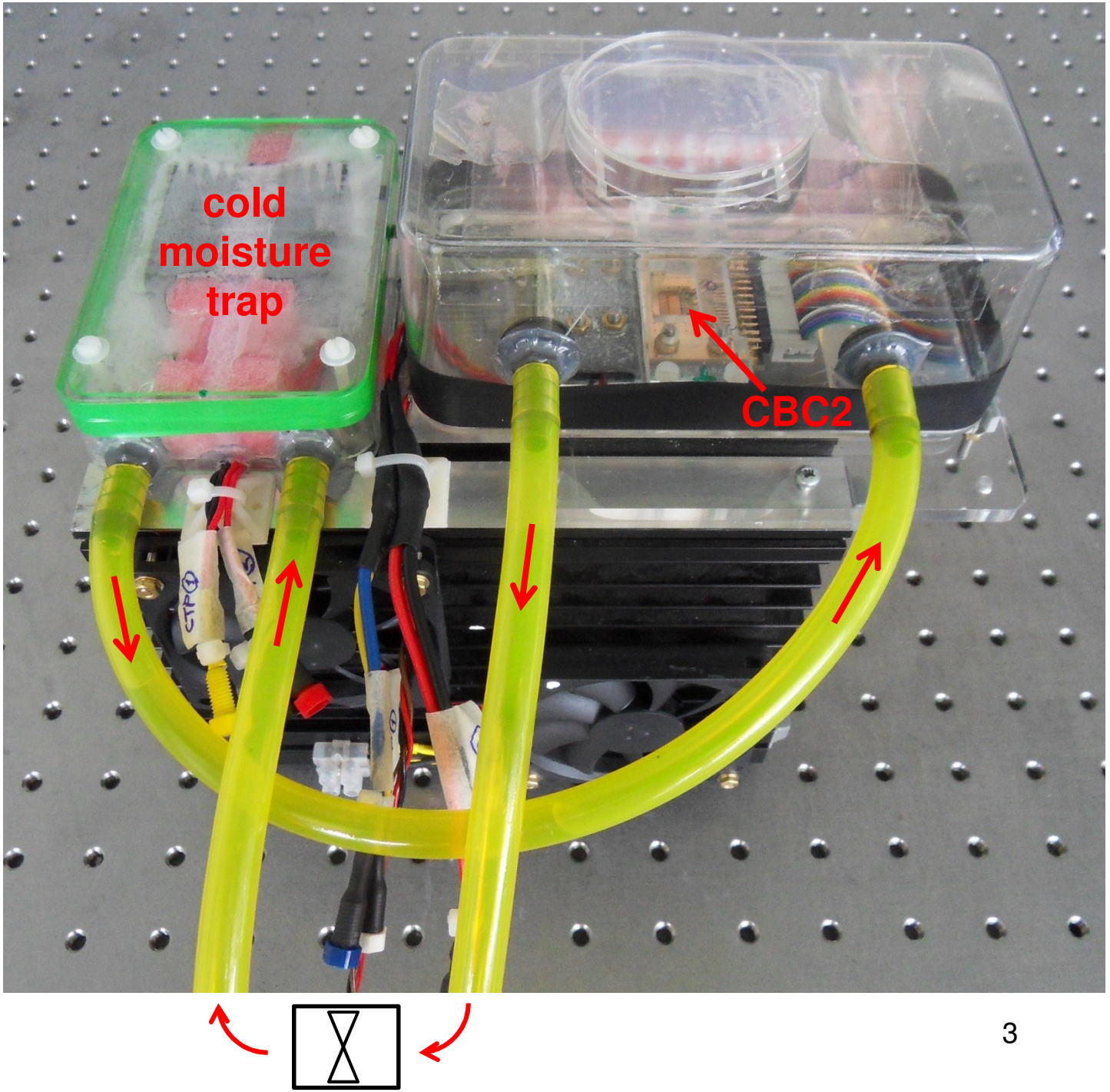
cooled setup

CBC2 mounted on stacked Peltiers mounted on massive heatsink

dry air circulated

CBC2 temperature regulated to -15°

(ambient ~+30° inside X-ray cabinet)



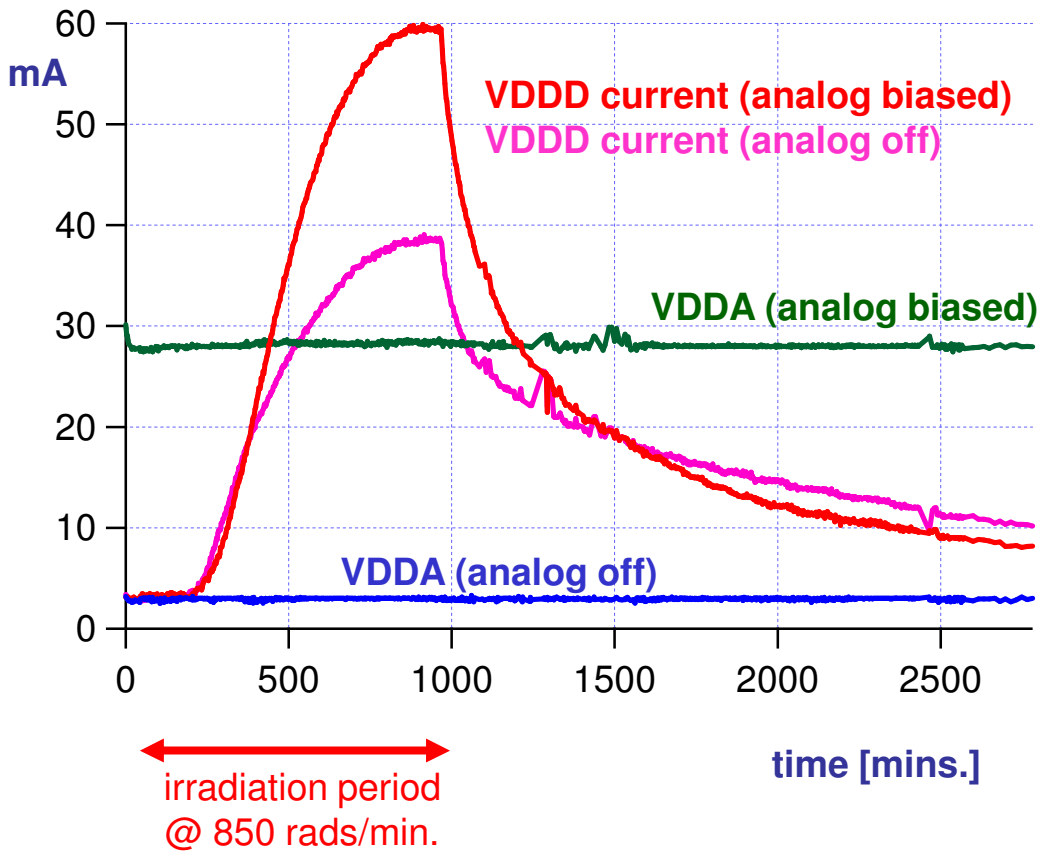
cooled setup results

VDDD and VDDA now supplied separately

current increase clearly confined to the digital rail (VDDD current)

but magnitude depends on whether analog stages biased or not

(this caused a lot of puzzlement & speculation…)



current saturates at around 800 krads
stopped irradiation at this point

current still decays away with time constant ~ 1000 minutes, even at this cold temperature
(c.f. ~200 minutes at ~30^{o})

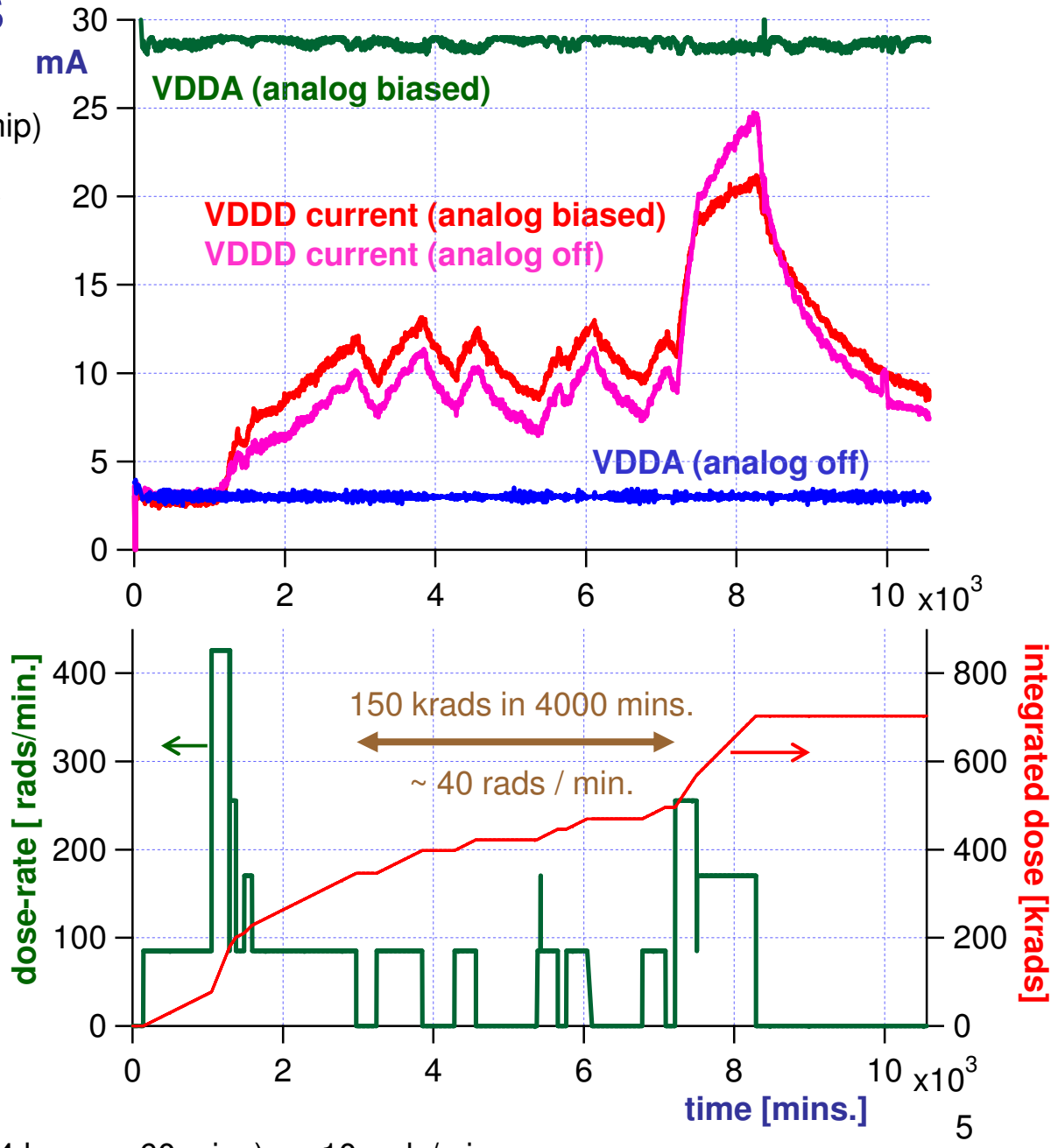
but 850 rads/min is ~ 85x the worst case doserate at HL-LHC
will we see anything in the experiment?

cooled setup results

try a low dose-rate irradiation (new chip)

couldn't get continuous dose-rate low enough as that at HL-LHC*

but current plateaus at
~ 40 rads / min.



*30 Mrads / (10 years x 200 days x 24 hours x 60 mins) = ~10 rads/min

summary so far

new cooled irradiation setup shows:

current increase confined to digital supply rail (VDDD)

but magnitude affected by values in analog bias registers (nominal or zero)

current is not “frozen in” by operation at low temperature (- 15^{o})

continuous “decay” process still going on

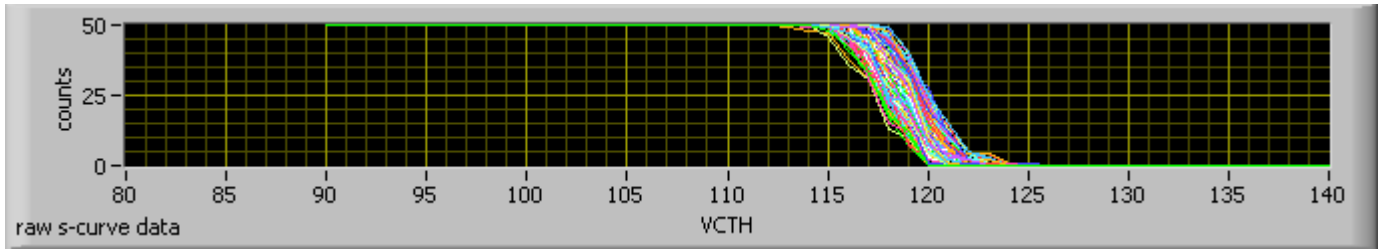
=> should not be significant at HL-LHC dose-rates

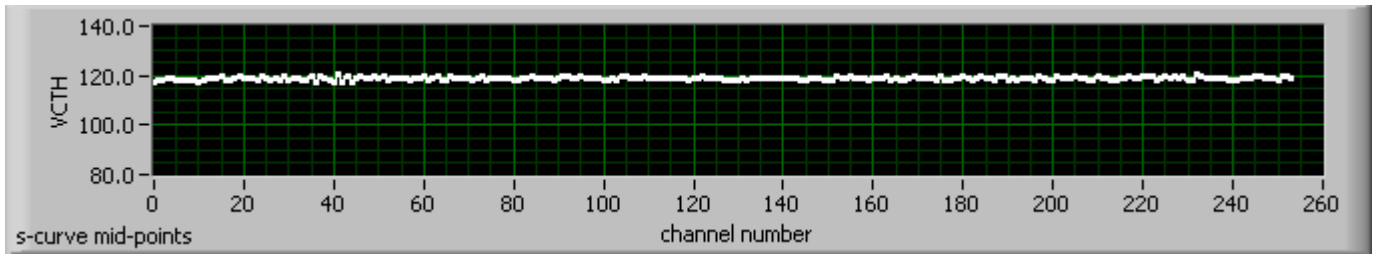
but where is the current flowing?

another clue: chip stops responding to test pulse when in high digital current regime

some kind of effect in front end? - but no VDDD there

s-curve data acquired before irradiation

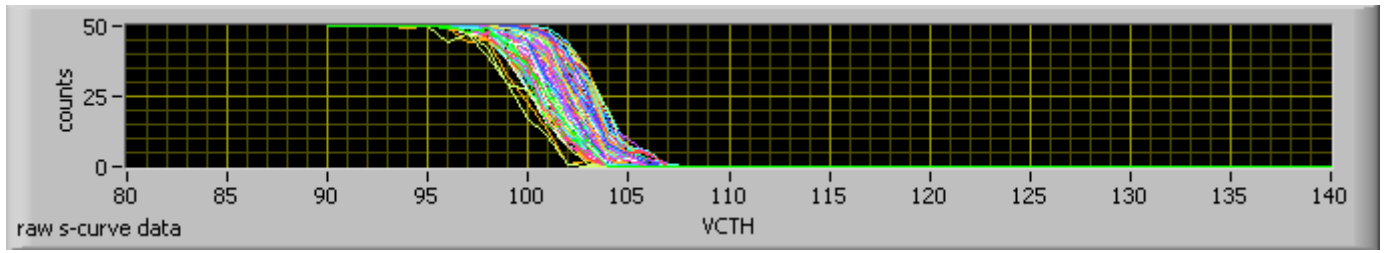


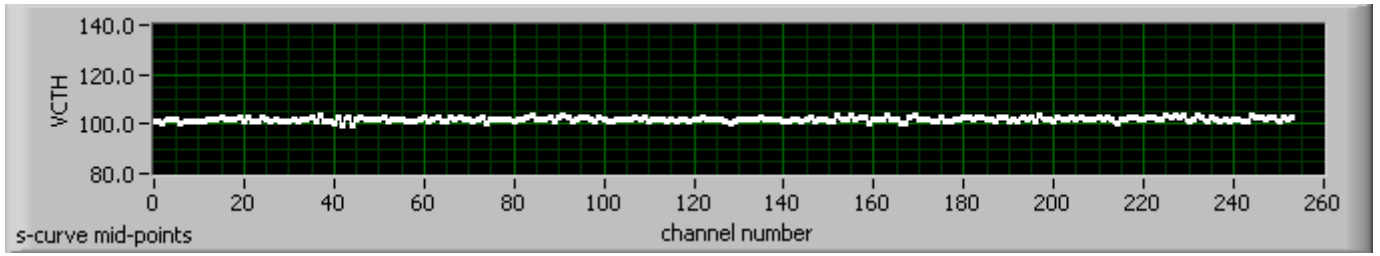


pedestals s-curves

offsets tuned for s-curve mid-points centred on VCTH = 120

results here show normal behaviour

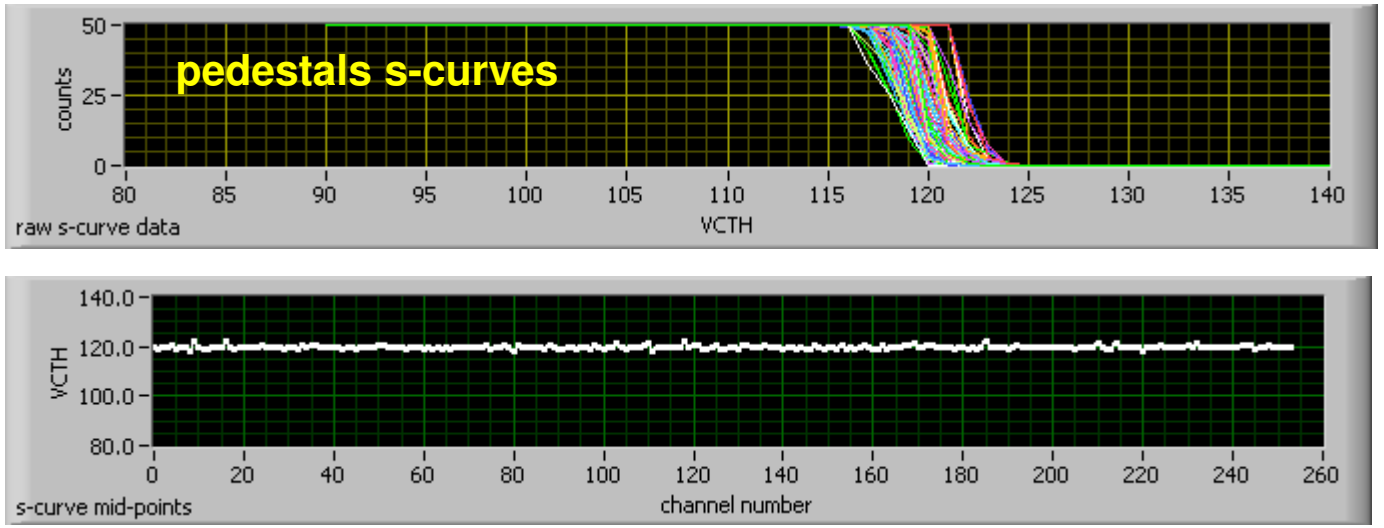




test pulse s-curves

s-curve mid-points at VCTH ~ 100

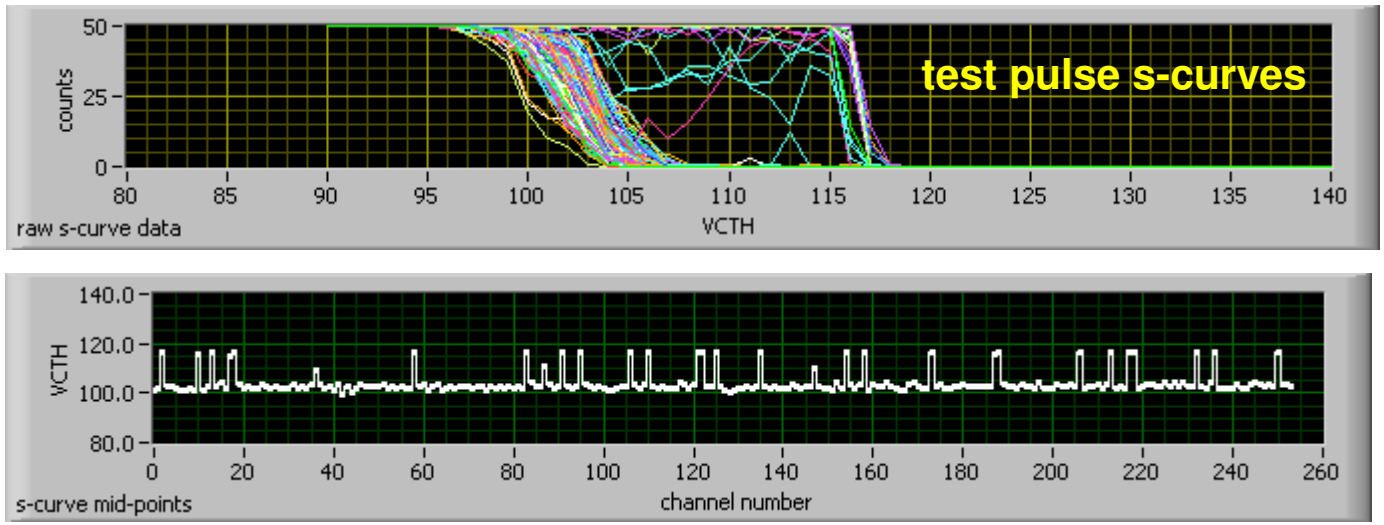
s-curve data acquired during irradiation



results here for increased VDDD current region

no obvious effect on pedestal s-curves

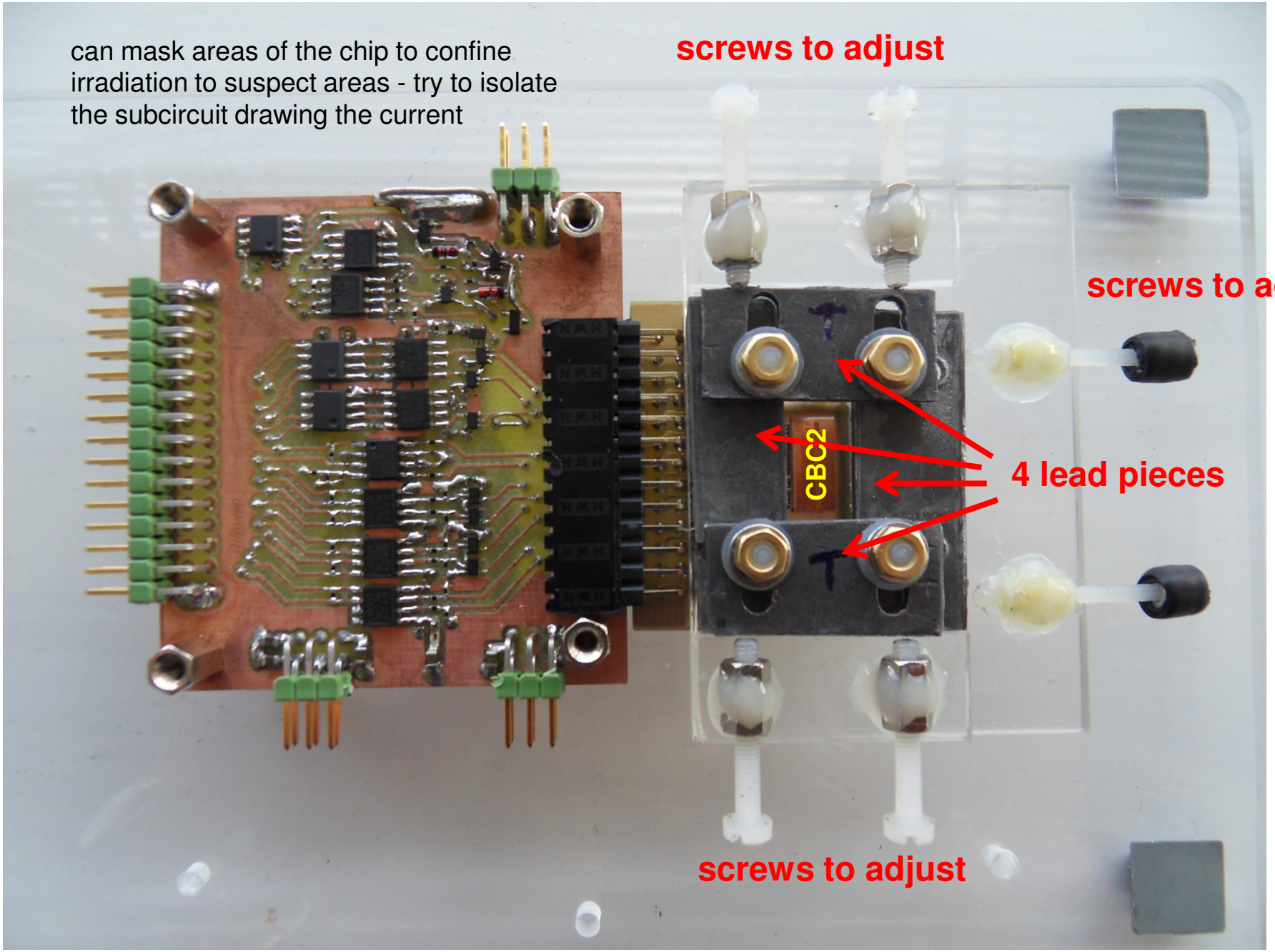
but obvious effect on test pulse s-curves - some (eventually all) channels stop responding in high current region



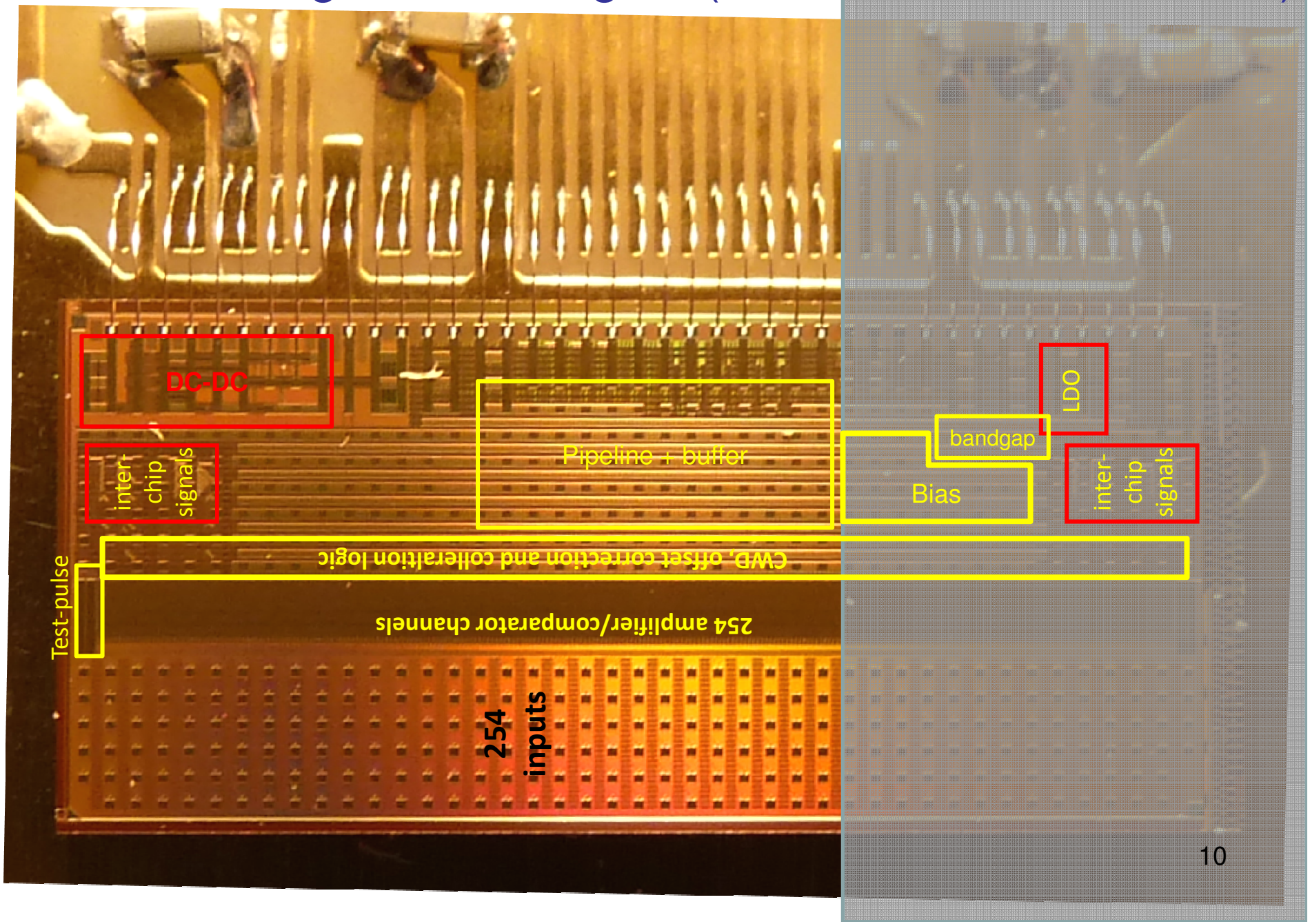
channels subsequently return to normal operation when high current region is passed

chip masking setup

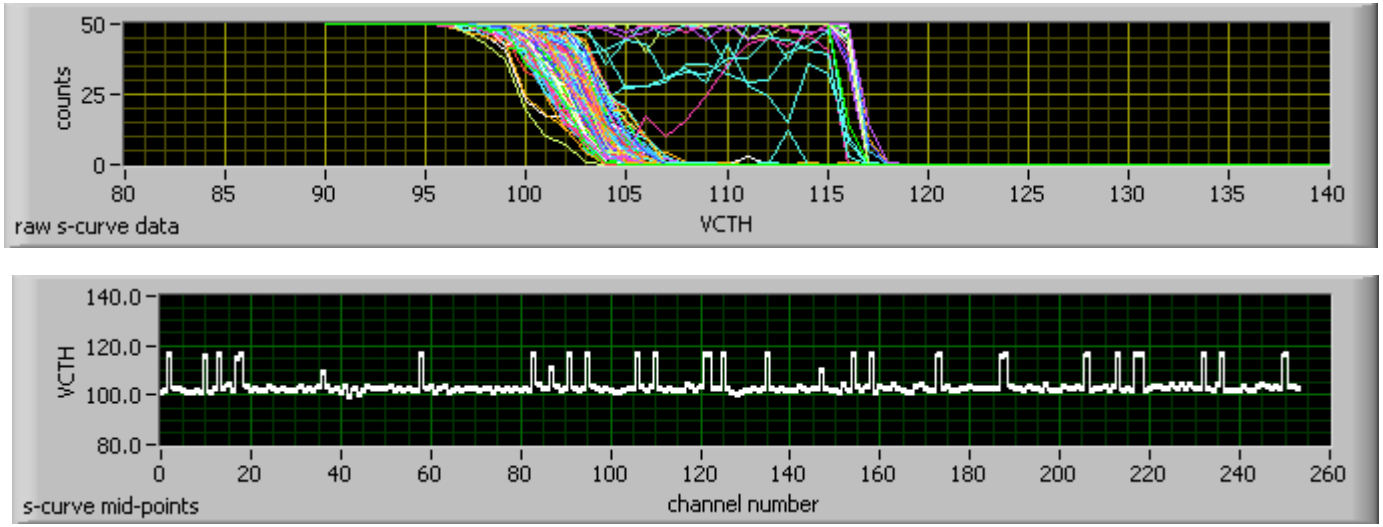
can mask areas of the chip to confine irradiation to suspect areas - try to isolate the subcircuit drawing the current



mask 1: bias generator region (& some front end chans.)



results for mask 1



results for higher VDDD current region

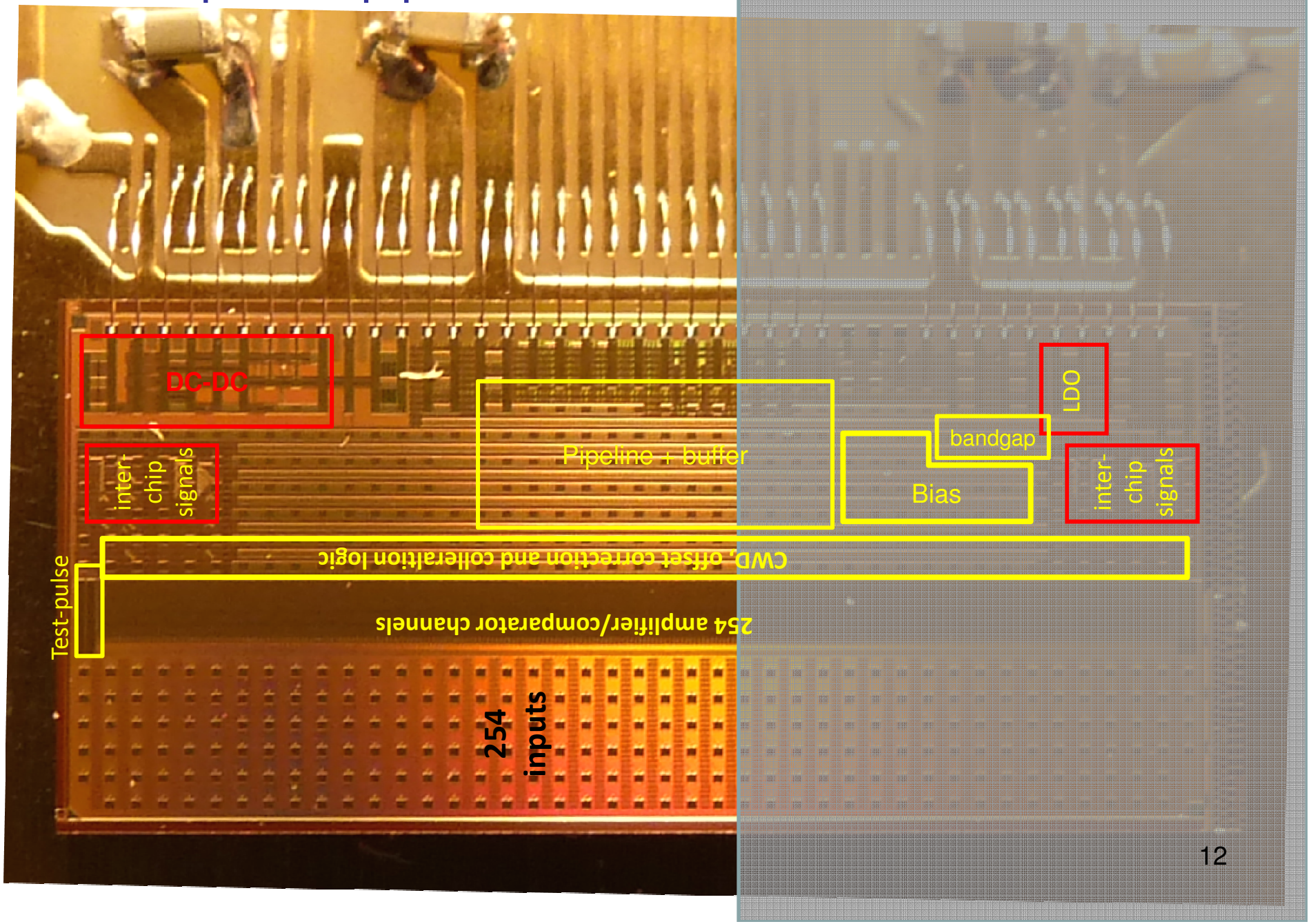
channels affected across whole chip width

no difference between those masked / not masked

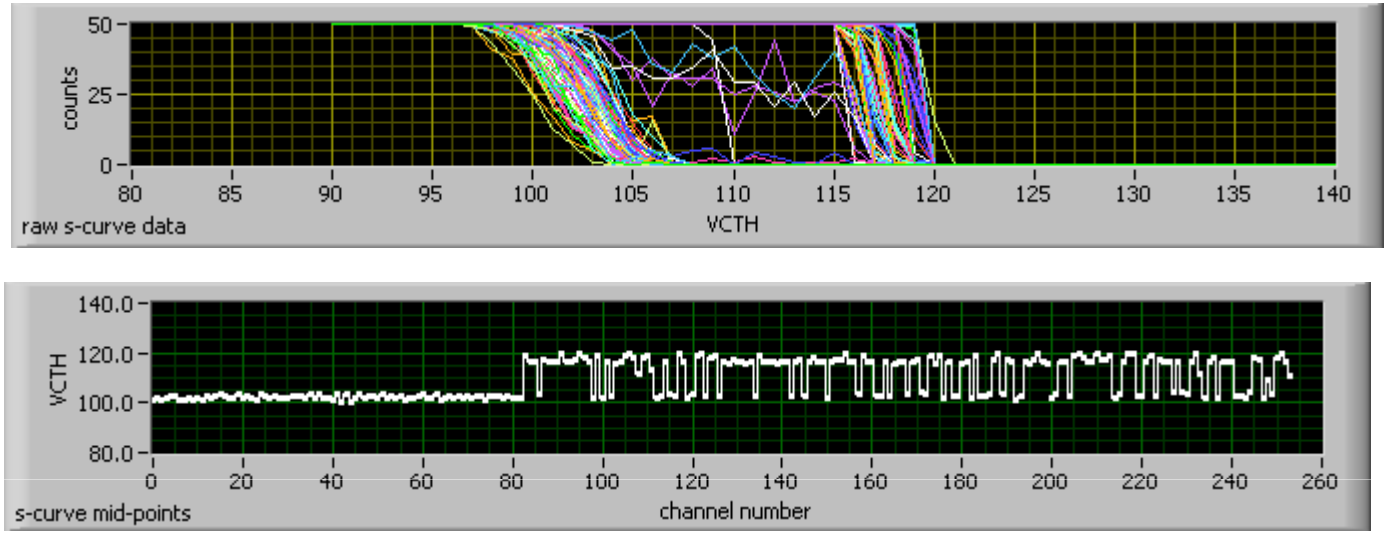
=> bias generator area of chip not implicated

so why the difference in excess current when chip biased or not?

mask 2: part of pipeline now masked



results for mask 2

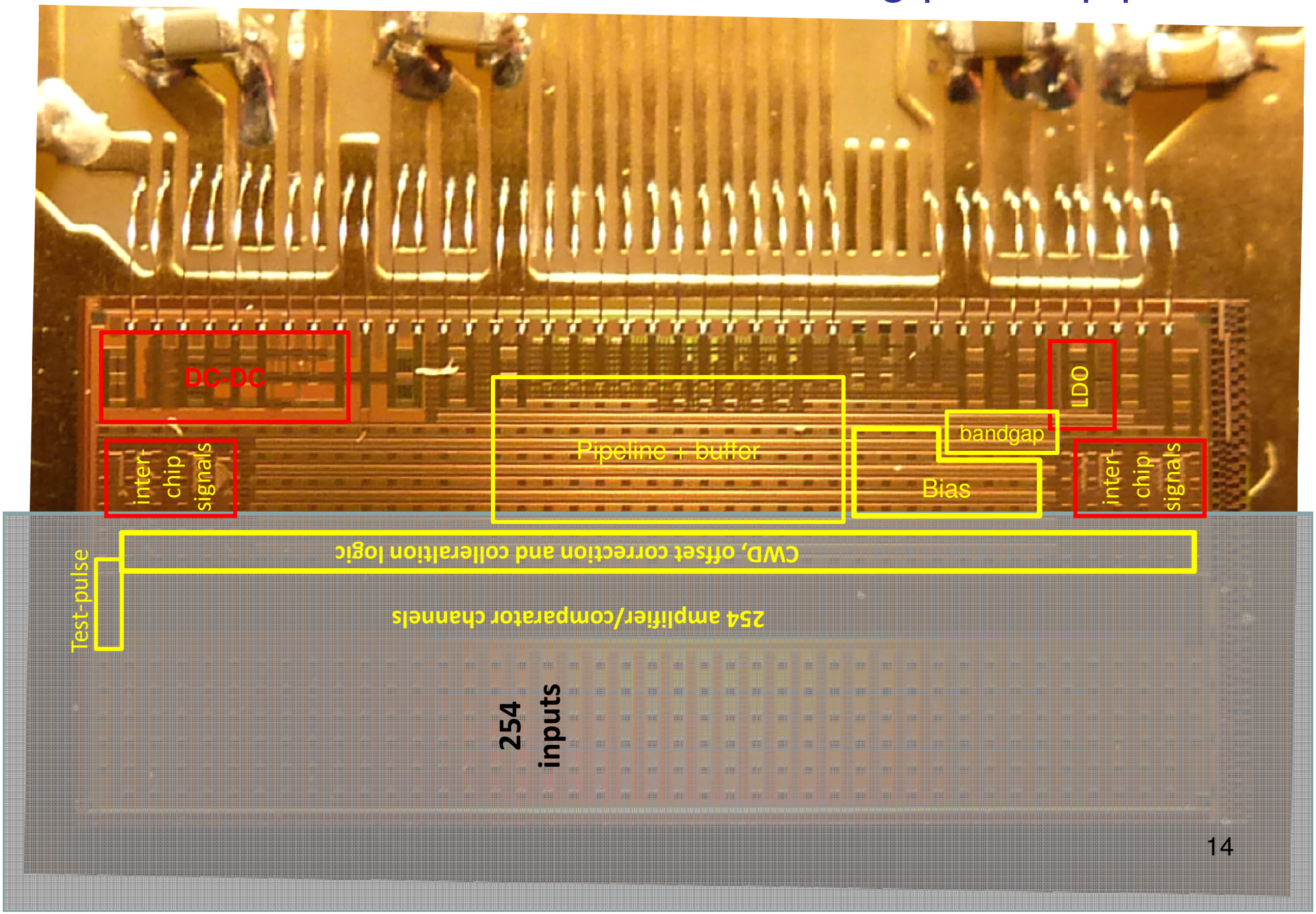


clear difference between masked and unmasked region

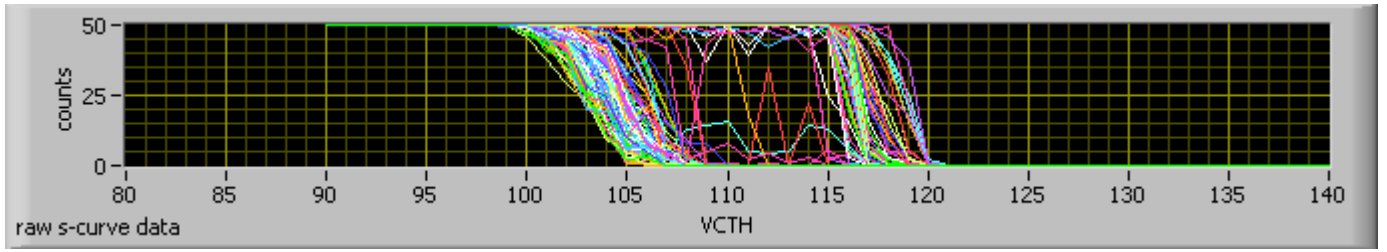
started to suspect hit detect circuit, pipeline driver/readout, …

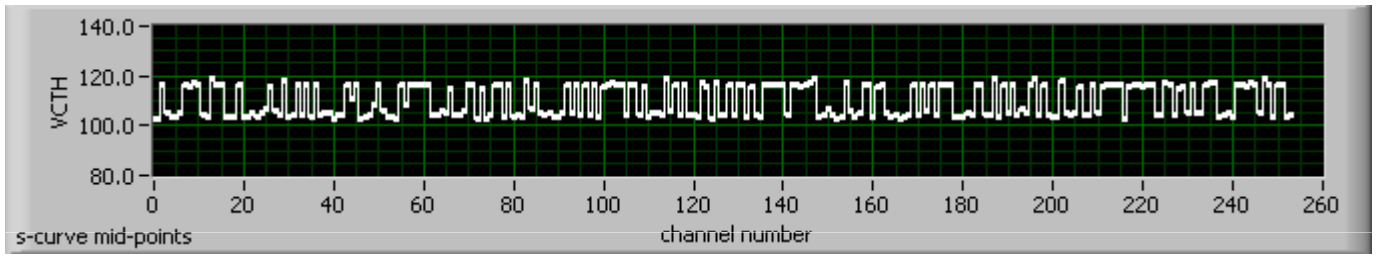
looks like front end not implicated, but why is test pulse response affected?

mask 3: all front end masked, including part of pipeline



results for mask 3

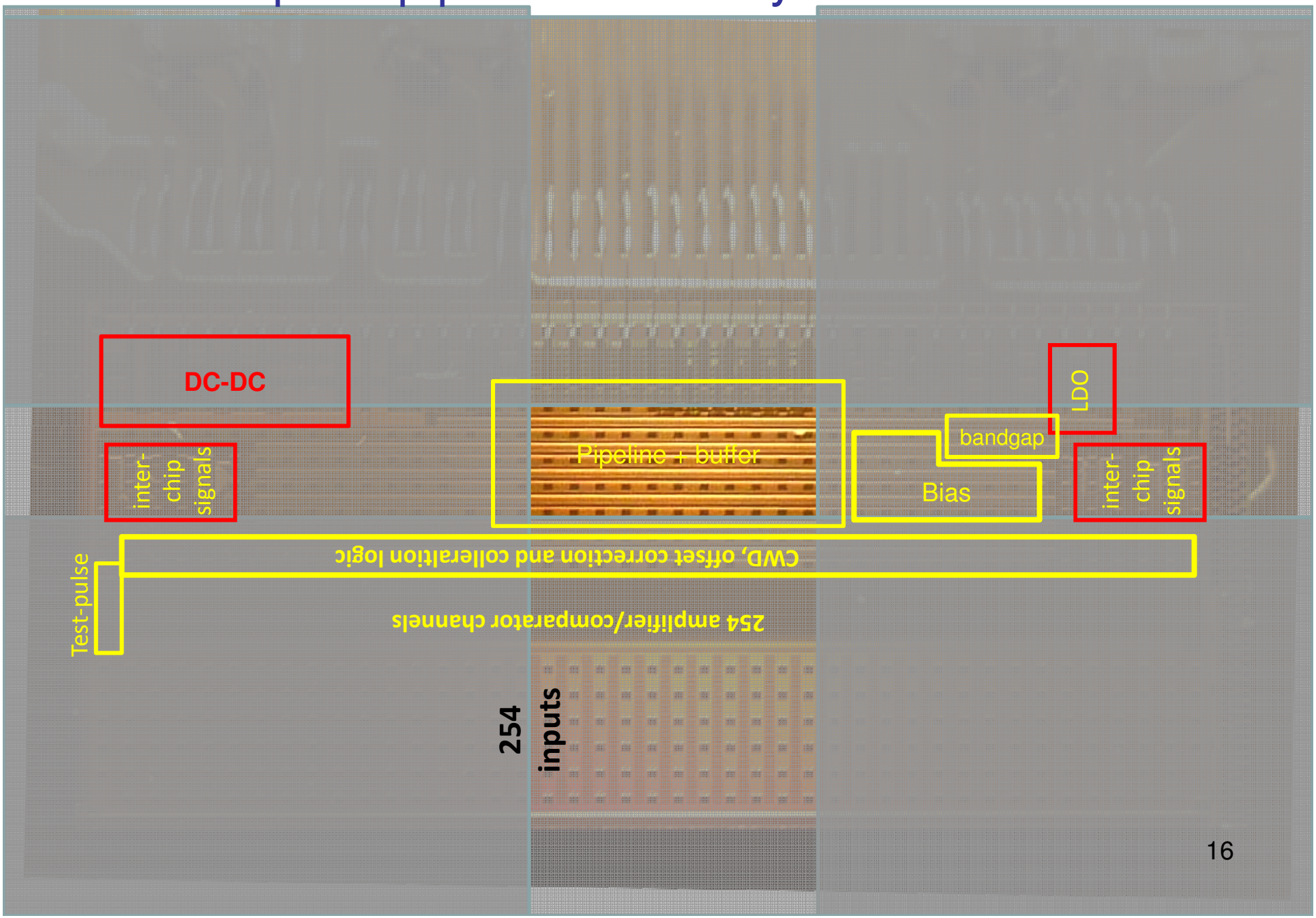




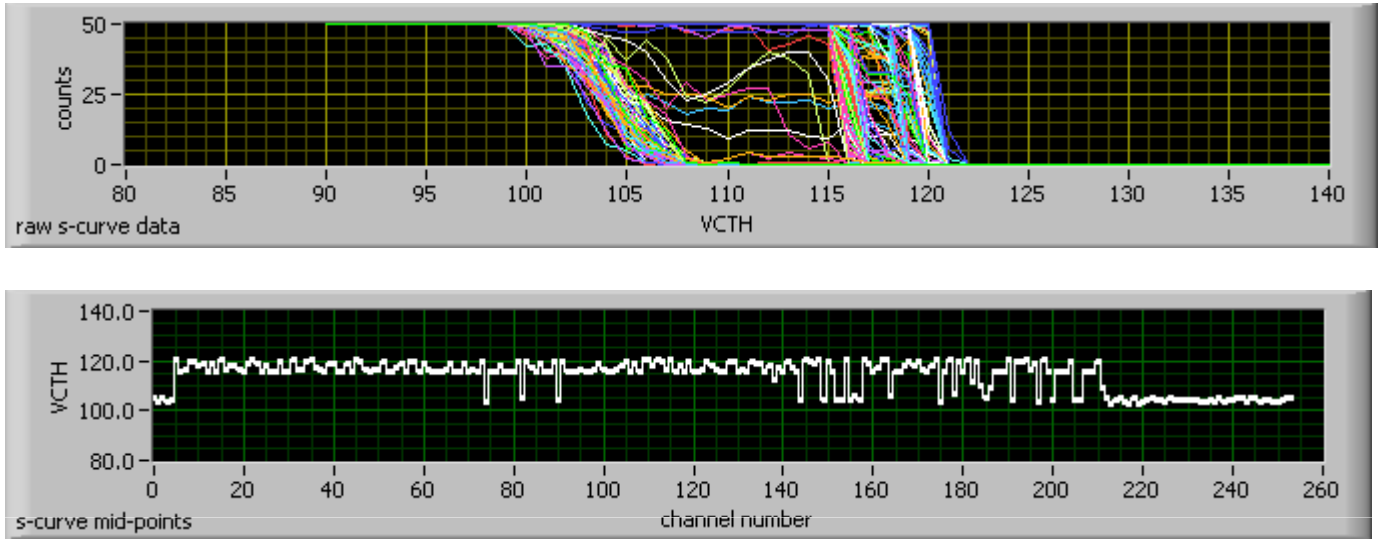
channels affected across whole chip width

front end effect excluded - what's left?

mask 4: expose pipeline core only



results for mask 4



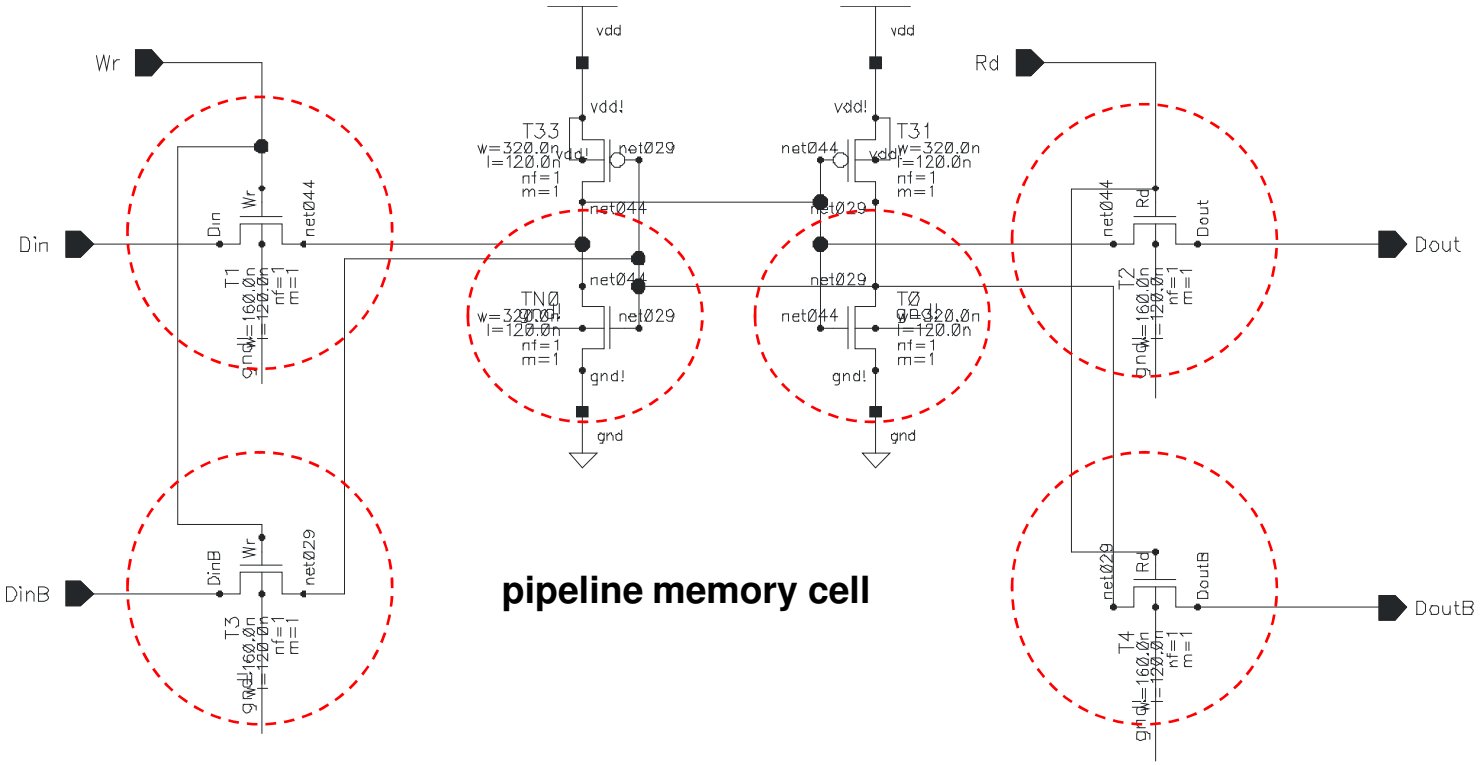
it's the pipeline

central channels fail
masked channels at top and bottom still functioning

not a completely "digital" failure in that channels still all change state at ~ close to pedestal level

=> still get an s-curve
(which was what previously led us to suspect some kind of front end effect)

what's going on?



have to suspect NMOS transistors in pipeline cell (not enclosed)

probably the pass transistors as well as those in the inverter

what's going on?

F. Faccio and G.Cervelli* have measured a peak in the leakage current for non-enclosed NMOS devices, and explain it by build up of oxide-trapped charge being compensated by slower charge trapping in interface states

probably something similar happening in CBC2 pipeline

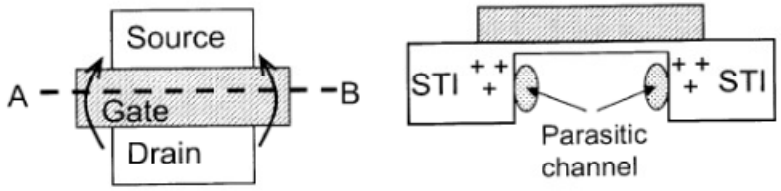


Fig. 1. Top view of an open-layout NMOS transistor (left). On the right, the same transistor is viewed along the A-B line (from the source or drain). The radiation-induced positive charge trapping in the STI is represented by the multiple crosses. This charge modifies the electric field at the edge of the transistor, possibly opening a conductive channel even when the main transistor is turned off. Leakage current can hence flow between source and drain—as indicated by the arrows in the top view.

there are some differences in that they used worse case bias conditions during irradiation

not the same for us - at least for the cross-coupled inverters

and we see a continuous recovery process

not clear (to me) whether they saw (or would have seen) the same thing for their measurement method

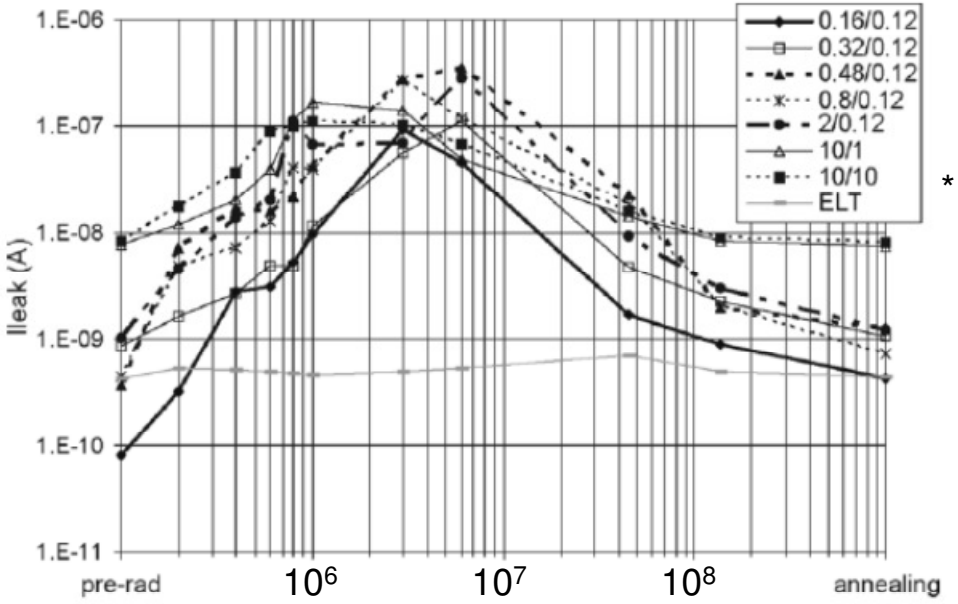


Fig. 3. Evolution of the leakage current with TID for different NMOS transistor size, up to 136 Mrd. The last point refers to full annealing at 100°C. The first point to the left is the pre-rad value.

* Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors, Federico Faccio and Giovanni Cervelli, IEEE Trans. Nucl. Sci., Vol.52, No.6, (2005) 2413

why does analog bias state affect current?

transistor bias state during irradiation affects charge trapping (field across oxide)

=> damage characteristic behaviour of a digital circuit will depend on the state of its nodes

(whether they spend most of their time as 1's or 0's)

in normal biased state comparator outputs are all low

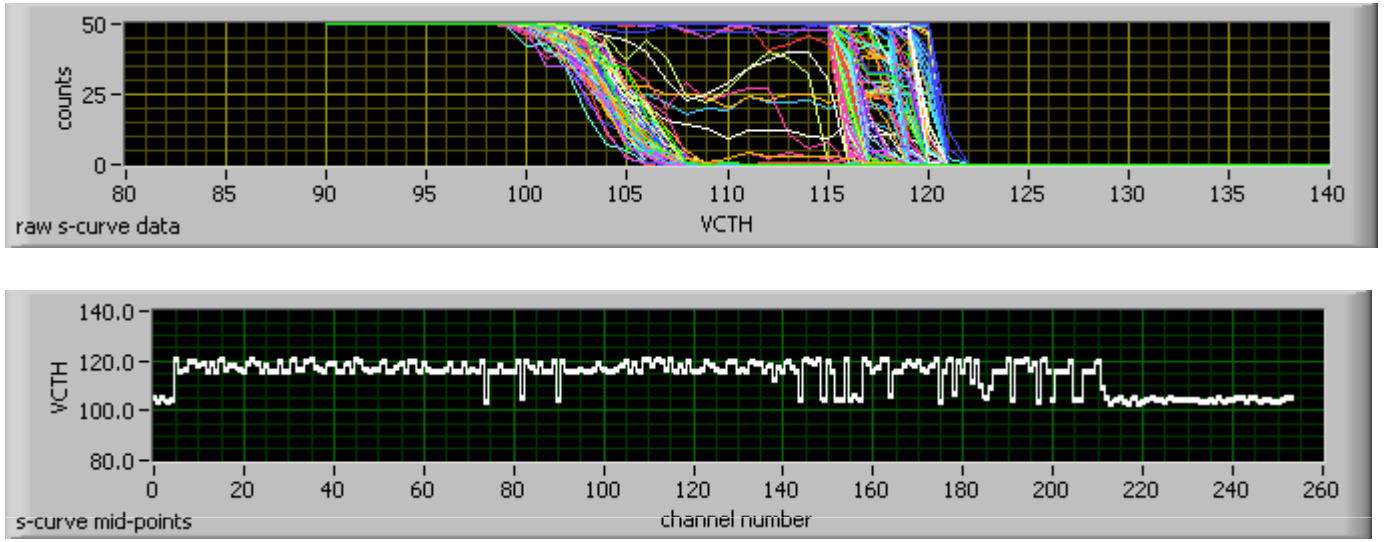
this is the state chip is mostly in during irradiation

but turns out that comparator outputs all flip state when bias currents set to zero

all nodes previously storing 1's now storing 0's and vice versa

=> plausible explanation for this effect

why is test pulse response affected?



test pulse response not easy to explain

response to test pulse disappears, but channels affected still all flip state at pedestal level

perhaps somehow related to load on pipeline driver affecting speed of response?

maybe can get some clues from simulation

this effect not currently understood

new summary so far

current increase at high dose-rates originates in pipeline

likely due to non-enclosed devices

exact mechanism not completely clear

Davide looking at pipeline simulations

should not cause problems for outer tracker (<30 Mrads over 10 years)

could cause problems at lower radii if CBC were to be used there

could think about improving by design

could adopt a pre-irradiation solution?

higher dose-rates

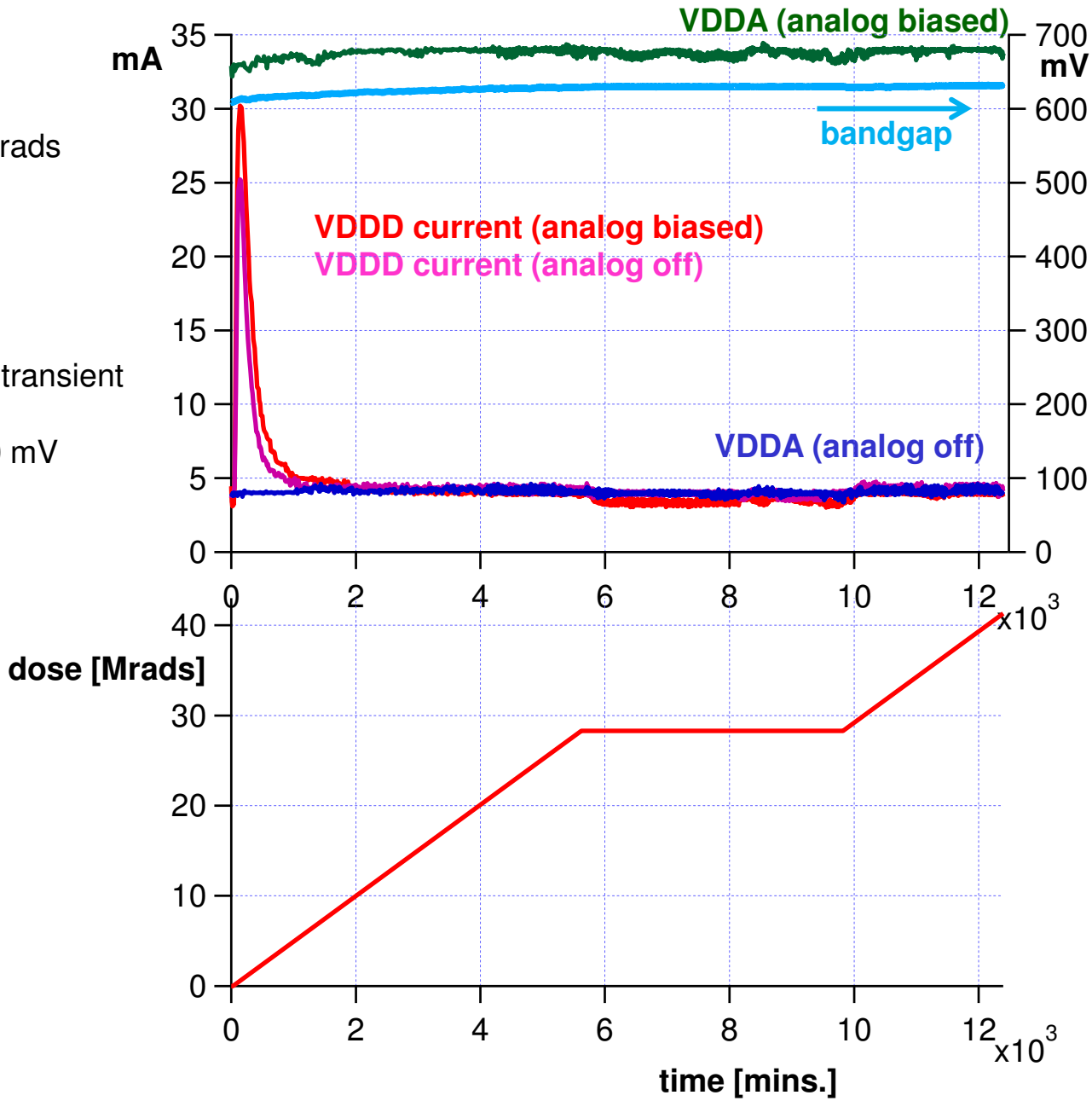
have now taken 1 chip to ~40 Mrads

~300 krad/hour

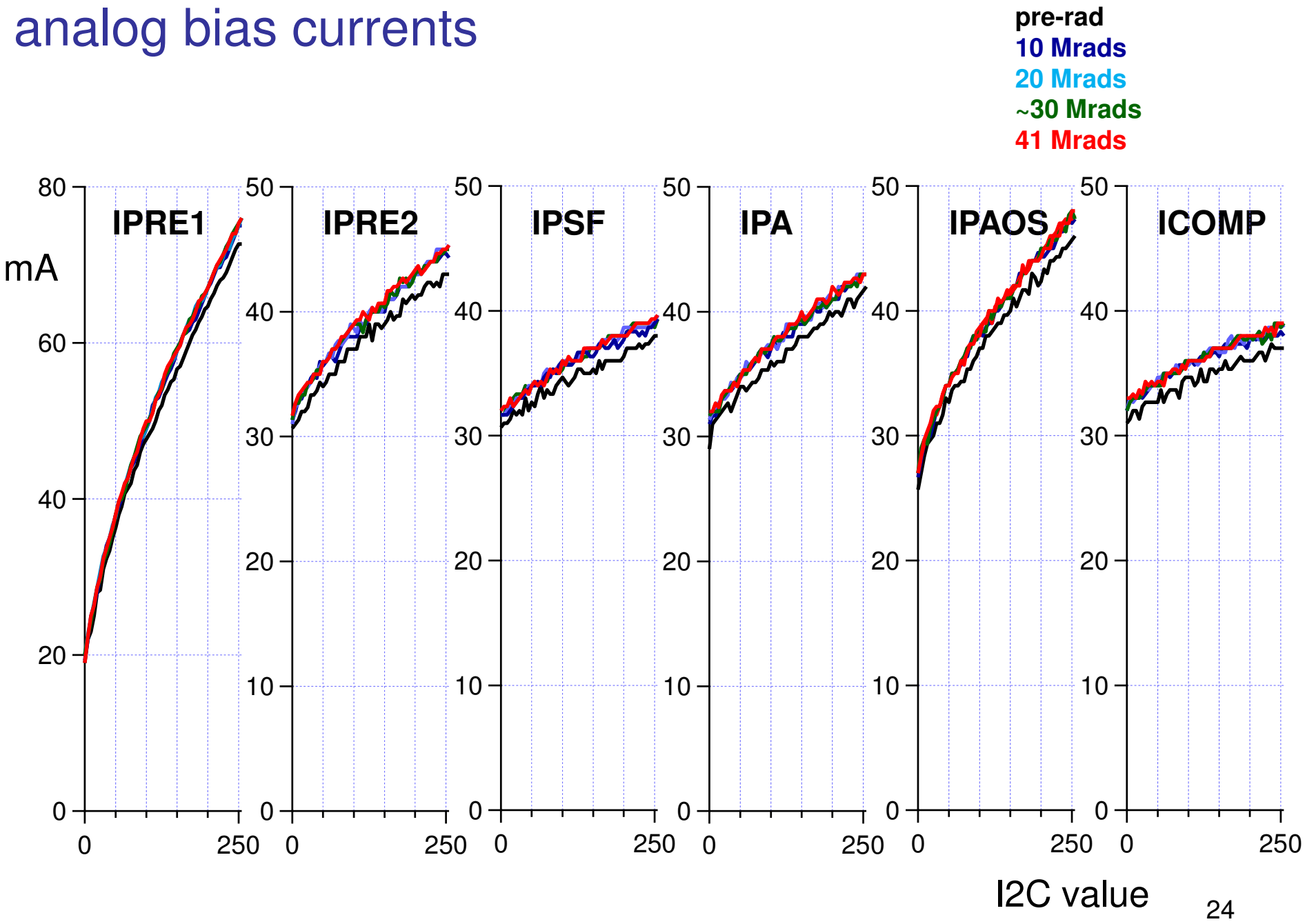
room temperature irradiation

power ~ static after initial digital transient

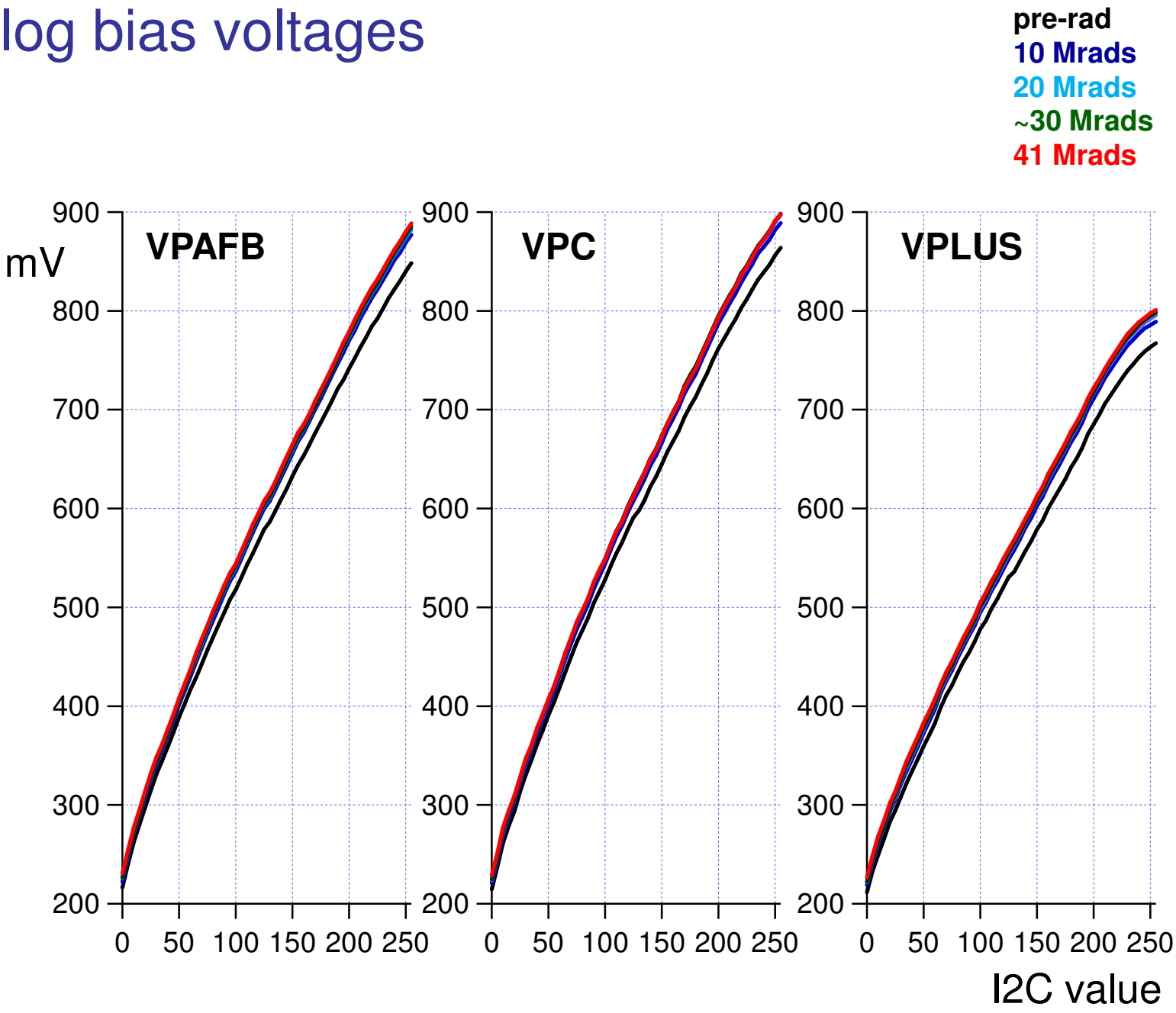
small shift in bandgap ~20 mV



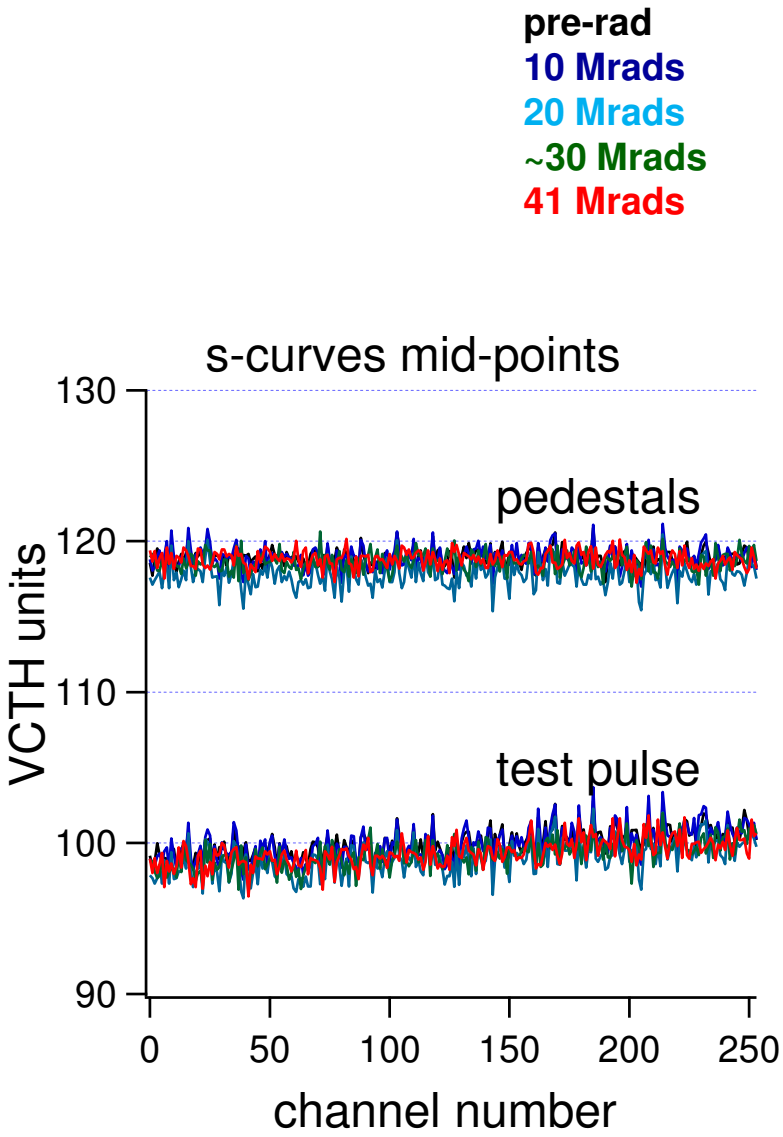
analog bias currents

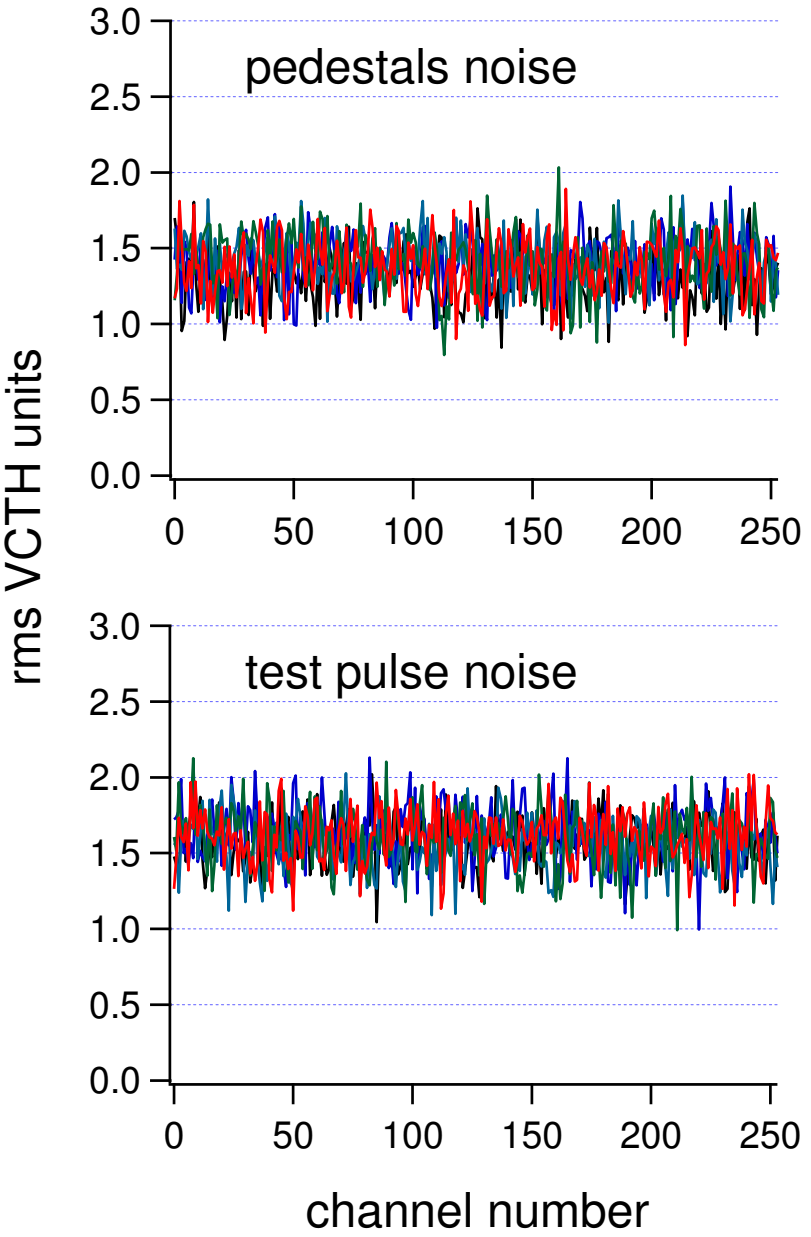


analog bias voltages



s-curves


pre-rad
10 Mrads
20 Mrads
~30 Mrads
41 Mrads
s-curves mid-points
pedestals
test pulse
VCTH units
130
120
110
100
90
0
50
100
150
200
250
channel number


pedestals noise
test pulse noise
rms VCTH units
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
50
100
150
200
250
channel number

high dose summary

CBC2 shows expected radiation **insensitivity** to ~ 40 Mrads as expected

40 Mrad limit dictated by availability of source

probably enough to allow us to conclude we are safe