CBC3 specifications and plans

repeat some previously shown material, but including further thoughts

some specs/features are already clear

some specs will develop during design phase

can be reviewed in these meetings as they develop

e.g. FE amplifier optimisation for speed/power/noise

others can be deferred for a while until the design of the relevant block is scheduled

will identify key decision points today

Mark Raymond / Mark Prydderch
systems meeting 29th July, 2014.

CBC3 front end

sensor choice

n-on-p, AC coupled, strip length **maybe** up to 8 cm (~12 pF)

=> **polarity defined, no DC sink/source requirement**

powering

VDDD converged on 1.2V +/- 10%

=> **as low as 1.08 V input to LDO**

front end amplifier

adjust for 1V VDDA

removal of DC coupling requirement will help, also polarity decision

re-examine pulse shape for dead-time issue

want pulse that returns to baseline within 50 ns

some overshoot acceptable

adjust preamplifier for larger sensor capacitance

maintain current noise performance

noise α $C/\sqrt{I_{DS}}$ (g_m α I_{DS})

to compensate (8/5) x C

need 2.6x current in input device

=> need to be able to increase current by factor ~3

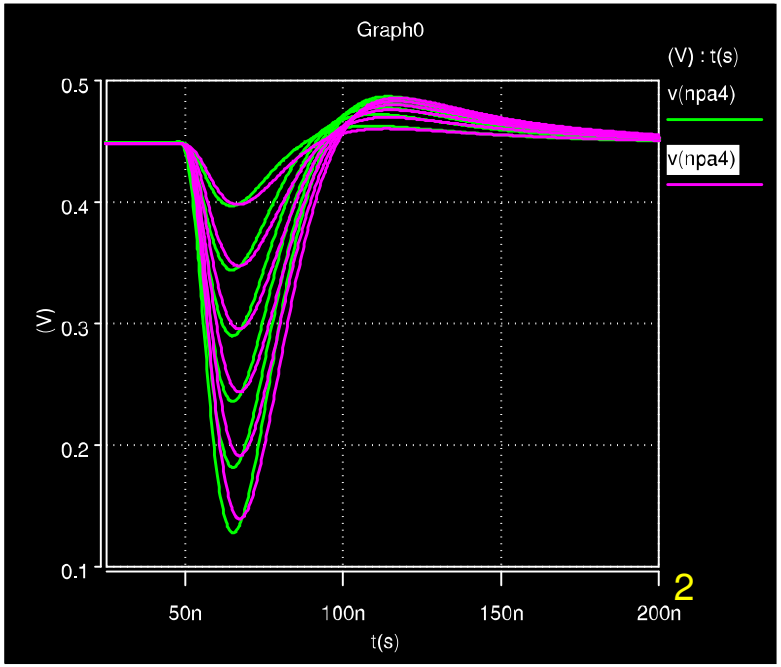
(even if don't actually do so)

=> **changes to biasing - IPRE1 fullscale x 3**

noise spec. TBD

noise/power/pulse shape trade-off

explore in simulation and revisit



CBC3 front end

comparator

2 comparators/channel? 5 sigma and 3 sigma thresholds?

(1 chan > 5σ) OR (2 neighbours > 3σ)=> hit

5σ outputs to pipeline, or 3σ if neighbour > 3 (or 5) σ

extra ~ 50 uW / channel

=> baseline is to stick with one comparator / channel

comparator output interface to pipeline

if amplifier pulse short then just sample comparator output into pipeline (and correlation cctry)

=> no deadtime

need adjustable sample time to comparator output (DLL)

but hip signal will keep comparator output high for long time

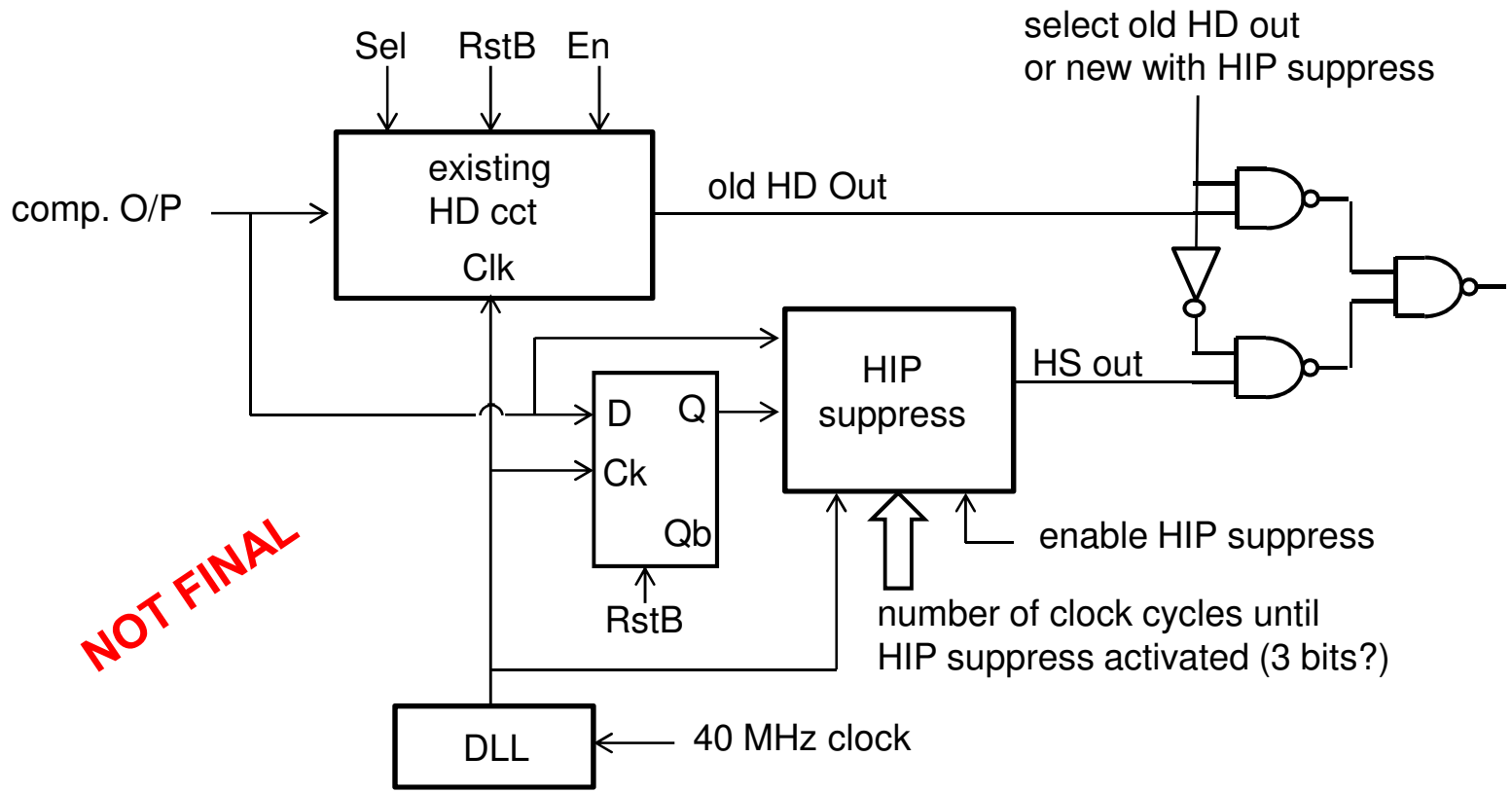
need additional circuit to suppress hips

e.g. block comparator output if high for longer than several BXs
(keep blocked till comparator output returns low)

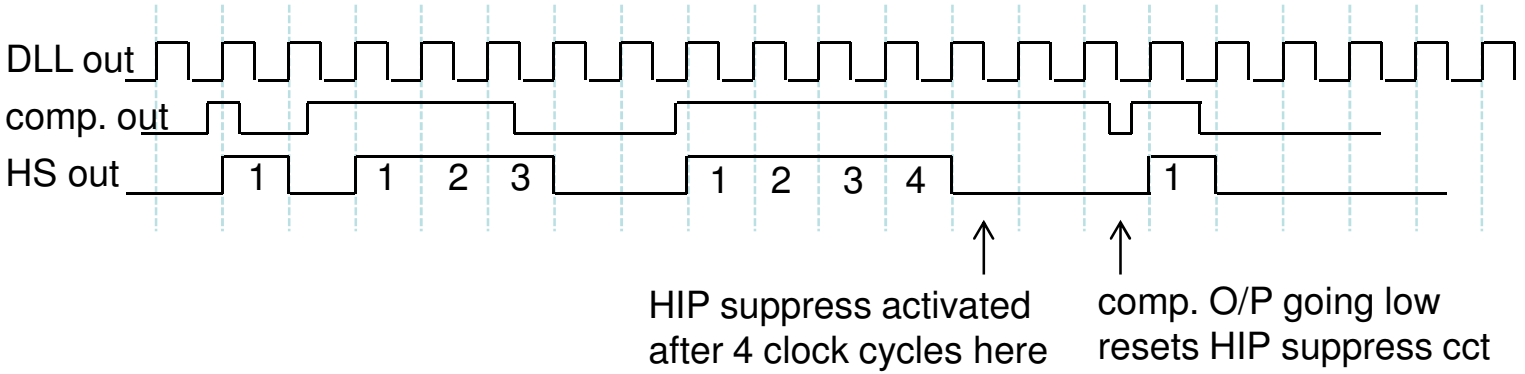
need to be able to swap comparator outputs between layers

to cope with modules flipped either side of rod/stave

new HIT detect functionality



HIP suppress functionality



CBC3 pipeline

pipeline

length increase: 12/25 usec?

propose 12 usec as baseline

radiation hardness

implications for improving (PMOS switches?/enclosed transistors?)

channel masking

currently only mask is before correlation logic to prevent spurious triggers from noisy channels

no masking of channels to pipeline (not necessary in unsparsified system)

1 MHz trigger rate => sparsification mandatory (in concentrator)

where to do channel masking? - not necessarily on CBC but might be best place

assume separate to mask for correlation logic - or could it be the same one?

propose to have a separate one

CBC3 offset correction and correlation

CWD

new cct to discriminate against clusters up to 4 strips (currently 3)

offset correction

4 domains / chip (only 2 in CBC2), +/- 3 strips, ½ strip resolution

correlation

+/- 7 strips window symmetric around centre strip, ½ strip res'n **note +/- 7 strips easier for logic**

½ strip resolution => 8 bit stub address

5 bit bend information

only one stub per window (highest pT one)

data for up to 3 stubs per chip will be transmitted off-chip

priority encoding of highest 3 pT stubs in the chip

is this necessary? **no - we propose not to include this**

bend codes

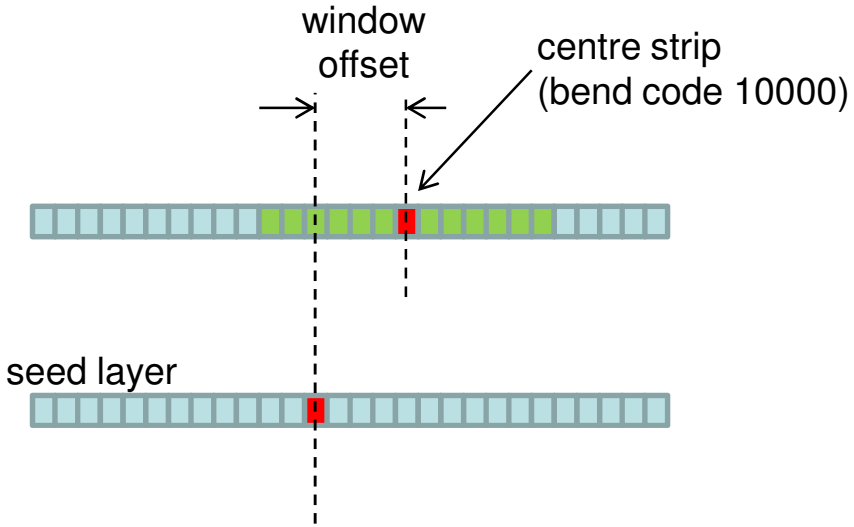
logic simpler if symmetric about centre strip

+/- 7 strips around centre strip

centre strip = centre strip of window
(remember window may be offset - e.g. below)

3 unused codes (00000, 11111, 01111)

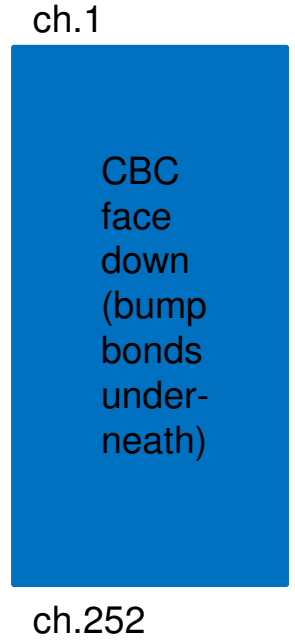
MSB sign bit (centre assigned +ve sign)



cluster centre	bend code
- 7	01110
- 6½	01101
- 6	01100
- 5½	01011
- 5	01010
- 4½	01001
- 4	01000
- 3½	00111
- 3	00110
- 2½	00101
- 2	00100
- 1½	00011
- 1	00010
- ½	00001
centre	10000
+ ½	10001
+1	10010
+1½	10011
+2	10100
+2½	10101
+3	10110
+3½	10111
+4	11000
+4½	11001
+5	11010
+5½	11011
+6	11100
+6½	11101
+7	11110

lower CBC channel numbers

higher CBC channel numbers



CBC3 readout

trigger rate capability to 1 MHz

see next slide for unsparsified format

output data format

how many lines at what rate?, differential/single-ended?

propose to adopt differential at 320 Mbps

=> 6 diff. pairs

S1	S2	S3	B1	B2	**R**
S1	S2	S3	B1	B2	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	B3	**R**
S1	S2	S3	B2	B3	**R**
S1	S2	S3	B2	-	**R**

25 ns

S = cluster ½ strip address
B = bend info
R = triggered readout data
(remains unsparsified)

trigger data format - how flexible can we be?

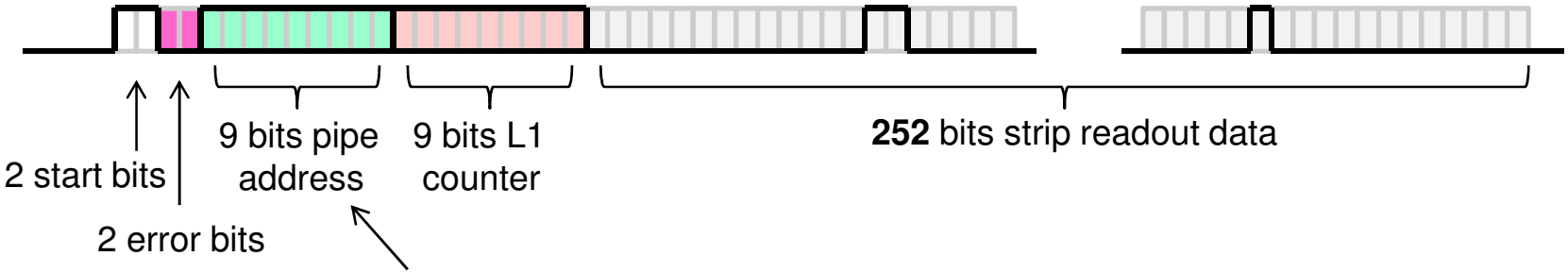
CBC3 readout data format

request for L1 counter

duplicate this in every front end chip?

functionality

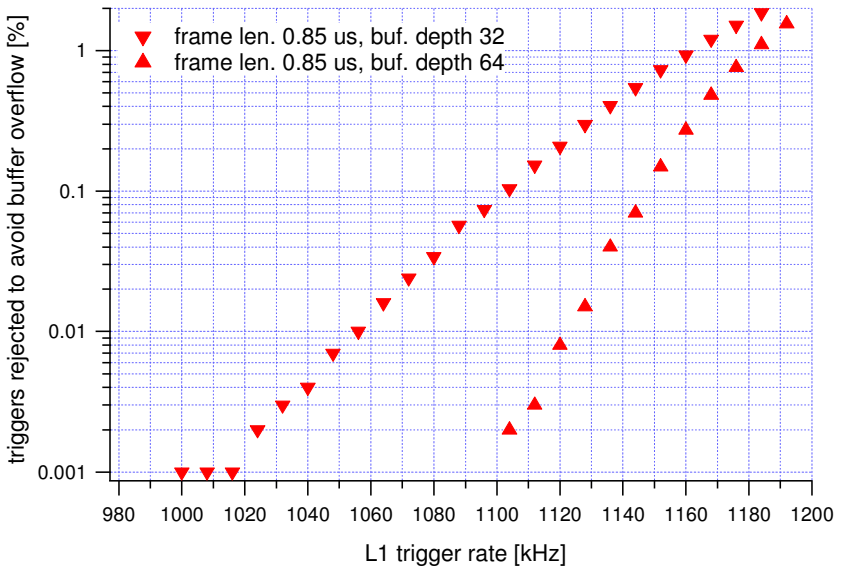
9 bits (up to 511), reset by fast reset Ored with dedicated reset (e.g. every orbit)



for **512** length pipeline (12.8 usec)

total frame length = 274 bits = 856.25 ns

=> existing buffer length 32 sufficient for v. low inefficiency at 1 MHz



interfaces

slow

stick with I2C, up to 1 MHz operation
have a broadcast address all 1's

this exists on CBC2 and has now been verified

CBC address = b10xxxxx, => global address b1111111, all chips respond

fast

320 MHz SLVS differential clock input
40 MHz SLVS differential clock input - do we have this or derive from 320?
6 x 320 Mbps stub and readout data lines

what about fast control?

differential serial line at 320 Mbps? - seems like overkill

commands are:
- fast reset
- trigger
- test pulse trigger
- (I2C refresh no longer)

have we defined this already? (if so - I missed it)

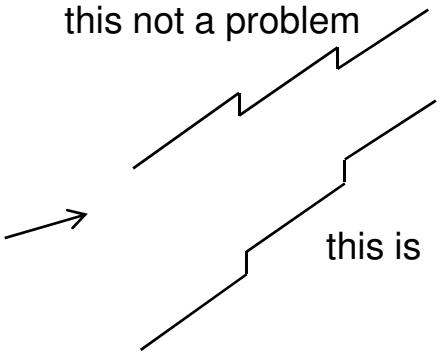
CBC3 miscellaneous(1)

biases

linear enough? monotonic enough? enough resolution?

modify VCTH to be monotonic and 1 mV resolution (10 bit)

make sure offset tuning non-monotonicity not a problem



clock domains

need DLL with programmable tap off to capture front end comparator O/P

powering

do we want to keep 2.5 -> 1.2 switched cap DC-DC option?

propose to remove switched cap DC-DC from CBC3

not currently considered as viable option (for PS) and frees up back end pad space

CBC3 miscellaneous(2)

others

remove the stub shift register
(CBC2 test feature)

keep the same pad pitch and layout as CBC2
assumes other viable manufacturers can be found

reduce to 252 channels
helps with strips wire-bond pad pattern layout

automatic I2C refresh (detect 1 out of 3 bits upset and restore to majority)

need to run at 40 MHz (as well as 320)
can’t wafer probe at 320 MHz

include prompt cell

CBC3 power consumption

start from existing CBC2 - all value in uW/channel

analogue

input device: 21 x C_{sensor} (=> 170 for 8 pF)

other analogue (amplifier, comparator): 130

digital: 50

CBC3 for 5cm strips
target 450 uW / chan

so for 5 cm sensor, ~ 8pF, get ~**350 uW/chan.**

CBC2 for 8cm sensor, same noise as CBC2 for 5 cm sensor

analogue

input device: $(8/5)^2$ x 170 = 435 (assume want same noise performance)

other analogue: 130

CBC2 digital: 50

so for 8 cm sensor, same noise performance as CBC2, estimate ~**615 uW/channel**

CBC3

need to add extra digital power for extra digital functionality

stub and bend info assembly, 1 MHz triggering, longer pipeline, …

hard to estimate - may not be negligible

off detector transmission estimate 6 diff. lines at 320 Mbps, 4 mW/diff.pr. (over-estimate)

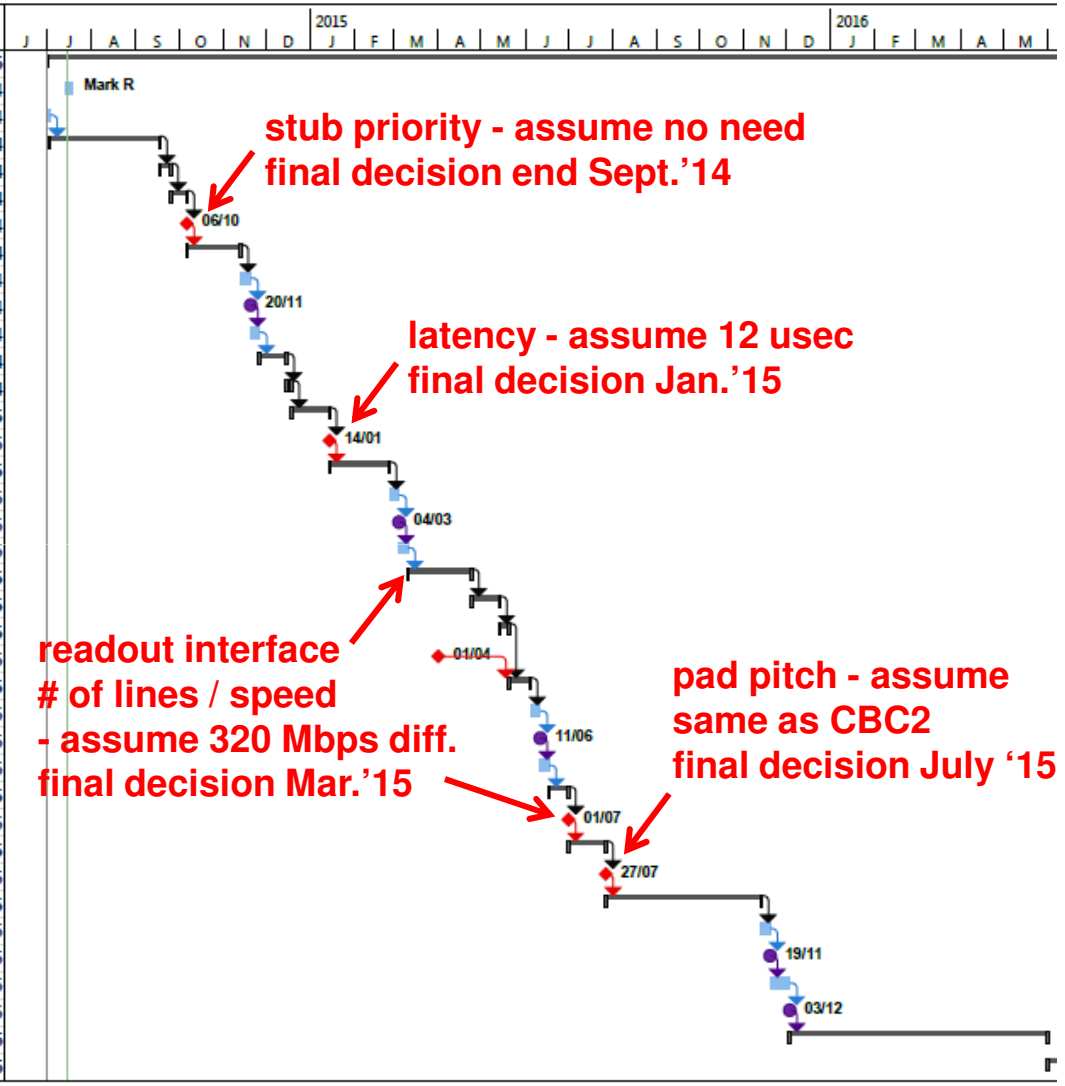
=> ~**100 uW/chan.**

=> could be looking at ~700 uW/channel (significant uncertainty - treat with caution)

=> 2.4 Amps from 1.2V rail for 16 chip module (16 cm x 10 cm sensor area)

CBC3 development Gannt - M. Prydderch

ID	Task Name	Duration	Start	Finish
1	CBC3 Design	617.34 days	Tue 01/07/14	Wed 07/09/16
2	TID Radiation Studies	1 wk	Mon 14/07/14	Fri 18/07/14
3	SEU Cross-section Calculation	2 days	Tue 01/07/14	Wed 02/07/14
4	Implement 1/2 Strip Resolution	59.34 days	Wed 02/07/14	Wed 17/09/14
9	Pipeline Mask	6 days	Wed 17/09/14	Thu 25/09/14
12	Hit Detect Modification	8 days	Thu 25/09/14	Mon 06/10/14
16	Decision on need for Stub Priority	0 days	Mon 06/10/14	Mon 06/10/14
17	Stub Readout Logic	30 days	Mon 06/10/14	Thu 13/11/14
22	Prepare for Review	5 days	Thu 13/11/14	Thu 20/11/14
23	Intermediate Project Review	0 days	Thu 20/11/14	Thu 20/11/14
24	Post Review Actions	5 days	Thu 20/11/14	Wed 26/11/14
25	Modify RAM cell	14 days	Wed 26/11/14	Mon 15/12/14
30	9 Bit L1 Counter	4 days	Mon 15/12/14	Fri 19/12/14
34	DLL for Hit Detect Synchronisation	20 days	Fri 19/12/14	Wed 14/01/15
38	Decision on latency & TID results.	0 days	Wed 14/01/15	Wed 14/01/15
39	Modify the Pipeline	32 days	Wed 14/01/15	Wed 25/02/15
44	Prepare for Review	5 days	Wed 25/02/15	Wed 04/03/15
45	Intermediate Project Review	0 days	Wed 04/03/15	Wed 04/03/15
46	Post Review Actions	5 days	Wed 04/03/15	Tue 10/03/15
47	Data Packet Assembly Logic	35 days	Tue 10/03/15	Fri 24/04/15
52	New 10 Bit VCTH DAC	15 days	Fri 24/04/15	Thu 14/05/15
56	Modify IPRE1 for 3x Full scale	5 days	Thu 14/05/15	Wed 20/05/15
60	Decision on Strip length	0 days	Wed 01/04/15	Wed 01/04/15
61	Modify Front End	12 days	Wed 20/05/15	Thu 04/06/15
64	Prepare for Review	5 days	Thu 04/06/15	Thu 11/06/15
65	Intermediate Project Review	0 days	Thu 11/06/15	Thu 11/06/15
66	Post Review Actions	5 days	Thu 11/06/15	Wed 17/06/15
67	Modify Configuration Registers	10 days	Wed 17/06/15	Wed 01/07/15
71	Hybrid electrical model decided	0 days	Wed 01/07/15	Wed 01/07/15
72	I/O Pad Optimisation	20 days	Wed 01/07/15	Mon 27/07/15
76	Decision on Pad Pitch	0 days	Mon 27/07/15	Mon 27/07/15
77	TOP LEVEL	85 days	Mon 27/07/15	Fri 13/11/15
80	Review Preparation	5 days	Fri 13/11/15	Thu 19/11/15
81	Pre-submission Project Review	0 days	Thu 19/11/15	Thu 19/11/15
82	Post Review Actions	10 days	Thu 19/11/15	Thu 03/12/15
83	Ship GDS File	0 days	Thu 03/12/15	Thu 03/12/15
84	Manufacture	140 days	Thu 03/12/15	Wed 01/06/16
88	Test	75 days	Wed 01/06/16	Wed 07/09/16



summary

CBC3 design process has begun

some specs and features are well-known

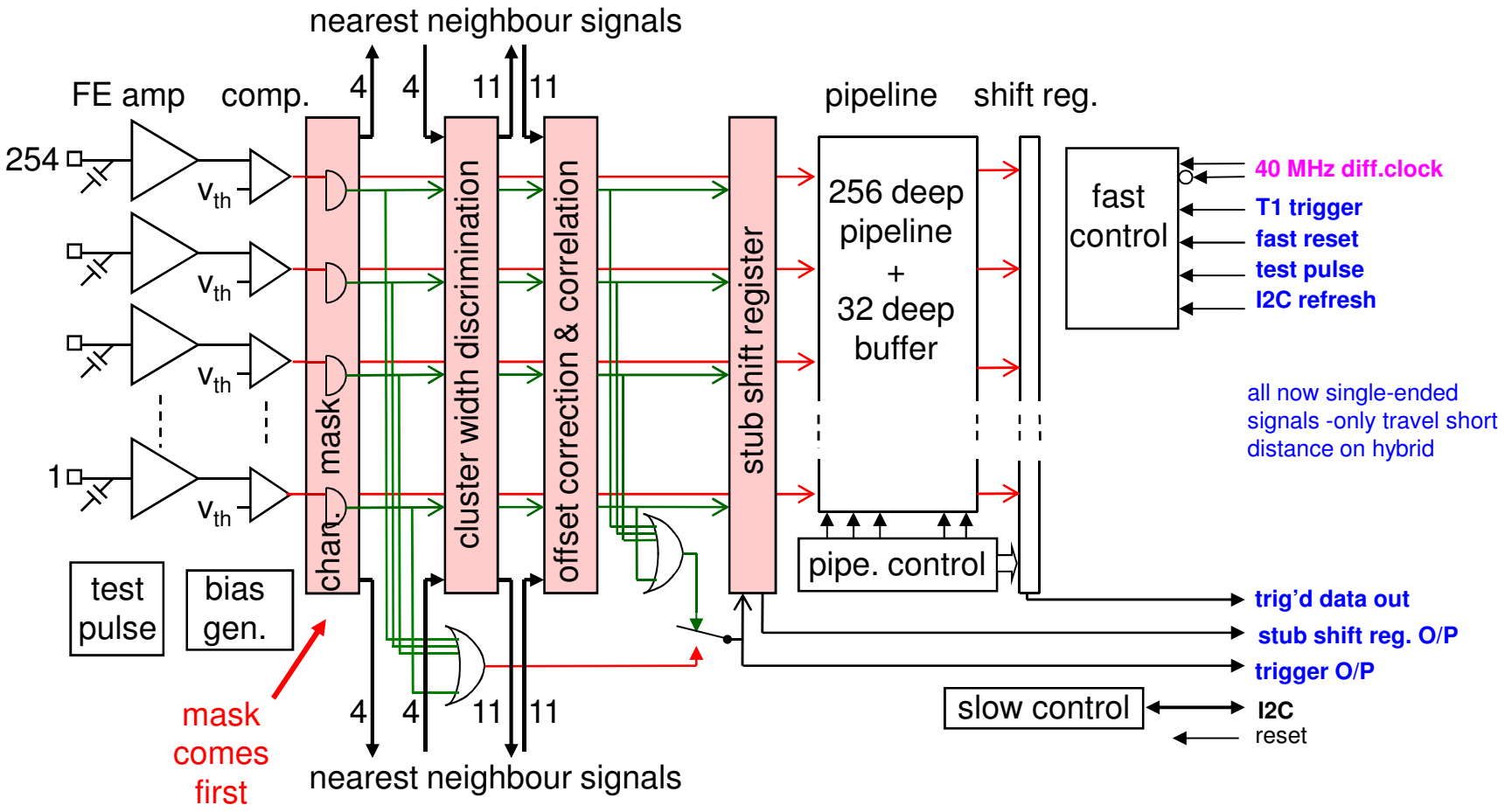
FE performance specs will be kept under review as design progresses

baseline assumptions on features and architectures have been made

latest dates for possible changes have been indicated

current schedule compatible with chip in hand ~middle 2016

CBC2 architecture



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)

cluster width discrimination: exclude wide clusters

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip
for normal operation choose correlation O/P