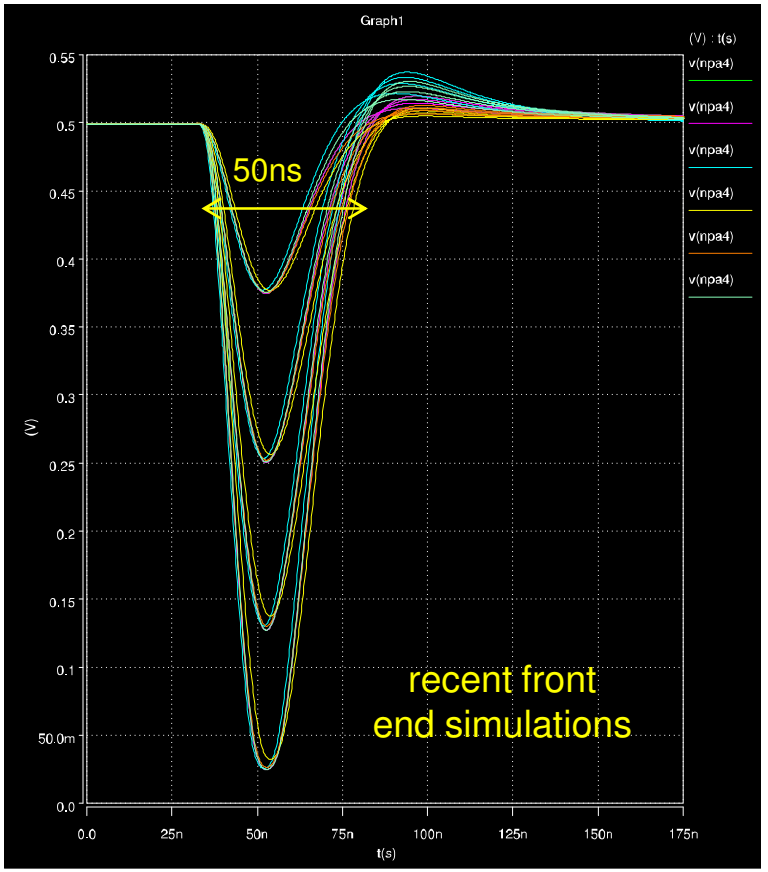
CBC3 specifications update

update on 29th July presentation

Mark Raymond / Mark Prydderch
systems meeting 30th September, 2014.

CBC3 front end specs summary

item	spec.
sensor	n-on-p, AC coupled strip length 5 - 8 cm (8 - 12 pF)
VDDA	> 1V via LDO from VDDD (VDDD= 1.2+/-10%)
pulse shape	~20ns peaking return to baseline within 50ns some overshoot acceptable
input device current	up to 500uA
noise	(noise/power/pulse shape trade-off)



comparator + hit detect

comparator discriminates postamp output pulse

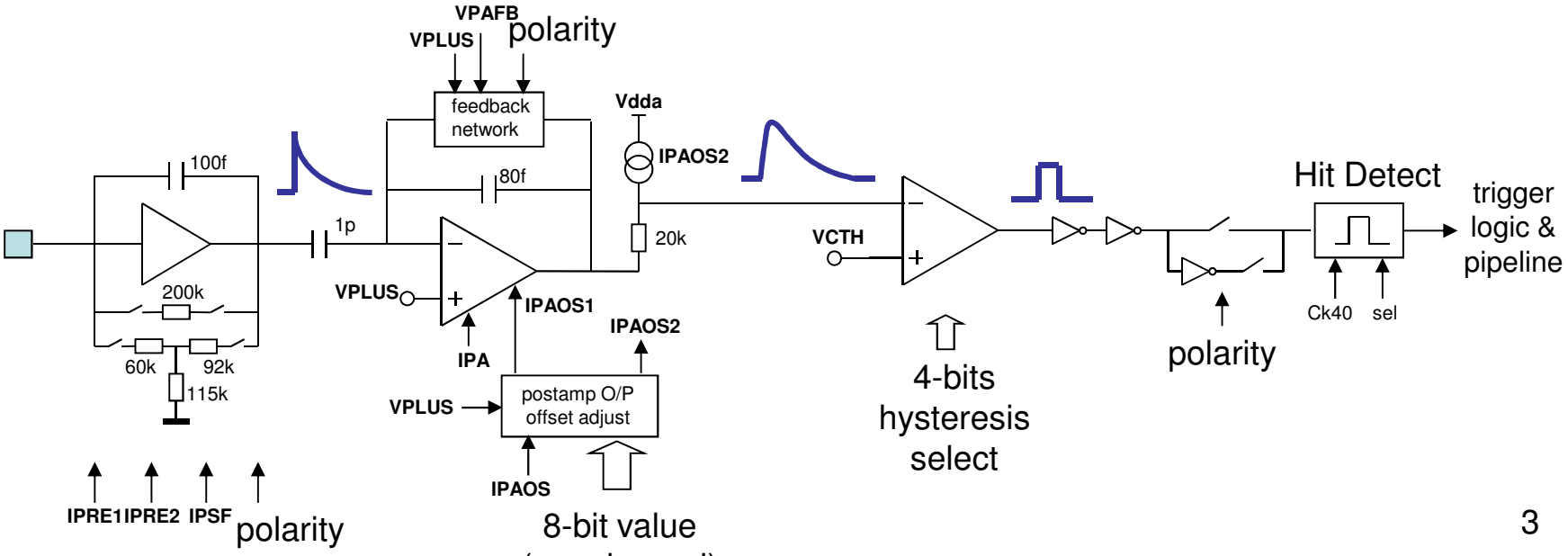
CBC2 hit detect cct functionality to provide high output for only one BX

leads to deadtime if postamp output pulse longer than 50nsec

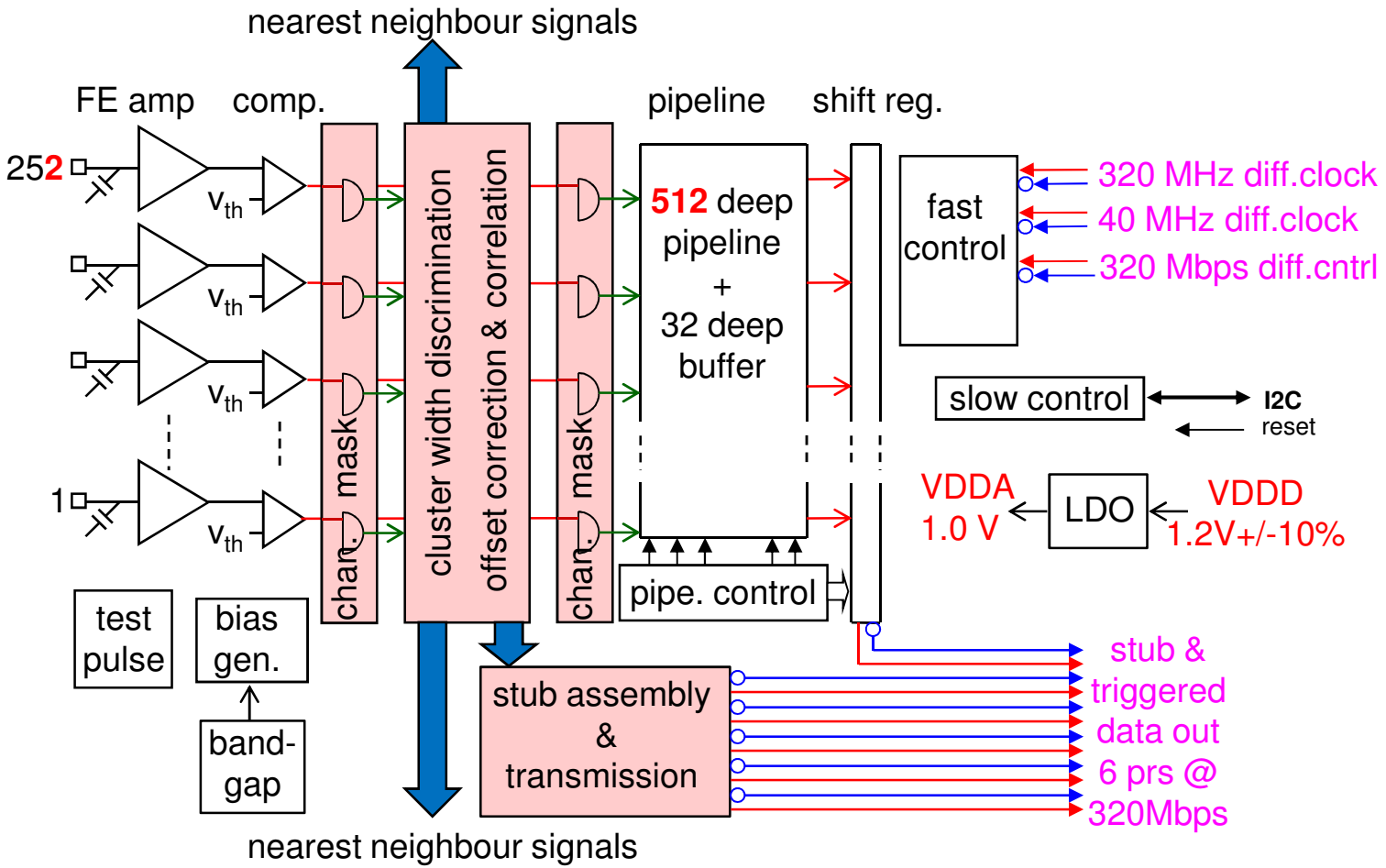
CBC3 pulse shape will be shorter so hit detect redundant

but hip signal will keep comparator output high for long time so need additional circuit to detect this and inhibit output to trigger logic

=> detailed functionality still needs some thought



CBC3 architecture



252 channels, 512 deep pipeline (12.8 us), extra chan. mask before pipeline, stub assembly and transmission, all differential I/O, 1 MHz trigger rate capable,

CBC3 bend codes - proposed last time

+/- 7 strips around centre strip (centre strip of window)

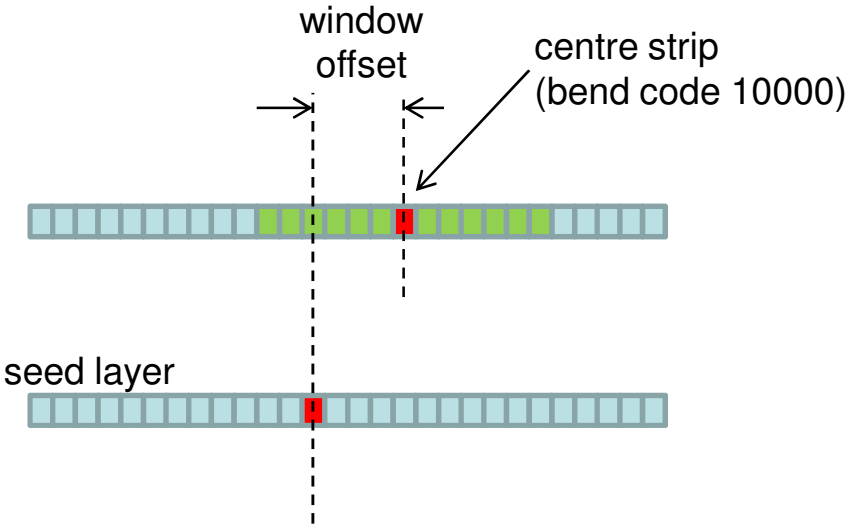
window may be offset

4 domains / chip, +/- 3 strips, ½ strip resolution

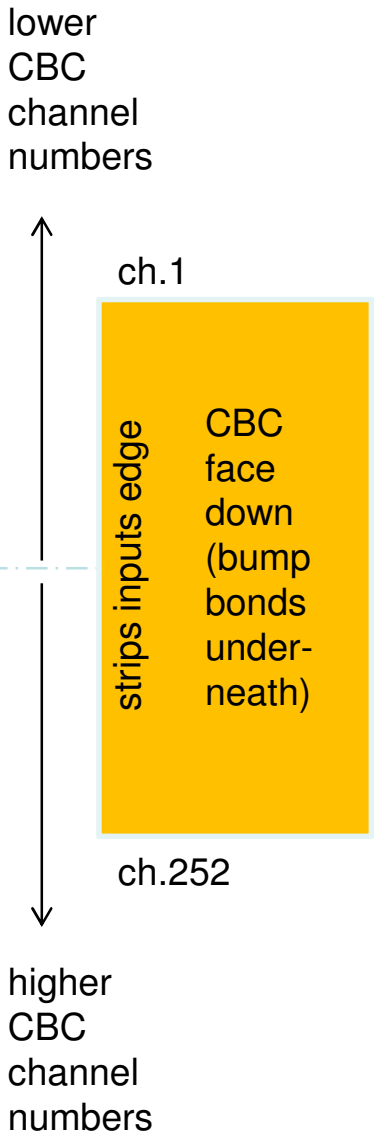
3 unused bend codes (00000, 11111, 01111)

MSB sign bit (centre assigned +ve sign)

only one stub produced per window (highest pT one)



cluster centre	bend code
- 7	01110
- 6½	01101
- 6	01100
- 5½	01011
- 5	01010
- 4½	01001
- 4	01000
- 3½	00111
- 3	00110
- 2½	00101
- 2	00100
- 1½	00011
- 1	00010
- ½	00001
centre	10000
+ ½	10001
+1	10010
+1½	10011
+2	10100
+2½	10101
+3	10110
+3½	10111
+4	11000
+4½	11001
+5	11010
+5½	11011
+6	11100
+6½	11101
+7	11110



MPA bend codes - slide from Davide C.

+/- ***4*** strips around centre strip

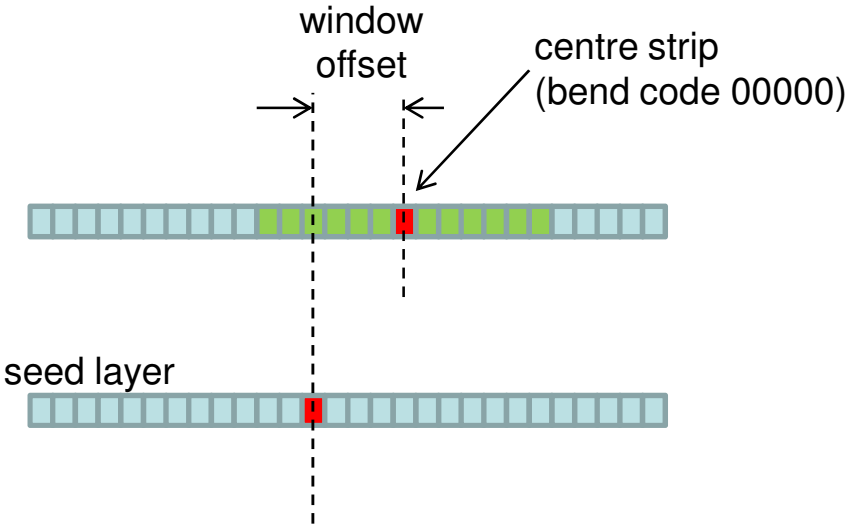
centre strip = centre strip of window

window may be offset

2 domains / chip, +/- 3 strips, ½ strip resolution

A lot of code unused – it is really necessary +/- 4 strips?

Negative bend code → ***Two`s complement***



cluster centre	bend code
- 4	11000
- 3½	11001
- 3	11010
- 2½	11011
- 2	11100
- 1½	11101
- 1	11110
- ½	11111
centre	00000
+ ½	00001
+1	00010
+1½	00011
+2	00100
+2½	00101
+3	00110
+3½	00111
+4	01000

lower MPA channel numbers

ch.1

ch.120

higher MPA channel numbers

comparison

	CBC3	MPA	CBC3 alternative suggestion from Mark Prydderch
- 7	01110		11110
- 6½	01101		11101
- 6	01100		11100
- 5½	01011		11011
- 5	01010		11010
- 4½	01001		11001
- 4	01000	11000	11000
- 3½	00111	11001	10111
- 3	00110	11010	10110
- 2½	00101	11011	10101
- 2	00100	11100	10100
- 1½	00011	11101	10011
- 1	00010	11110	10010
- ½	00001	11111	10001
centre	10000	00000	00000
+ ½	10001	00001	00001
+1	10010	00010	00010
+1½	10011	00011	00011
+2	10100	00100	00100
+2½	10101	00101	00101
+3	10110	00110	00110
+3½	10111	00111	00111
+4	11000	01000	01000
+4½	11001		01001
+5	11010		01010
+5½	11011		01011
+6	11100		01100
+6½	11101		01101
+7	11110		01110

symmetrical without the sign bit so any arithmetic to prioritise the least bent stubs could discard the sign bit and operate on just the 4 LSB

CBC3 trigger output data format

6 differential pairs @ 320 Mbps

S1	S2	S3	B1	B2	**R**
S1	S2	S3	B1	B2	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	B3	**R**
S1	S2	S3	B2	B3	**R**
S1	S2	S3	B2	sync	**R**

25 ns

S = cluster ½ strip address
B = bend info
R = triggered readout data
(remains unsparsified)

trigger data format - how flexible can we be?

sync bit

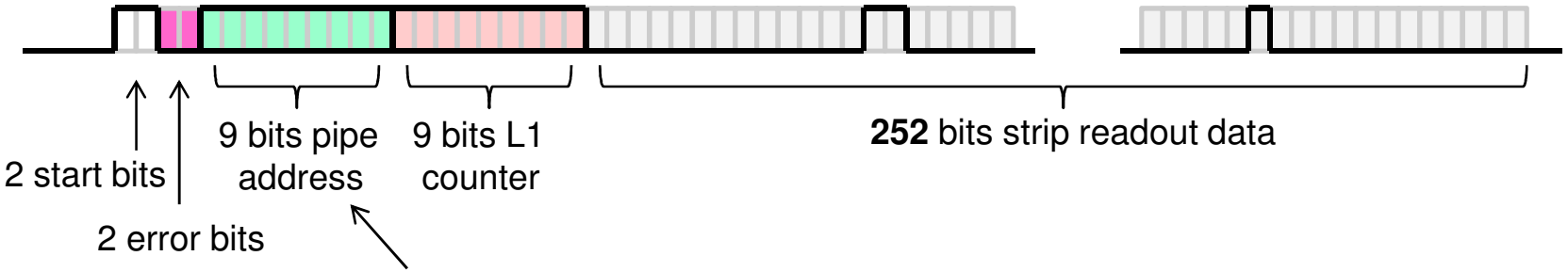
CBC3 readout data format

trigger rate capability to 1 MHz

L1 counter in every chip

functionality

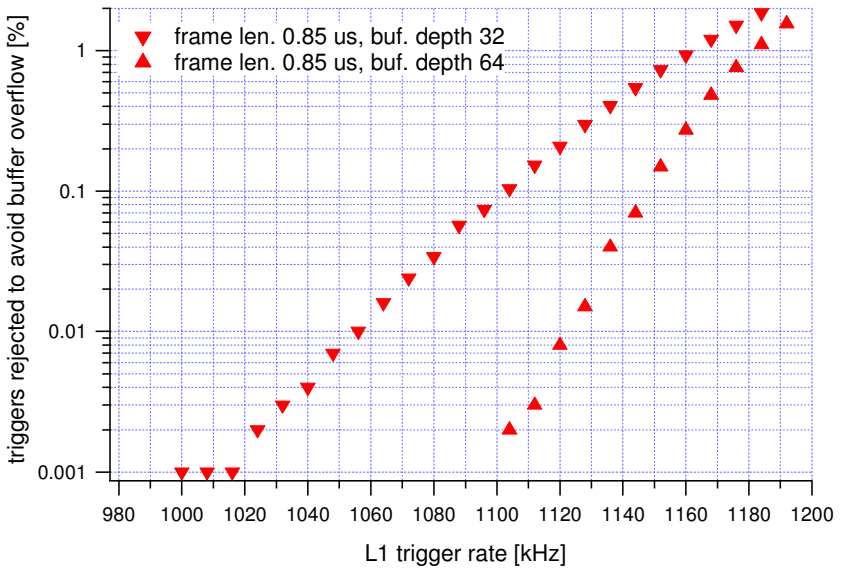
9 bits (up to 511), reset by fast reset ORed with dedicated reset (e.g. every orbit)



for **512** length pipeline (12.8 usec)

total frame length = 274 bits = 856.25 ns

=> existing buffer length 32 sufficient for v. low inefficiency at 1 MHz



interfaces

slow

I2C, up to 1 MHz operation
have a broadcast address all 1's

exists on CBC2

CBC address = b10xxxxx, => global address b1111111, all chips respond

fast

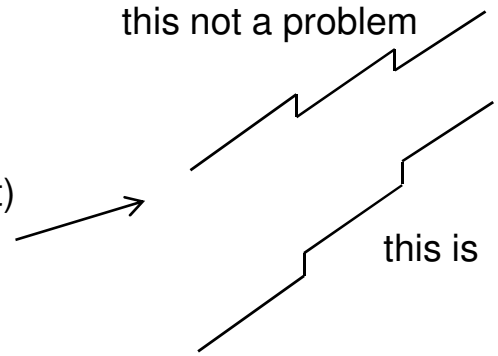
320 MHz SLVS differential clock input
40 MHz SLVS differential clock input
6 x 320 Mbps stub and readout data lines

320 Mbps differential control line

not decoded so 8 commands possible

commands are
- fast reset
- trigger
- test pulse trigger
- reset L1 counter
- (I2C refresh no longer)

CBC3 miscellaneous



biases
- modify VCTH to be monotonic and 1 mV resolution (10 bit)
- make sure offset tuning non-monotonicity not a problem

powering
- single supply @ 1.2V +/- 10%

keep the same pad pitch and layout as CBC2
- assumes other viable manufacturers can be found

reduce to 252 channels
- helps with strips wire-bond pad pattern layout

automatic I2C refresh (detect 1 out of 3 bits upset and restore to majority)
- need to review following SEU results

need to run at 40 MHz (as well as 320)
- can't wafer probe at 320 MHz

include prompt cell
- is this necessary now?

counters for events
- hips, SEU's, …

extra

CBC3 power consumption

start from existing CBC2 - all value in uW/channel

analogue

input device: 21 x C_{sensor} (=> 170 for 8 pF)

other analogue (amplifier, comparator): 130

digital: 50

CBC3 for 5cm strips
target 450 uW / chan

so for 5 cm sensor, ~ 8pF, get ~**350 uW/chan.**

CBC2 for 8cm sensor, same noise as CBC2 for 5 cm sensor

analogue

input device: $(8/5)^2$ x 170 = 435 (assume want same noise performance)

other analogue: 130

CBC2 digital: 50

so for 8 cm sensor, same noise performance as CBC2, estimate ~**615 uW/channel**

CBC3

need to add extra digital power for extra digital functionality

stub and bend info assembly, 1 MHz triggering, longer pipeline, …

hard to estimate - may not be negligible

off detector transmission estimate 6 diff. lines at 320 Mbps, 4 mW/diff.pr. (over-estimate)

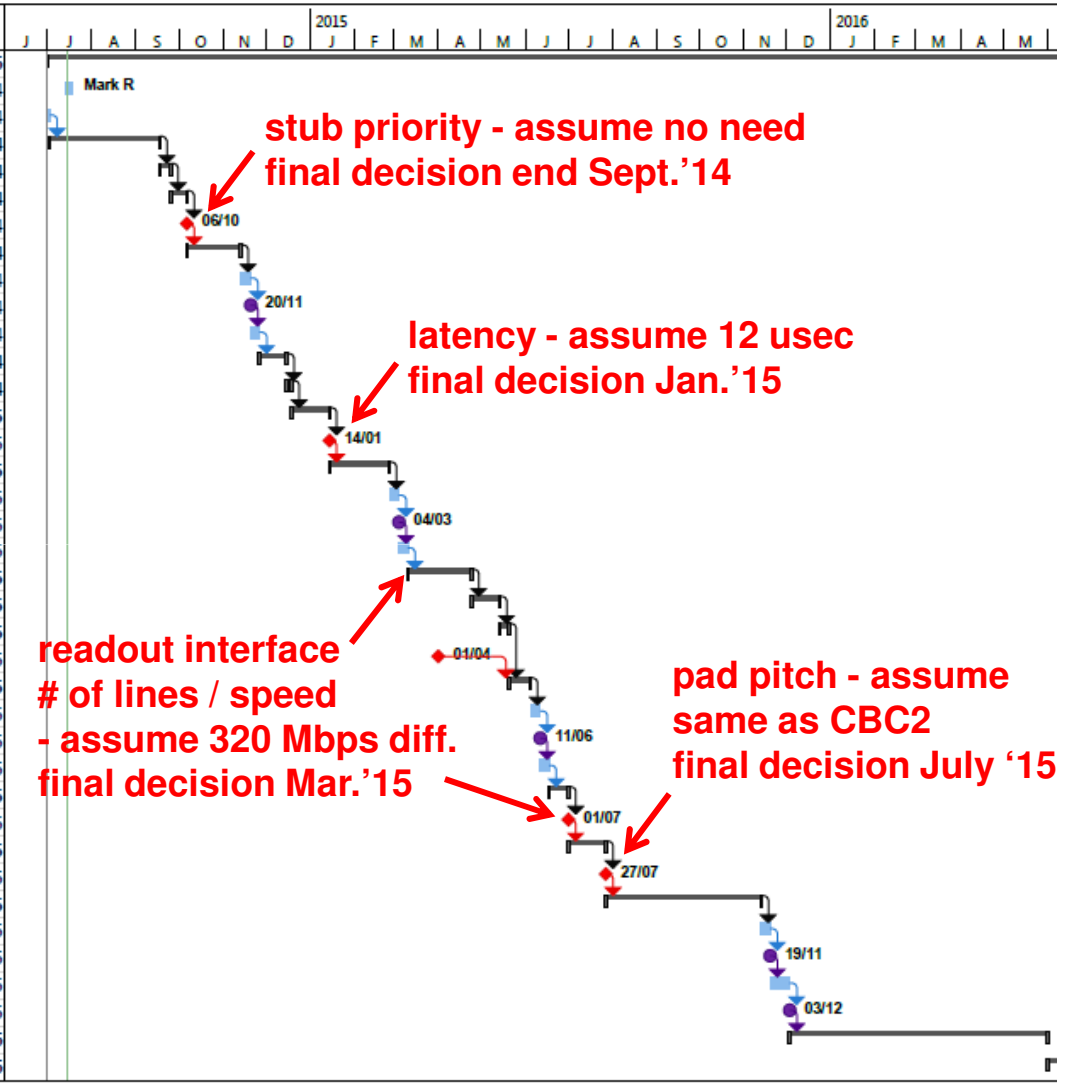
=> ~**100 uW/chan.**

=> could be looking at ~700 uW/channel (significant uncertainty - treat with caution)

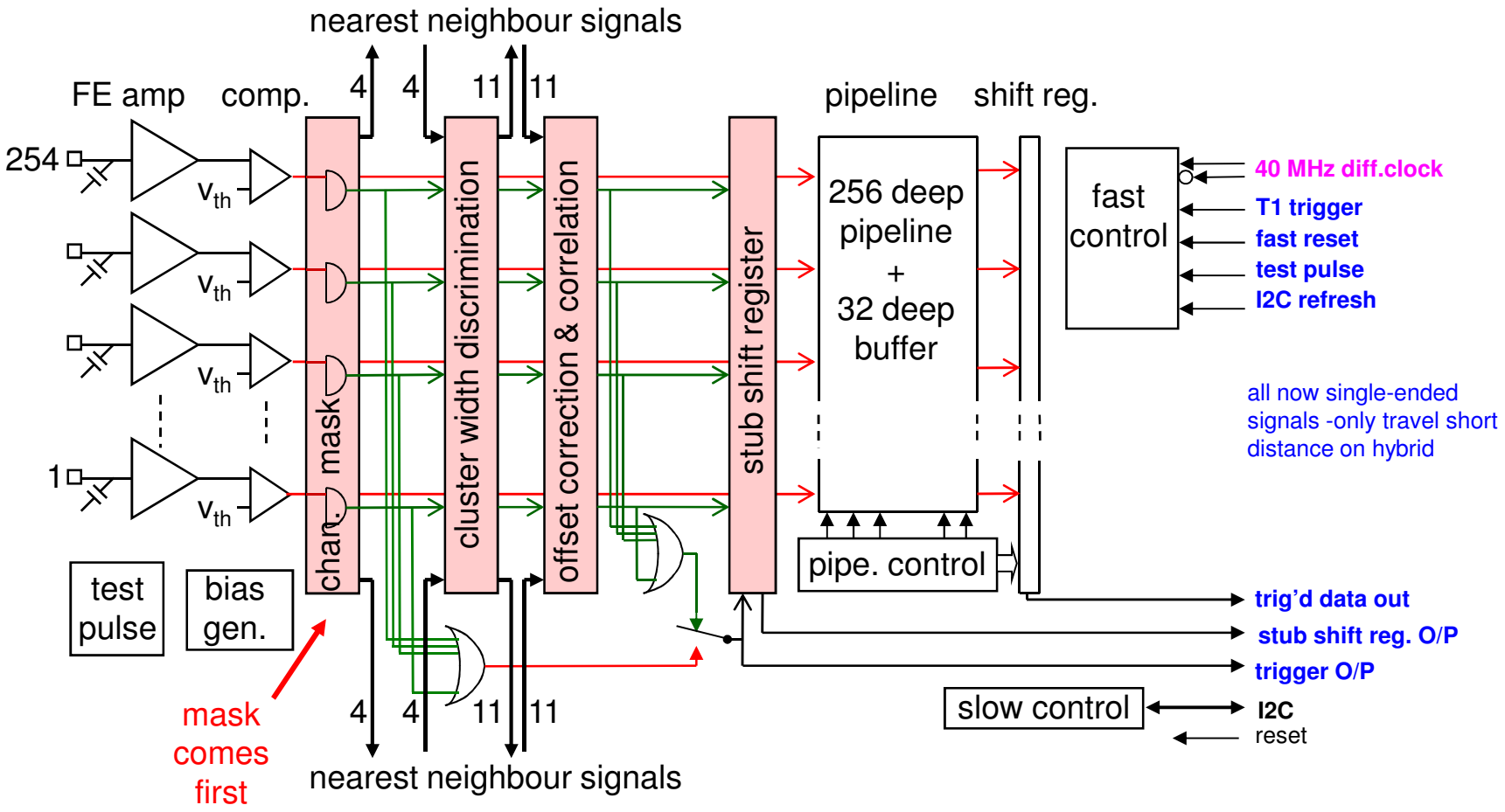
=> 2.4 Amps from 1.2V rail for 16 chip module (16 cm x 10 cm sensor area)

CBC3 development Gannt - M. Prydderch

ID	Task Name	Duration	Start	Finish
1	CBC3 Design	617.34 days	Tue 01/07/14	Wed 07/09/16
2	TID Radiation Studies	1 wk	Mon 14/07/14	Fri 18/07/14
3	SEU Cross-section Calculation	2 days	Tue 01/07/14	Wed 02/07/14
4	Implement 1/2 Strip Resolution	59.34 days	Wed 02/07/14	Wed 17/09/14
9	Pipeline Mask	6 days	Wed 17/09/14	Thu 25/09/14
12	Hit Detect Modification	8 days	Thu 25/09/14	Mon 06/10/14
16	Decision on need for Stub Priority	0 days	Mon 06/10/14	Mon 06/10/14
17	Stub Readout Logic	30 days	Mon 06/10/14	Thu 13/11/14
22	Prepare for Review	5 days	Thu 13/11/14	Thu 20/11/14
23	Intermediate Project Review	0 days	Thu 20/11/14	Thu 20/11/14
24	Post Review Actions	5 days	Thu 20/11/14	Wed 26/11/14
25	Modify RAM cell	14 days	Wed 26/11/14	Mon 15/12/14
30	9 Bit L1 Counter	4 days	Mon 15/12/14	Fri 19/12/14
34	DLL for Hit Detect Synchronisation	20 days	Fri 19/12/14	Wed 14/01/15
38	Decision on latency & TID results.	0 days	Wed 14/01/15	Wed 14/01/15
39	Modify the Pipeline	32 days	Wed 14/01/15	Wed 25/02/15
44	Prepare for Review	5 days	Wed 25/02/15	Wed 04/03/15
45	Intermediate Project Review	0 days	Wed 04/03/15	Wed 04/03/15
46	Post Review Actions	5 days	Wed 04/03/15	Tue 10/03/15
47	Data Packet Assembly Logic	35 days	Tue 10/03/15	Fri 24/04/15
52	New 10 Bit VCTH DAC	15 days	Fri 24/04/15	Thu 14/05/15
56	Modify IPRE1 for 3x Full scale	5 days	Thu 14/05/15	Wed 20/05/15
60	Decision on Strip length	0 days	Wed 01/04/15	Wed 01/04/15
61	Modify Front End	12 days	Wed 20/05/15	Thu 04/06/15
64	Prepare for Review	5 days	Thu 04/06/15	Thu 11/06/15
65	Intermediate Project Review	0 days	Thu 11/06/15	Thu 11/06/15
66	Post Review Actions	5 days	Thu 11/06/15	Wed 17/06/15
67	Modify Configuration Registers	10 days	Wed 17/06/15	Wed 01/07/15
71	Hybrid electrical model decided	0 days	Wed 01/07/15	Wed 01/07/15
72	I/O Pad Optimisation	20 days	Wed 01/07/15	Mon 27/07/15
76	Decision on Pad Pitch	0 days	Mon 27/07/15	Mon 27/07/15
77	TOP LEVEL	85 days	Mon 27/07/15	Fri 13/11/15
80	Review Preparation	5 days	Fri 13/11/15	Thu 19/11/15
81	Pre-submission Project Review	0 days	Thu 19/11/15	Thu 19/11/15
82	Post Review Actions	10 days	Thu 19/11/15	Thu 03/12/15
83	Ship GDS File	0 days	Thu 03/12/15	Thu 03/12/15
84	Manufacture	140 days	Thu 03/12/15	Wed 01/06/16
88	Test	75 days	Wed 01/06/16	Wed 07/09/16



CBC2 architecture



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)

cluster width discrimination: exclude wide clusters

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip
for normal operation choose correlation O/P