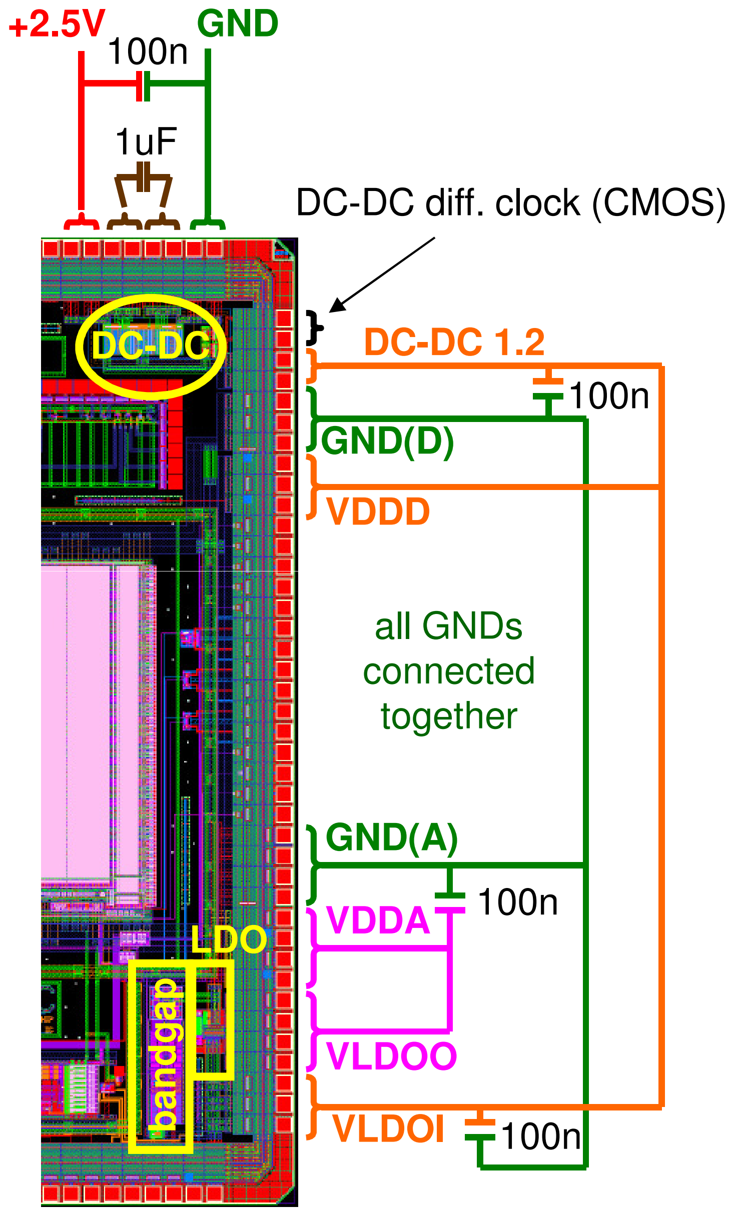
CBC2 performance with switched capacitor DC-DC converter

systems meeting, 12/2/14

reminder of results from CBC1



can power CBC from single **+2.5V** supply

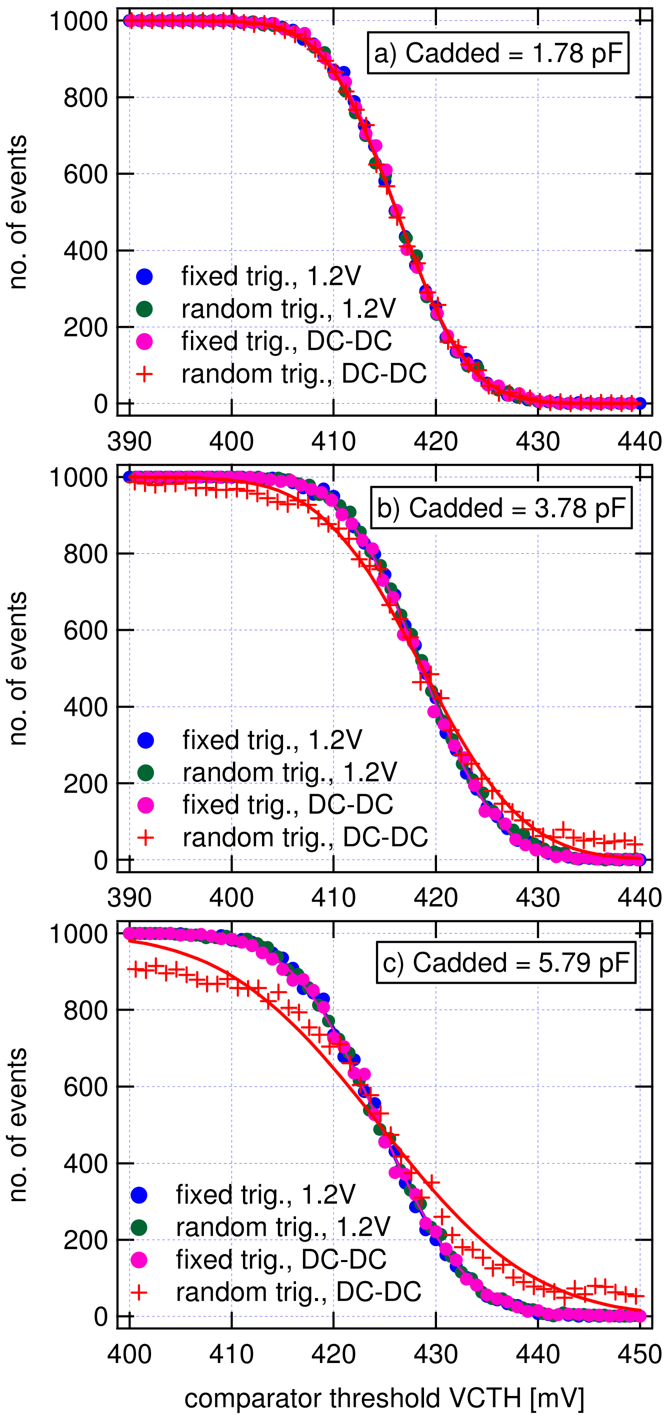
1 MHz diff. clock to DC-DC circuit

DC-DC 1.2V feeds **VDDD** (dig. supply) and **VLDOI** (LDO I/P)

1.1V LDO O/P **VLDOO** feeds analogue stages supply **VDDA**

alternatively can choose not to use the DC-DC powering

and just power VDDD from 1.2V DC supply



DCDC effects on S-curves

triggering conditions

fixed trig: always send trigger at same phase w.r.t. 1 MHz DC-DC clock phase

random trig. trigger at any random time within DC-DC clock cycle

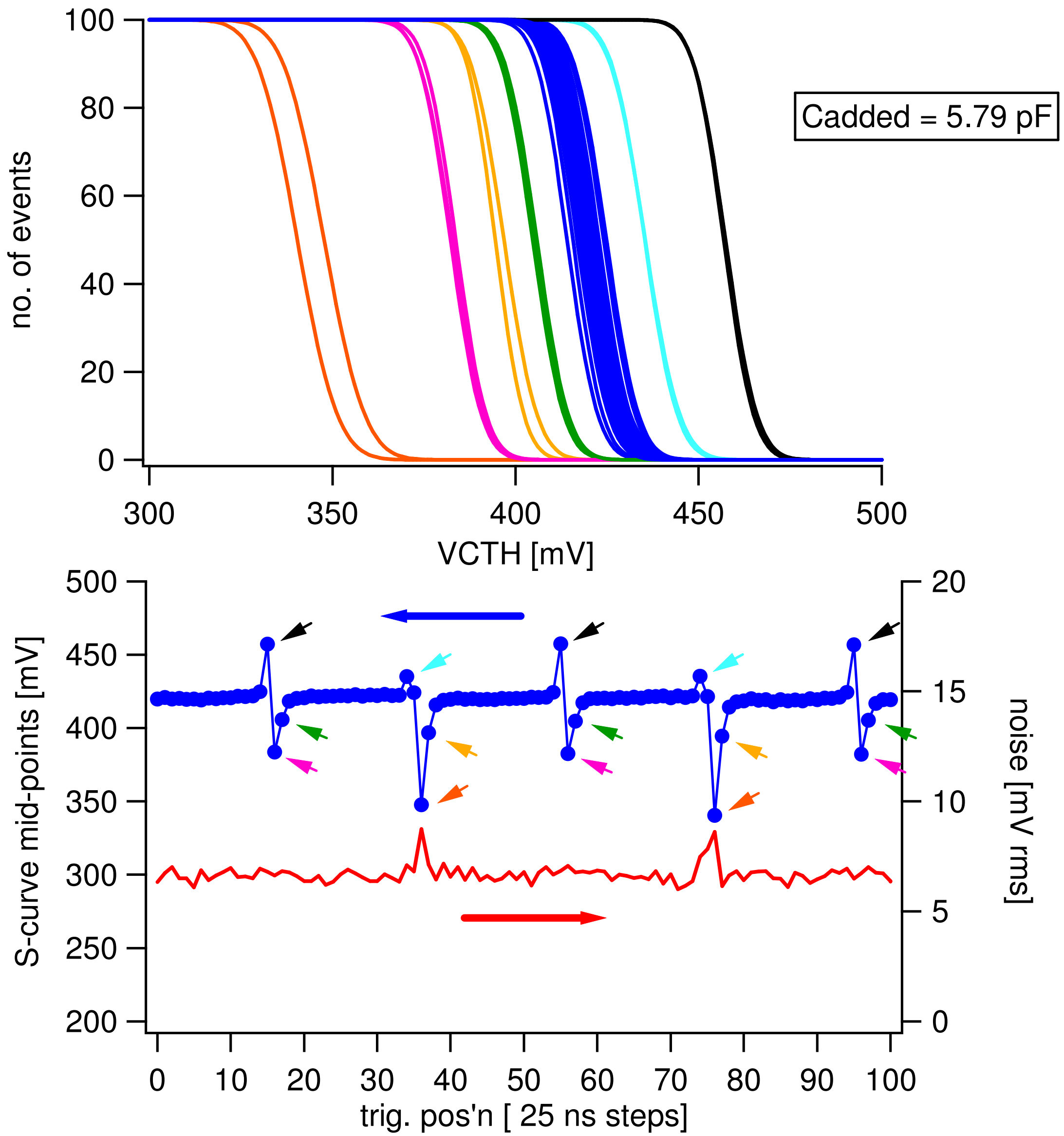
results

no effects at all if CBC powered from 1.2V DC rail (irrespective of triggering conditions)

no effects if CBC triggered at fixed time relative to 1 MHz DC-DC clock phase

increasing s-curve distortion with external capacitance if CBC triggered with random phase relationship to 1 MHz

for largest external capacitance



systematic study (DC-DC circuit operating)

acquire s-curves with increasing separation between fast reset time and trigger position (25 nsec steps)

not all s-curves in same position

plotting s-curve mid-point vs vs. trigger position shows repetitive structure

separation between positive (or negative) shifts = 40 steps = 1 usec = DC-DC period

pedestal shift only, no change in shape

=> intrinsic noise unaffected

magnitude of effect proportional to external capacitance to ground

s-curves in top plot colour coded to show which ones correspond to which point in bottom plot

summary for CBC1

fundamental performance of DC-DC circuit itself is good

high efficiency for 2:1 step down conversion

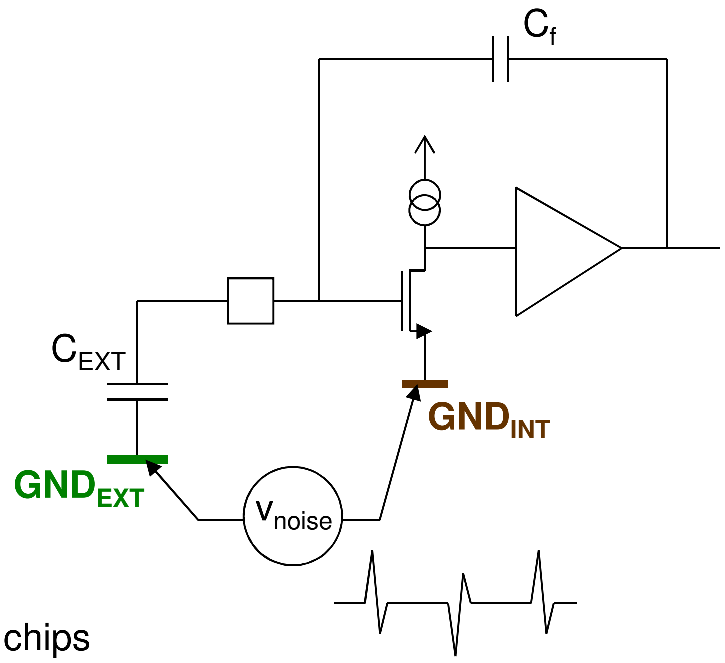
no significant effect on intrinsic noise

but switching transients appear to couple to internal chip ground causing pedestal shifts

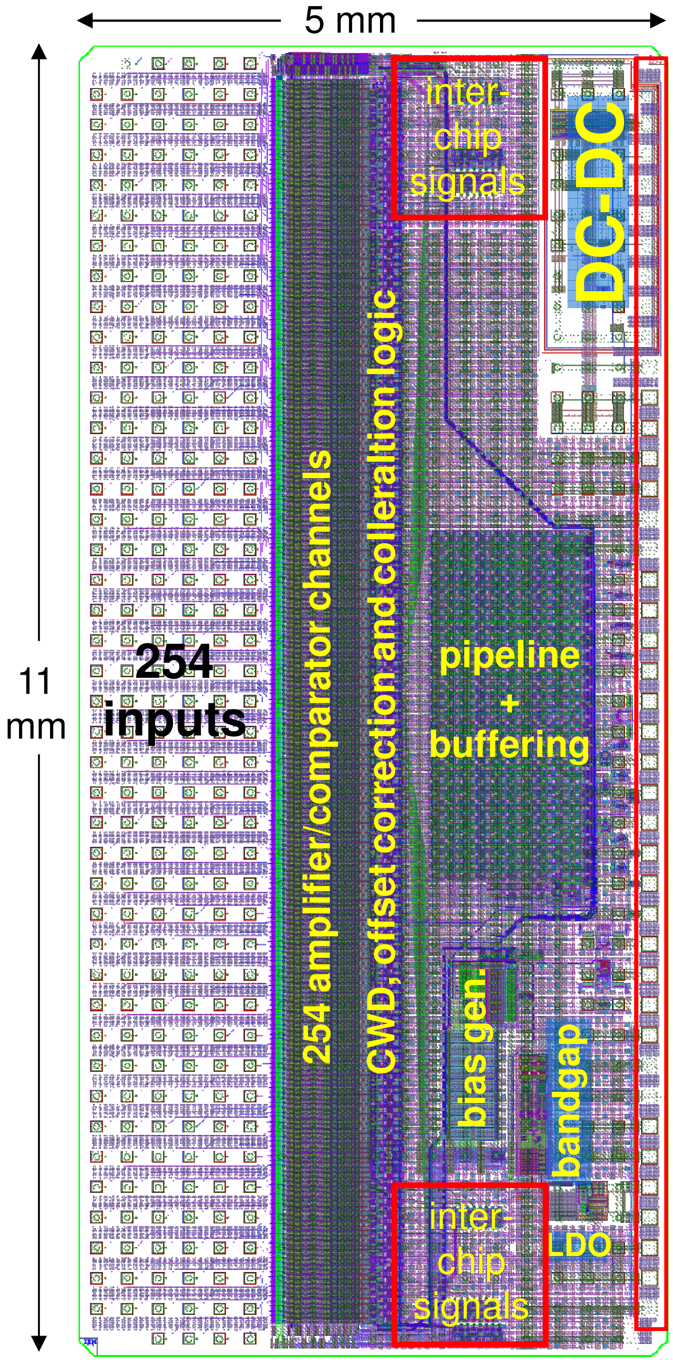
- magnitudes dependent on external capacitance

worth noting: this would likely not be a problem for hybrid pixel chips

low sensor capacitance
low inductance bump-bond coupling between sensor and chip grounds



CBC2

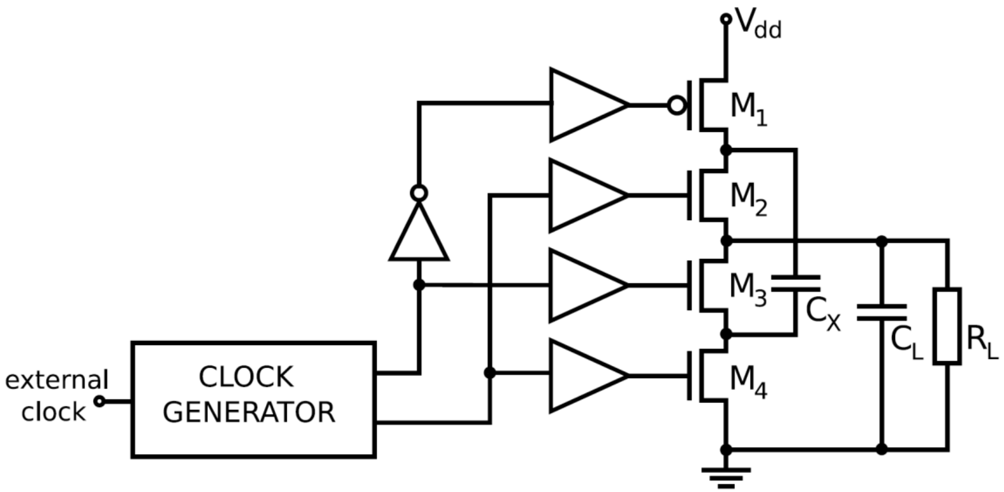


C4 layout, 250um pitch, 19 columns x 43 rows

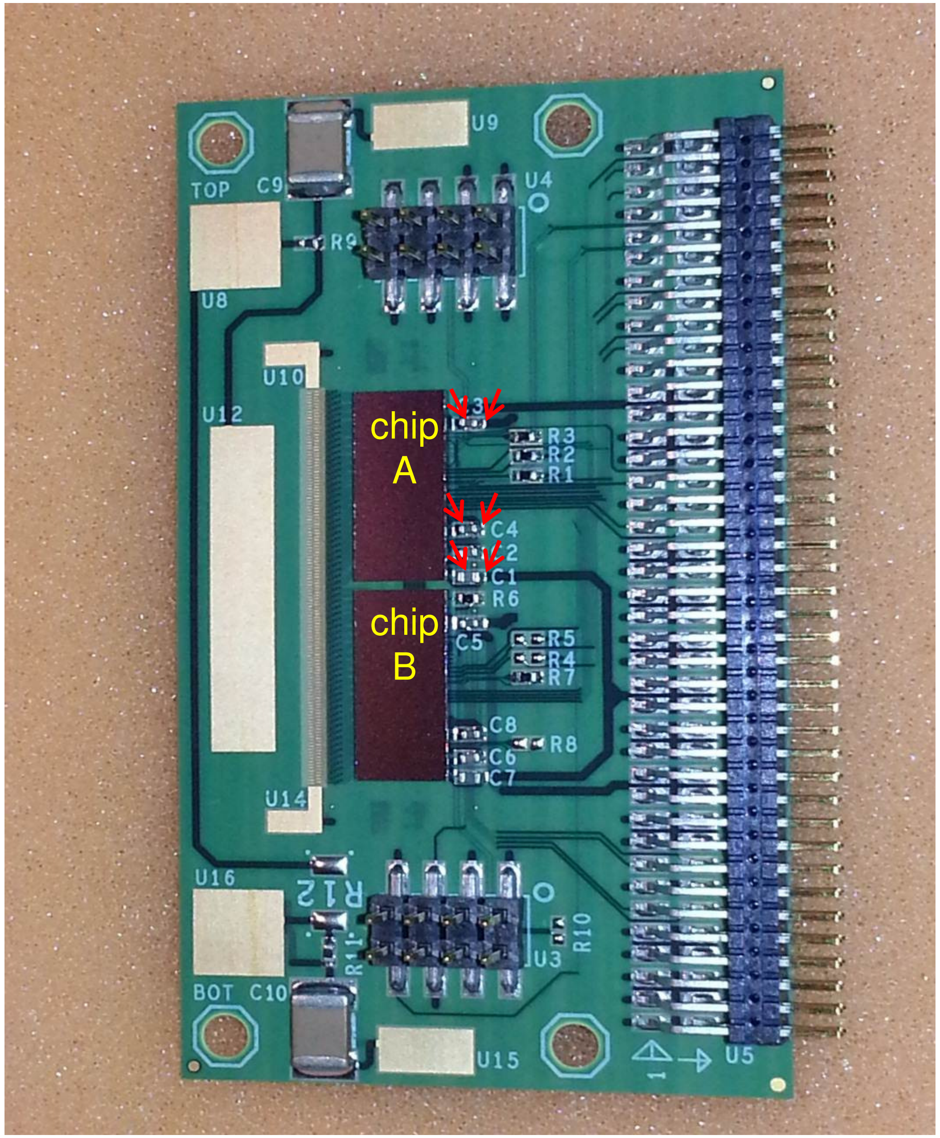
DC-DC powering features retained

- bandgap, LDO for analogue powering, same as prototype
- improved step-down DC-DC switched capacitor circuit
  - slower switching edges & rad-hard layout

design by Stefano Michelis (CERN)



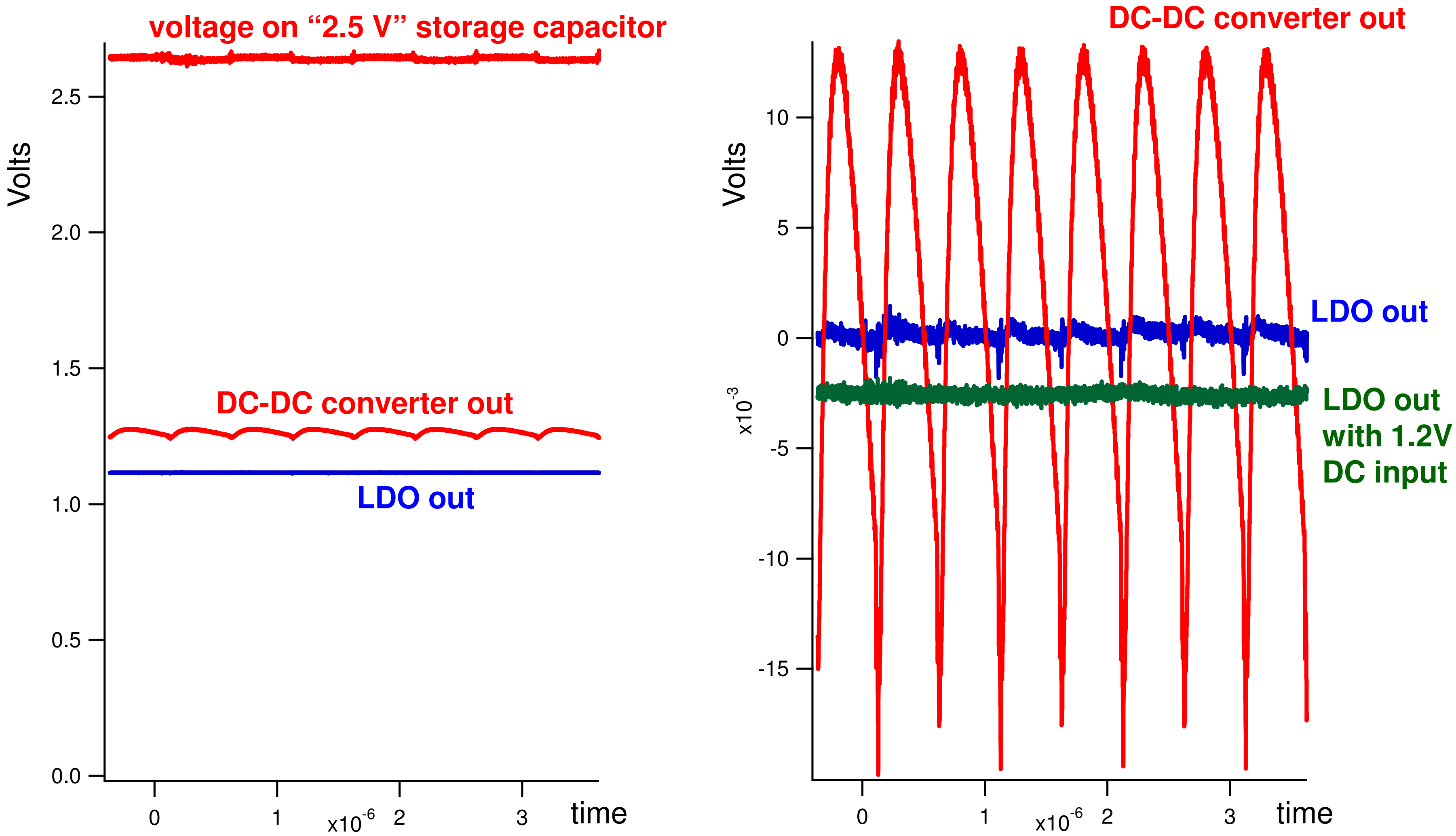
start by looking at power rails on scope



use diff probe on capacitors

C1/C7 2.5 V in
C4/C8 DCDC output voltage ~1.2
C3/C5 LDO out ~1.1

probing voltages



efficiency measurement

DC powering: 2 chips draw 141 mA from 1.21 V => 171 mW

DC-DC powering: 73.2 mA from 2.6V => 190 mW

=> ~90% efficiency

effect on noise

experimental study results here performed using module#5

one CNM n-on-p sensor only => half of channels see capacitive load of sensor
other half channels unbonded

interesting to see differences between bonded and unbonded channels

module powered using either:

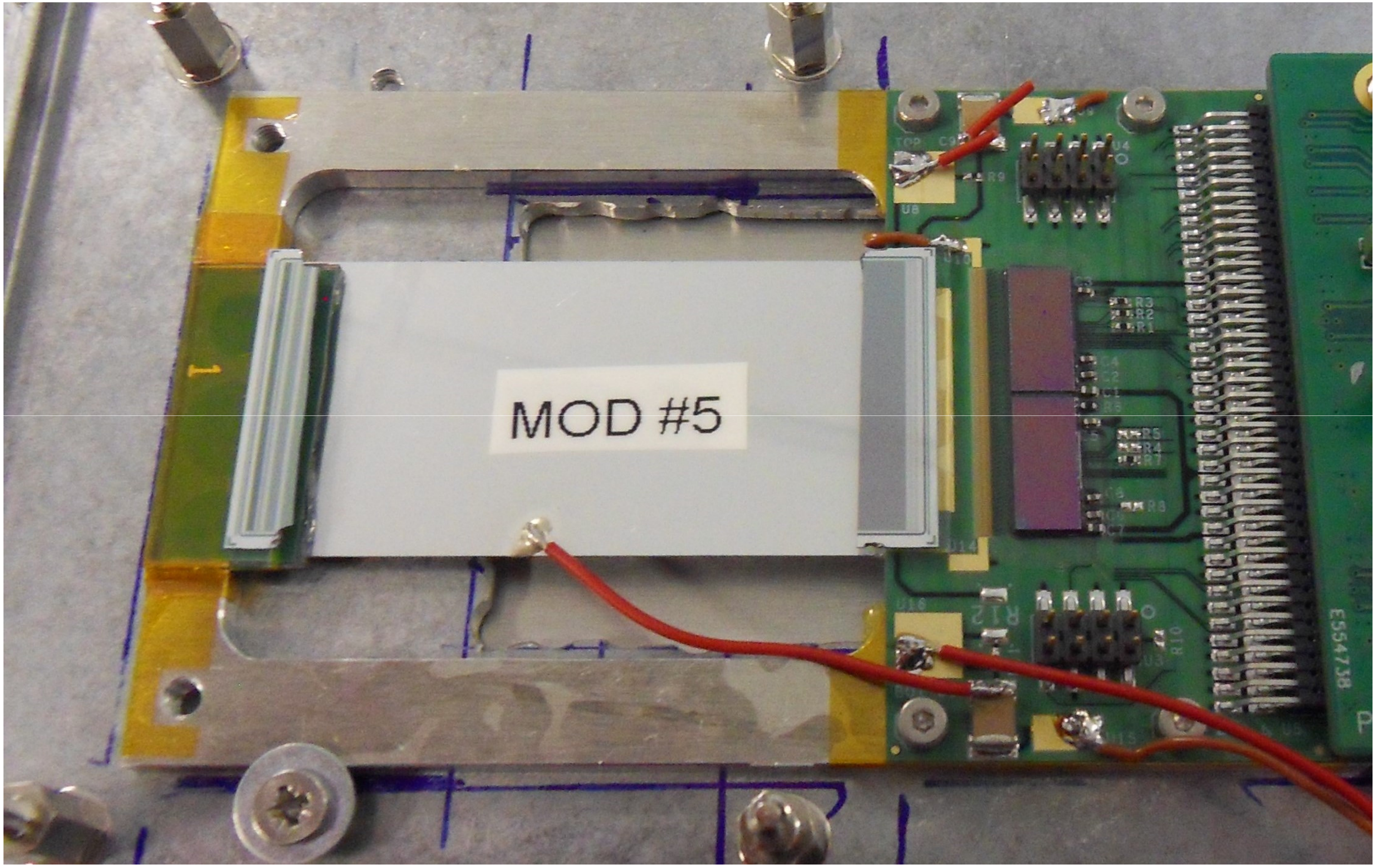
DC: ~1.2 V supplied to VDDD (digital rail)
1.1 V VDDA derived from VDDD via LDO

DC-DC: ~2.6 V supplied to switched cap circuit running at 1 MHz
DC-DC supplies ~1.2 V VDDD
1.1 V VDDA derived from VDDD via LDO

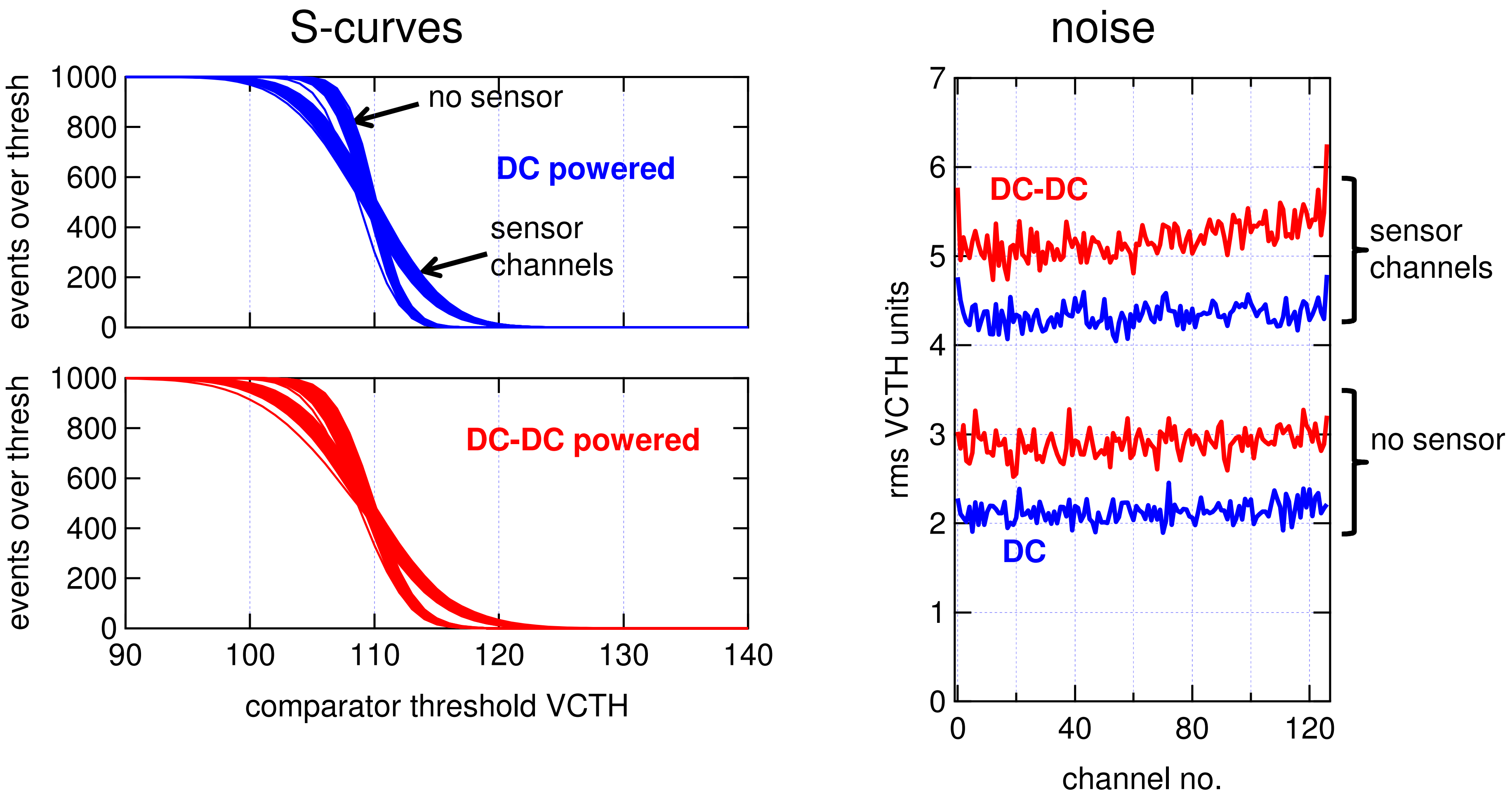
initial triggering conditions

pseudo-random triggered readout (i.e. no fast reset between triggers)
1 MHz DC-DC clock provided by external oscillator
(not synchronized to 40 MHz)

module #5



effect on noise



results for chip A here - results for chip B look the same
significant noise increase for DC-DC powering

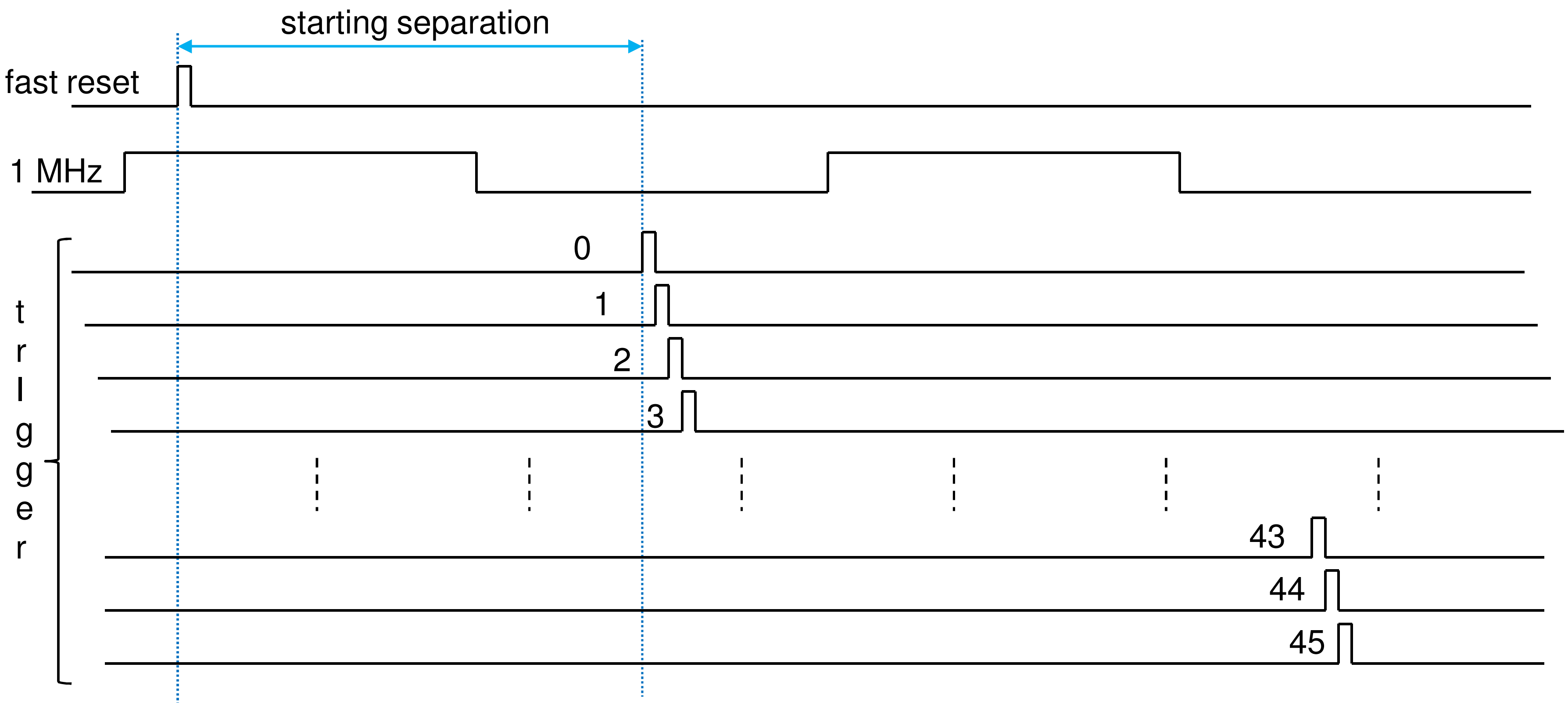
study more systematically

synchronize 1 MHz DC-DC clock with 40 MHz

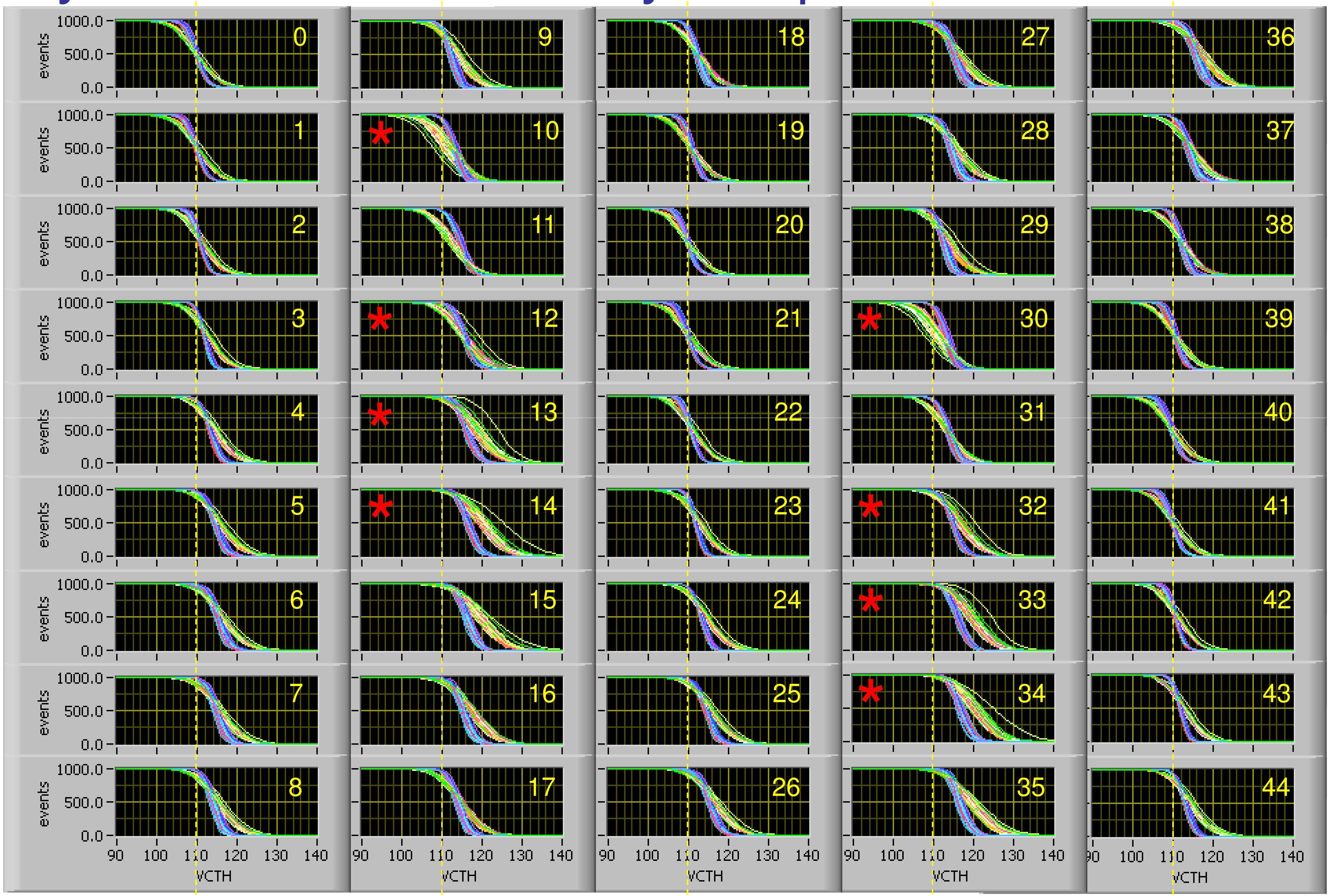
include fast reset in trigger sequence

look at s-curve dependence on fast reset - trigger separation

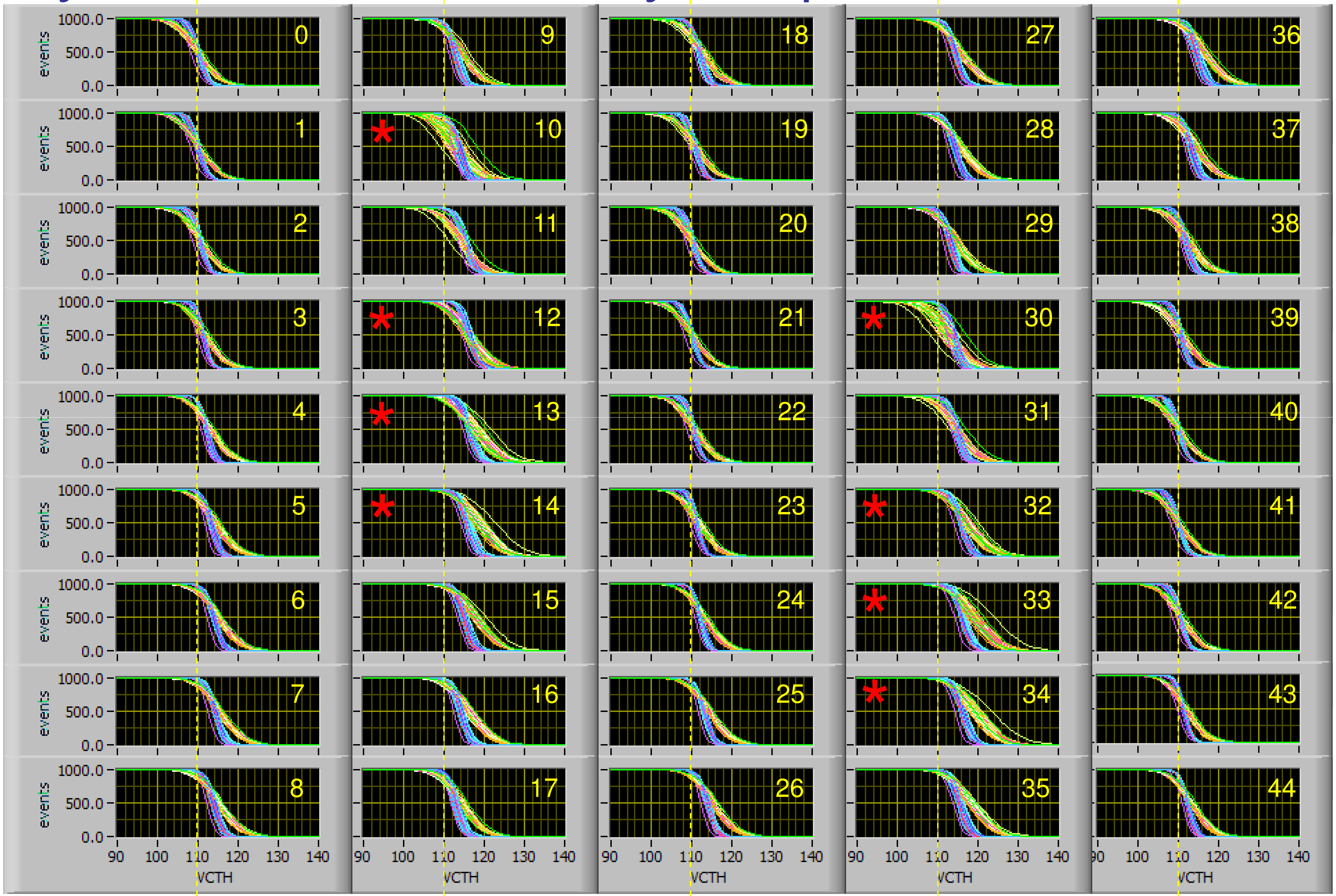
increase separation in 25 ns steps (0, 1, 2, 3, ……43, 44, 45) to cover complete 1 MHz period



systematic s-curve study - chip A



systematic s-curve study - chip B



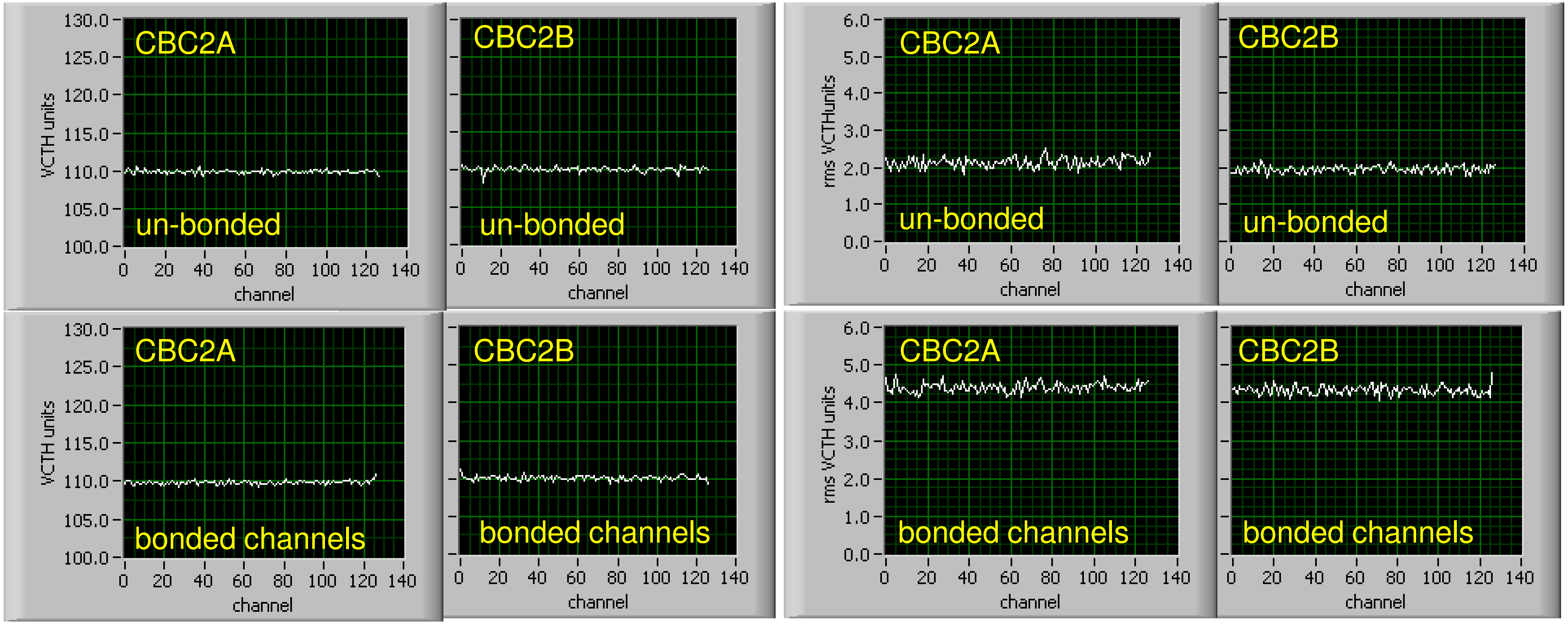
explanatory key to following 44! slides

25ns step value

0

s-curve mid-points

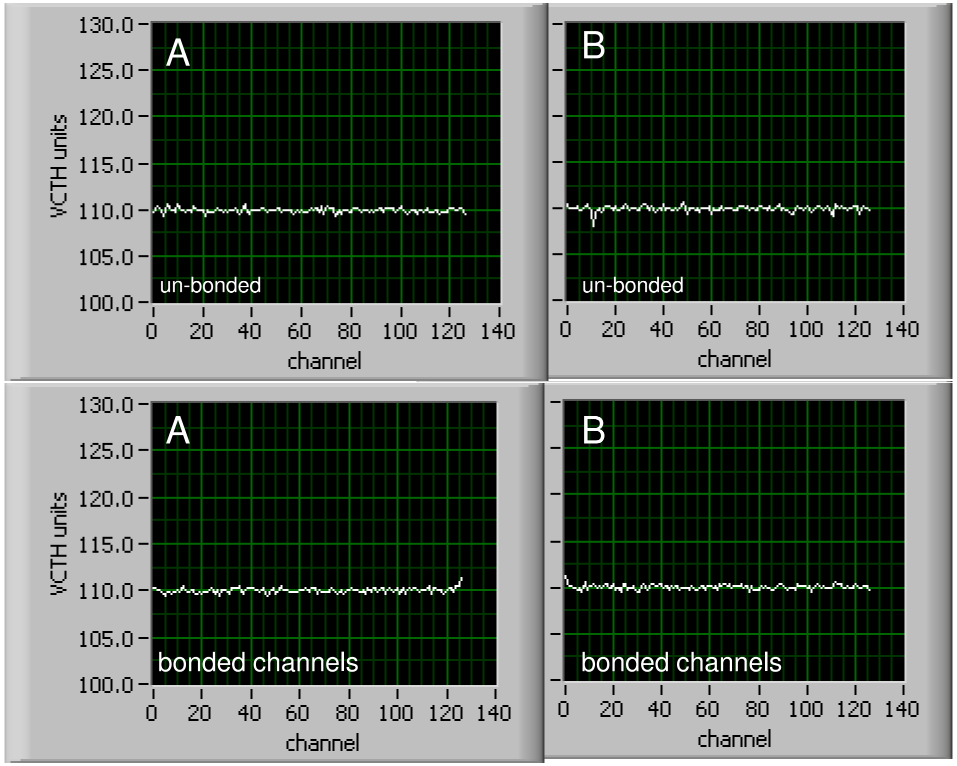
noise



CBC1 results suggest to look for systematic pedestal shifts - can see that from s-curve mid-point plots in 4 leftmost panels

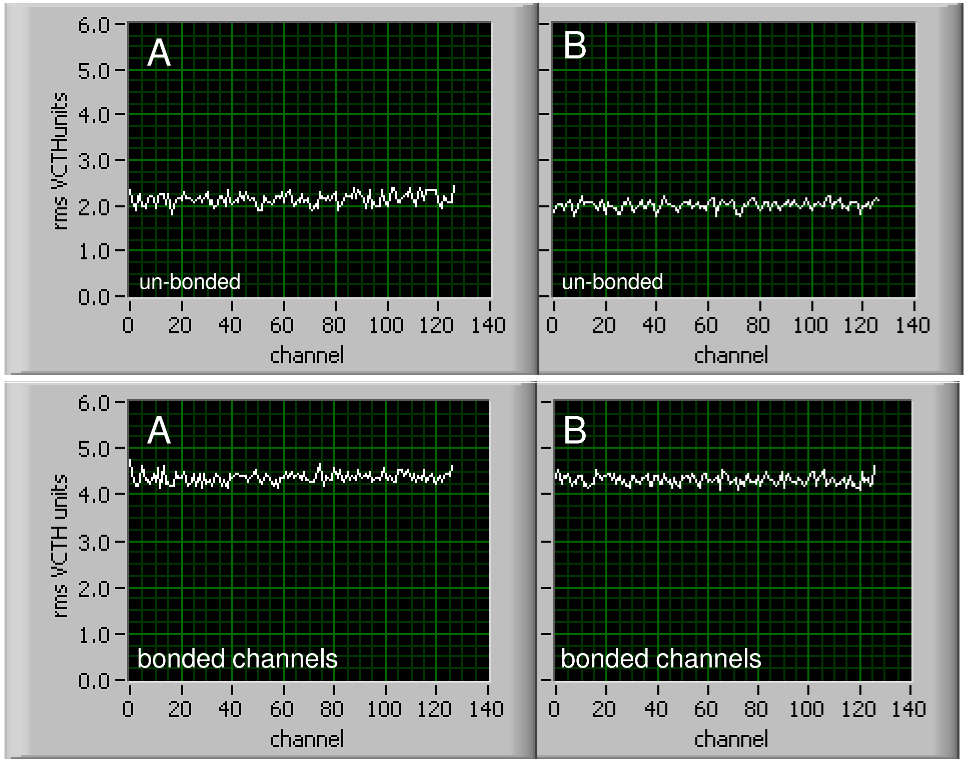
4 rightmost panels show noise calculated from s-curves

s-curve mid-points



noise

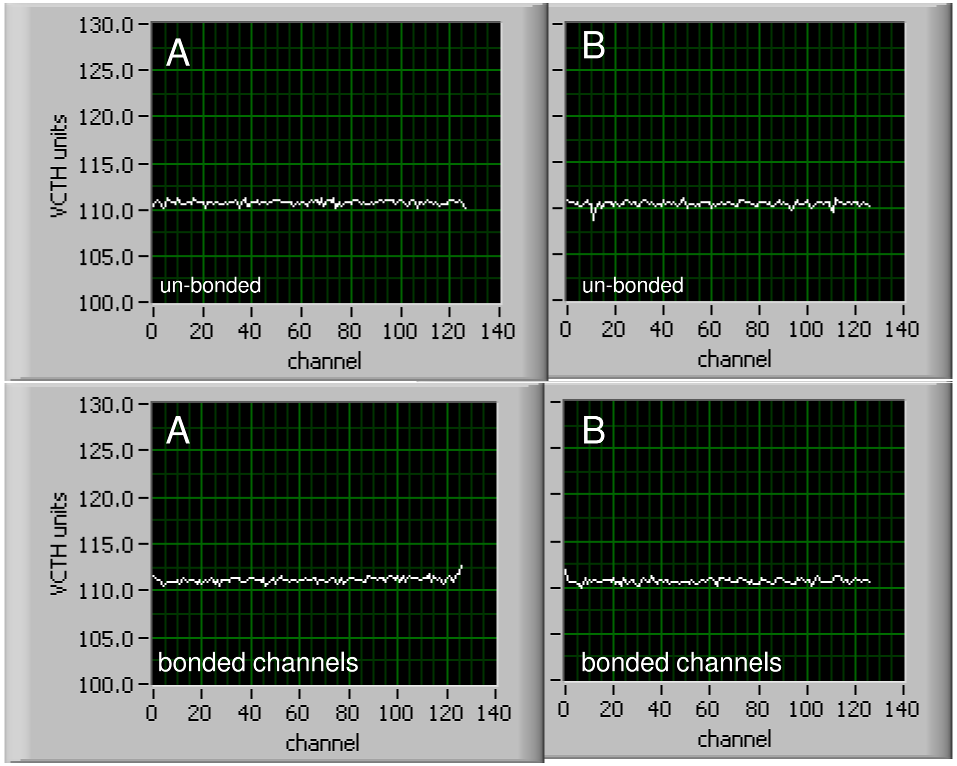
1

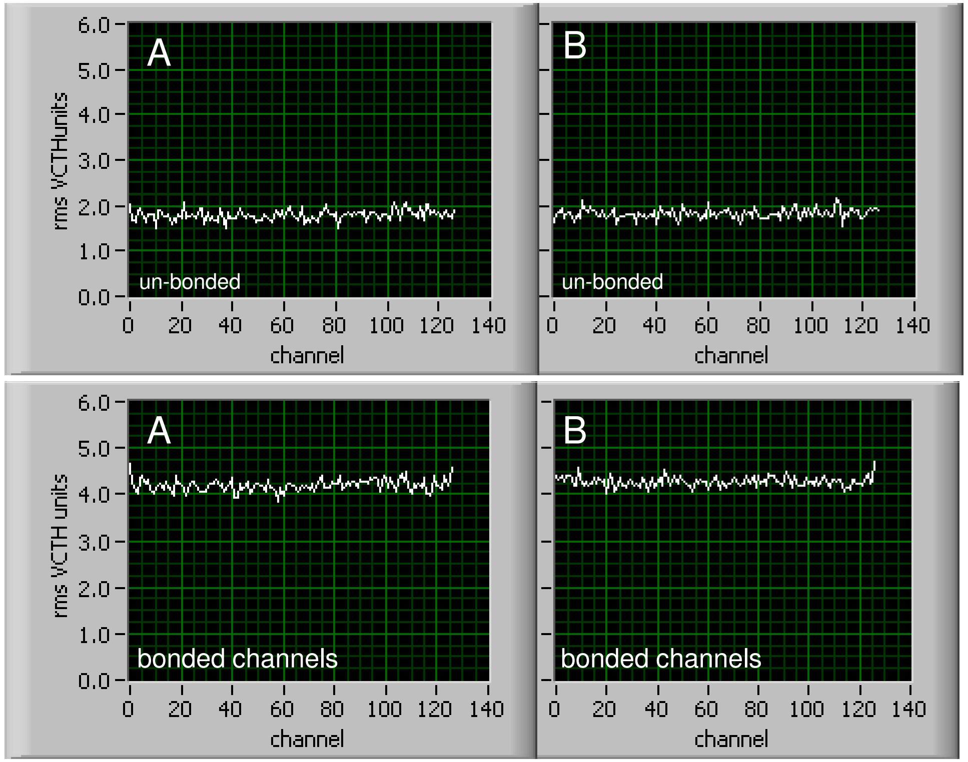


s-curve mid-points

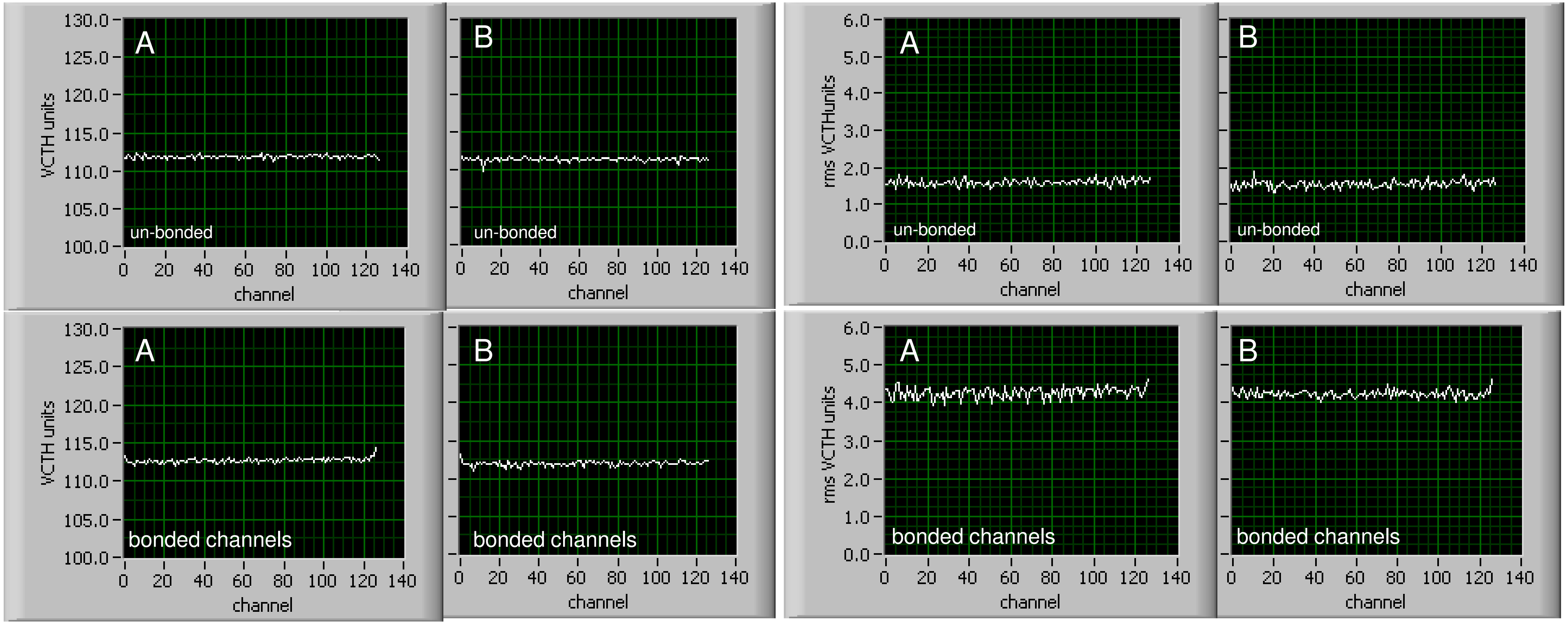
noise

2



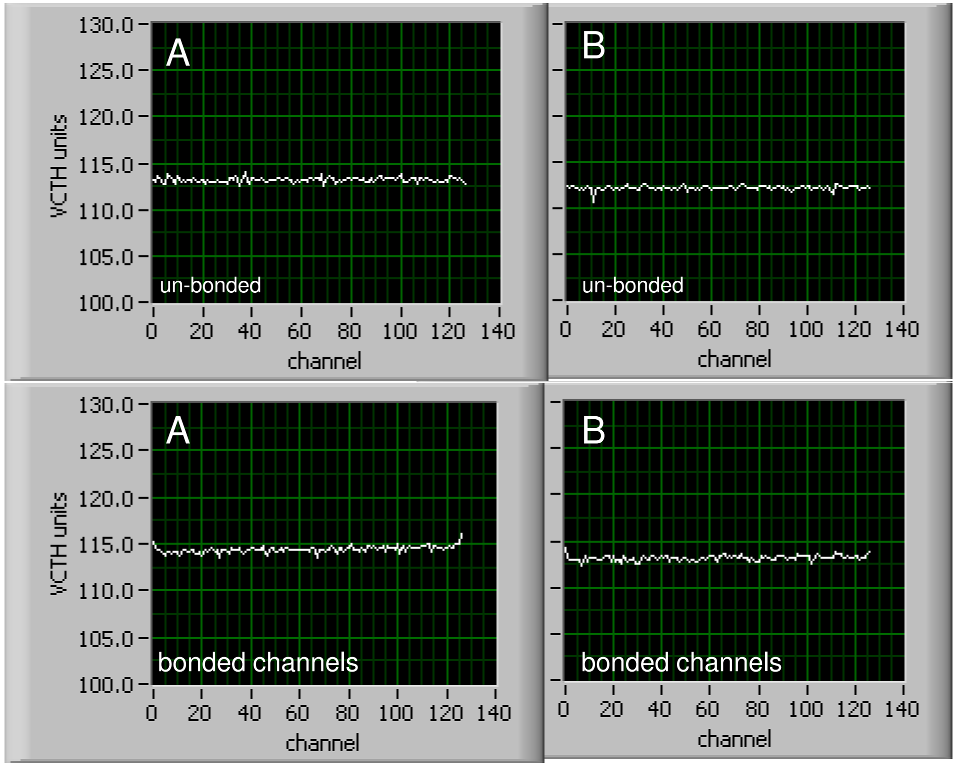


s-curve mid-points noise 3



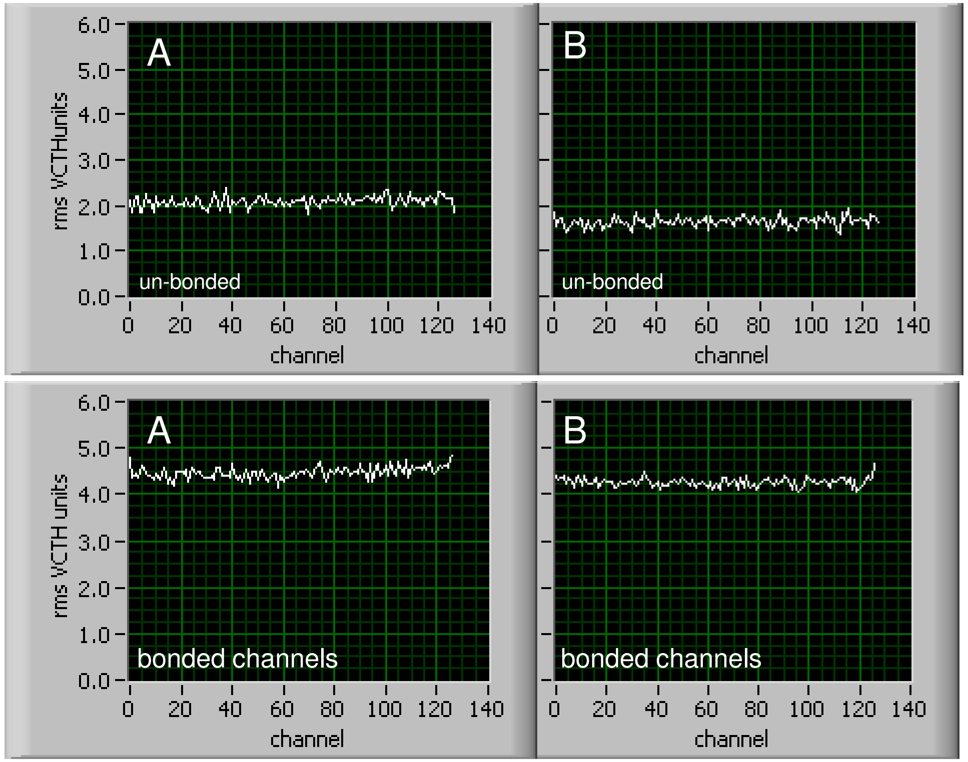
notice “common-mode” pedestal shifts

s-curve mid-points



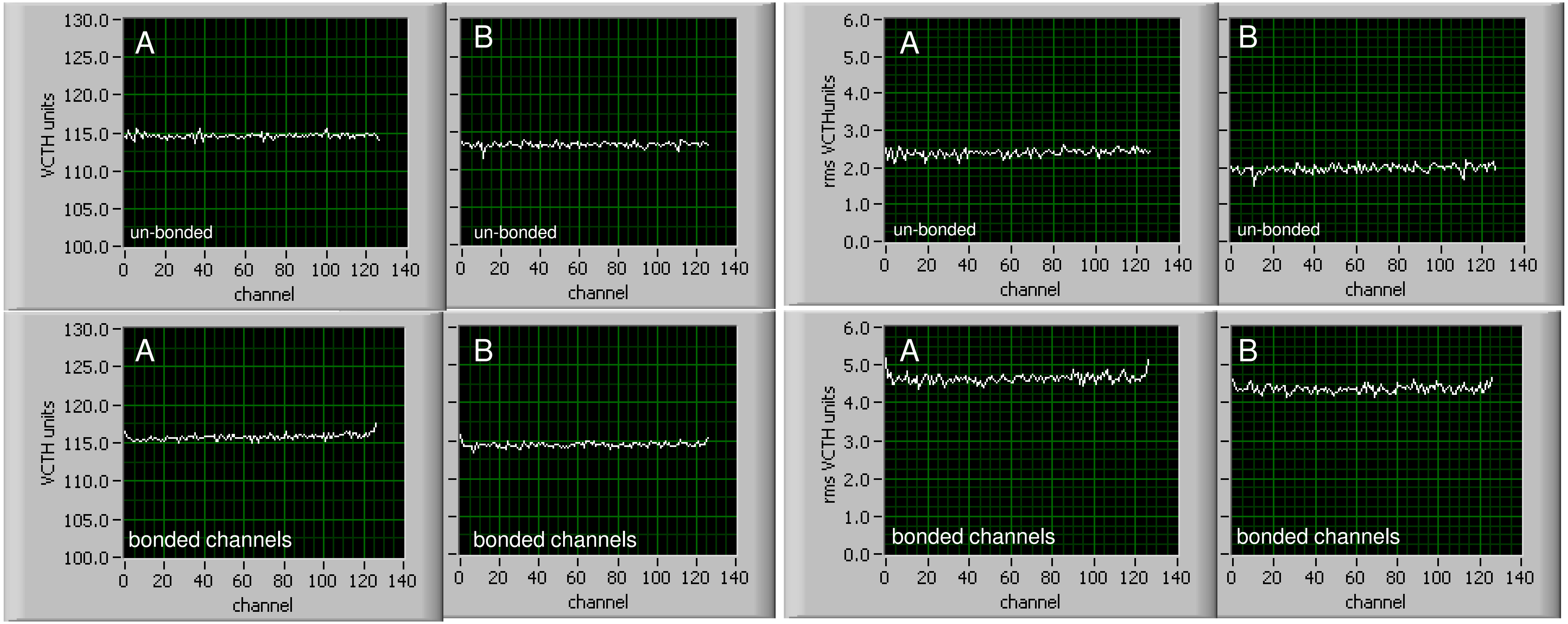
noise

4



notice “common-mode” pedestal shifts

s-curve mid-points   noise   5

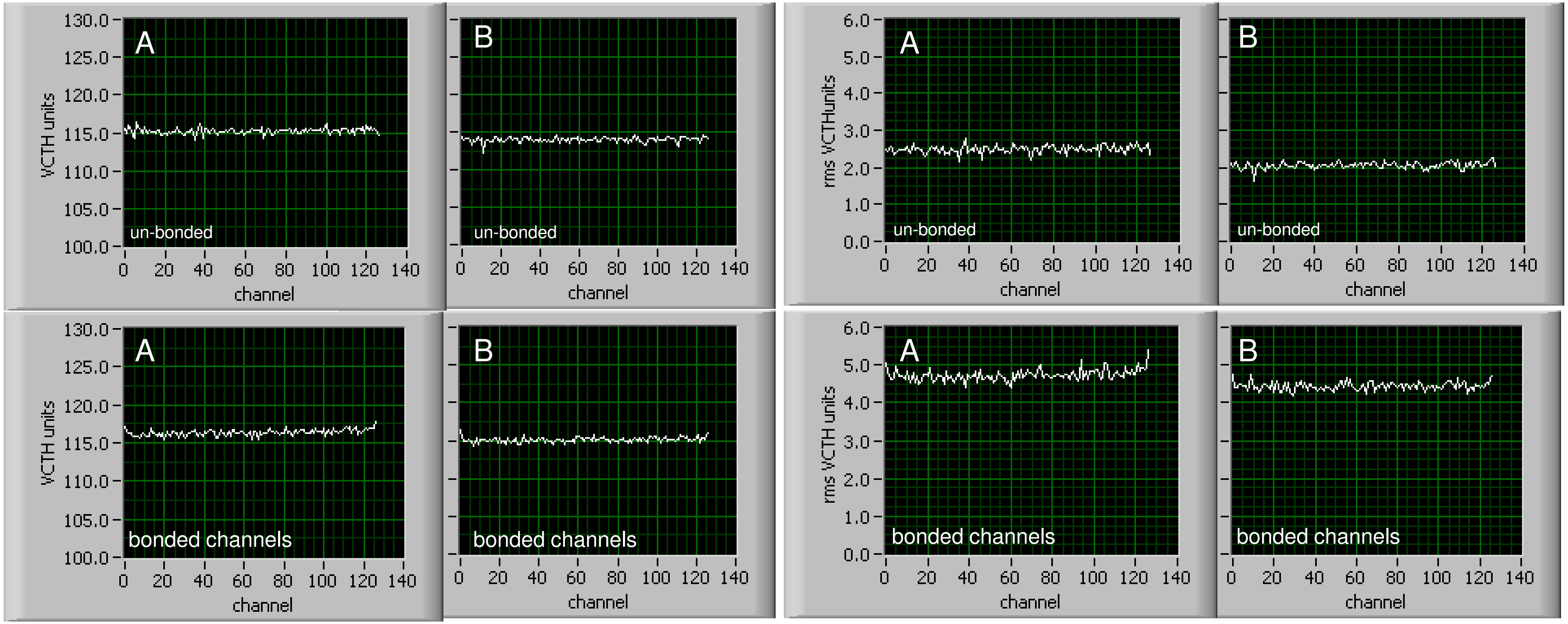


notice “common-mode” pedestal shifts

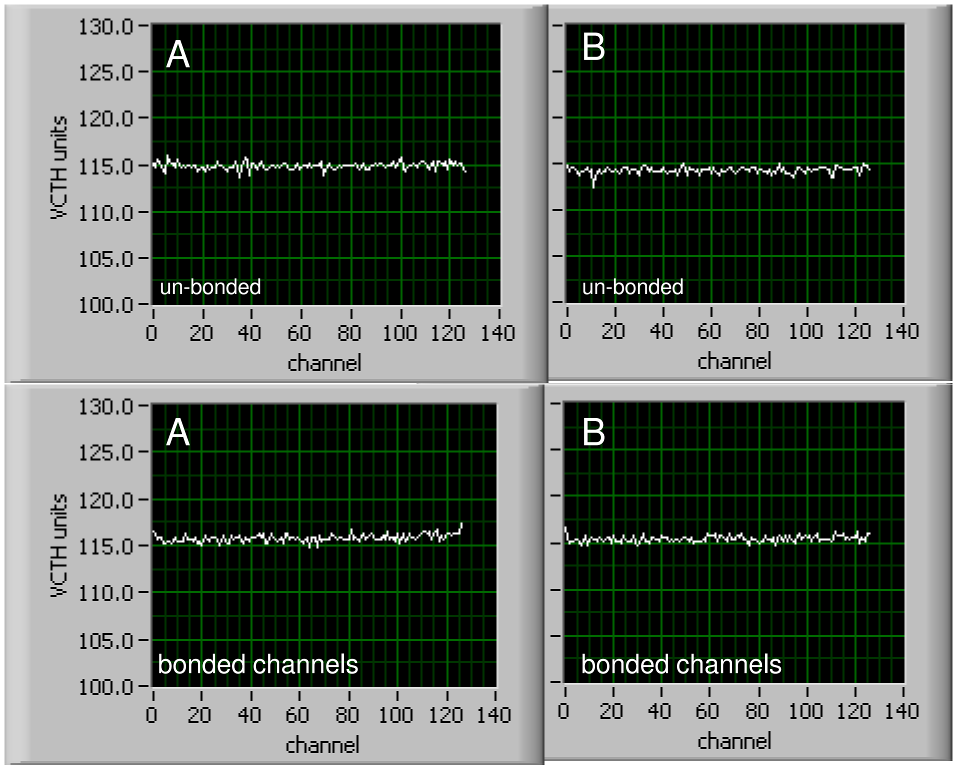
s-curve mid-points

noise

6

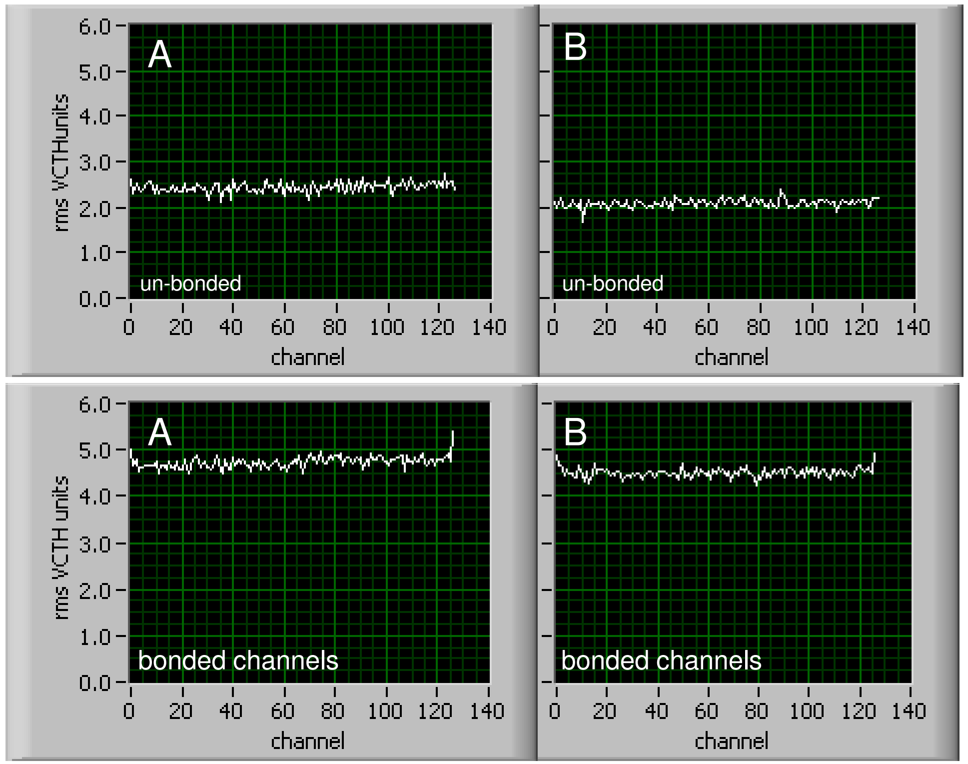


s-curve mid-points

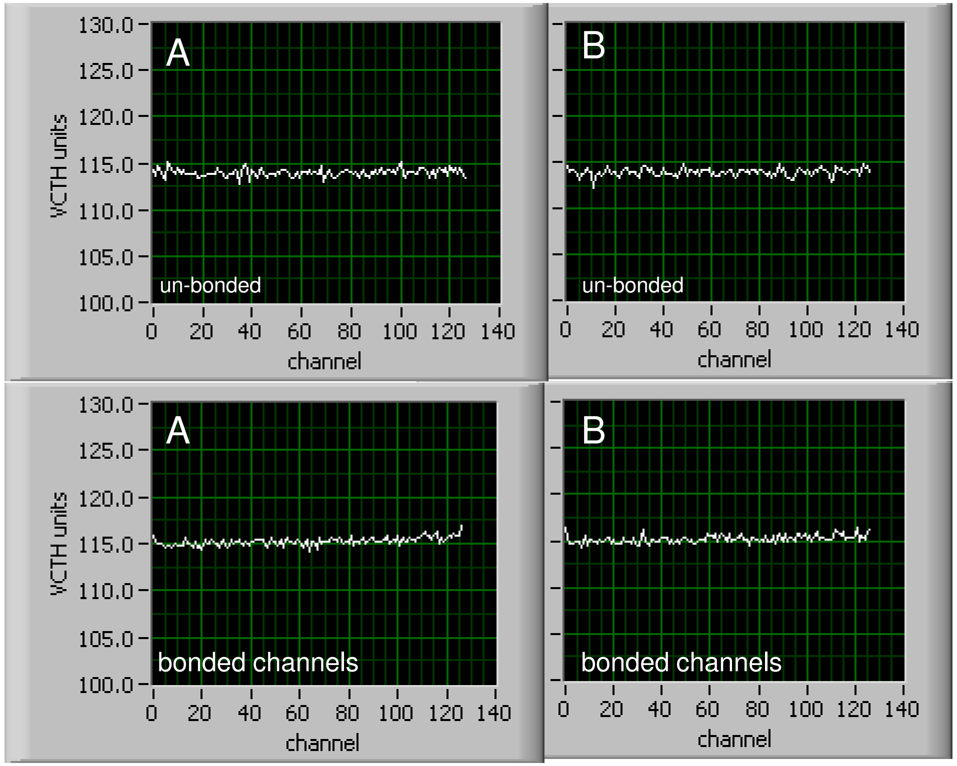


noise

7

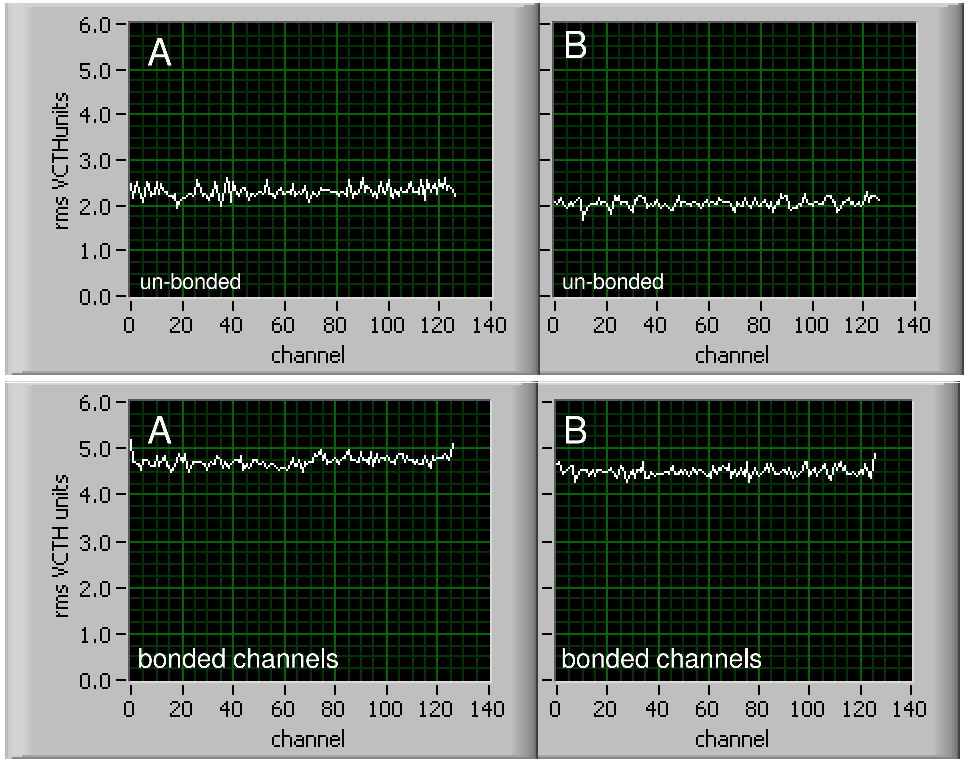


s-curve mid-points

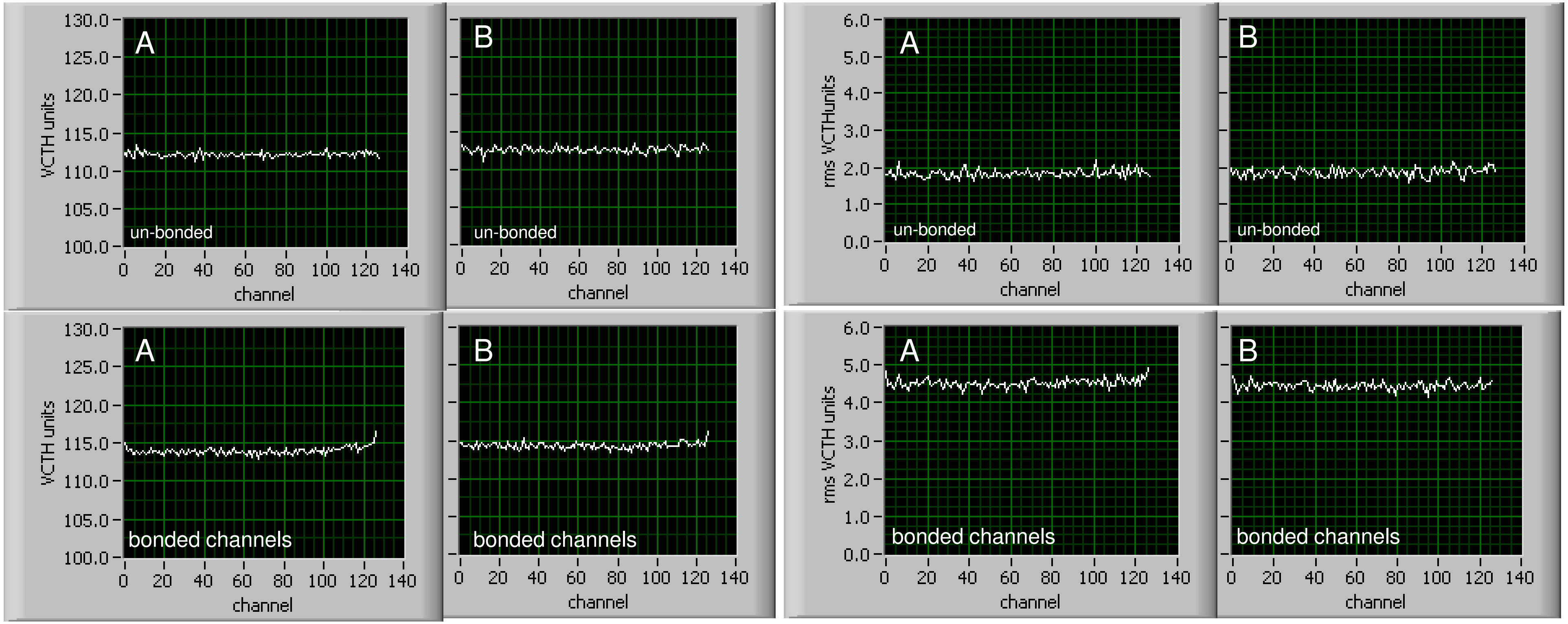


noise

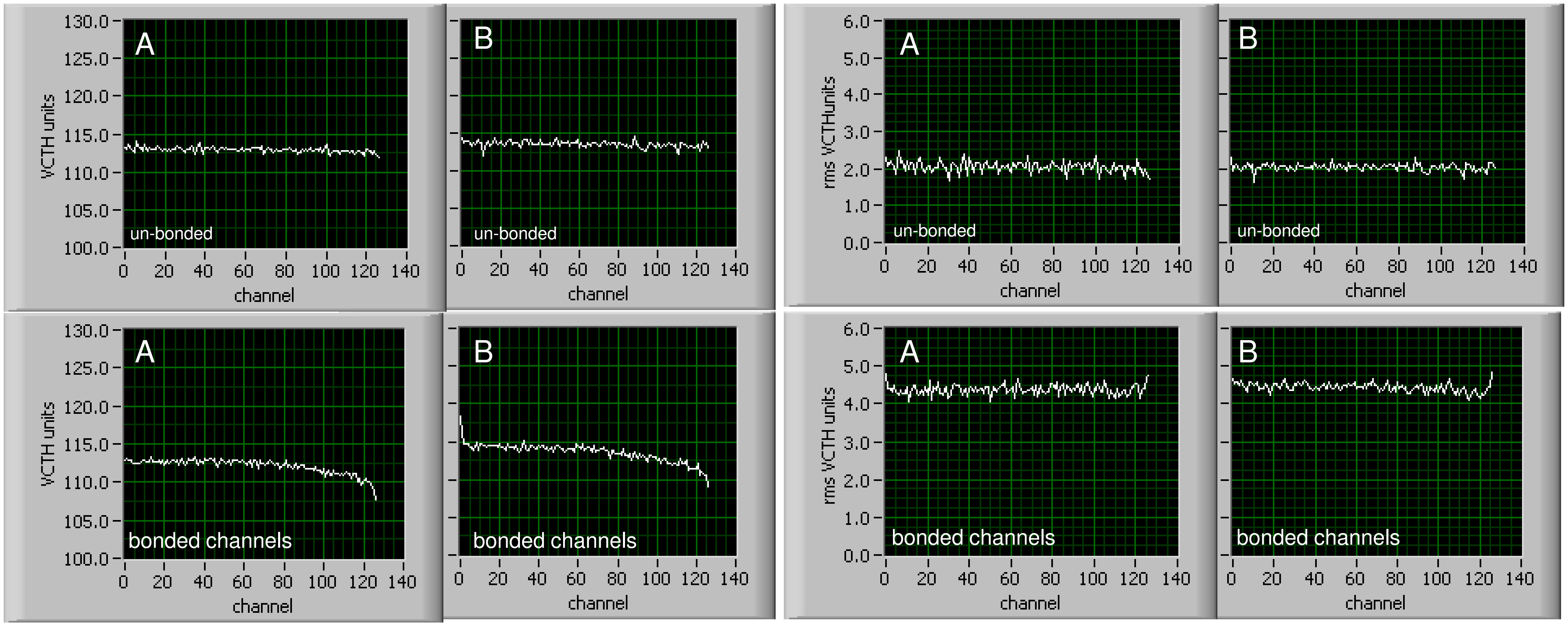
8



s-curve mid-points noise 9



* s-curve mid-points noise 10

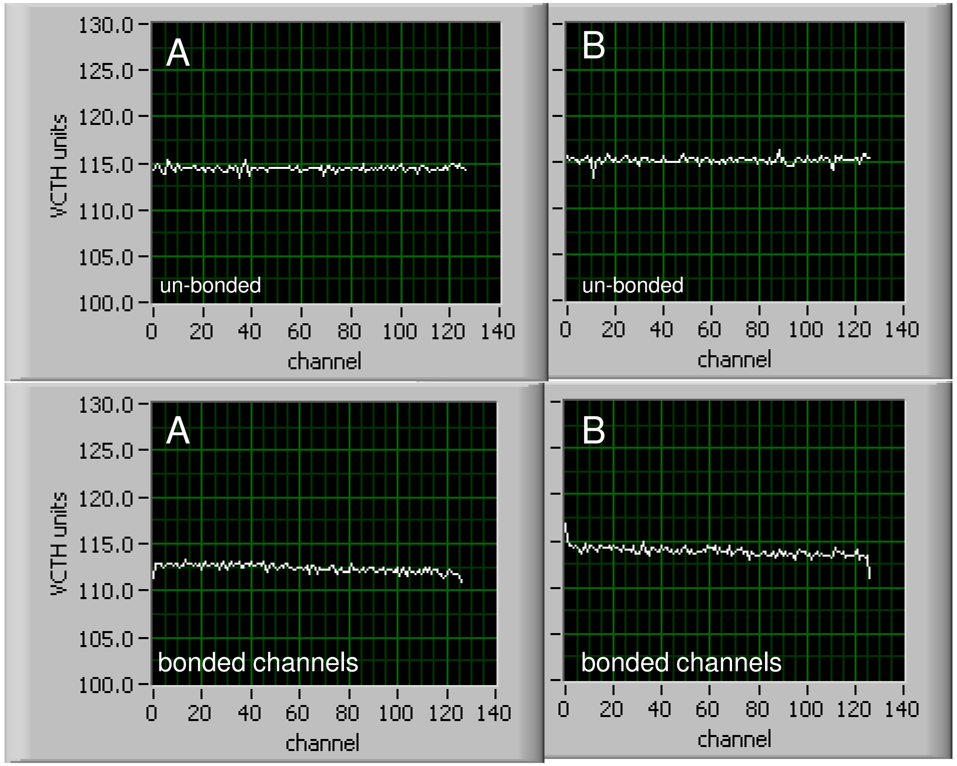


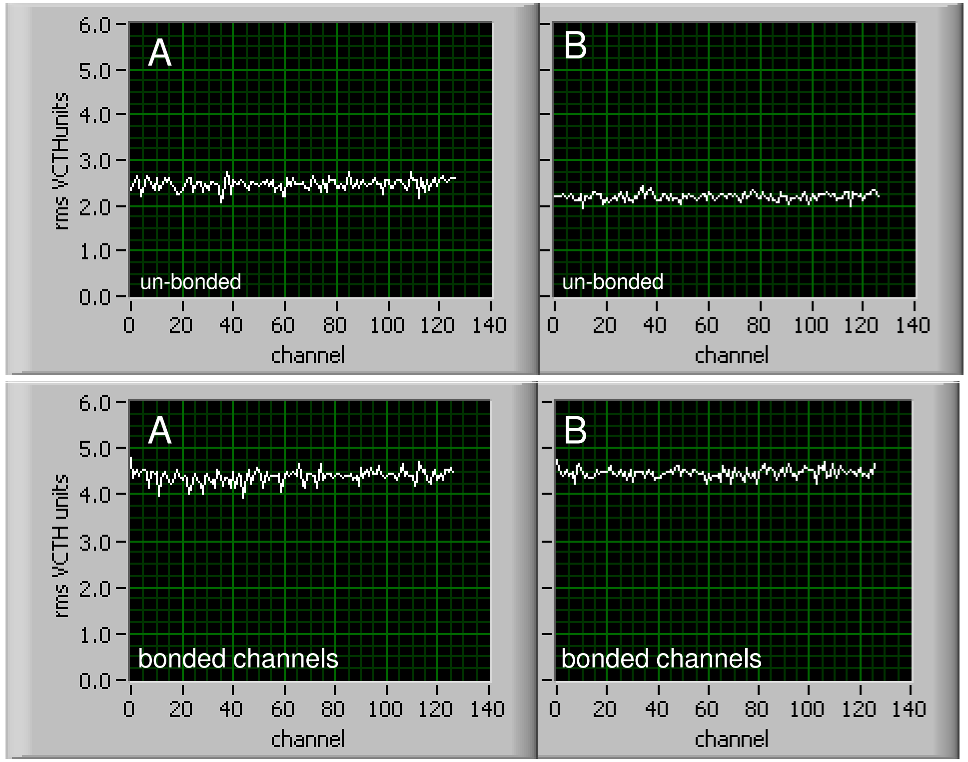
pedestal shift varies across chip - same shape for both chips

s-curve mid-points

noise

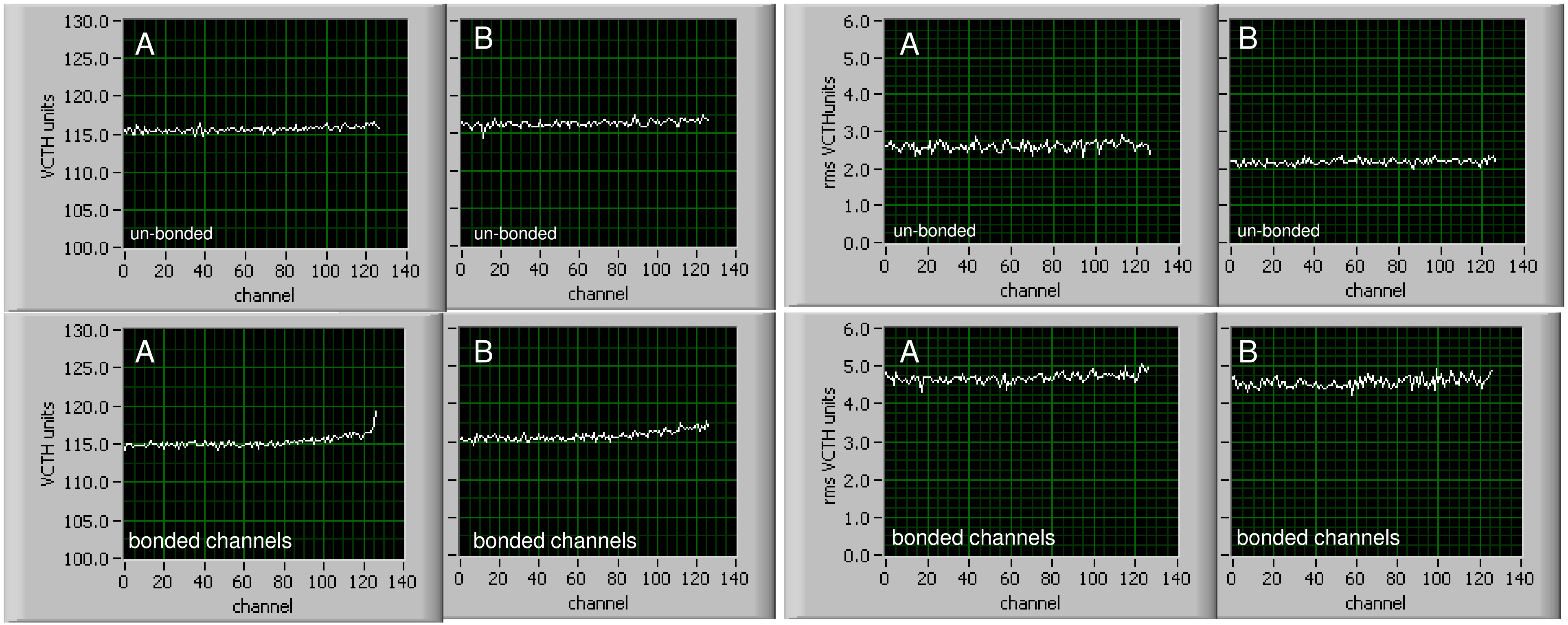
11





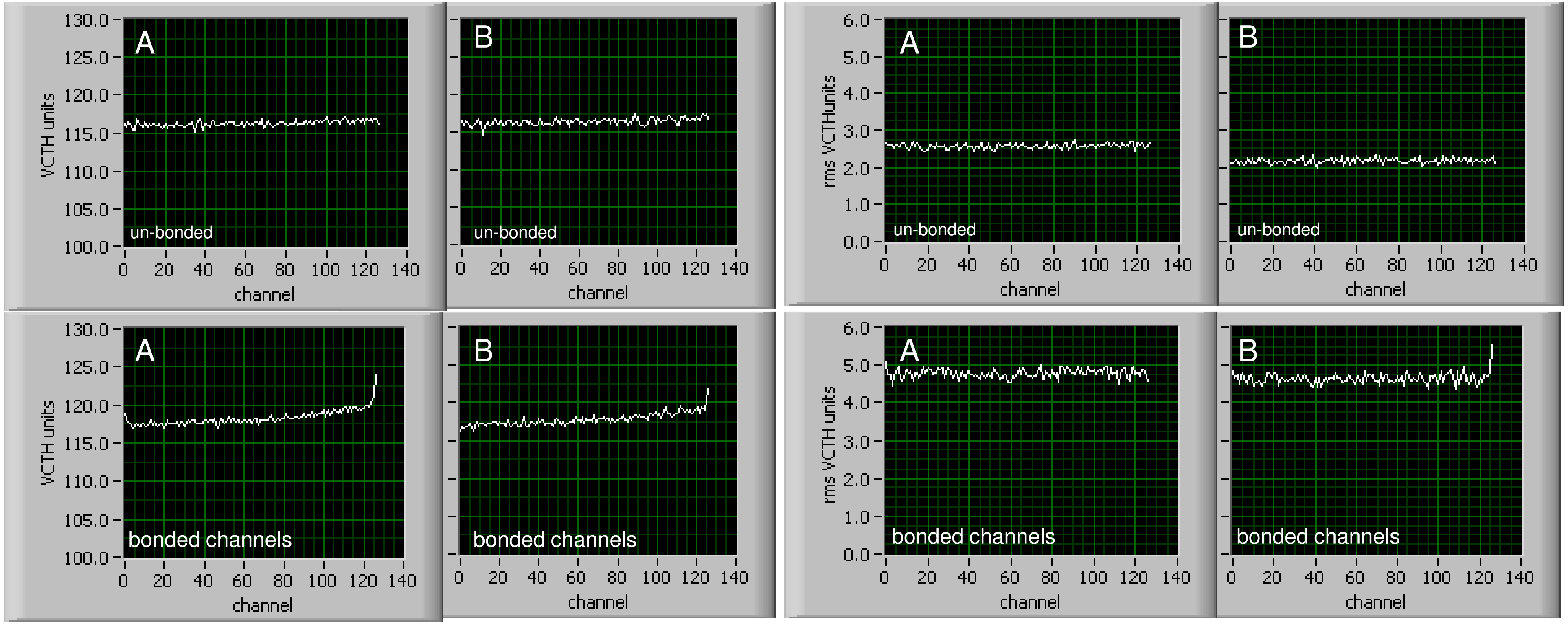
*

s-curve mid-points   noise   12



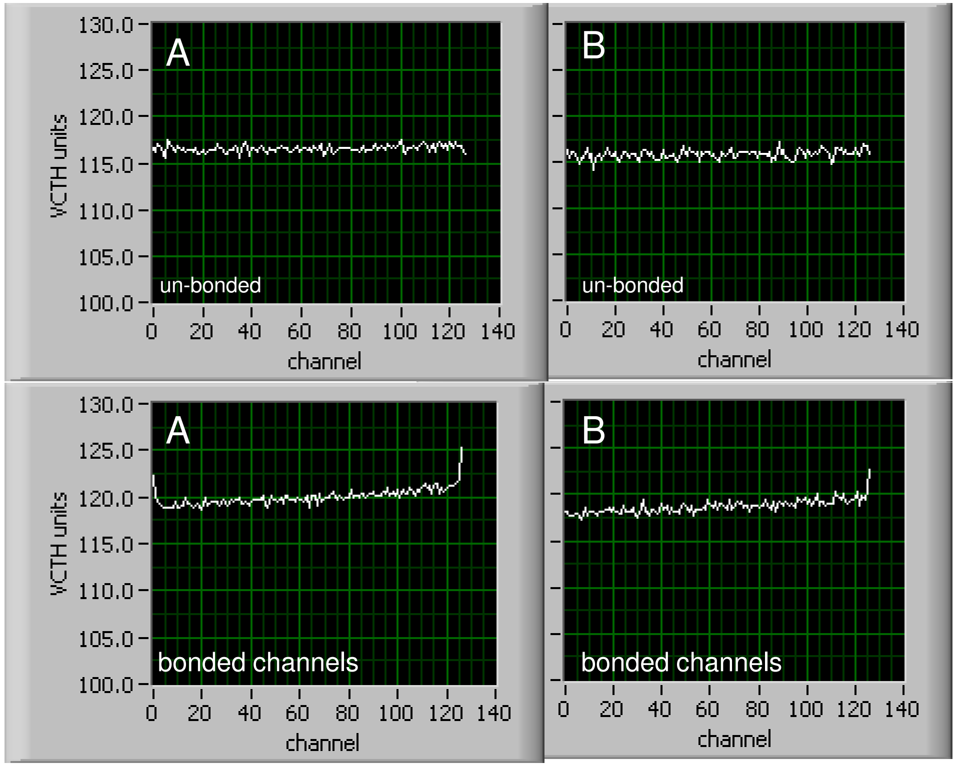
pedestal shift varies across chip - same shape for both chips

* s-curve mid-points noise 13



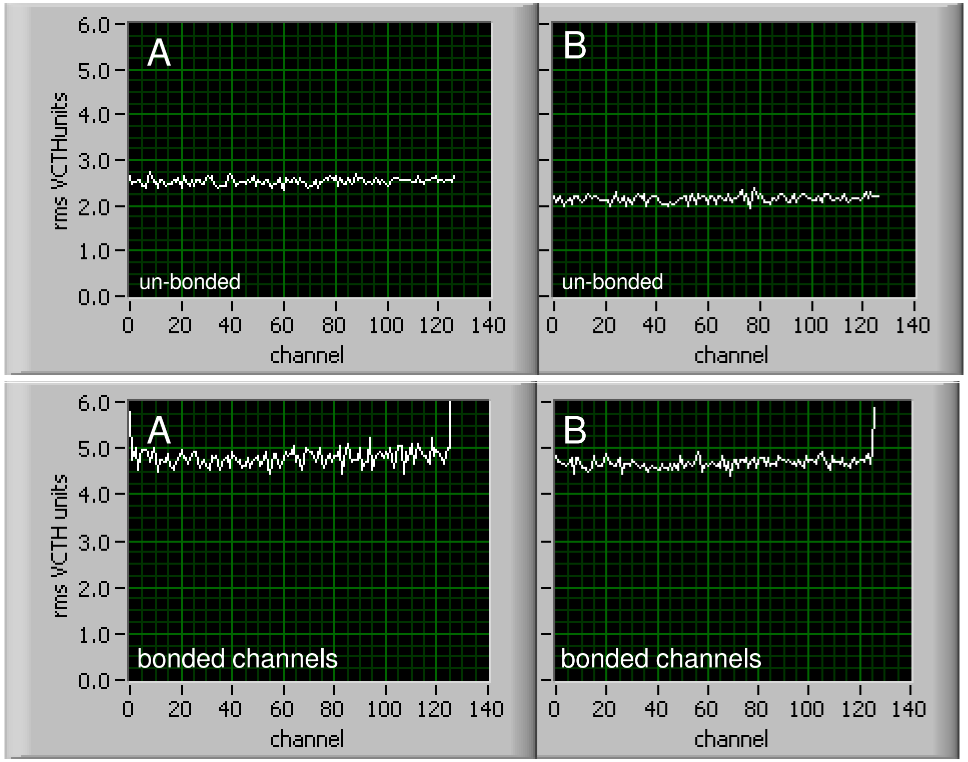
pedestal shift varies across chip - same shape for both chips

* s-curve mid-points



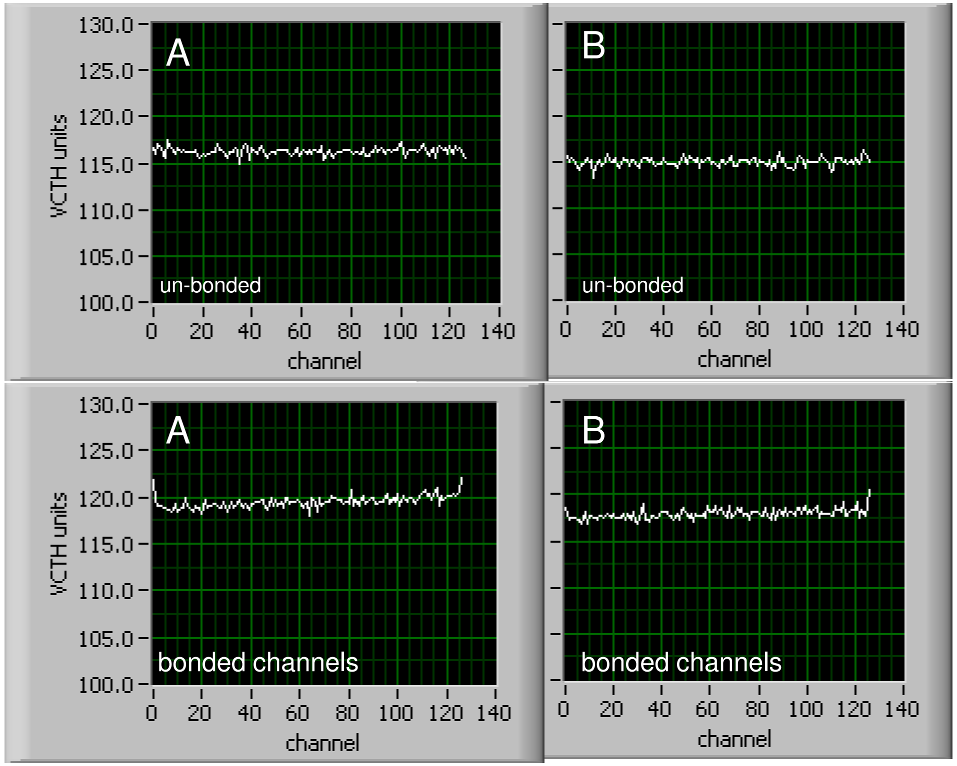
noise

14



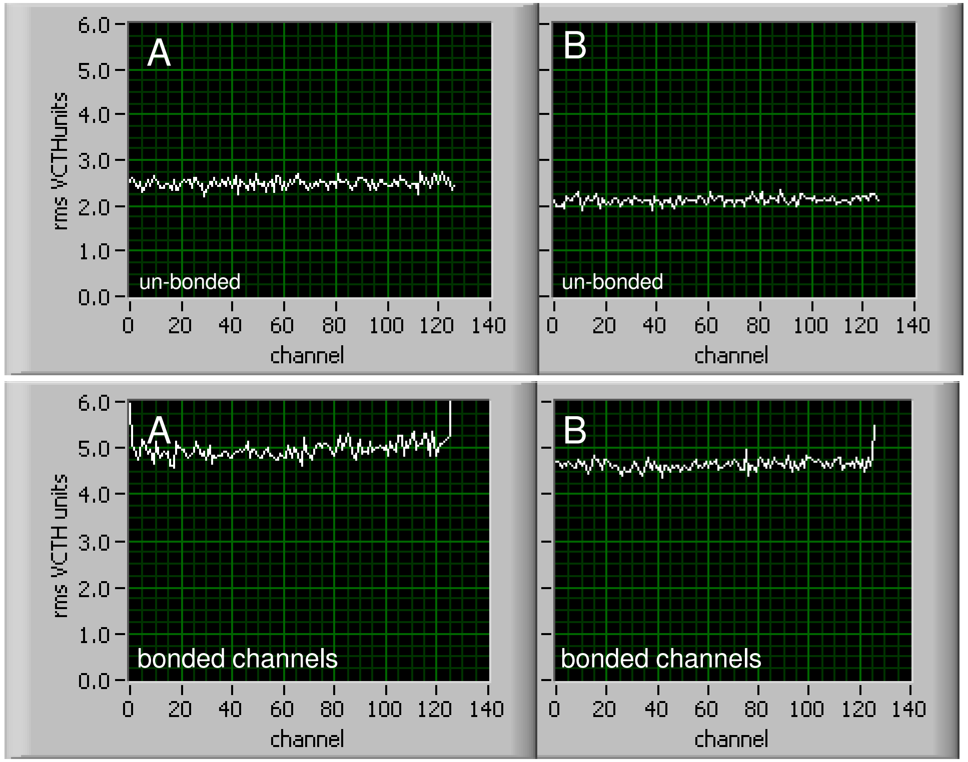
pedestal shift varies across chip - same shape for both chips

s-curve mid-points



noise

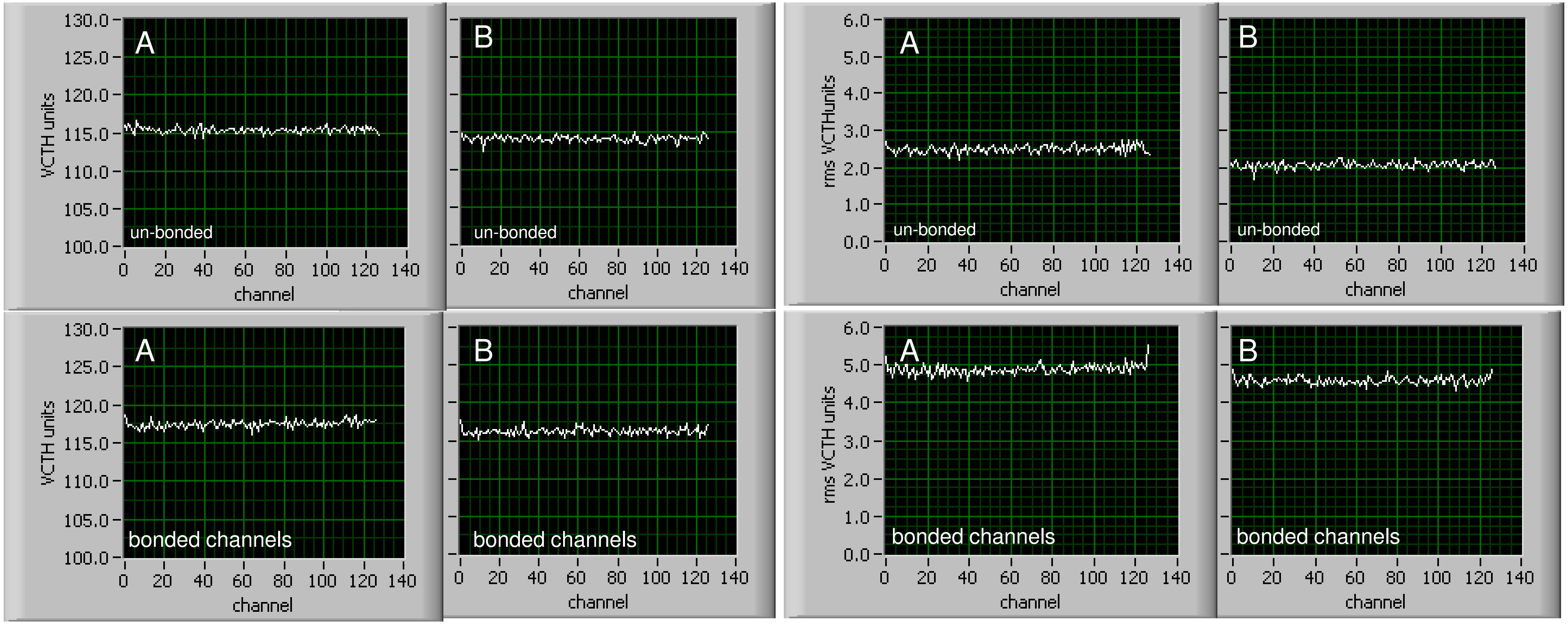
15



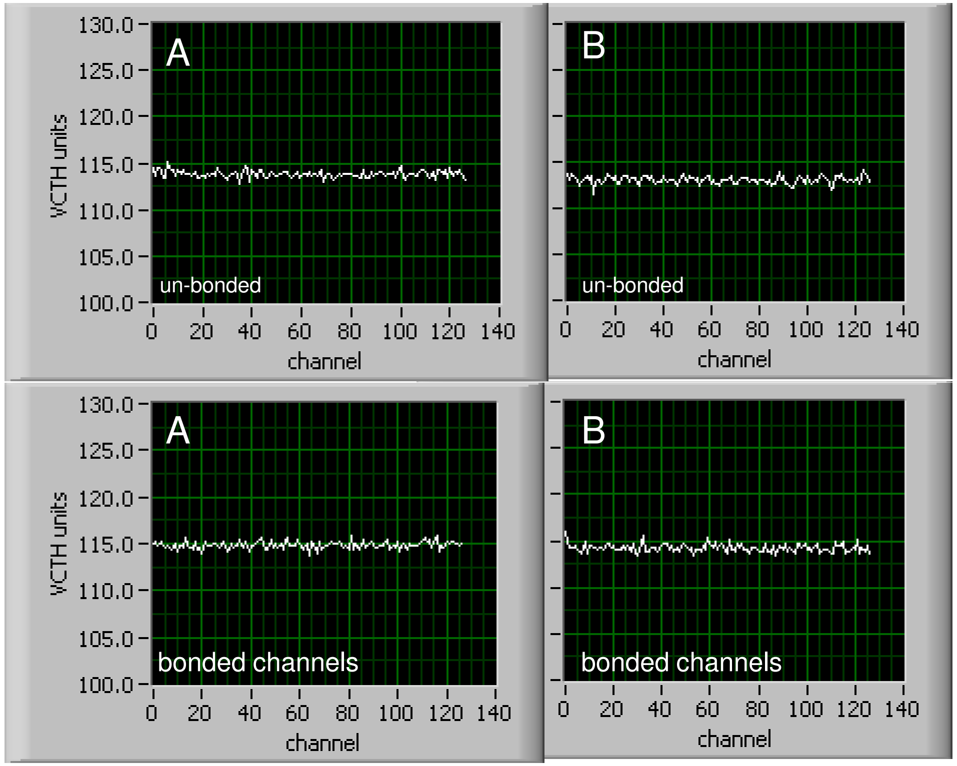
s-curve mid-points

noise

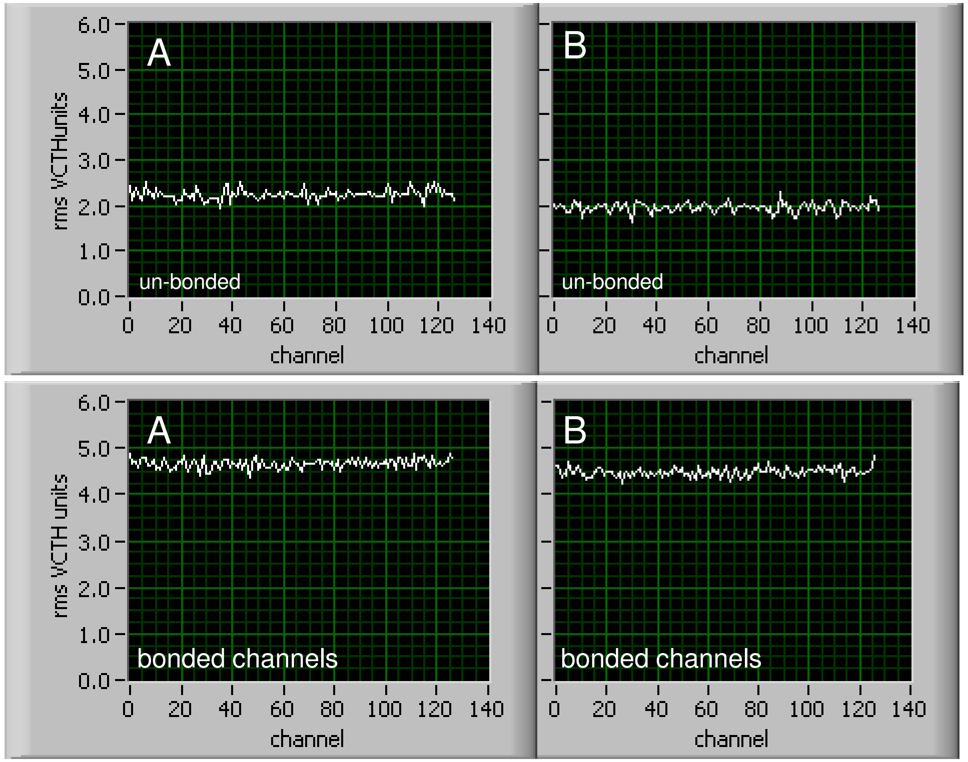
16



s-curve mid-points

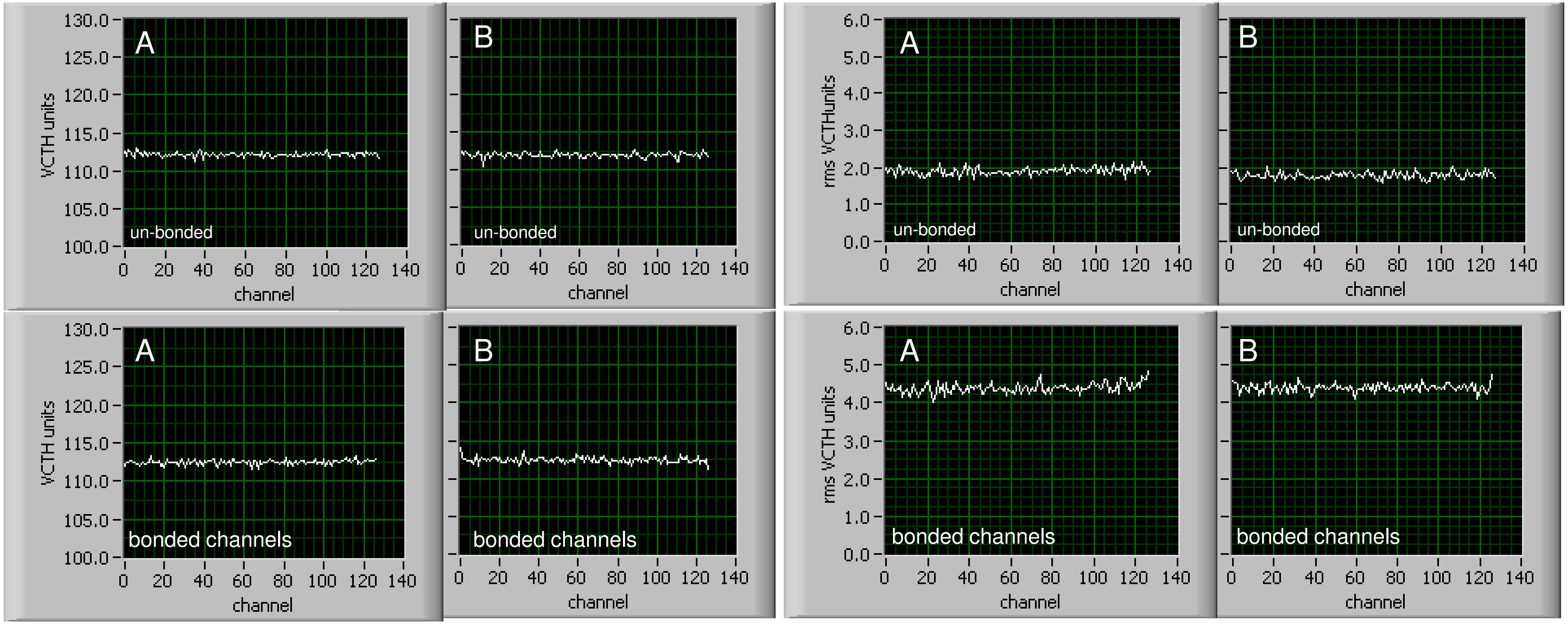


noise

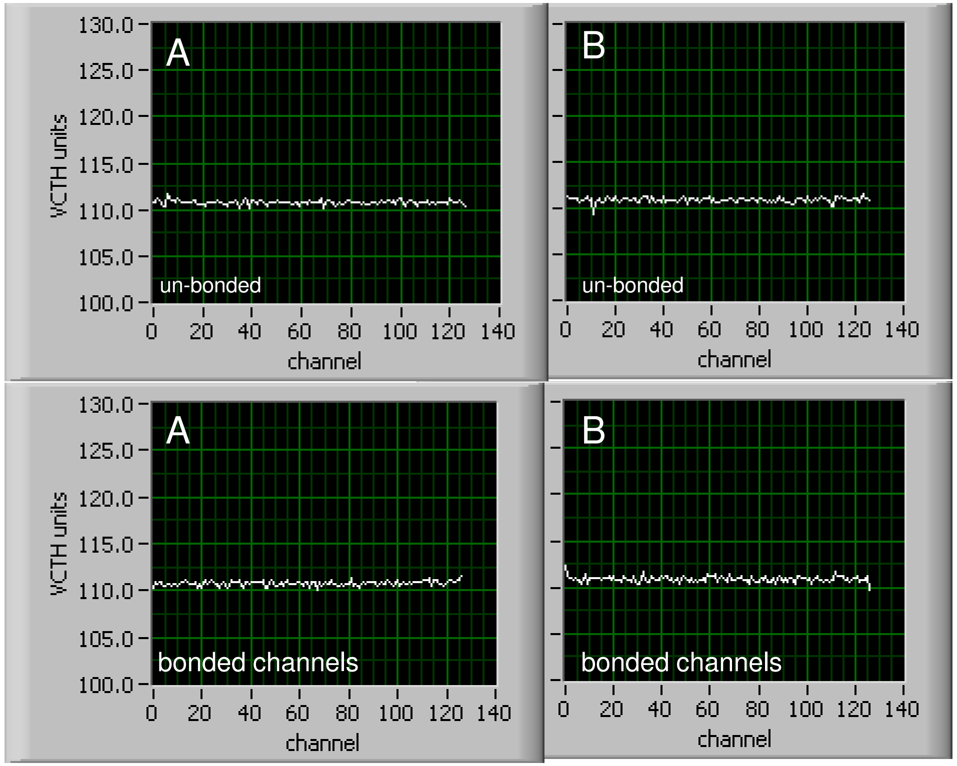


17

s-curve mid-points noise 18

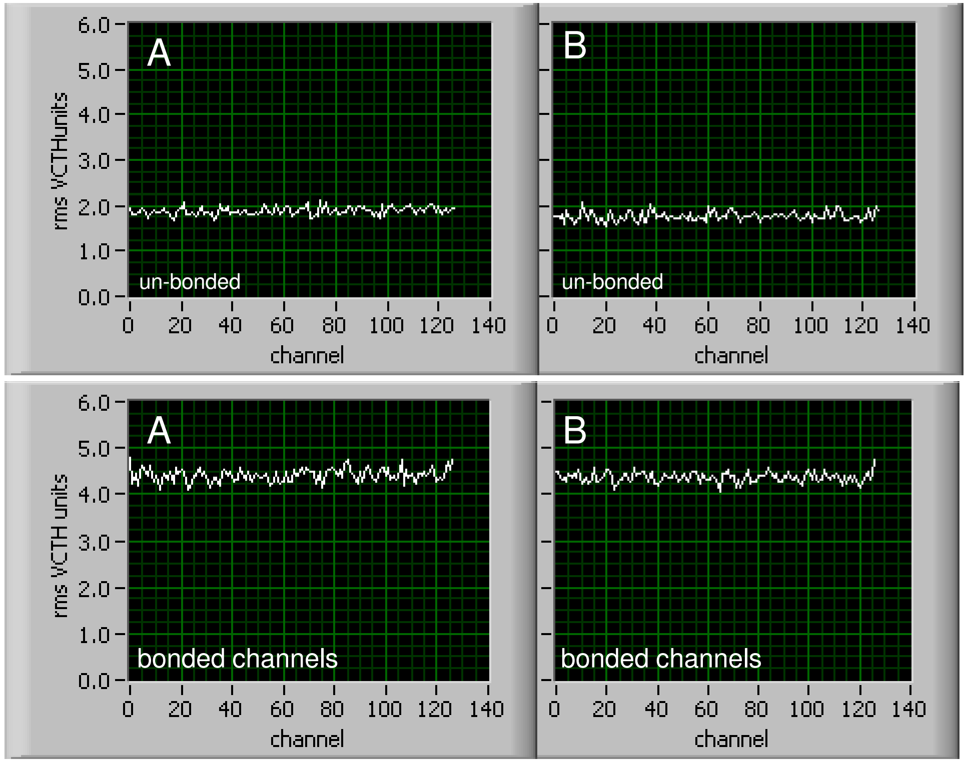


s-curve mid-points



noise

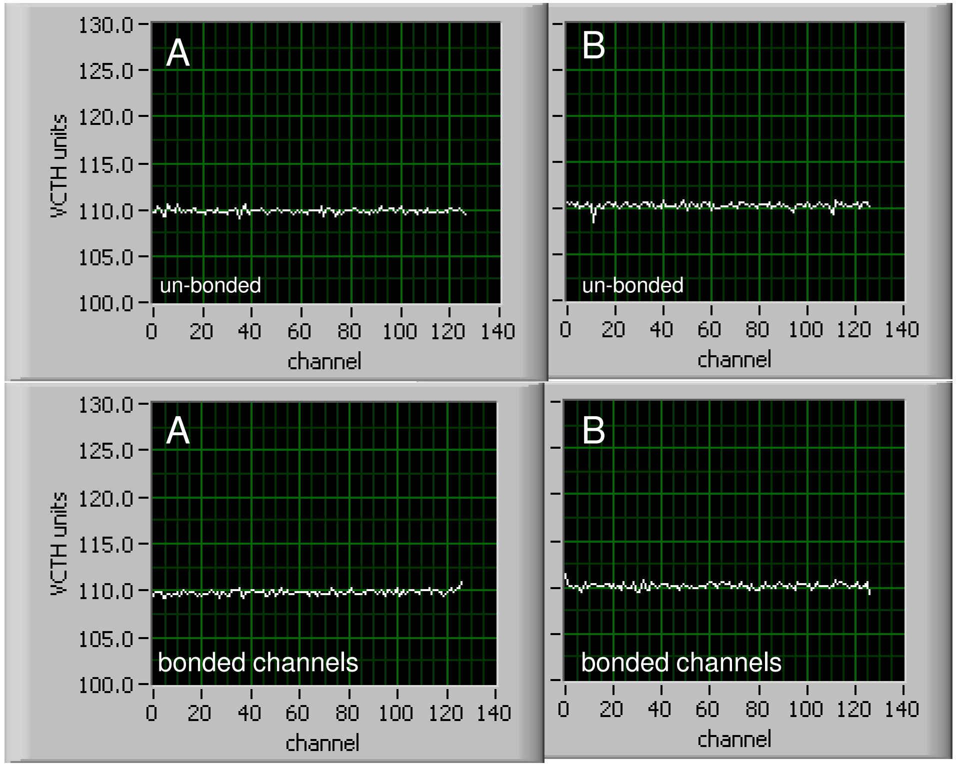
19

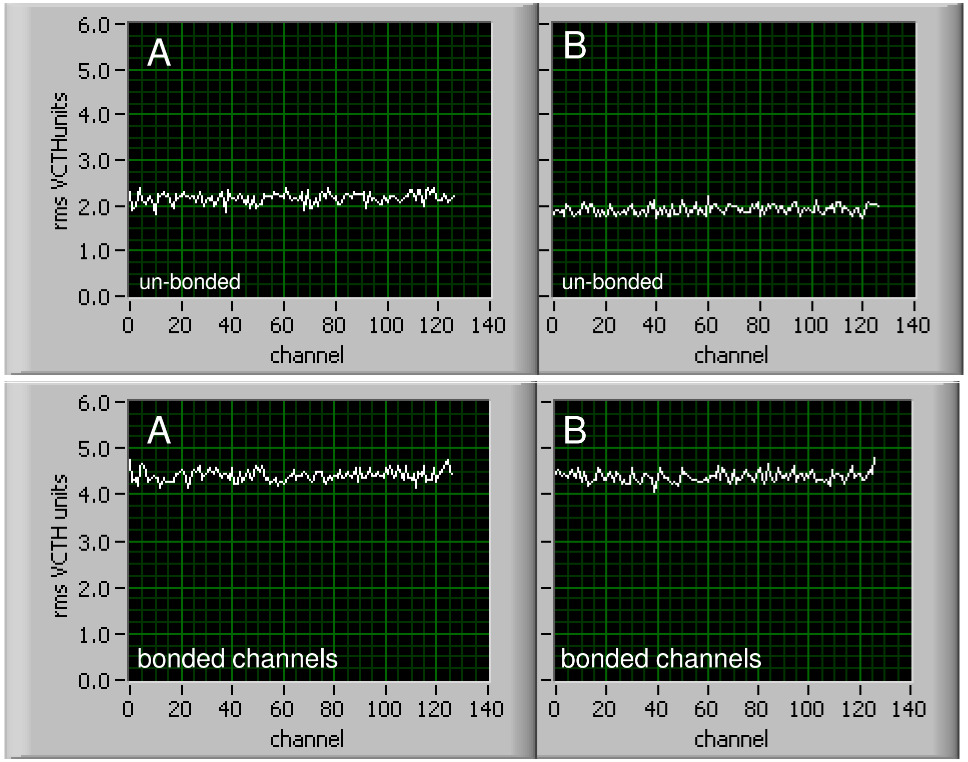


s-curve mid-points

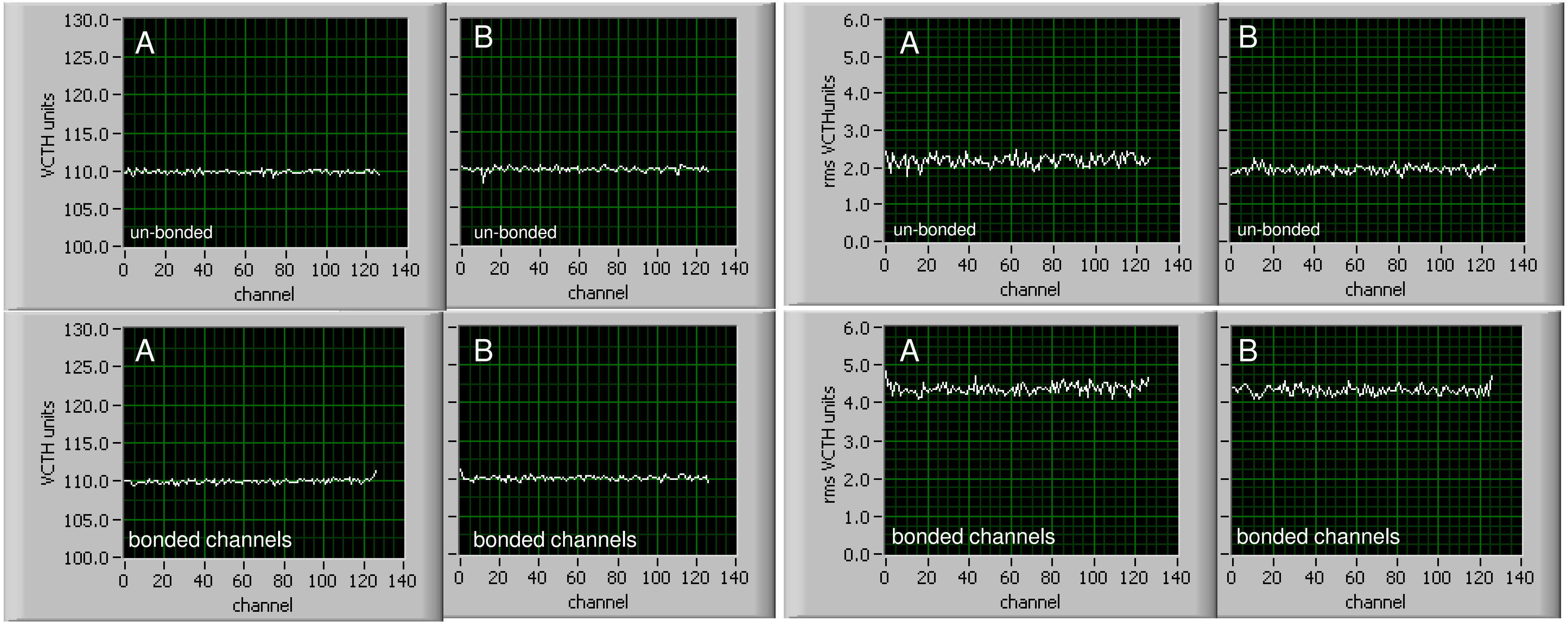
noise

20

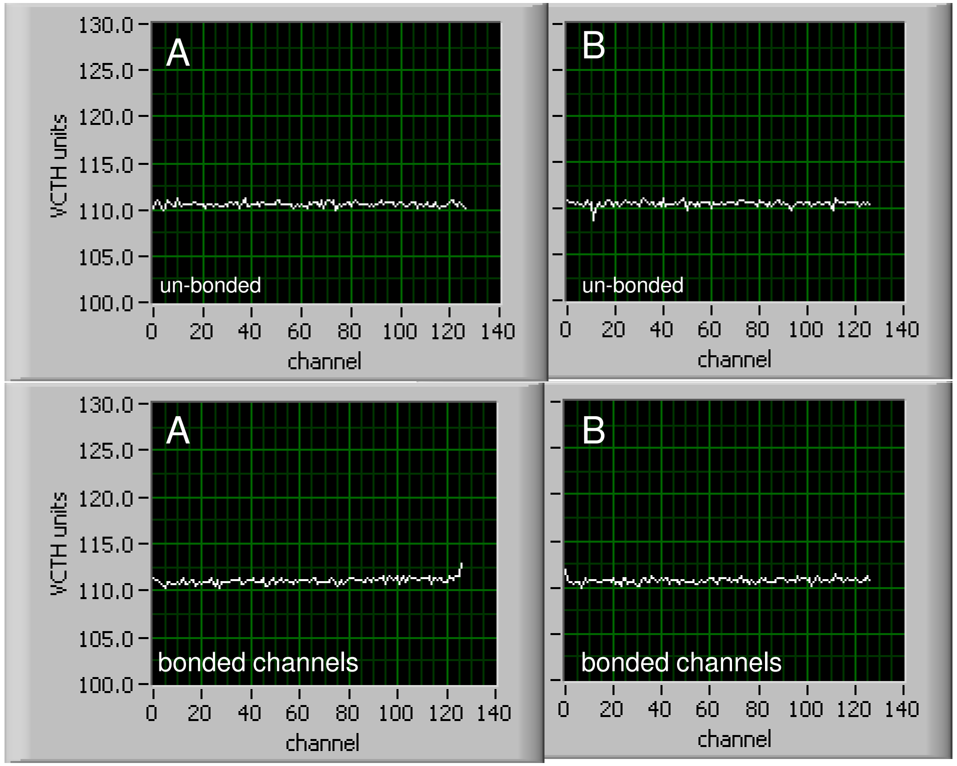




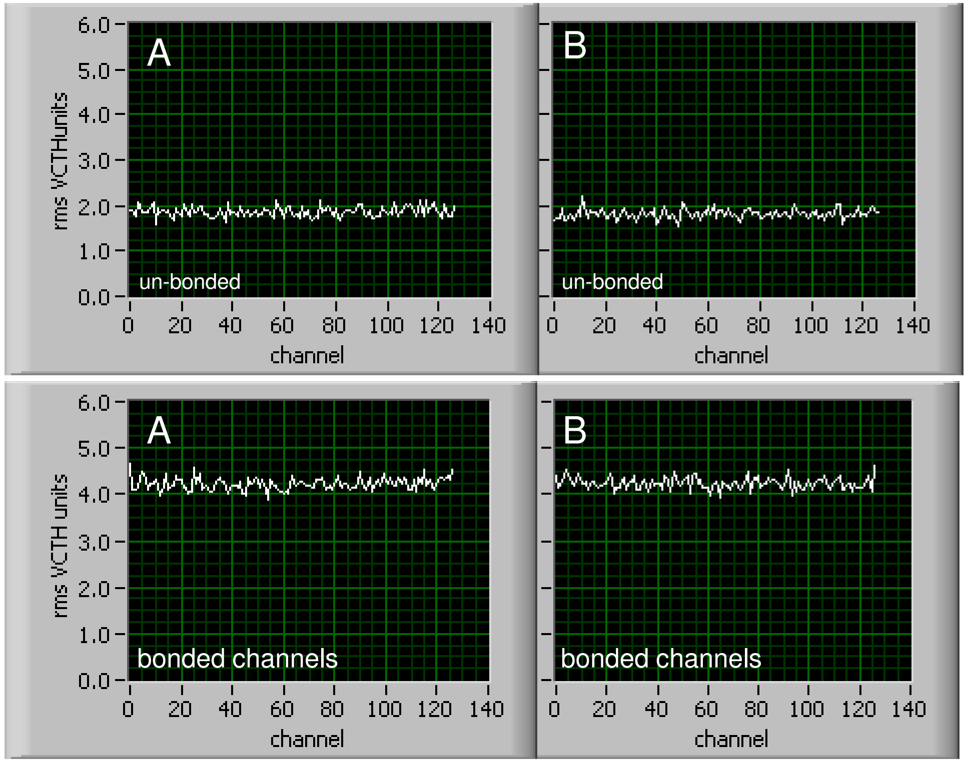
s-curve mid-points   noise   21



s-curve mid-points

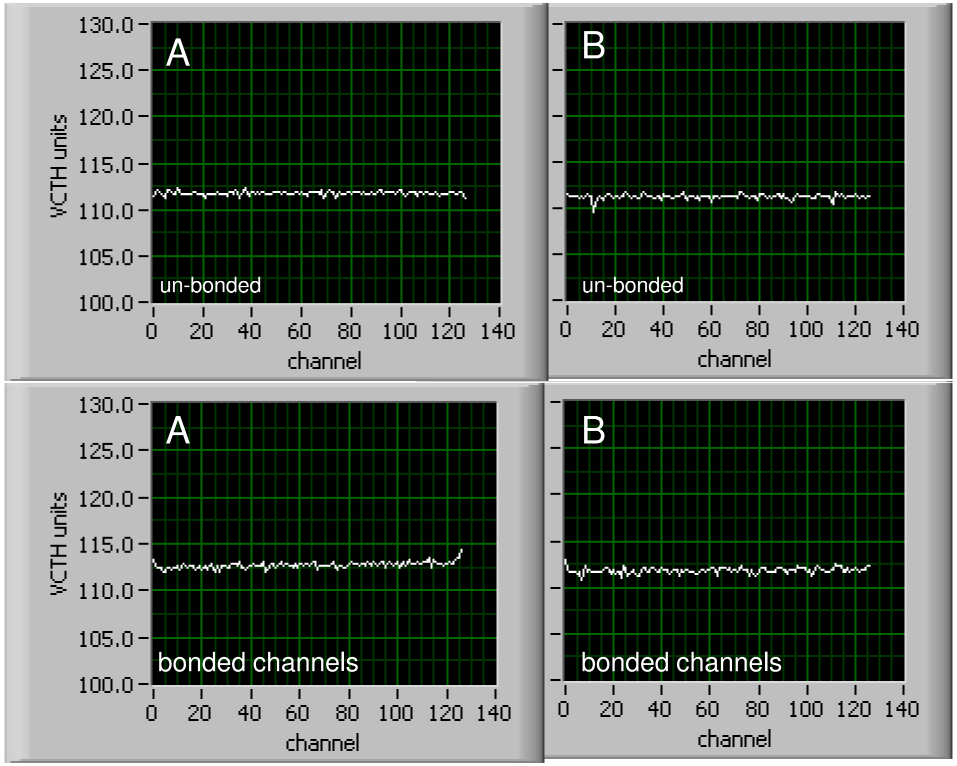


noise



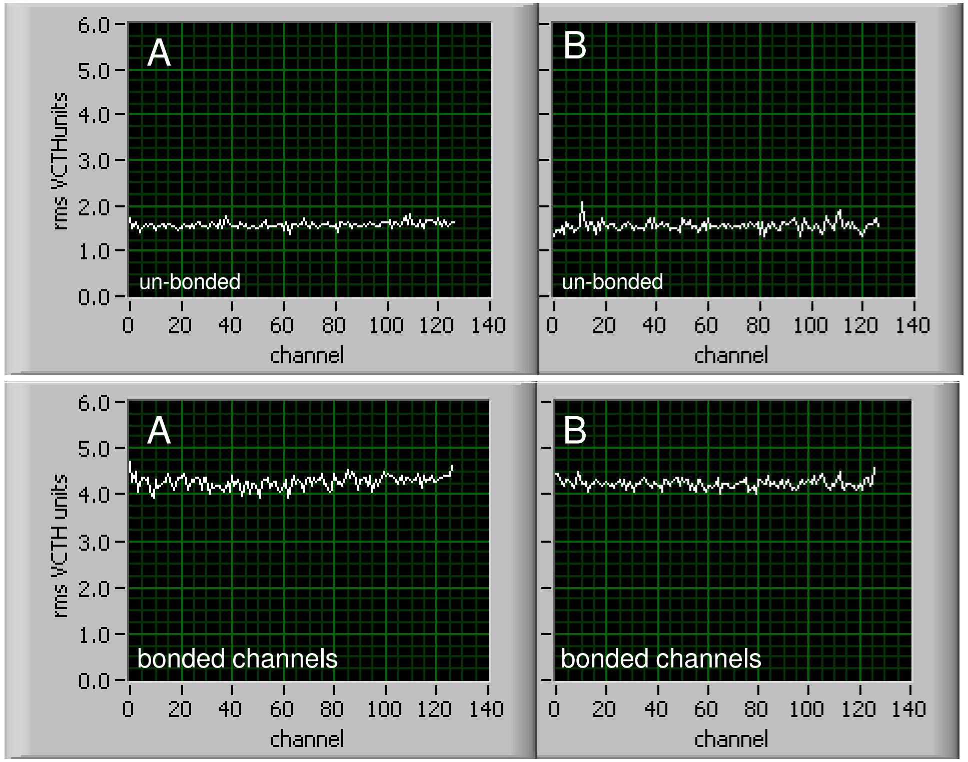
22

s-curve mid-points



noise

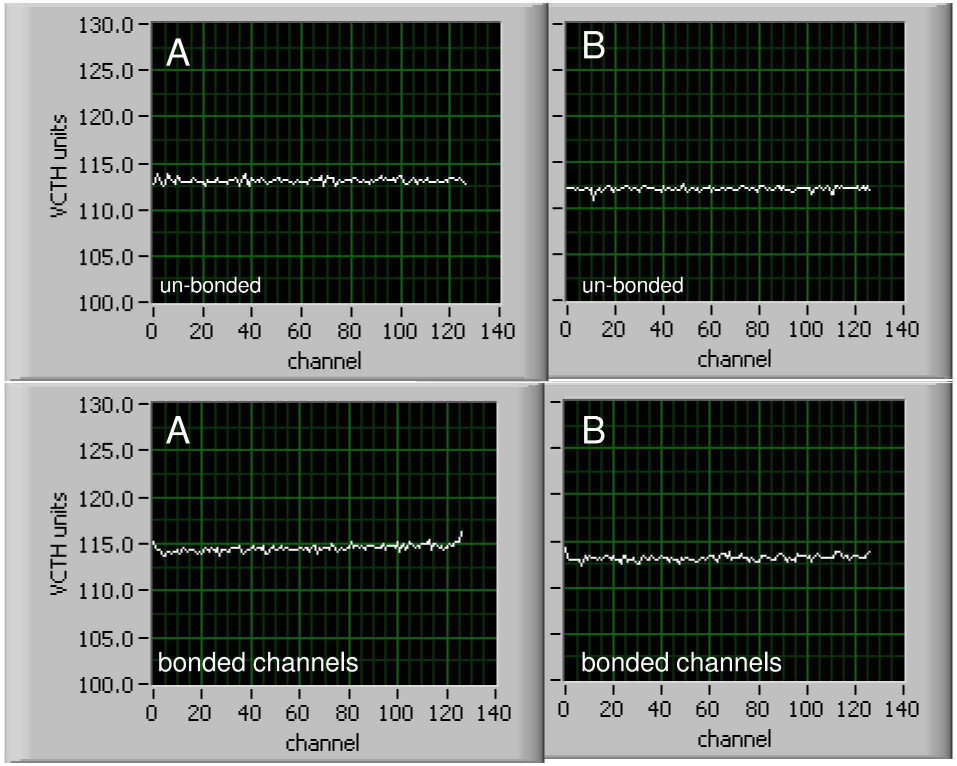
23

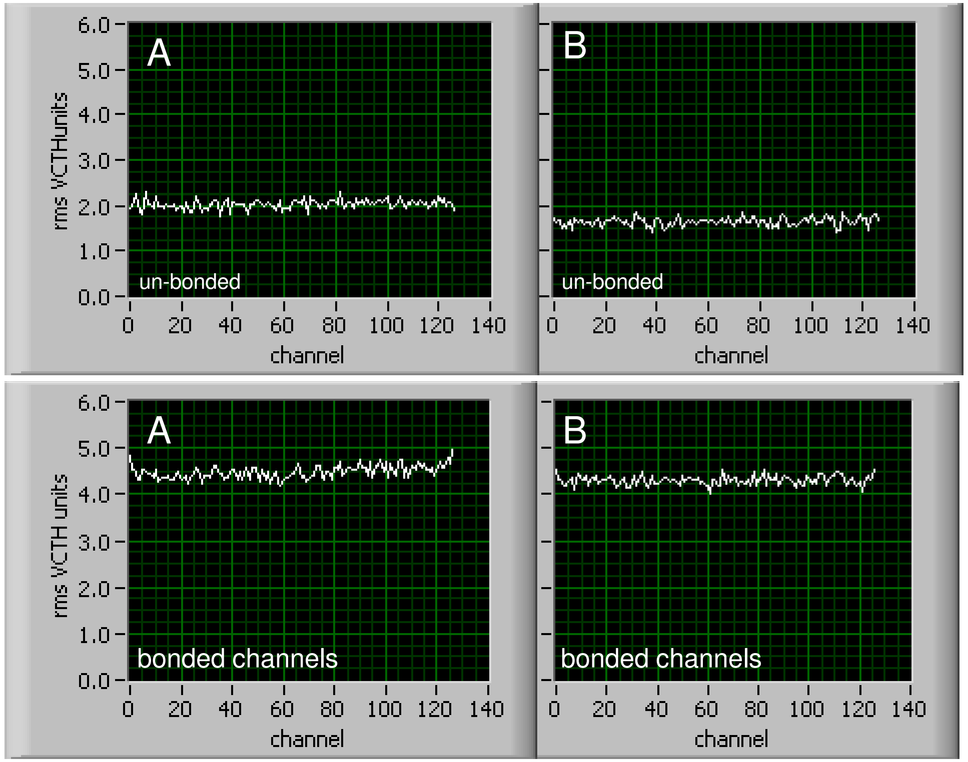


s-curve mid-points

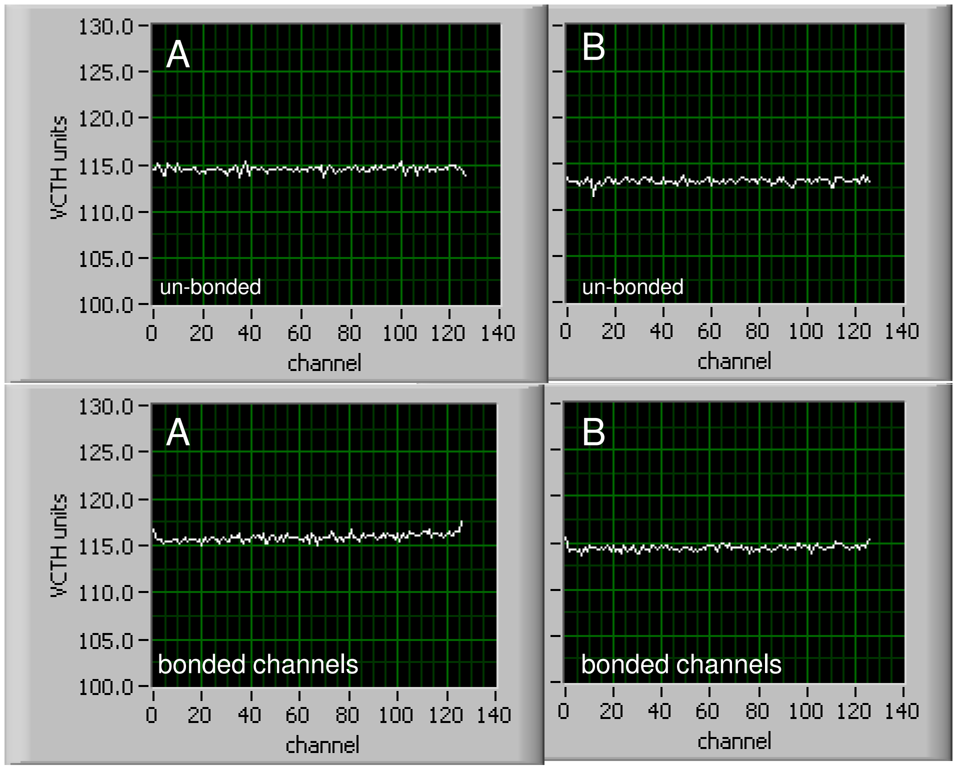
noise

24





s-curve mid-points



noise

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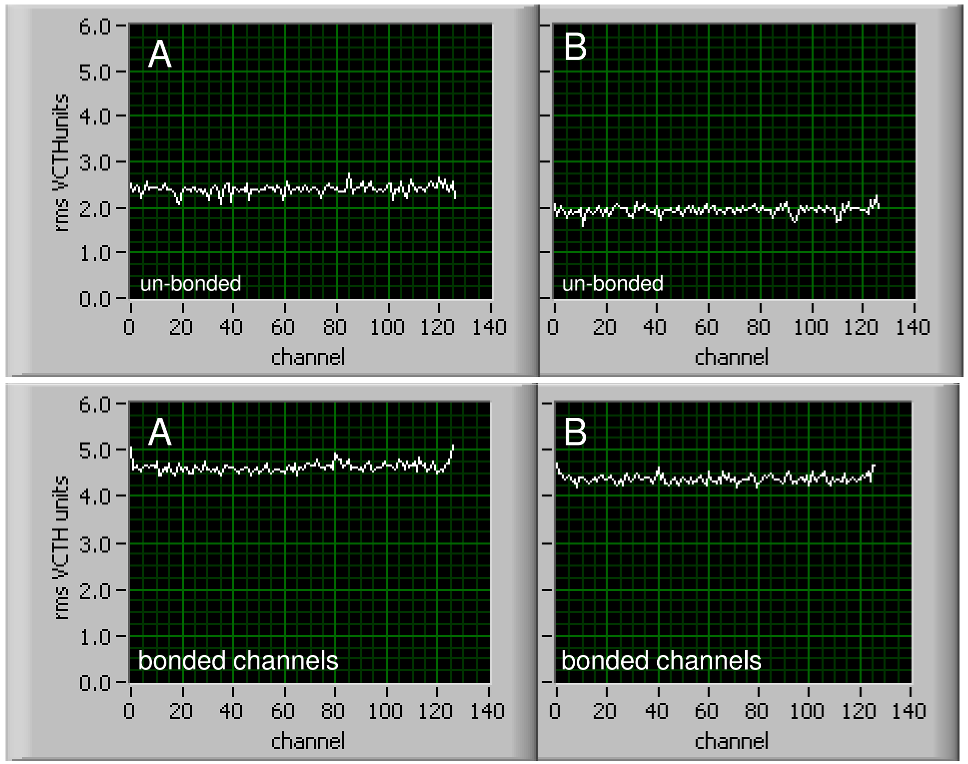
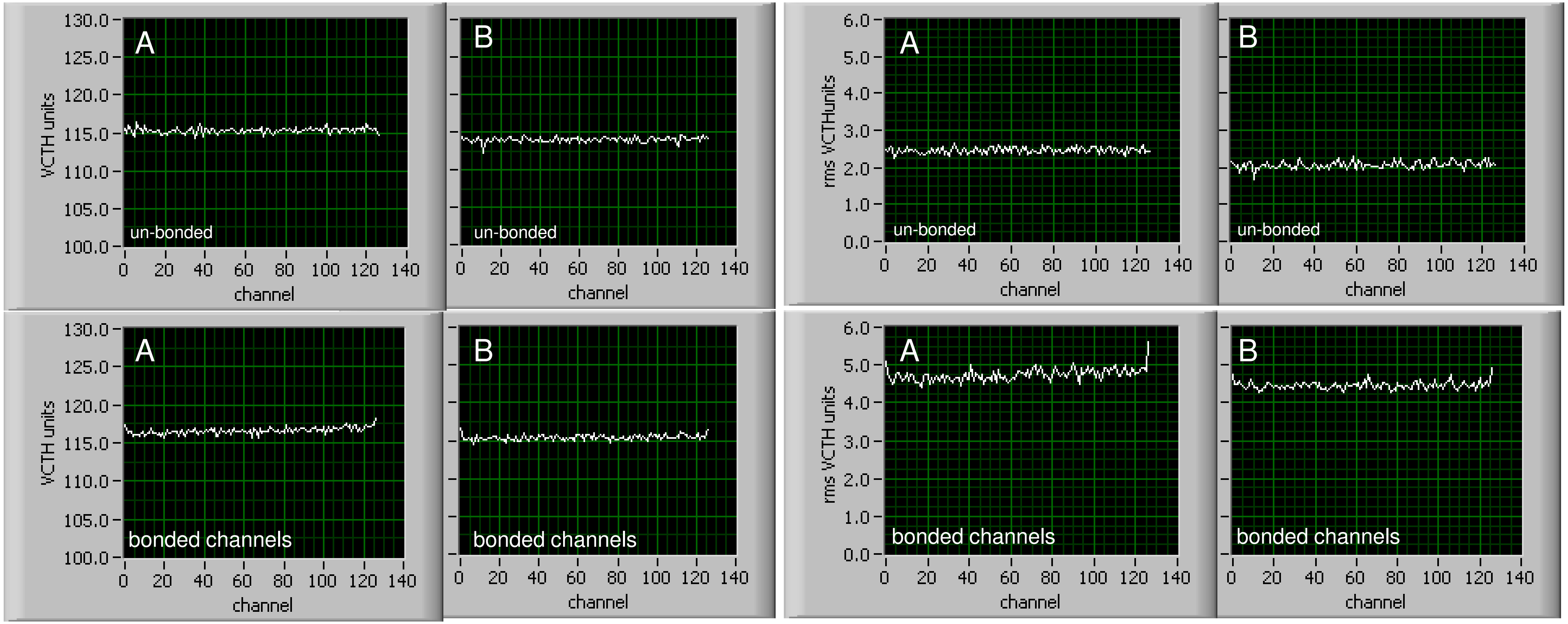
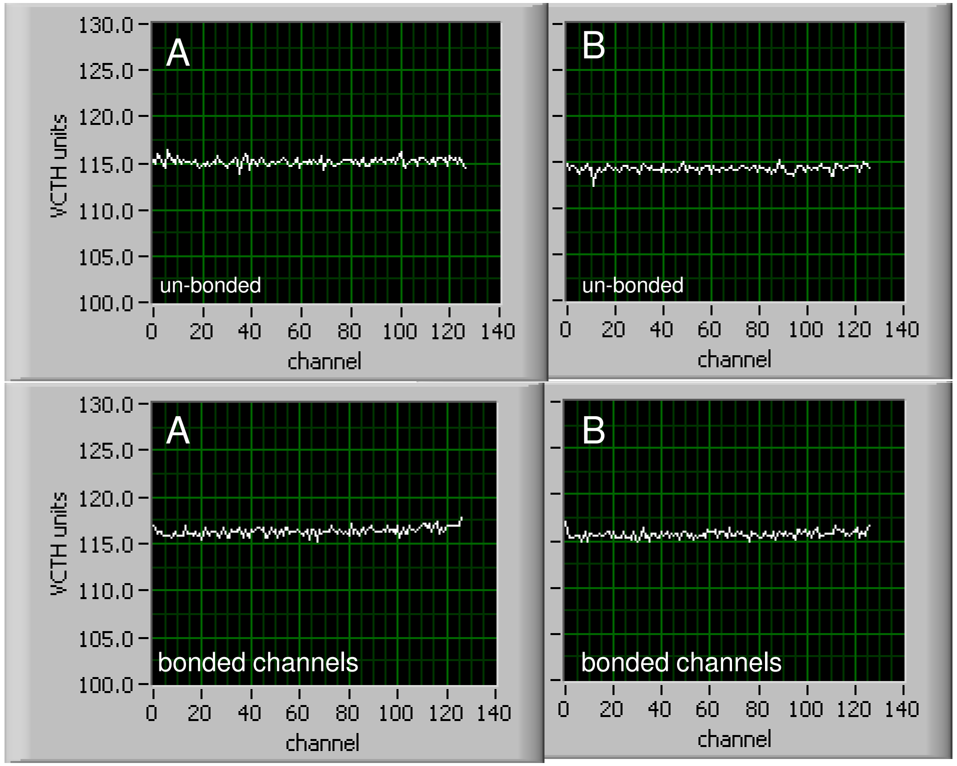


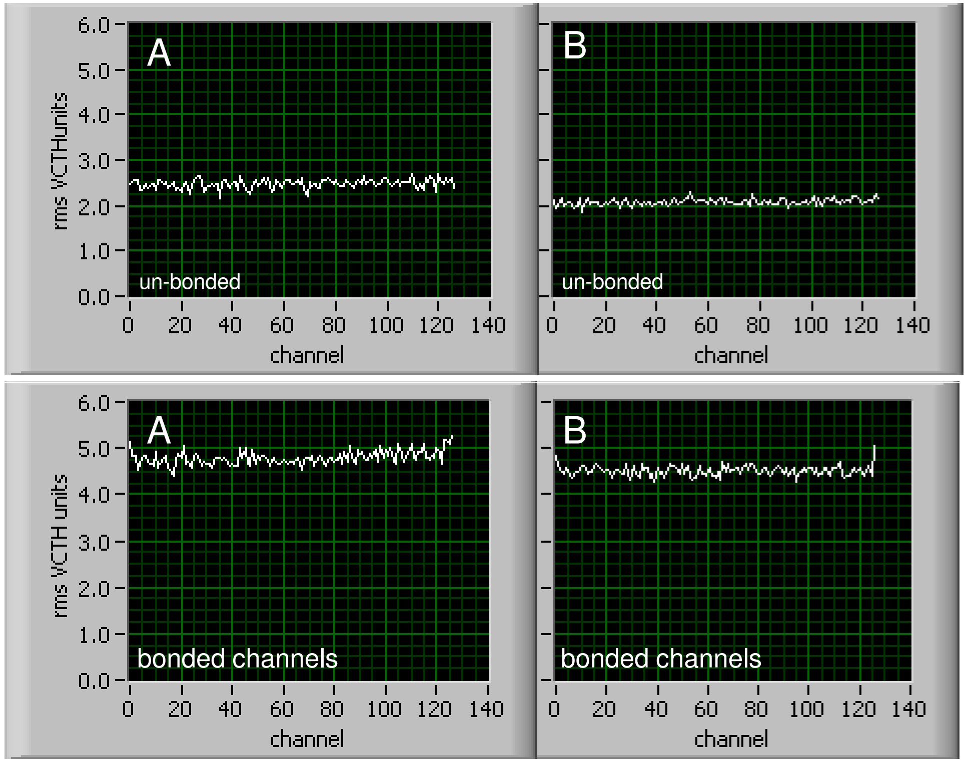
s-curve mid-points noise



s-curve mid-points



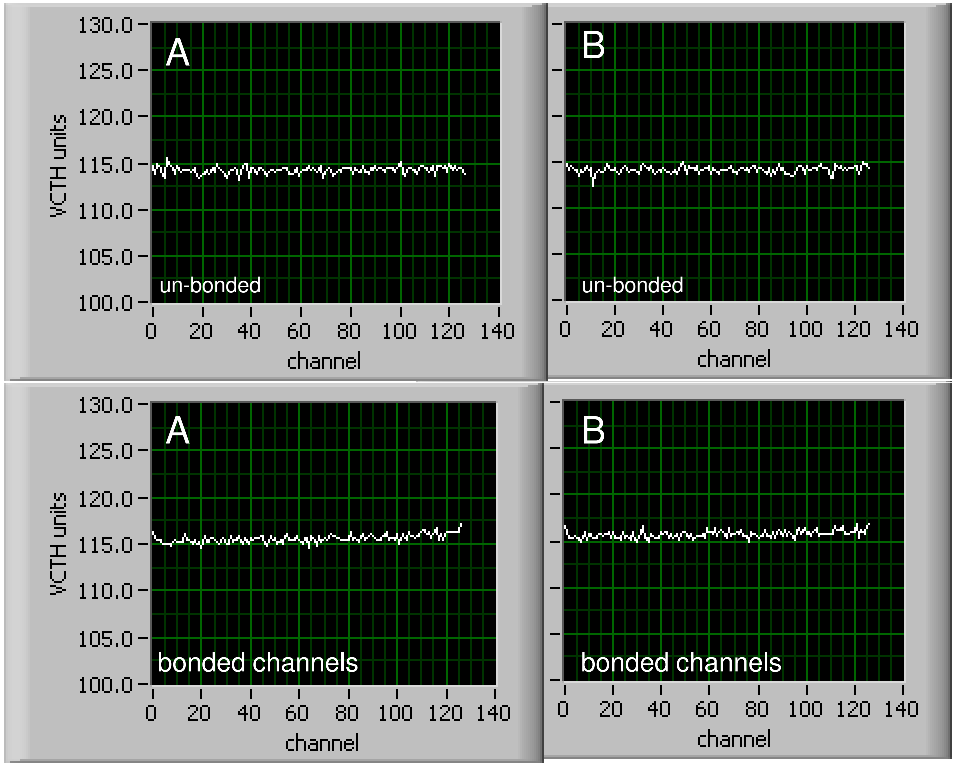
noise

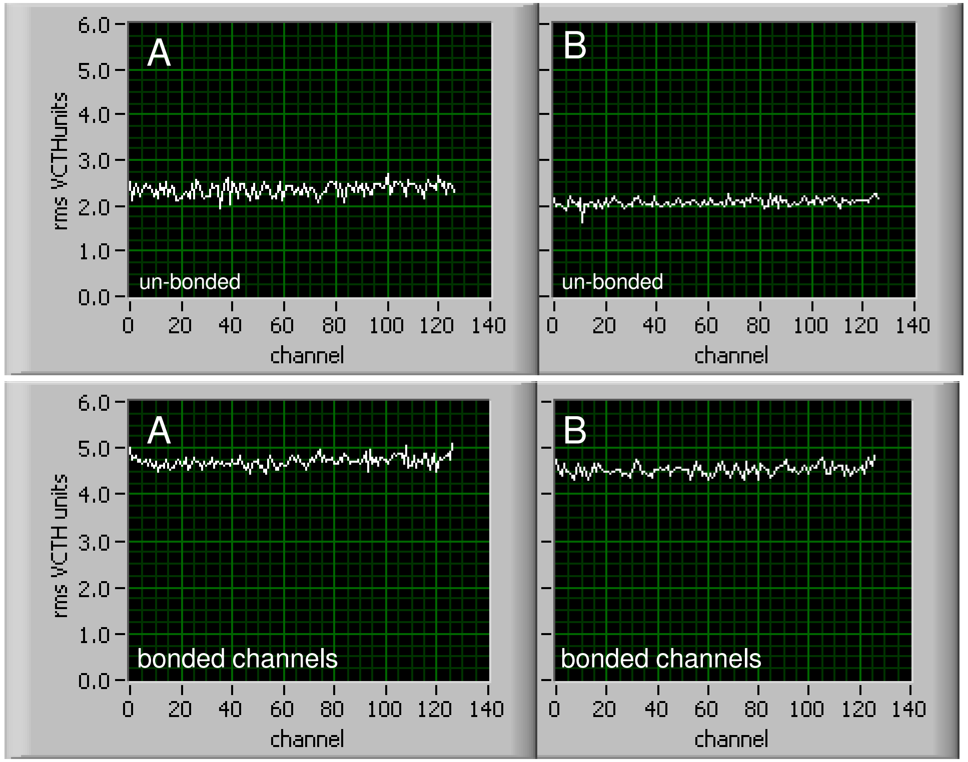


s-curve mid-points

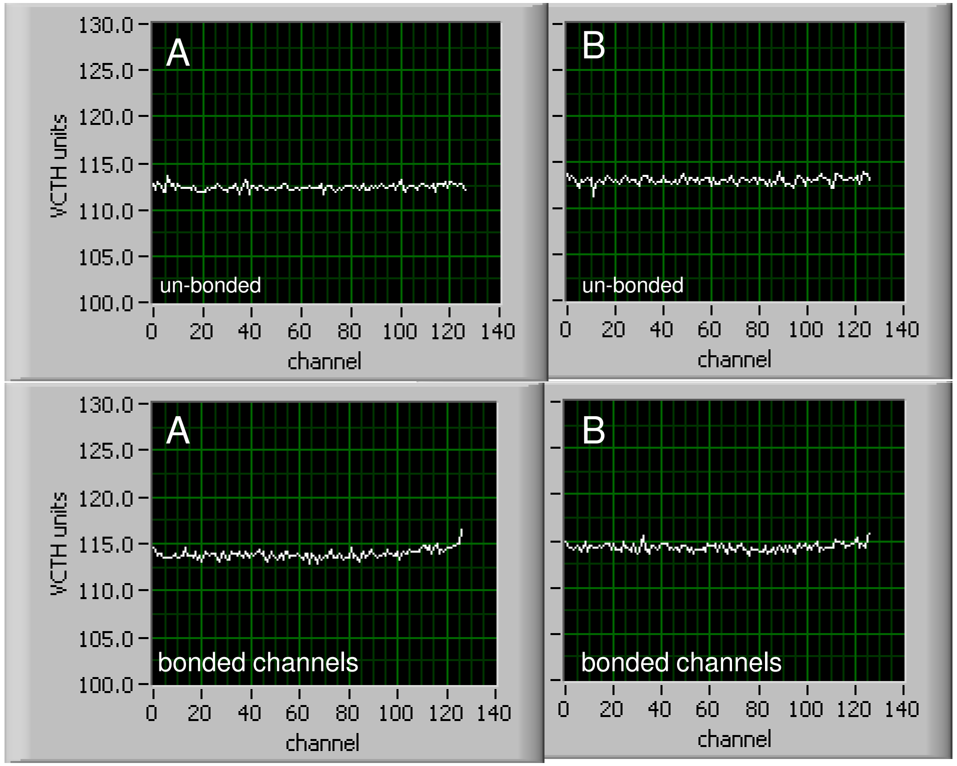
noise

28



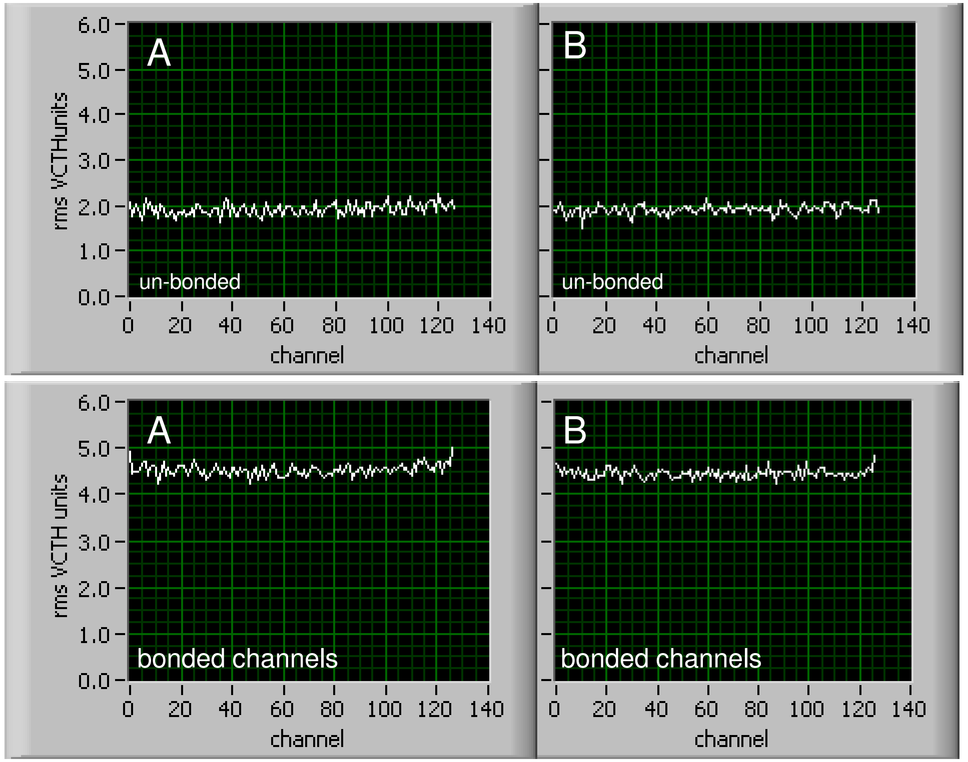


s-curve mid-points

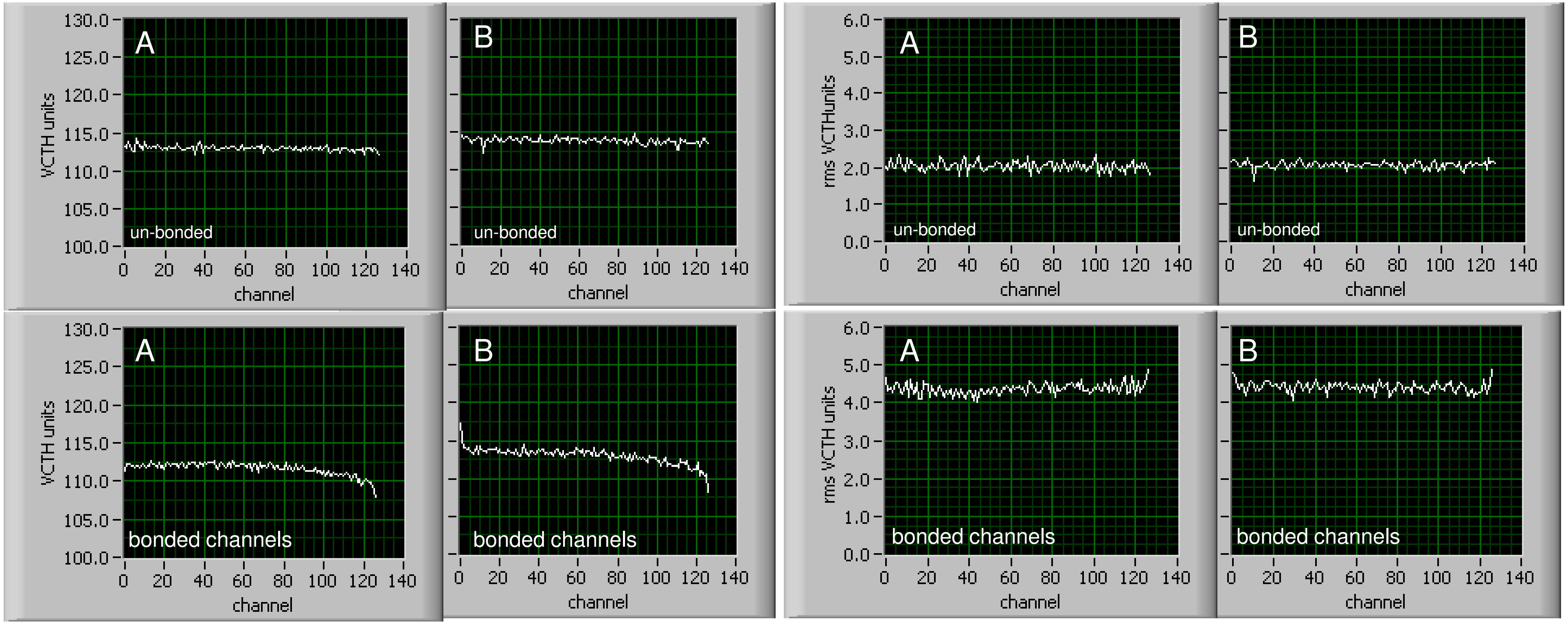


noise

29

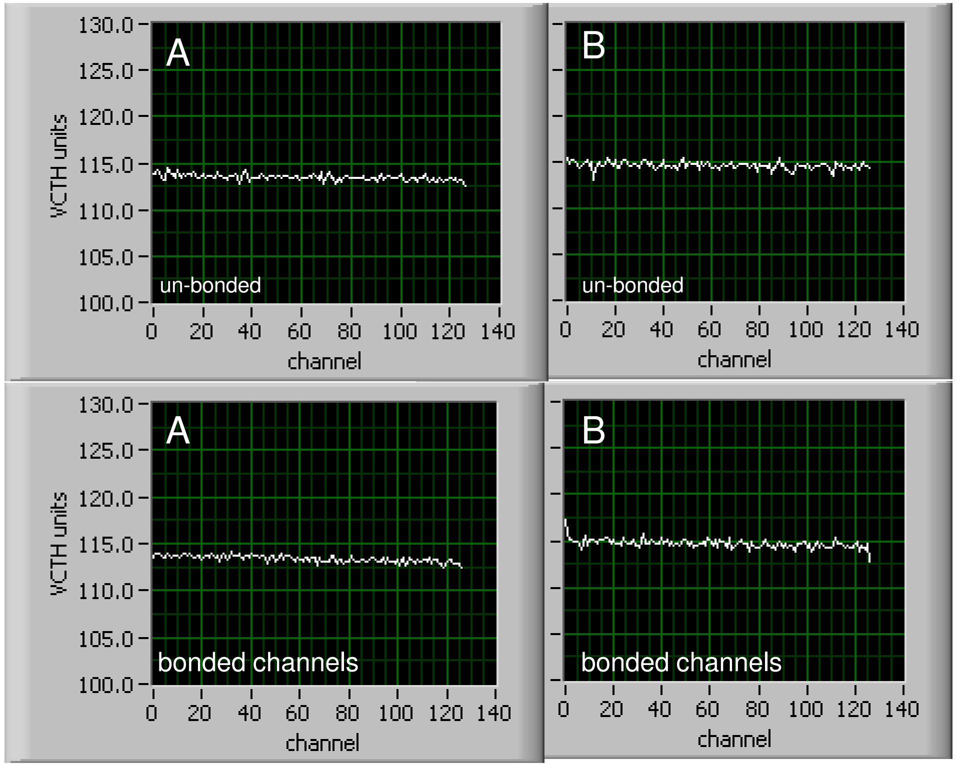


* s-curve mid-points noise 30



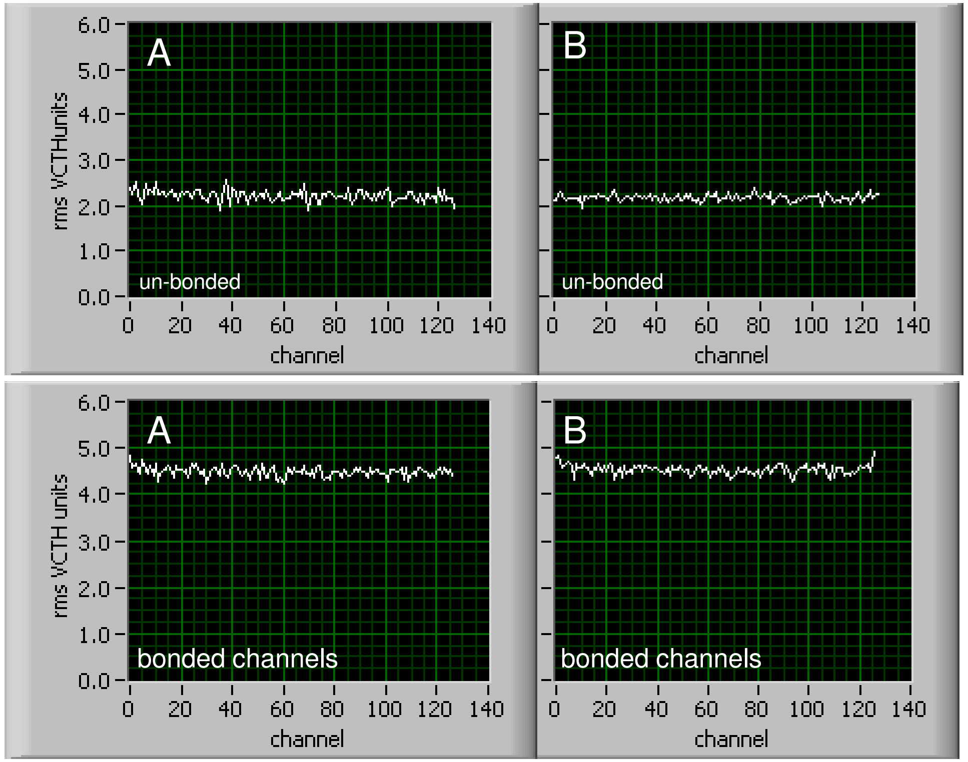
pedestal shift varies across chip - same shape for both chips
same shape as step 10 (500 nsec previous)

s-curve mid-points

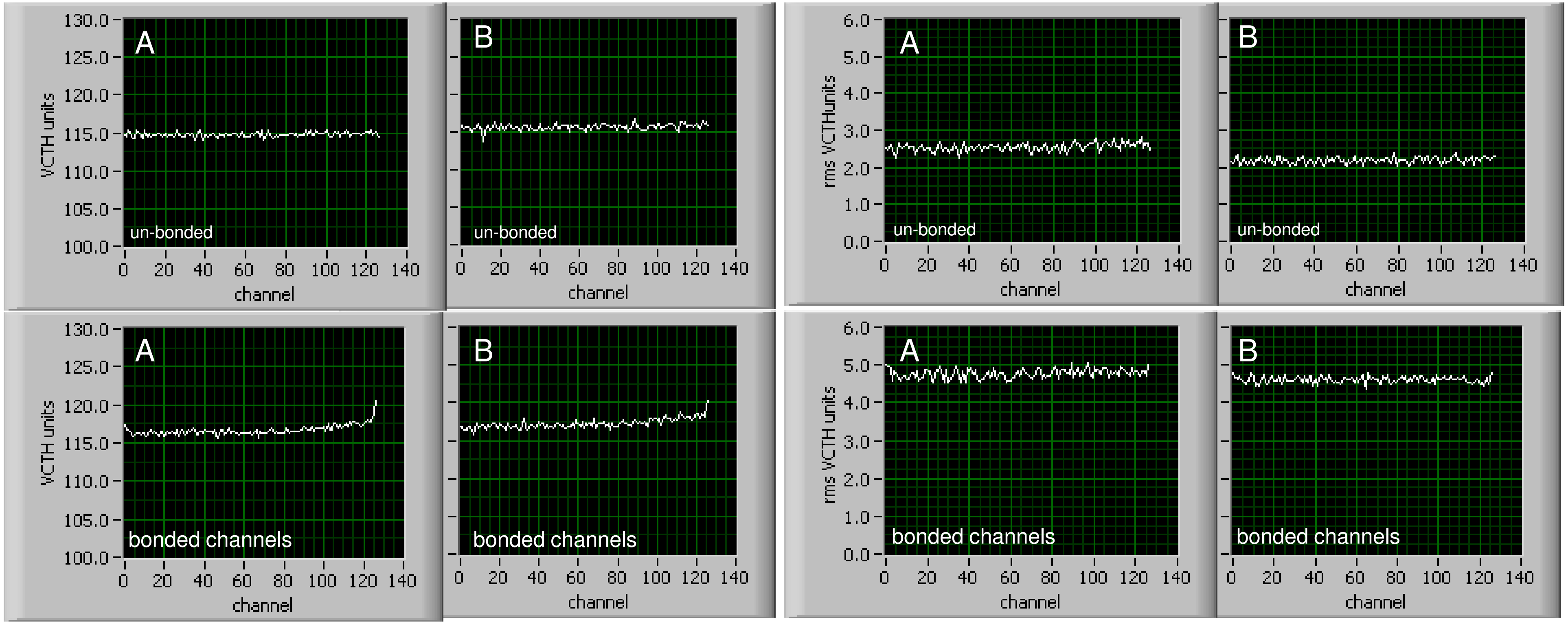


noise

31

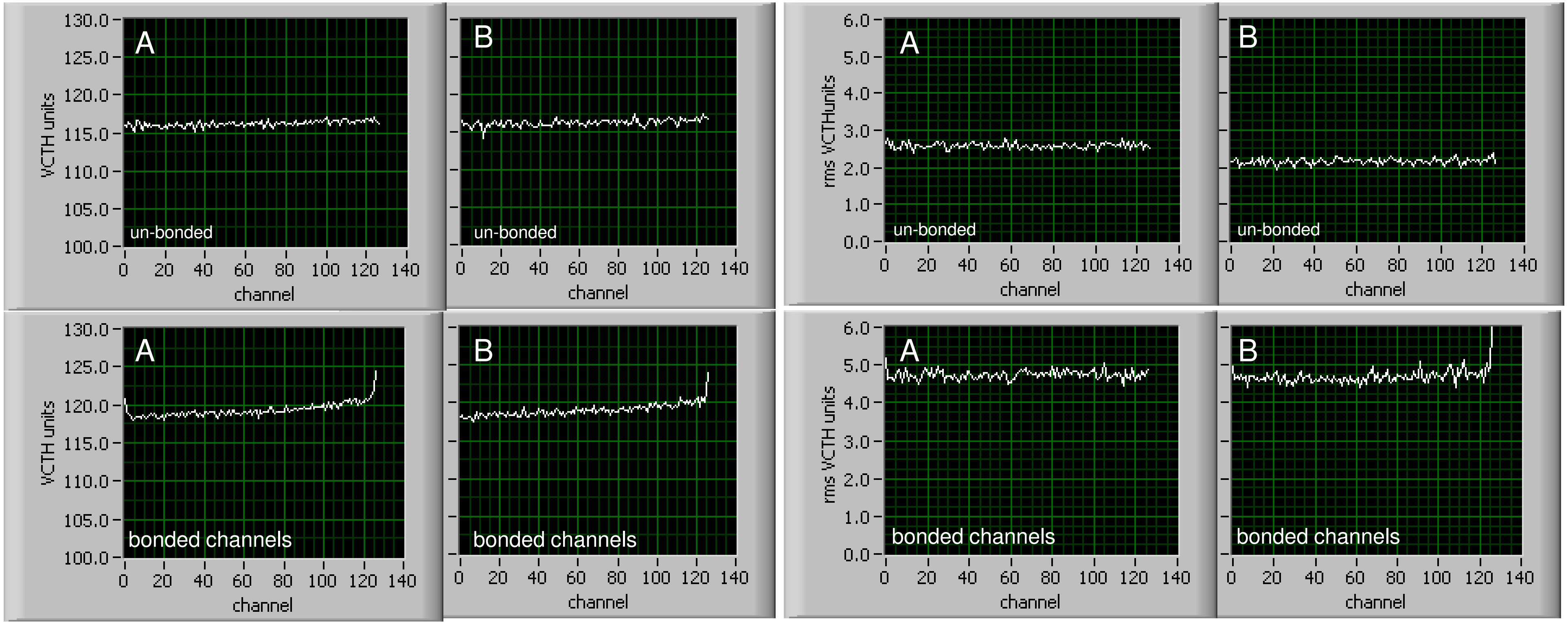


* s-curve mid-points noise 32



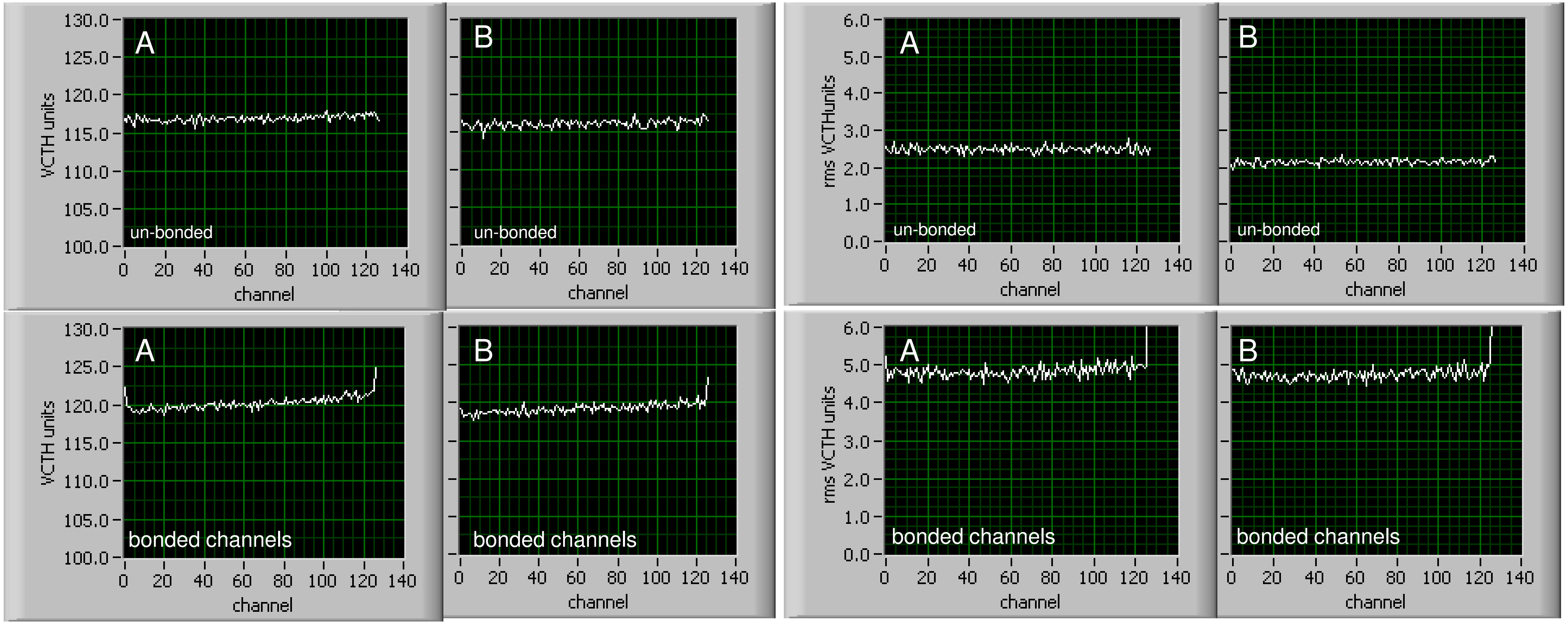
pedestal shift varies across chip - same shape for both chips
same shape as step 12 (500 nsec previous)

* s-curve mid-points noise 33



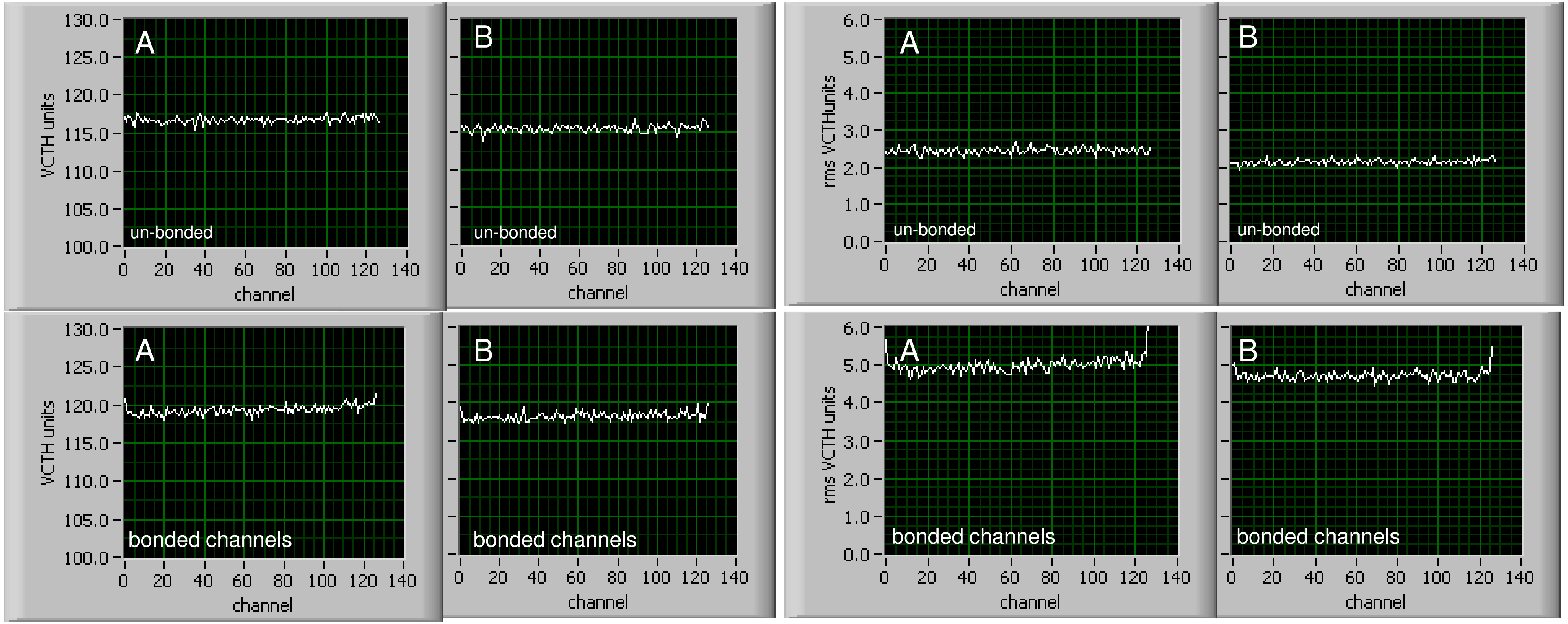
pedestal shift varies across chip - same shape for both chips
same shape as step 13 (500 nsec previous)

* s-curve mid-points noise 34



pedestal shift varies across chip - same shape for both chips
same shape as step 14 (500 nsec previous)

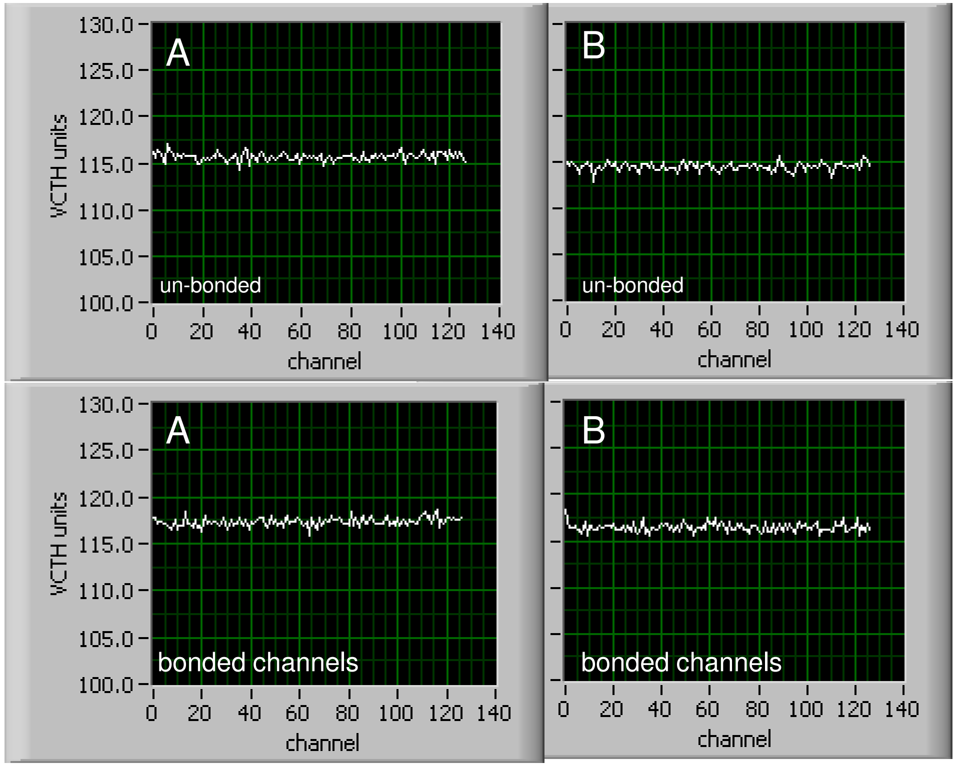
s-curve mid-points   noise   35

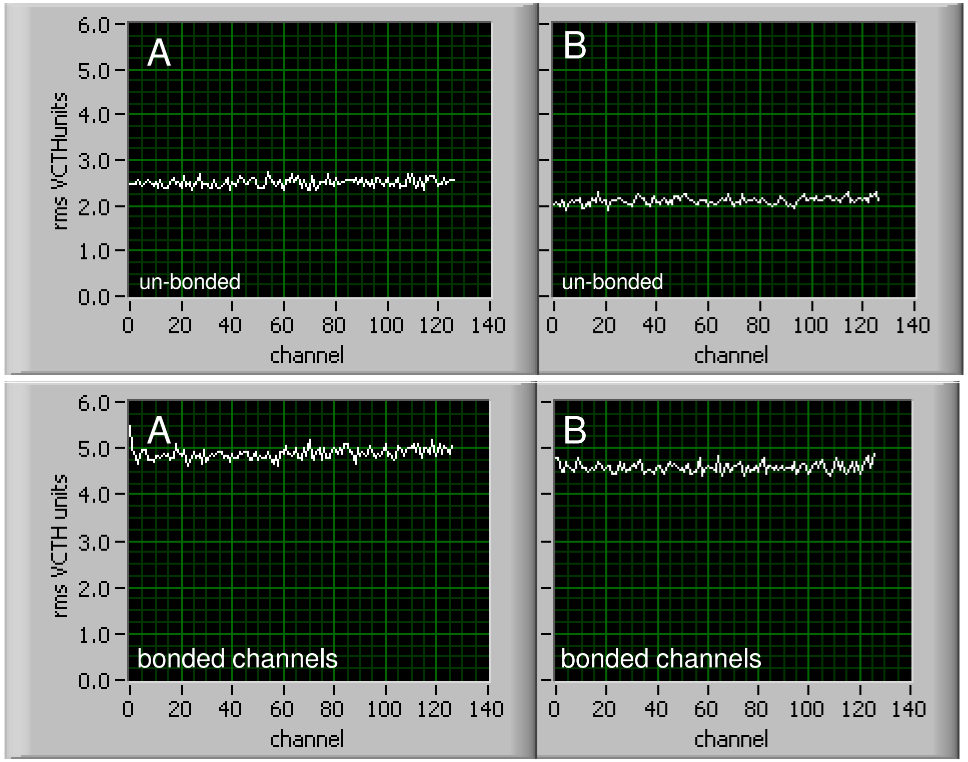


s-curve mid-points

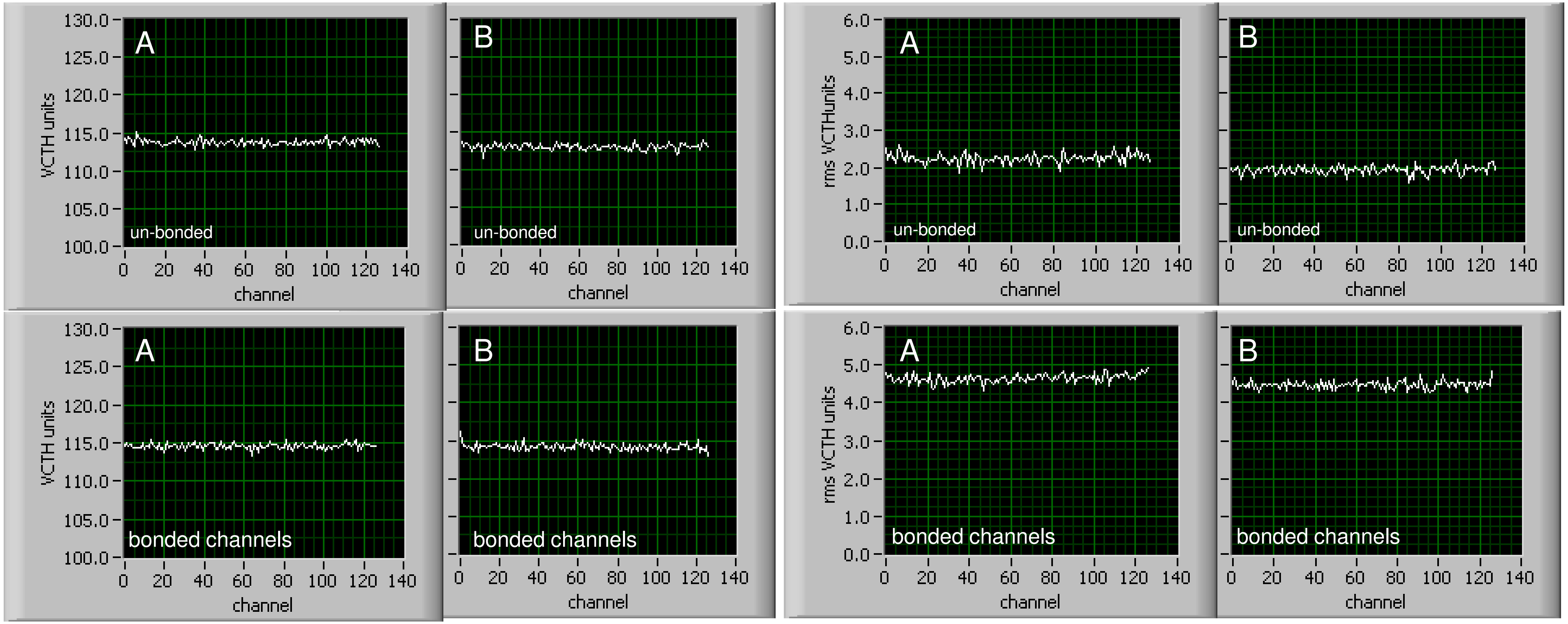
noise

36

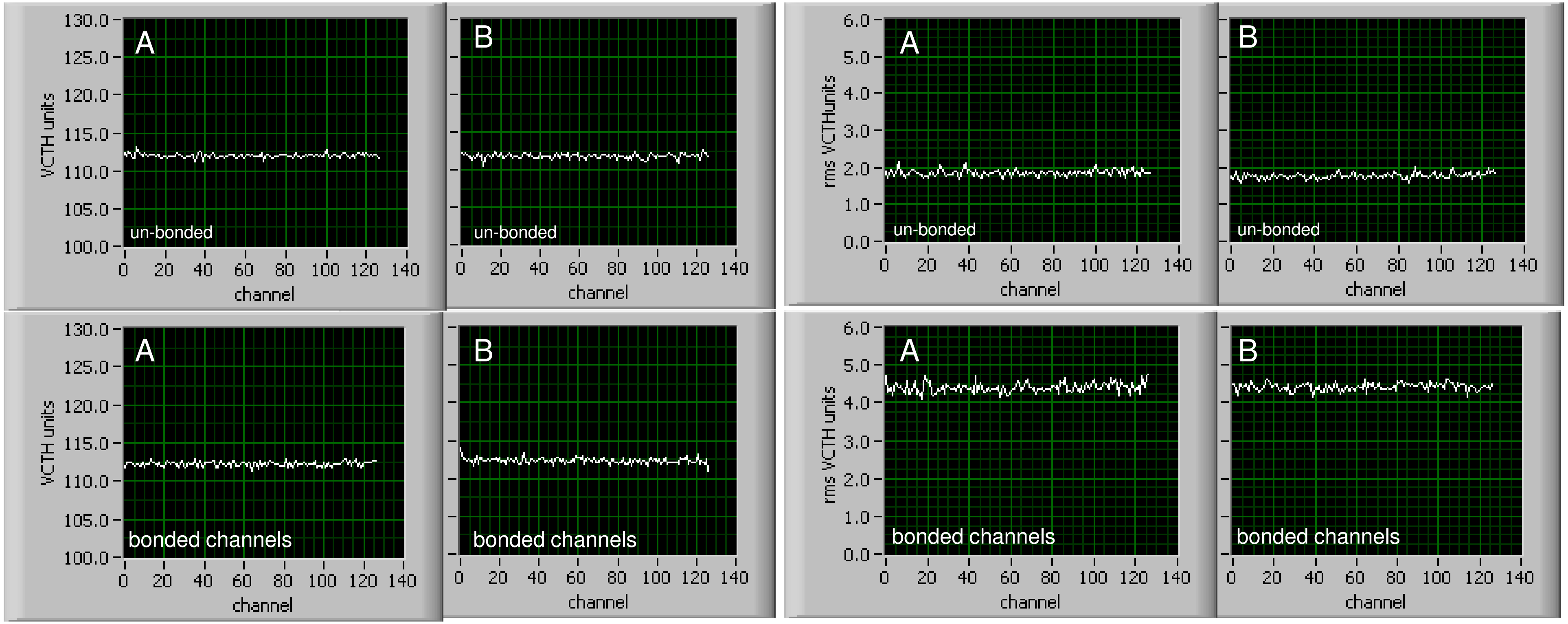




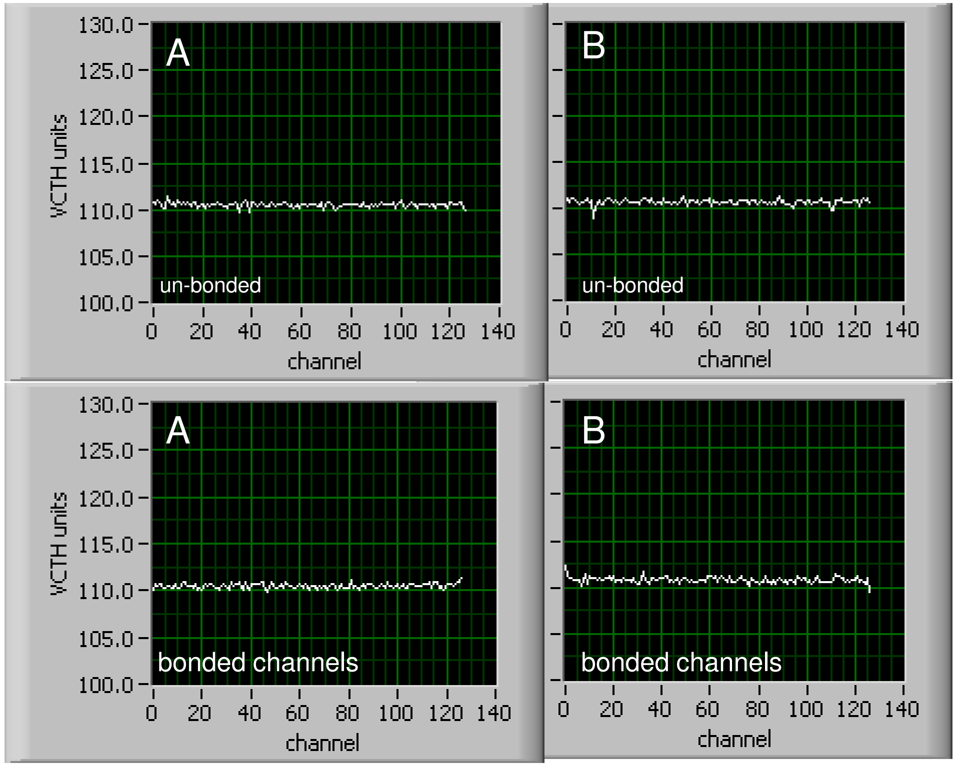
s-curve mid-points noise 37



s-curve mid-points noise 38

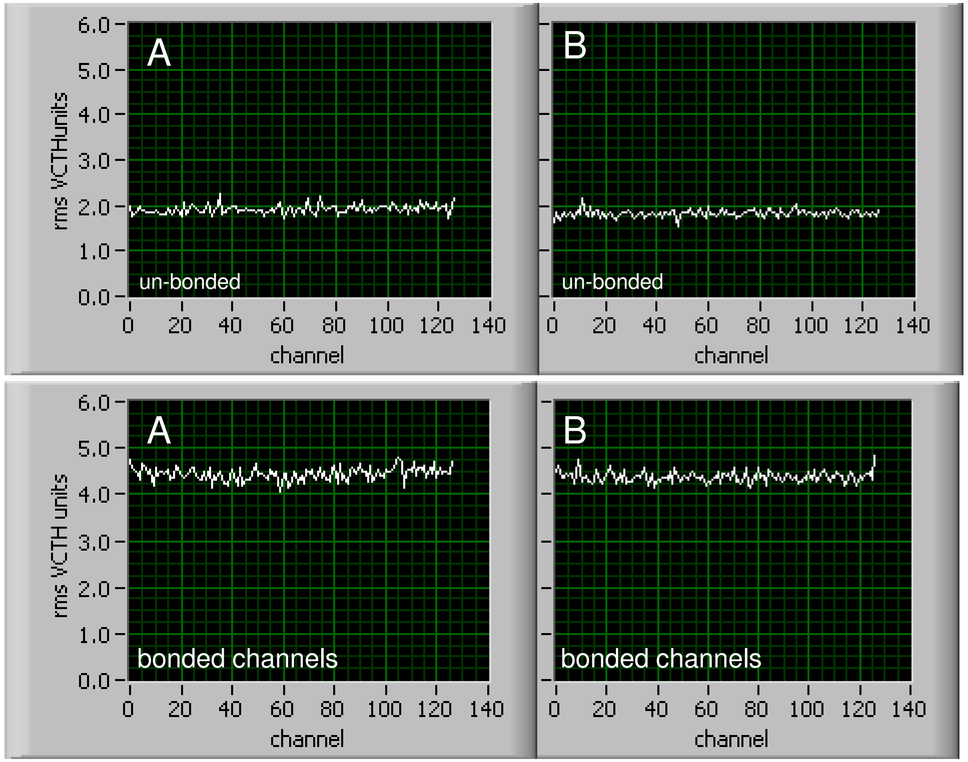


s-curve mid-points



noise

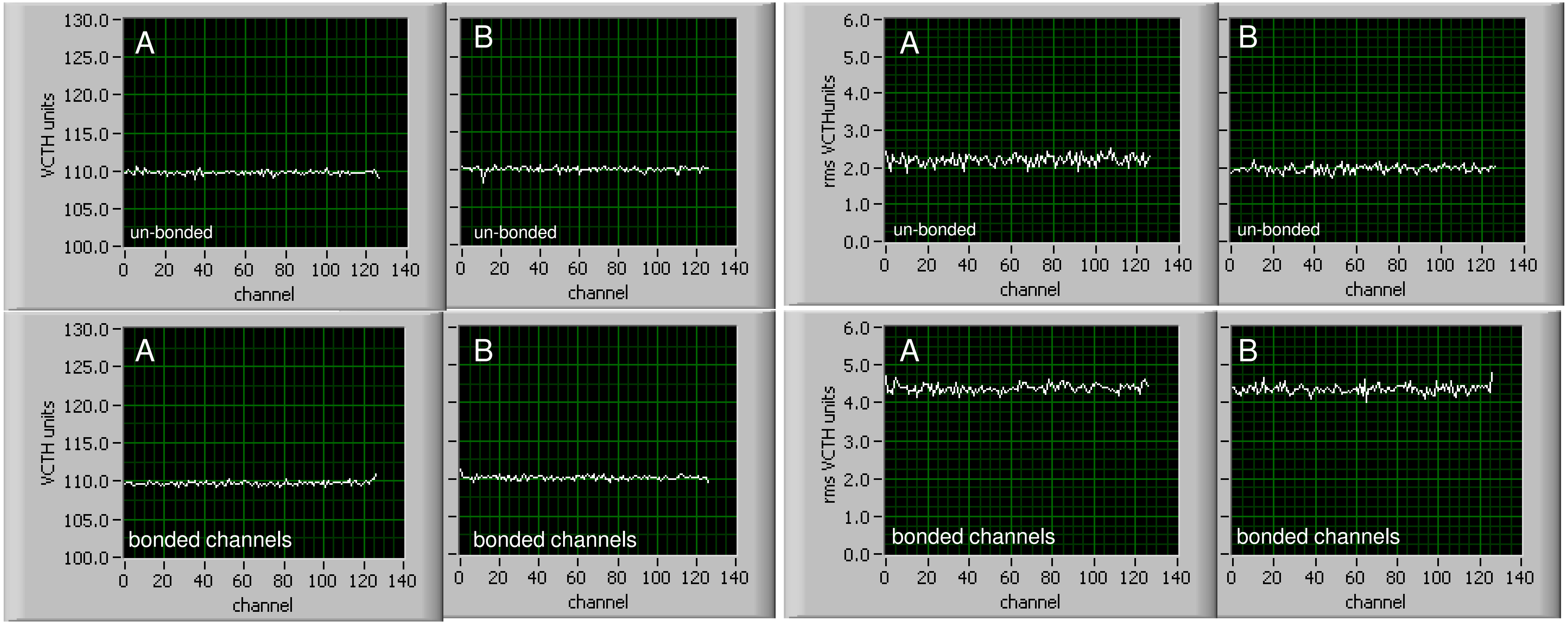
39



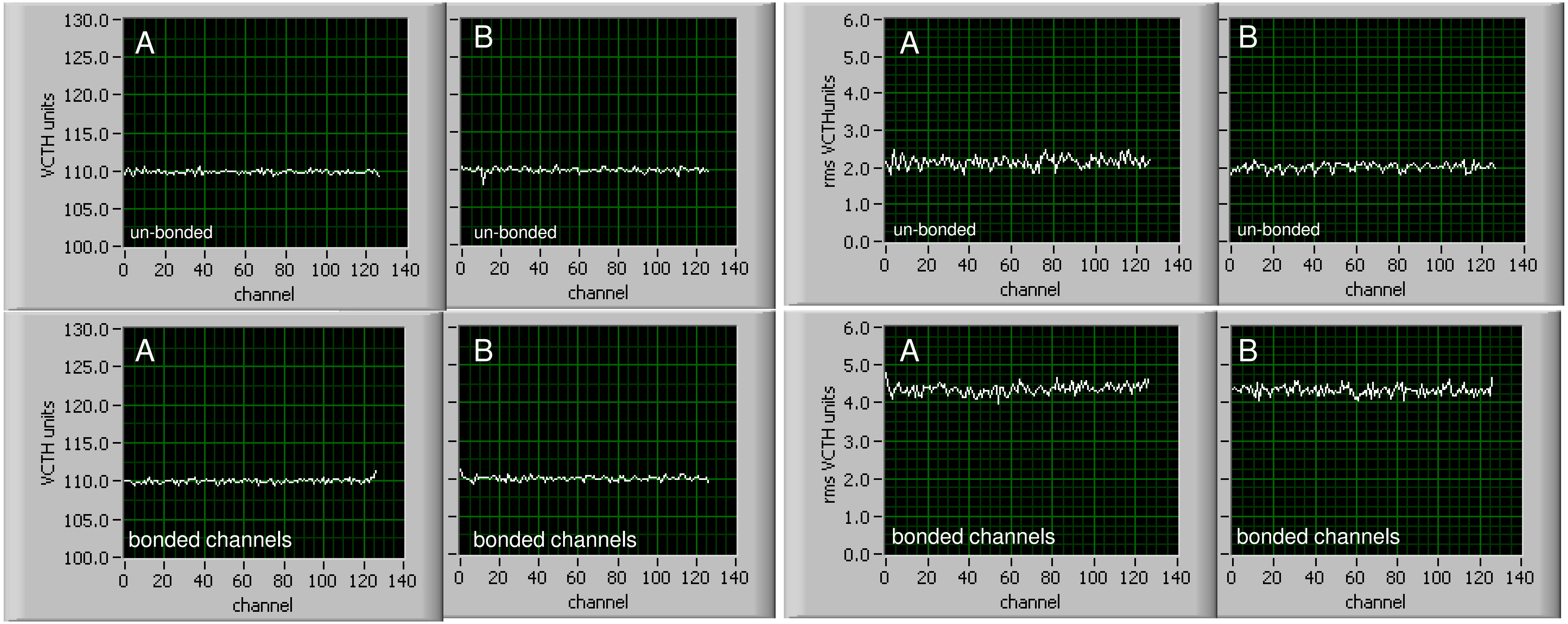
s-curve mid-points

noise

40



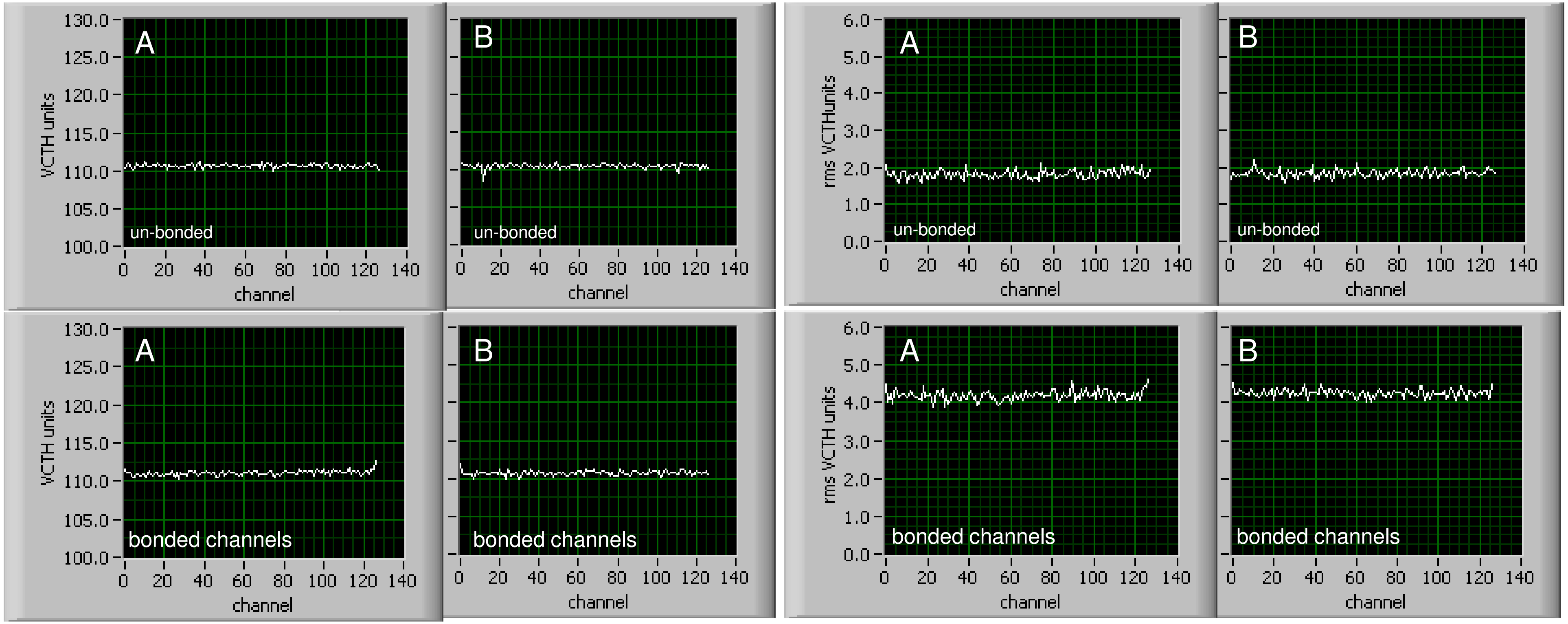
s-curve mid-points   noise   41



s-curve mid-points

noise

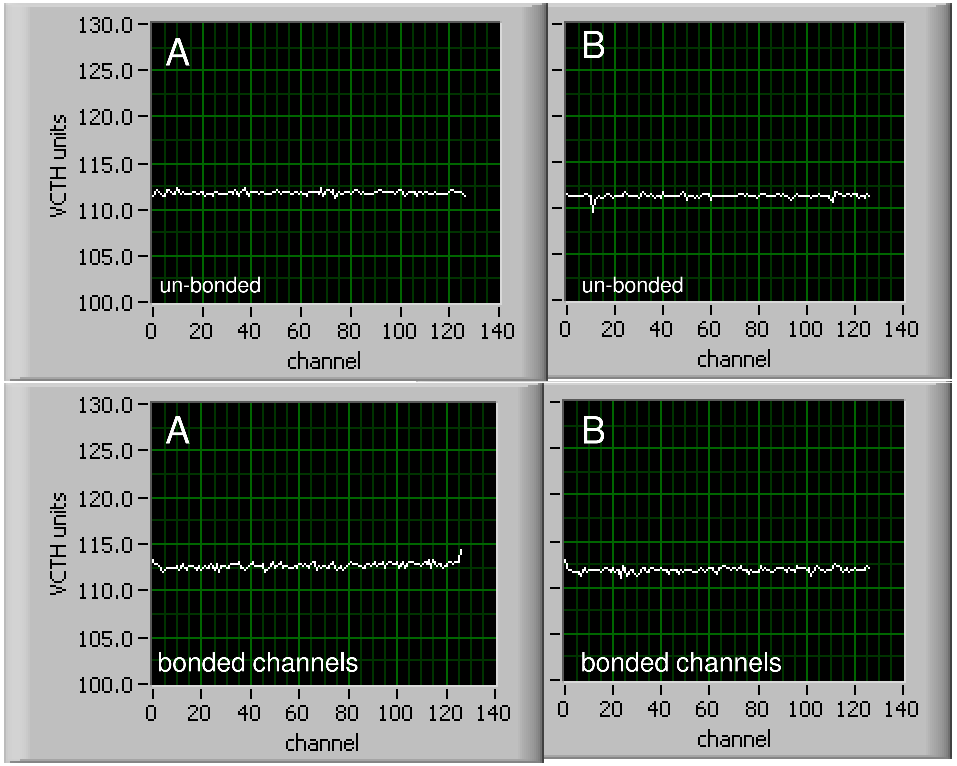
42

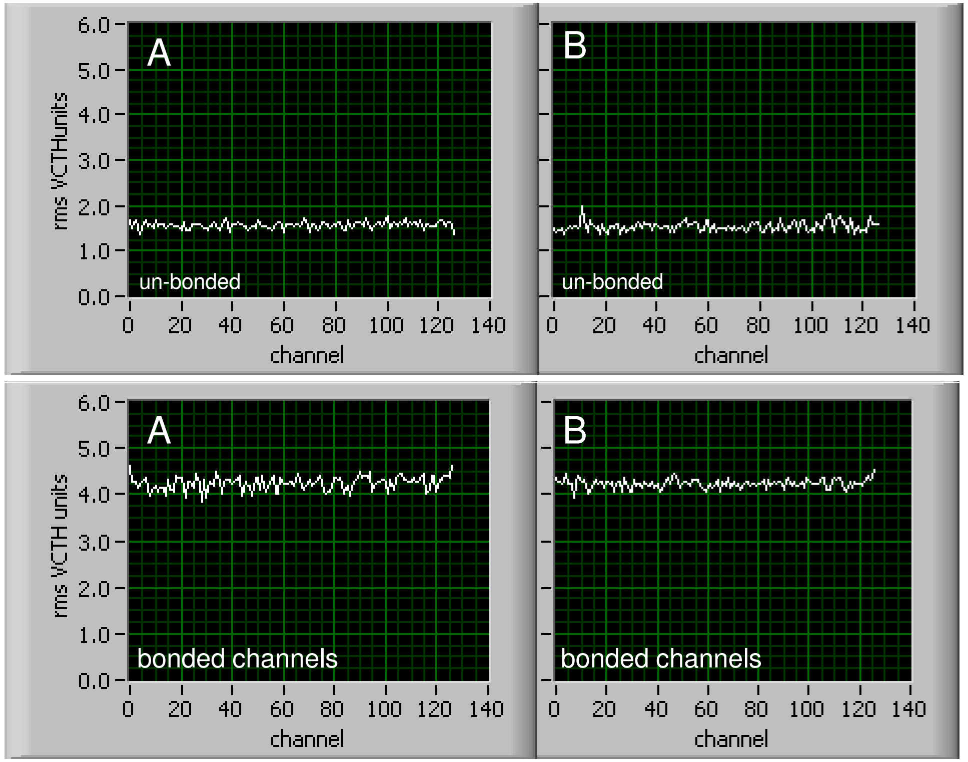


s-curve mid-points

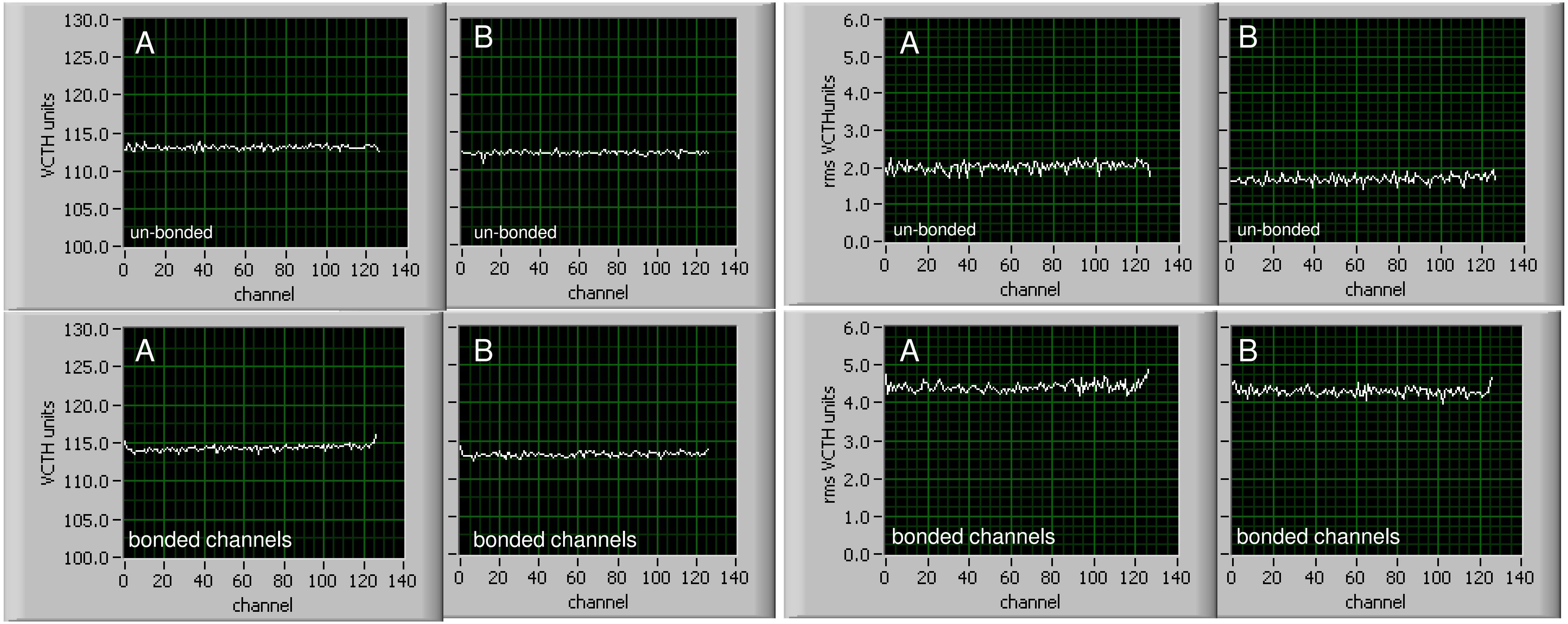
noise

43

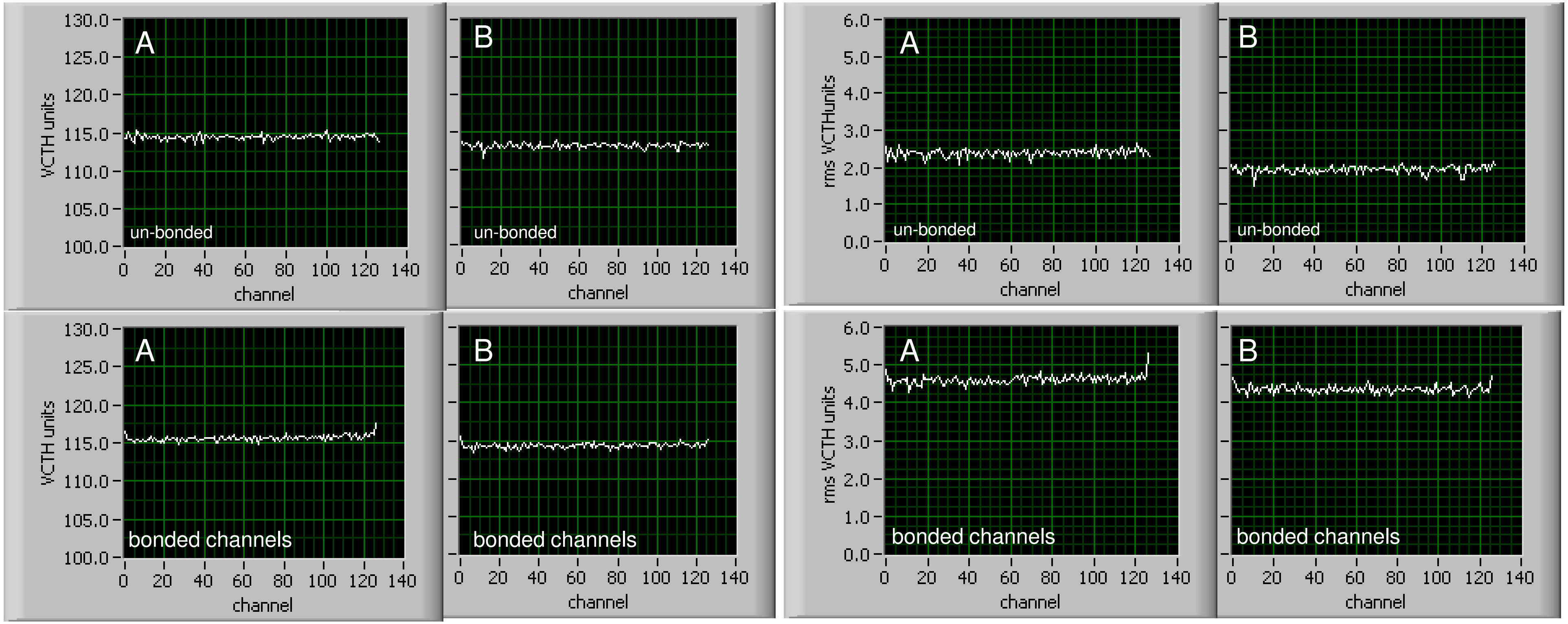




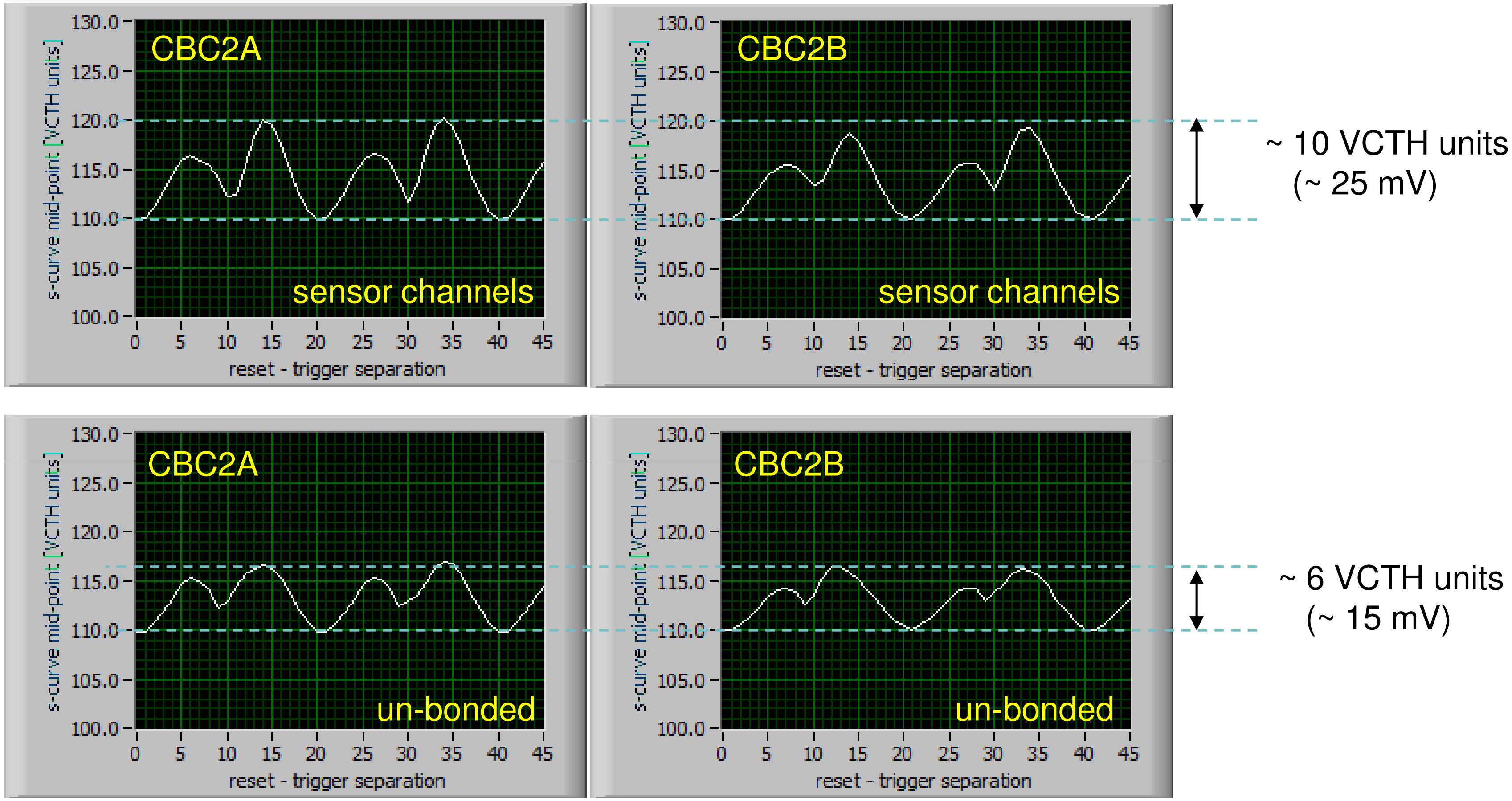
s-curve mid-points noise 44



s-curve mid-points   noise   45



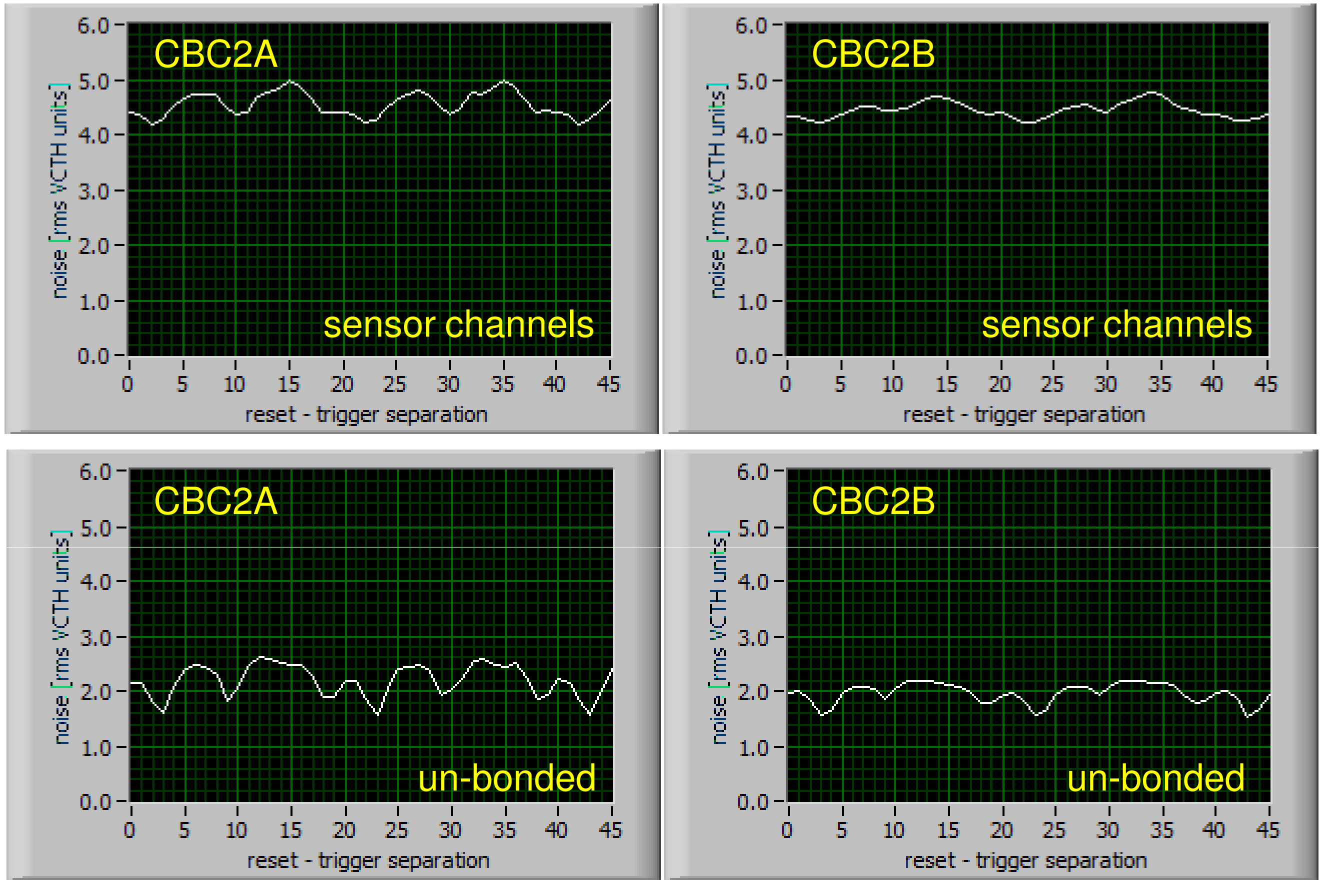
average s-curve mid-point vs. time step



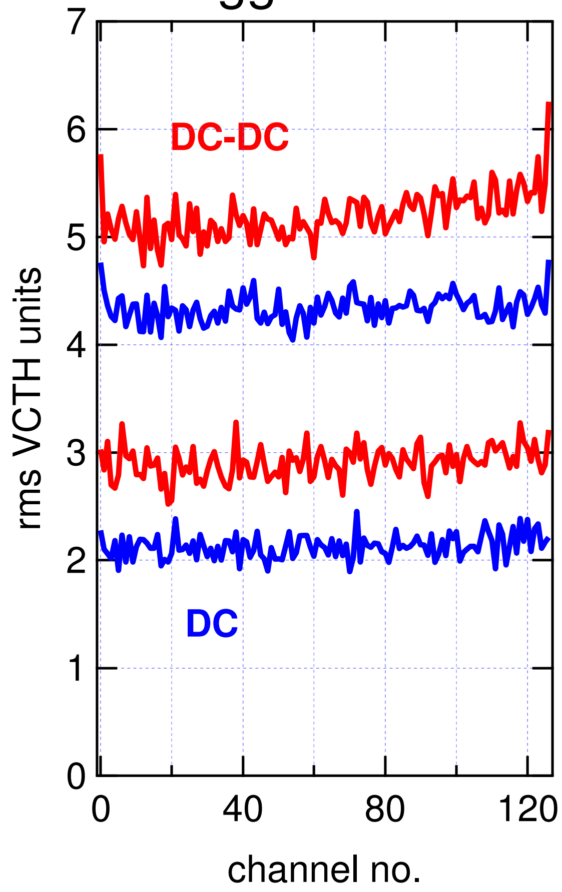
periodicity of pedestal shift behaviour 500 nsec (1/2 the 1 MHz clock period)

amplitude of pedestal movement vs. trigger time depends on whether channel bonded or not

average noise vs. time step



reminder of random trigger result

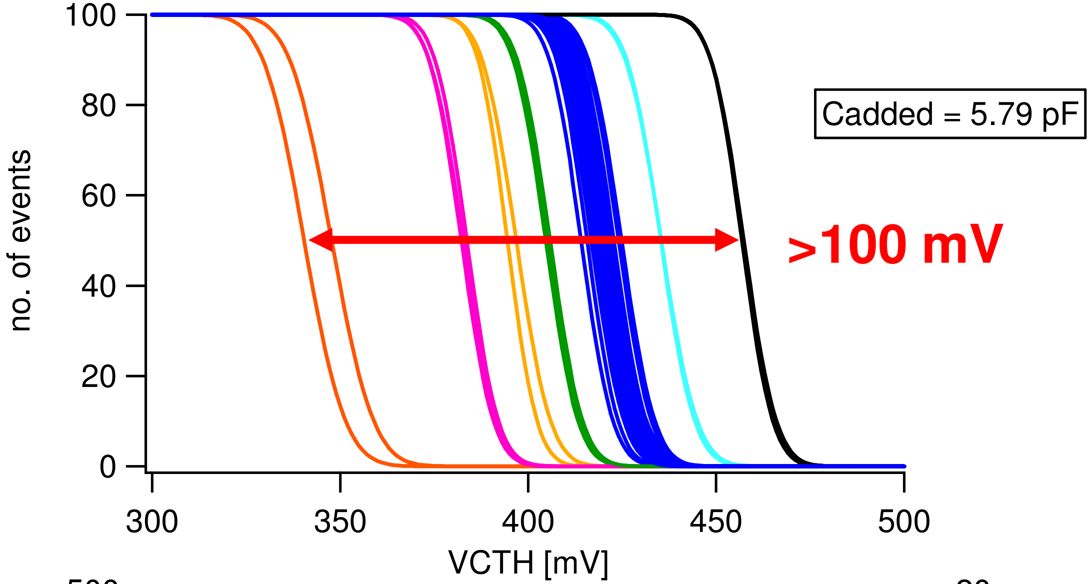


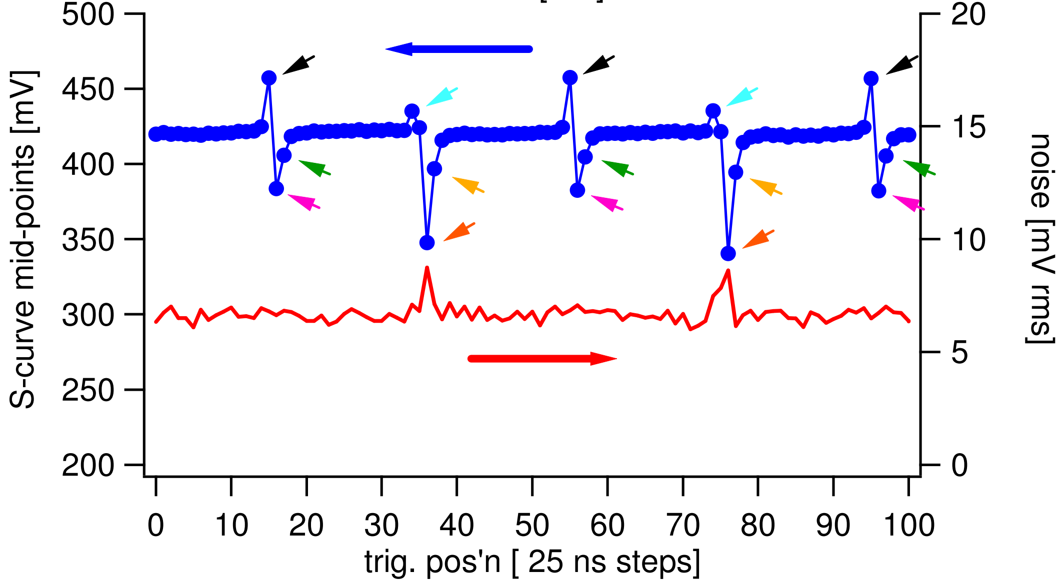
some variation of intrinsic noise with time-step

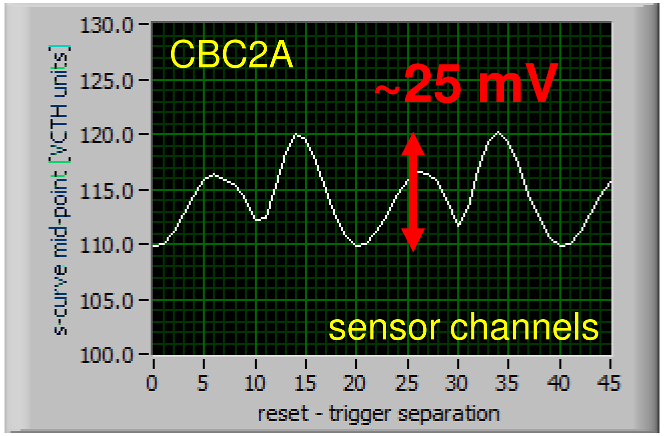
(could just be due to non-linearities in VCTH)

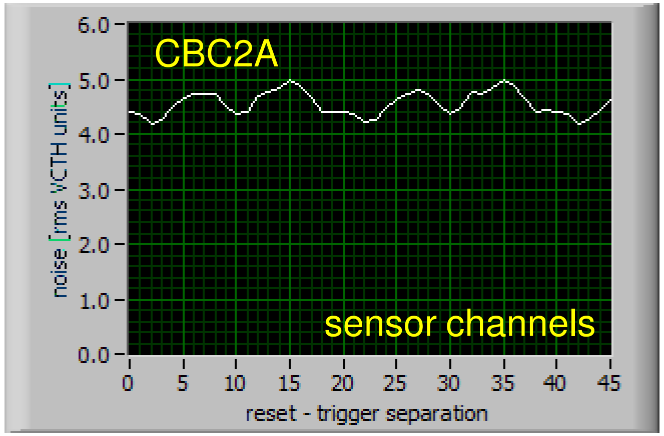
but dominant extra noise (with DC-DC powering) coming from pedestal movement

CBC1:CBC2 comparison









summary

like CBC1, fundamental performance of DC-DC circuit is good

- high efficiency for 2:1 step down conversion
- no significant effect on intrinsic noise

systematic pedestal shift effects remain

- much smaller in amplitude than for CBC1
- characteristic behaviour different
    - pedestal shifts vary ~continuously throughout 1 MHz DC-DC cycle (not just at clock edges)
    - across chip pedestal shift variation at certain phases

some slides from previous CBC1 talk follow

CBC performance with switched capacitor DC-DC converter

Mark Raymond, Tracker Upgrade Power Working Group, February 2012.

CBC power features

2 powering features included on CBC prototype

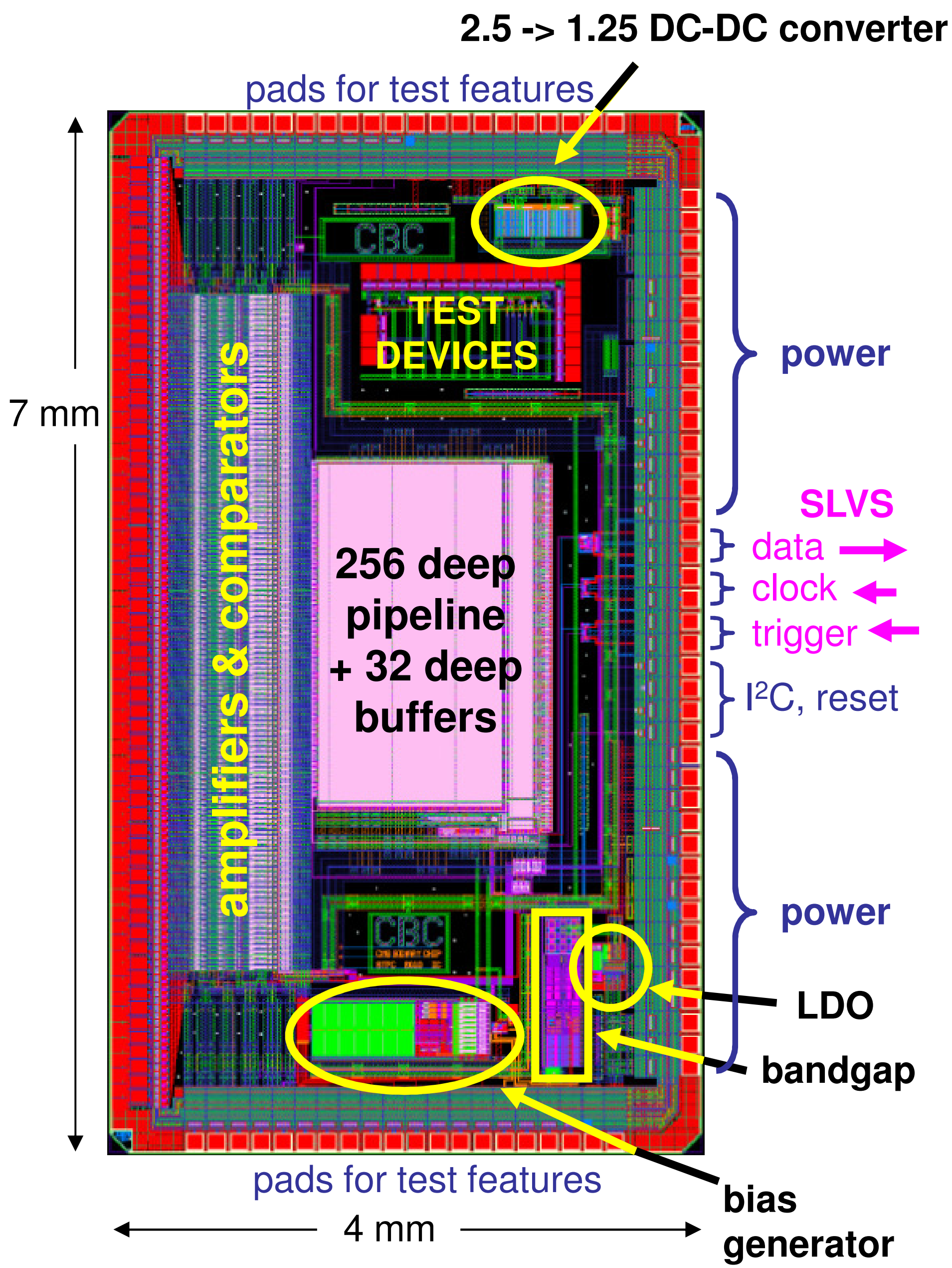
LDO regulator (1.2 -> 1.1) feeds analog FE

provides stable voltage rail
and supply noise rejection

2.5 -> 1.2 DC-DC converter

allows to power CBC using single 2.5 V rail

thanks to Michal Bochenek and Federico Faccio
for the design and help with incorporating the
layout into the CBC



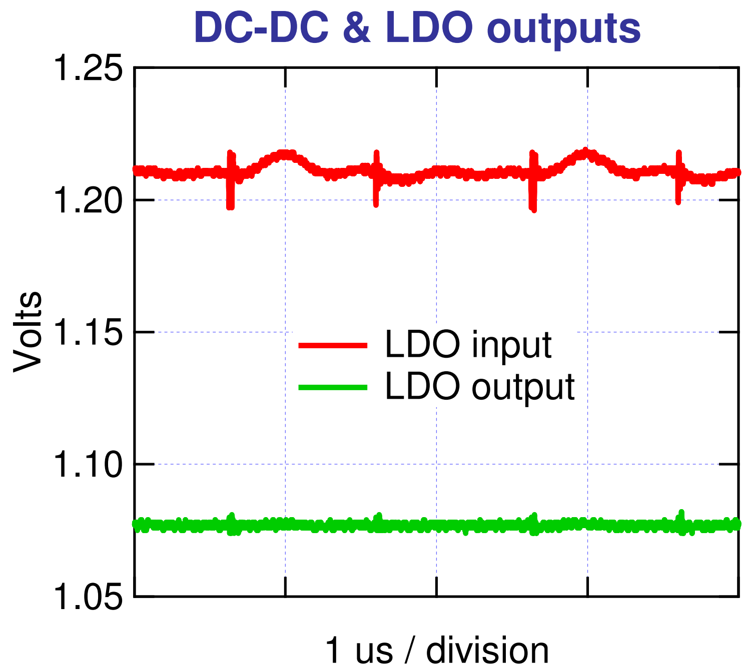
CBC power features - DC performance

DC-DC switched capacitor converter

converts 2.5 -> ~ 1.2

clearly functioning, high efficiency ~ 90%

study of DC-DC switching effects on noise follows in next slides



LDO linear regulator

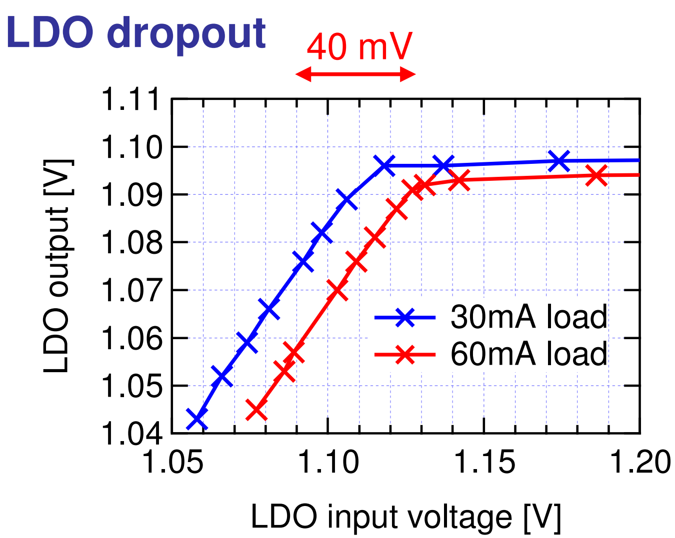
provides clean,regulated rail to analog FE

~ 1.2 Vin, 1.1 Vout

dropout ~ 40 mV for 60 mA load

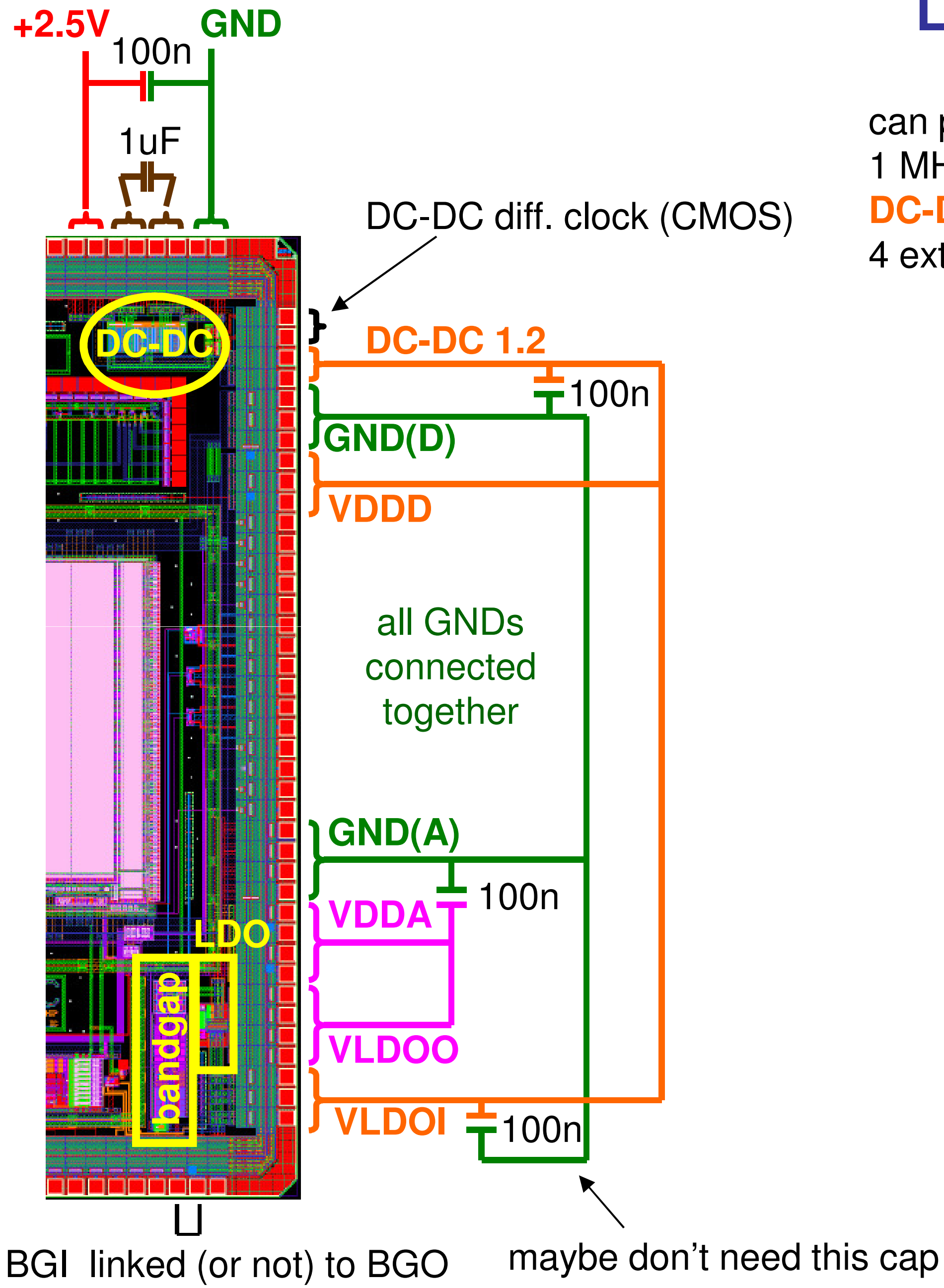
provides > 30dB supply rejection up to 10 MHz

for further details see:
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_Tracker_Electronics_May_11.pdf

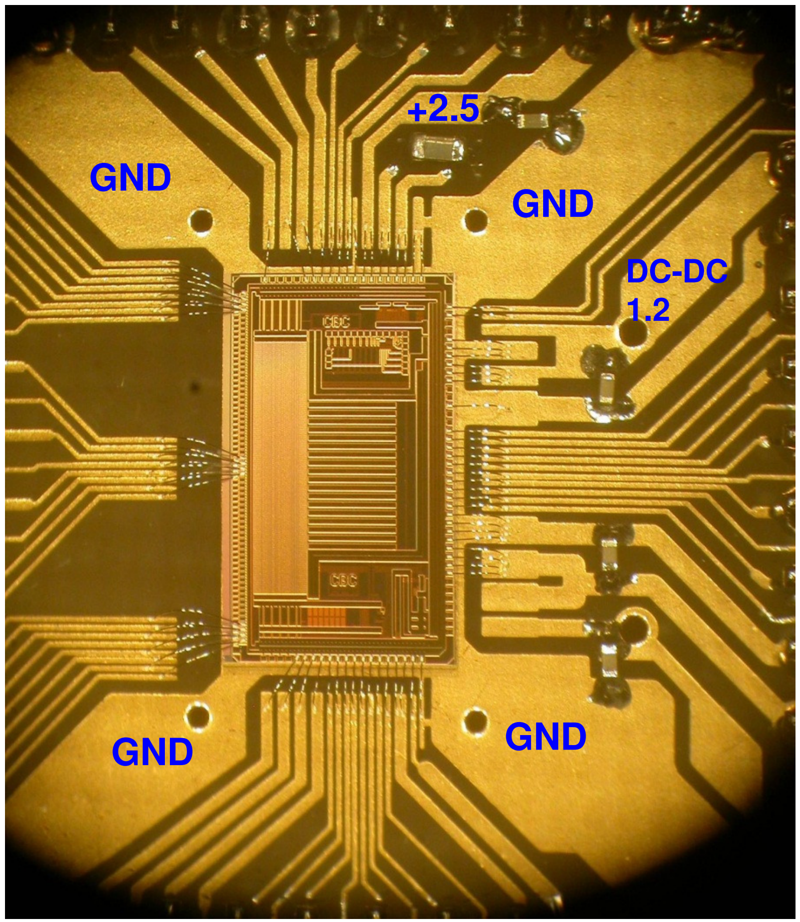


DC-DC powering option

can power CBC from single **+2.5V** supply
1 MHz diff. clock to DC-DC circuit
DC-DC 1.2V feeds **VDDD** (dig. supply) and **VLDOI** (LDO I/P)
4 external capacitors minimum
(actually 5 in this picture)

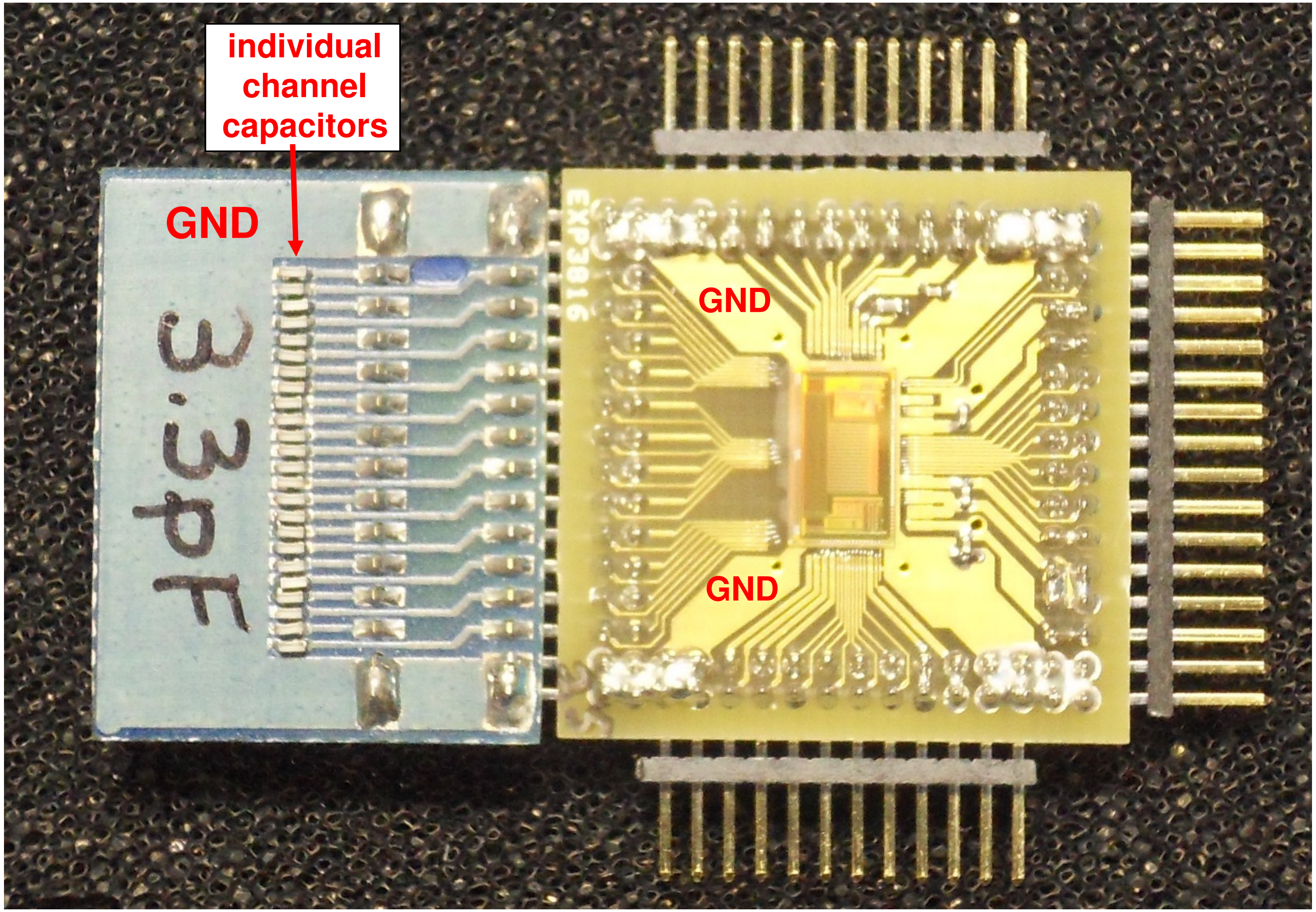


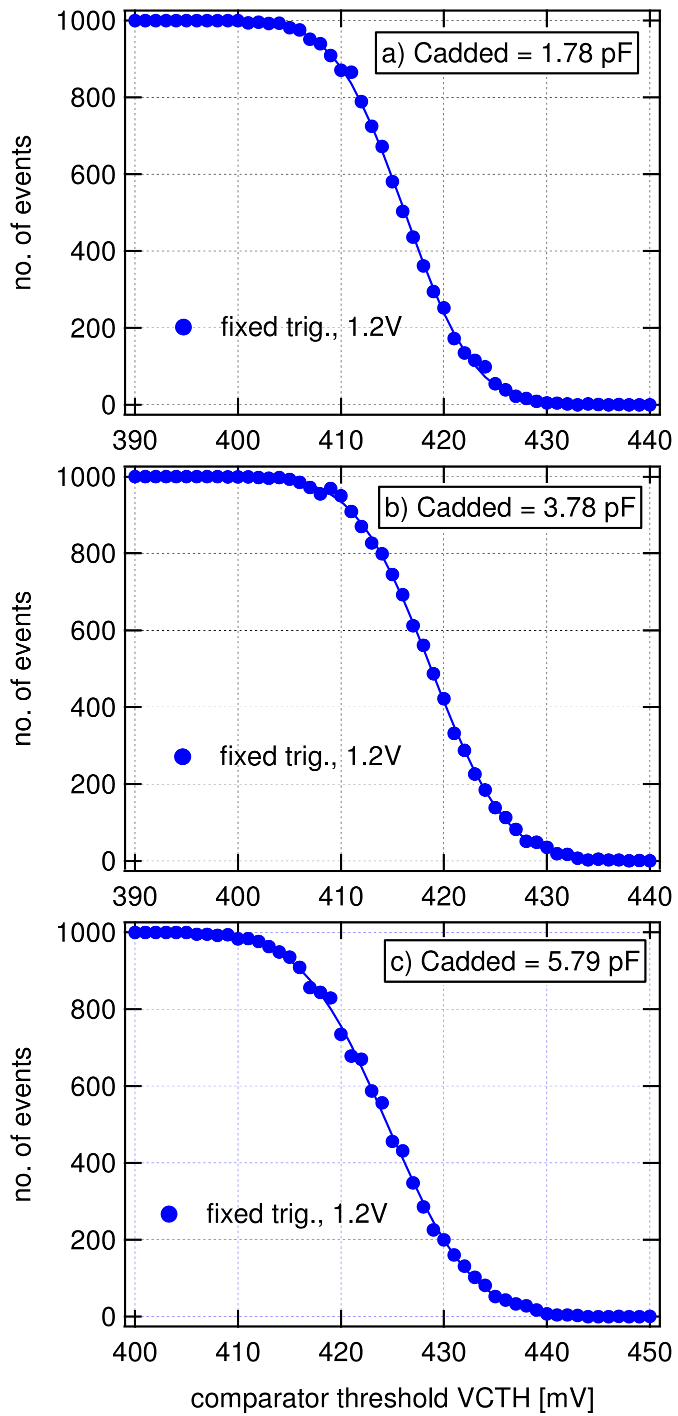
CBC on test board



adding external capacitance

want to measure noise (from s-curves) dependence on external capacitance
plug-on boards containing arrays of capacitors connect to bonded out channels
acquire s-curve for one of the bonded out channels





s-curves:reference measurement

measure s-curves for single channel for different external capacitances

conditions for measurements on <u>this</u> slide

digital circuitry supplied with external 1.2 V supply

DC-DC not running

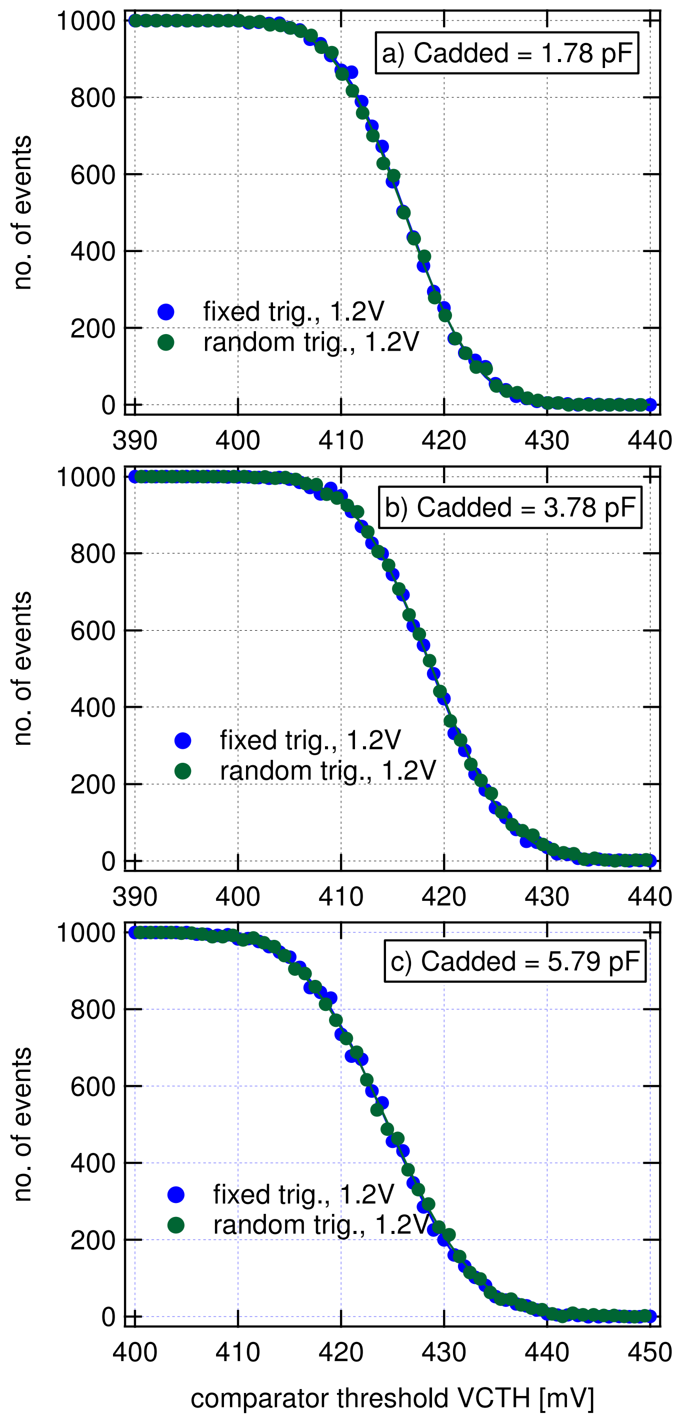
CBC triggered at fixed time following a fast reset

=> always triggering same pipeline location

gives cleanest possible measurement as reference

(no reason to expect any effect from random triggering, but just to check)

s-curves: DC supply (random trigger)



now repeat for random triggering

digital circuitry still supplied with external 1.2V supply

DC-DC still not running

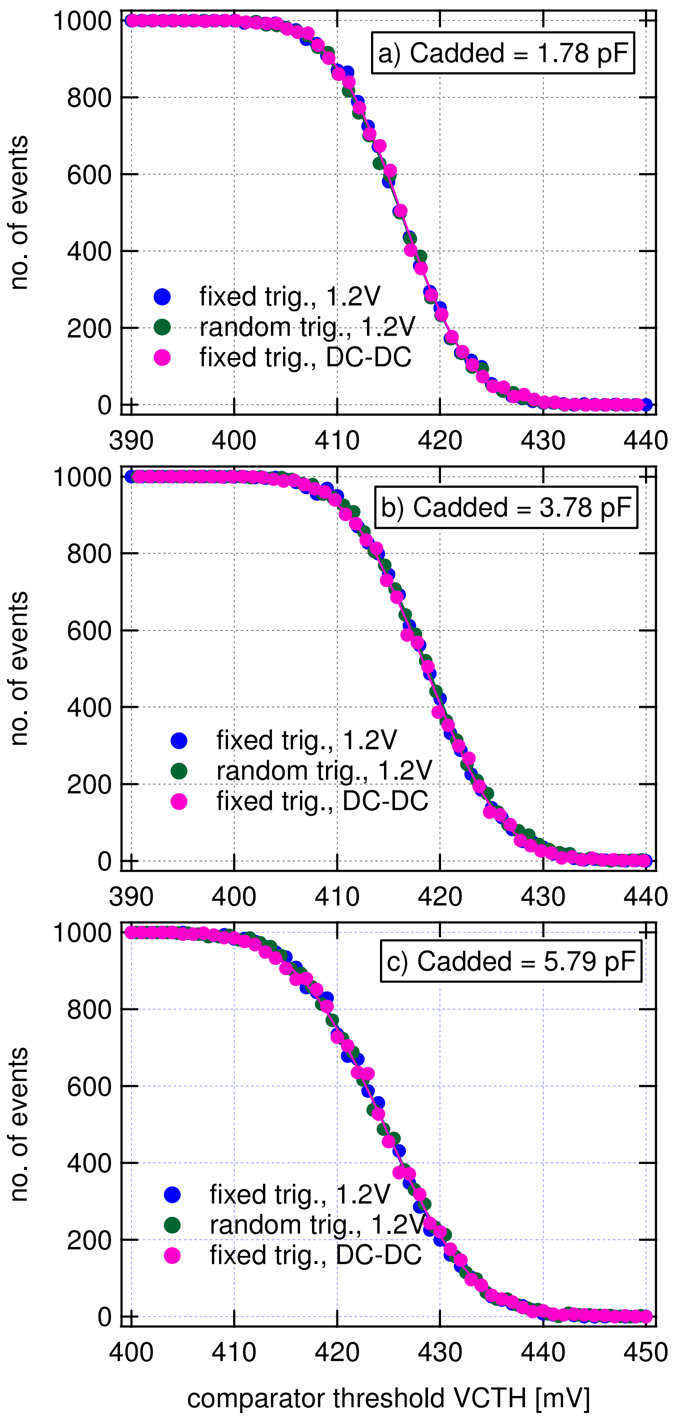
but fast reset removed

pseudo-random trigger, so now triggering locations throughout pipeline

no effect on s-curves visible (i.e. no effect on noise)

(as expected)

s-curves: DC-DC running (fixed trigger time)



now feed digital circuitry with DC-DC 1.2 V

DC-DC now running

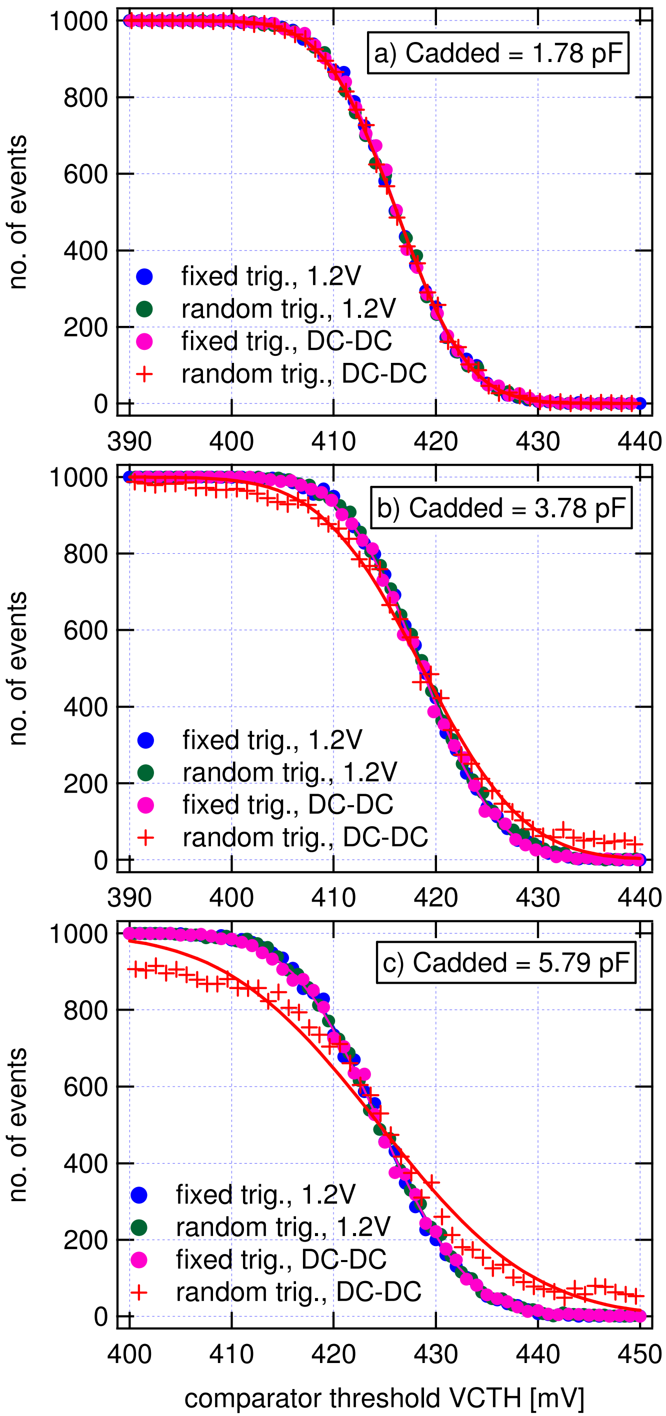
return to triggering at fixed time following a fast reset

DC-DC clocked at 1 MHz
with fixed phase relationship to fast reset

once again - no significant effect on s-curves

=> **DC-DC circuit doesn't affect intrinsic noise**

s-curves: DC-DC running (random trigger)



now try pseudo-random triggering again

DC-DC still running

s-curves now distorted for larger capacitance

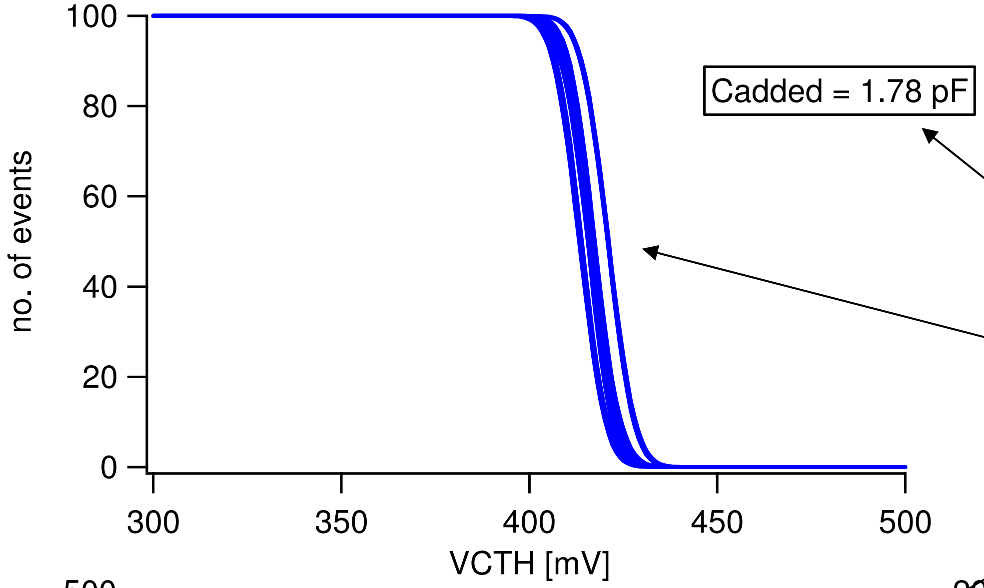
=> something to do with random triggering when DC-DC circuit operating

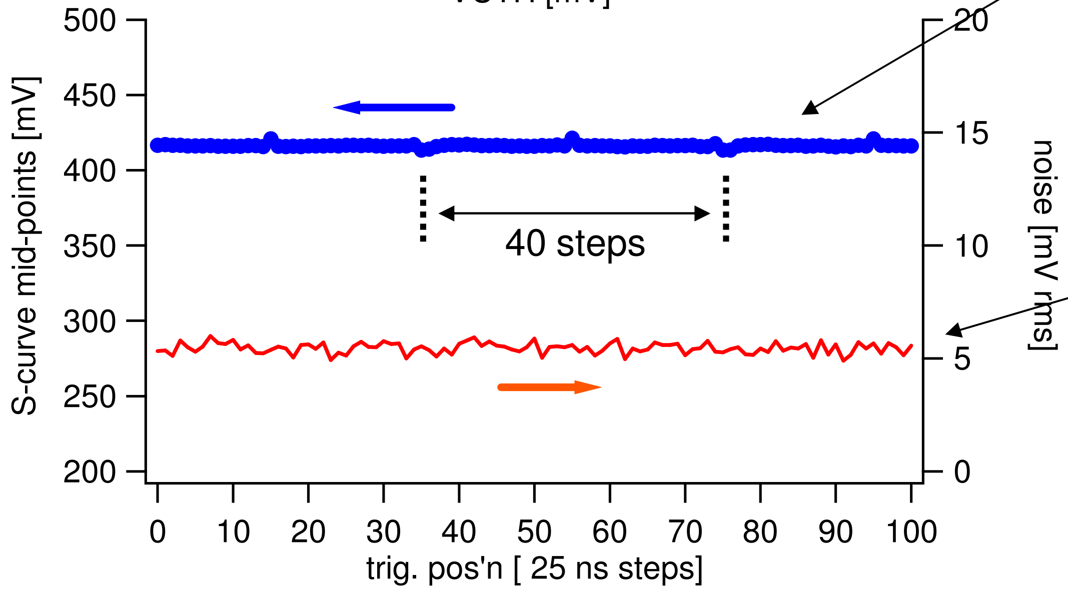
an effect associated with specific pipeline locations?

try to understand what's going on with a more systematic study

=> look at s-curve dependence on triggered pipeline location

s-curve dependence on triggered pipeline loc'n





acquire s-curves with increasing separation between fast reset time and trigger position (25 nsec steps)

DC-DC circuit operating

results here for smallest capacitance:

not all s-curves in same position

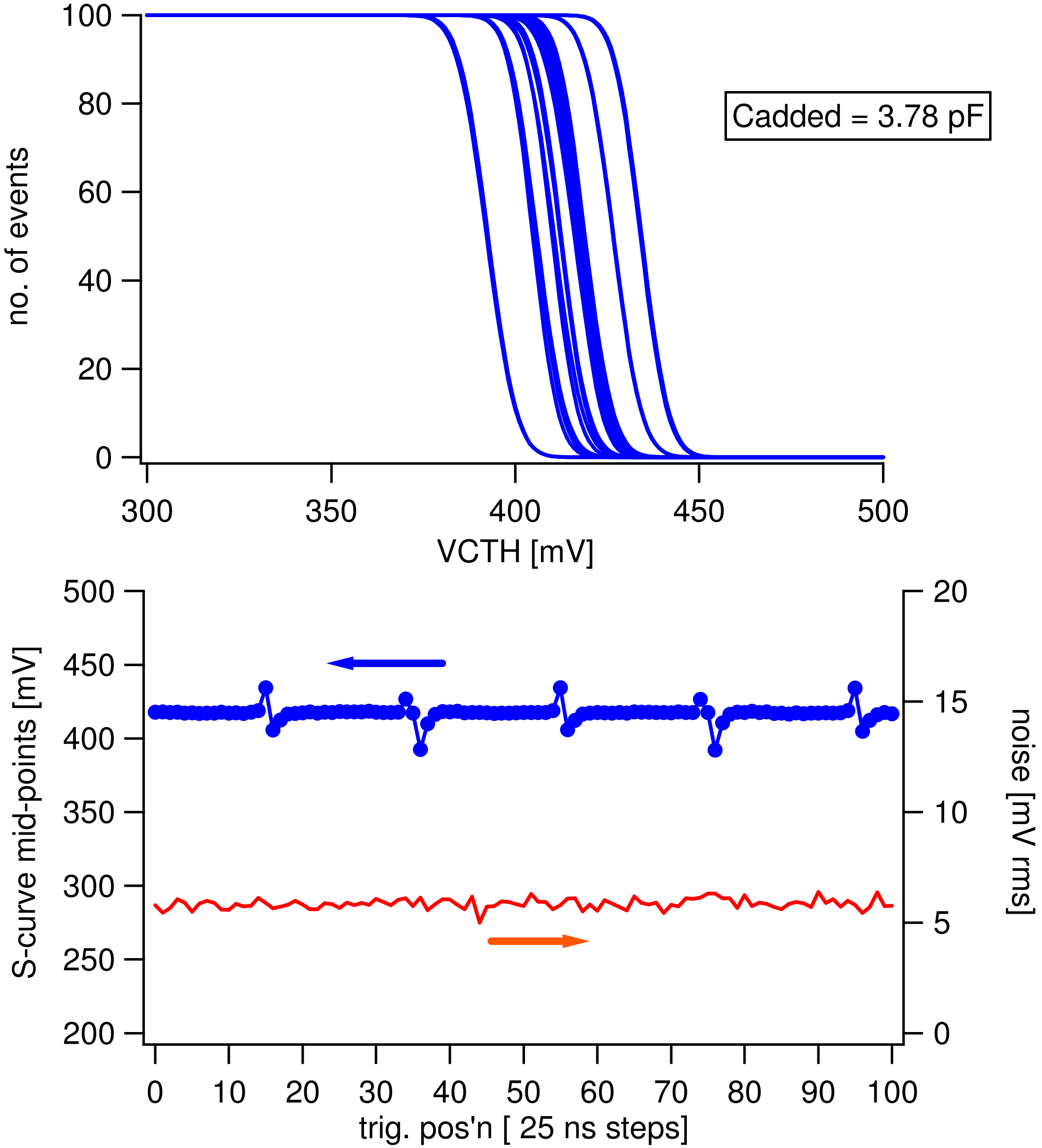
plotting s-curve mid-point vs vs. trigger position shows repetitive structure

separation between positive (or negative) shifts = 40 steps = 1 μsec = DC-DC period

pedestal shift only, no change in shape

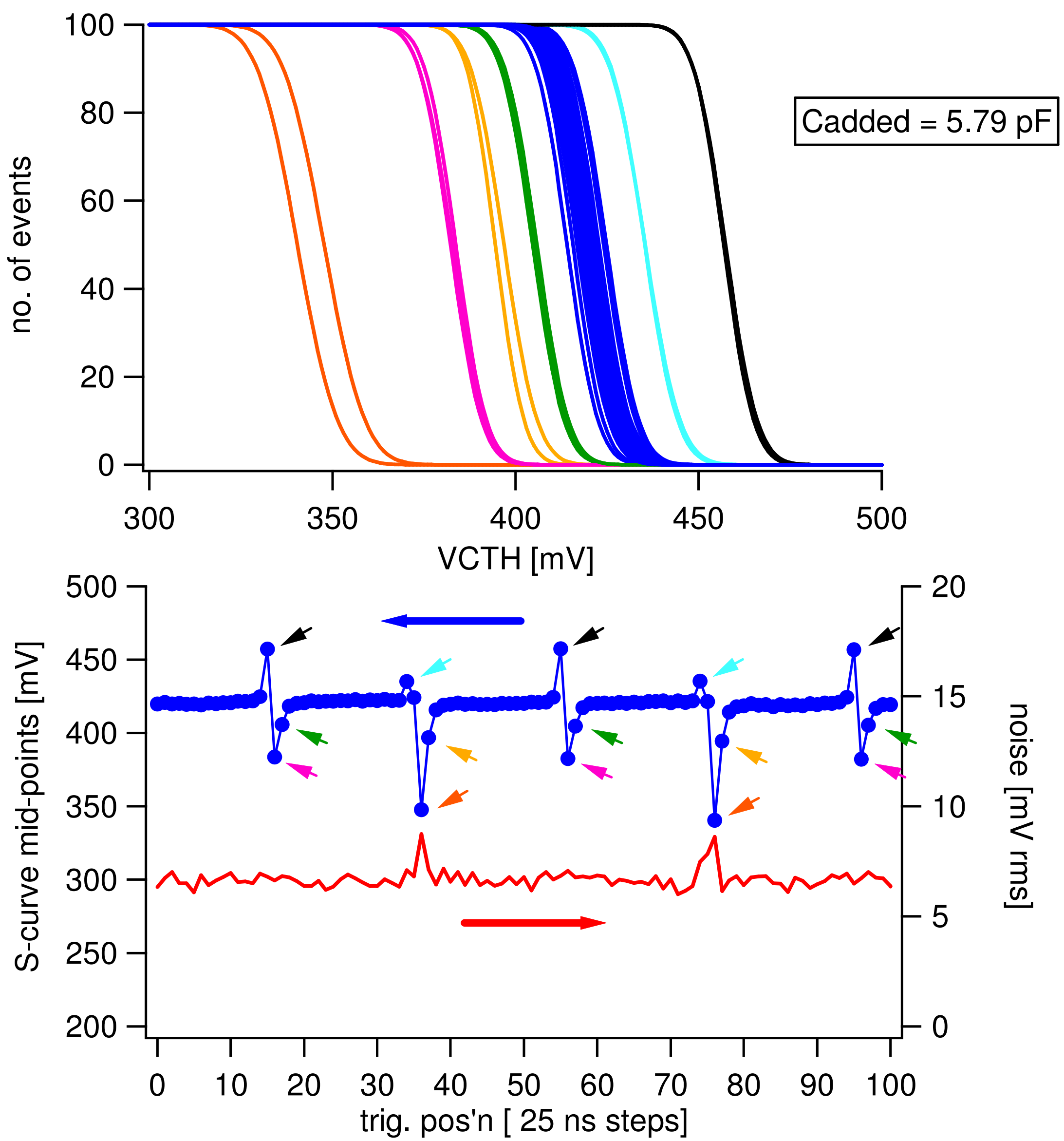
=> intrinsic noise unaffected

increasing external capacitance



effect becomes much more noticeable

for largest external capacitance



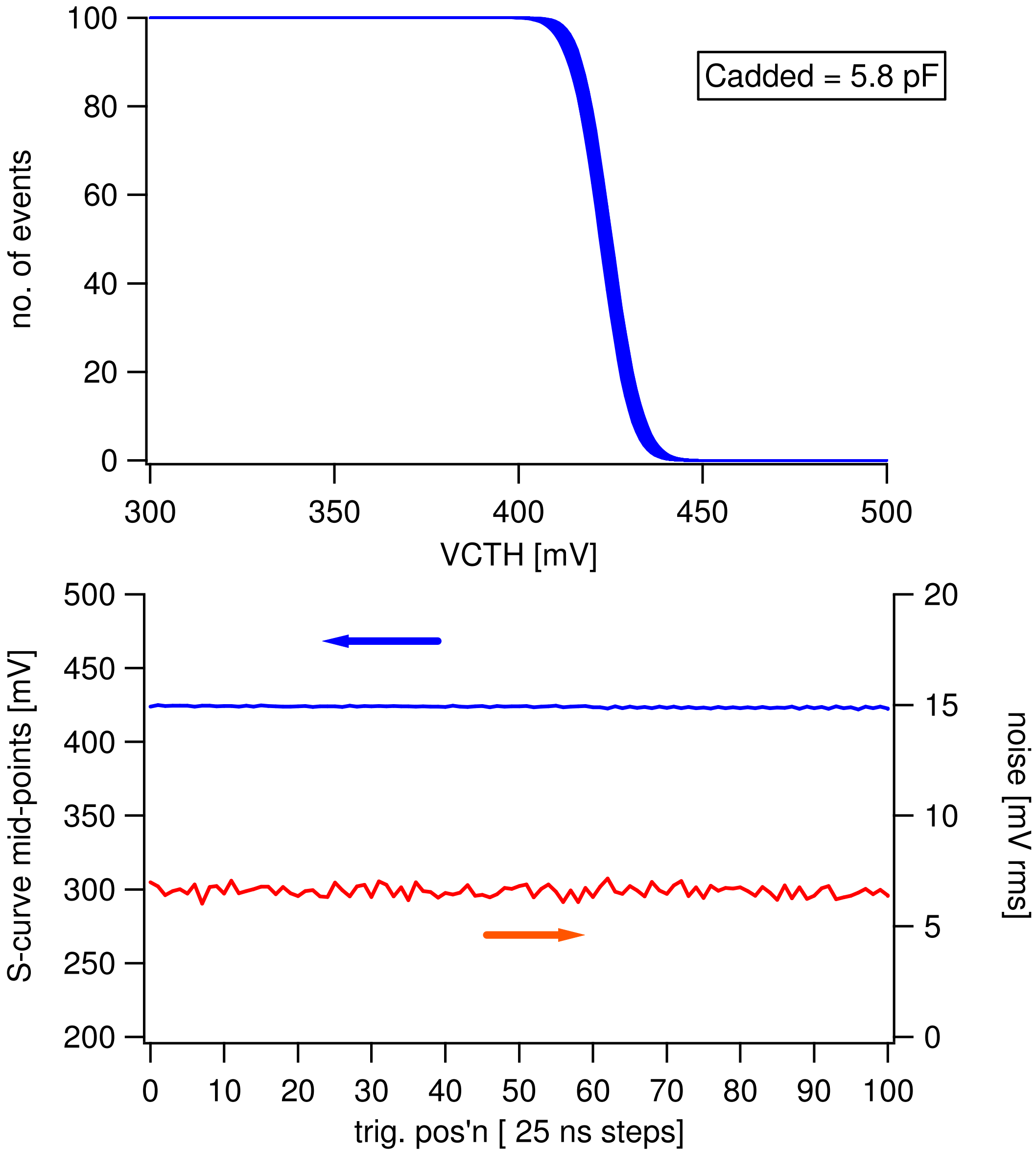
s-curves in top plot colour coded to show which ones correspond to which point in bottom plot

some distortion visible for most negatively shifted curves (out of amplifier linear range)

so DC-DC circuit operation somehow affects channel pedestal

magnitude of effect proportional to external capacitance to ground

repeat for external DC supplies



just to check

effect goes away completely if DC-DC circuit not operational