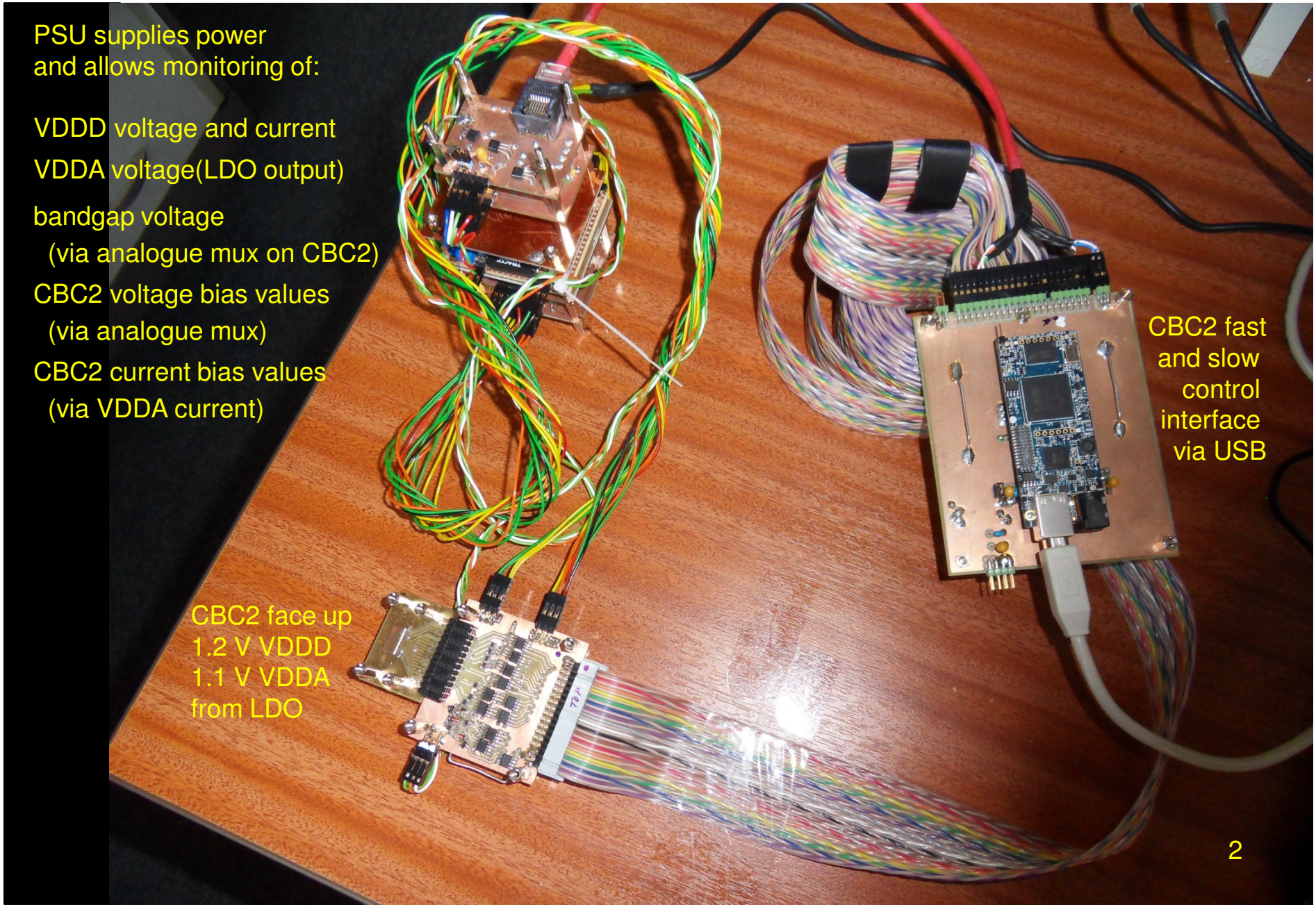
CBC2 test plans

CBC3 specs, thoughts and plans

systems meeting, 12/2/14

CBC2 ionising test - hardware



CBC2 ionising test - software

labview based software

chip biased to normal I2C biases, constantly triggered

periodic adjustment and monitoring:

~ hourly
- auto-tune offsets, takes ~ 10 minutes

~ every minute
- bandgap voltage
- power supplies currents and voltages - nominal bias
- power supplies currents and voltages - analogue biases set to zero -> digital baseline

~ every 10 minutes
- perform bias scan for one of the front end analogue biases (voltage or current)
- rotate through ~ 10 parameters
- => each bias gets detailed study every ~ 100 minutes

all data saved to file

CBC2 test plans

ionising: Davide, Mark R

test setup ready, irradiation starting next week

SEU: UK team + Louvain

still in the planning stage, aim to be ready by summer 2014

expect to use protons

DAQ system not yet decided - “test beam like” GLIB DAQ? / ionising USB setup?

other CBC2 tests

still details to understand to feed into CBC3 design

e.g. biases
linear enough? monotonic enough? enough resolution?
- VCTH is the critical one here

CBC3 requirements and plans

some requirements already clear (I think)

- e.g. stub info, longer pipeline, higher trigger rate capability
- but still some open questions - e.g. output data line rate, diff. or s.e.

other requirements have been suggested

- e.g. 2 comparators / channel?

take this opportunity to begin to assemble specifications & identify some open questions

CBC3 front end

sensor choice

n-on-p, AC coupled, strip length up to 8 cm (~12 pF)
=> polarity defined, no DC sink/source requirement

front end amplifier

adjust for 1V VDDA:
removal of DC coupling requirement will help, also polarity decision

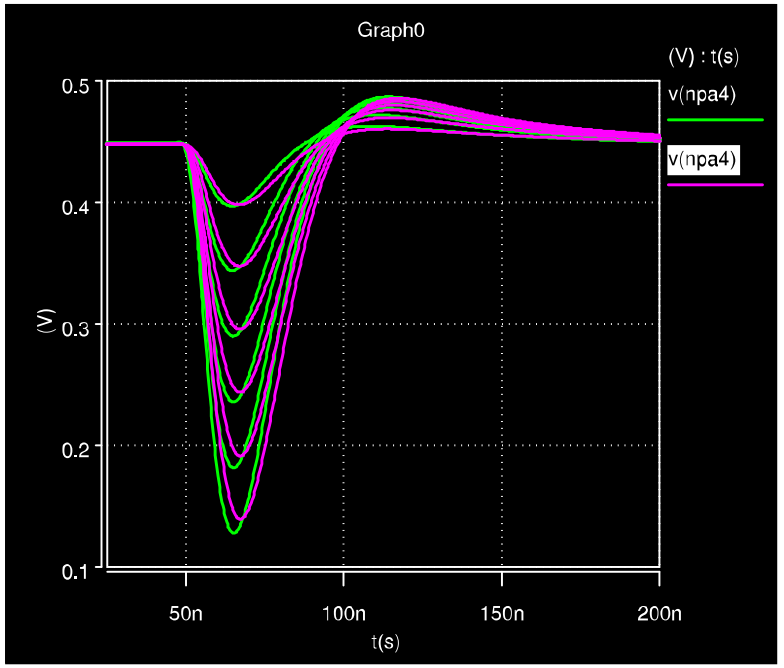
re-examine pulse shape for dead-time issue

want pulse that returns to baseline within 50 ns
some overshoot unavoidable

adjust preamplifier for larger sensor capacitance

maintain current noise performance
noise α $C/\sqrt{I_{DS}}$ ($g_m \alpha I_{DS}$)

to compensate (8/5) x C
need 2.6x current in input device



CBC3 front end

comparator

2 comparators/channel? 5 sigma and 3 sigma thresholds?

(1 chan > 5σ) OR (2 neighbours > 3σ)=> hit

issues of what to do with comparator outputs
e.g. 2 bits/channel pipeline? (increased data volume)
more signals to cross chip boundaries?

some big implications for architecture here - needs more thought

extra ~ 50 uW / channel

comparator output interface to pipeline

if ampifier pulse short then just sample comparator output into pipeline (and correlation cctry)

=> no deadtime

but hip signal will keep comparator output high for long time

need additional circuit to suppress hips

e.g. block comparator output if high for longer than several BXs
(keep blocked till comparator output returns low)

CBC3 pipeline

pipeline

length increase: 12/25 usec?

channel masking

currently only mask is before correlation logic to prevent spurious triggers from noisy channels

no masking of channels to pipeline (not necessary in unsparsified system)

1 MHz trigger rate => sparsification mandatory (in concentrator)

where to do channel masking? - not necessarily on CBC but might be best place

assume separate to mask for correlation logic - or could it be the same one?

CBC3 offset correction and correlation

offset correction

4 domains / chip (only 2 in CBC2)

correlation

+/- 8 channels, ½ strip resolution => 8 bit address

5 bit bend information

priority encoding of highest 3 pT stubs (Mephisto)

is this necessary?

CBC3 readout

trigger rate capability to 1 MHz

how much does current pipeline readout architecture have to change?

output data format

how many lines at what rate?, differential/single-ended?

CBC3 miscellaneous

biases

linear enough? monotonic enough? enough resolution?
would be nice if VCTH monotonic

slow ADC?

with “band-gap accuracy” can at least get an accurate value for the voltage biases
could be useful but is it worth it?
probably not if have to develop from scratch

clock domains

need DLL with programmable tap off to capture front end comparator O/P

powering

do we want to keep switched cap DC-DC option?

CBC3 power consumption

start from existing CBC2 - all value in uW/channel

analogue

input device: 21 x C_{sensor} (=> 170 for 8 pF)

other analogue (amplifier, comparator): 130

digital: 50

so for 5 cm sensor, ~ 8pF, get ~**350 uW/chan.**

CBC2 for 8cm sensor, same noise as CBC2 for 5 cm sensor

analogue

input device: $(8/5)^2$ x 170 = 435 (assume want same noise performance)

other analogue: 130

CBC2 digital: 50

so for 8 cm sensor, same noise performance as CBC2, estimate ~**570 uW/channel**

CBC3

need to add extra digital power for extra digital functionality

stub and bend info assembly, 1 MHz triggering, longer pipeline, …

hard to estimate - may not be negligible

off detector transmission estimate 6 diff. lines at 320 Mbps, 4 mW/diff.pr.

=> ~**100 uW/chan.**

=> could be looking at ~700 uW/channel (significant uncertainty - treat with caution)

=> 2.4 Amps from 1.2V rail for 16 chip module (16 cm x 10 cm sensor area)

CBC3 timescale

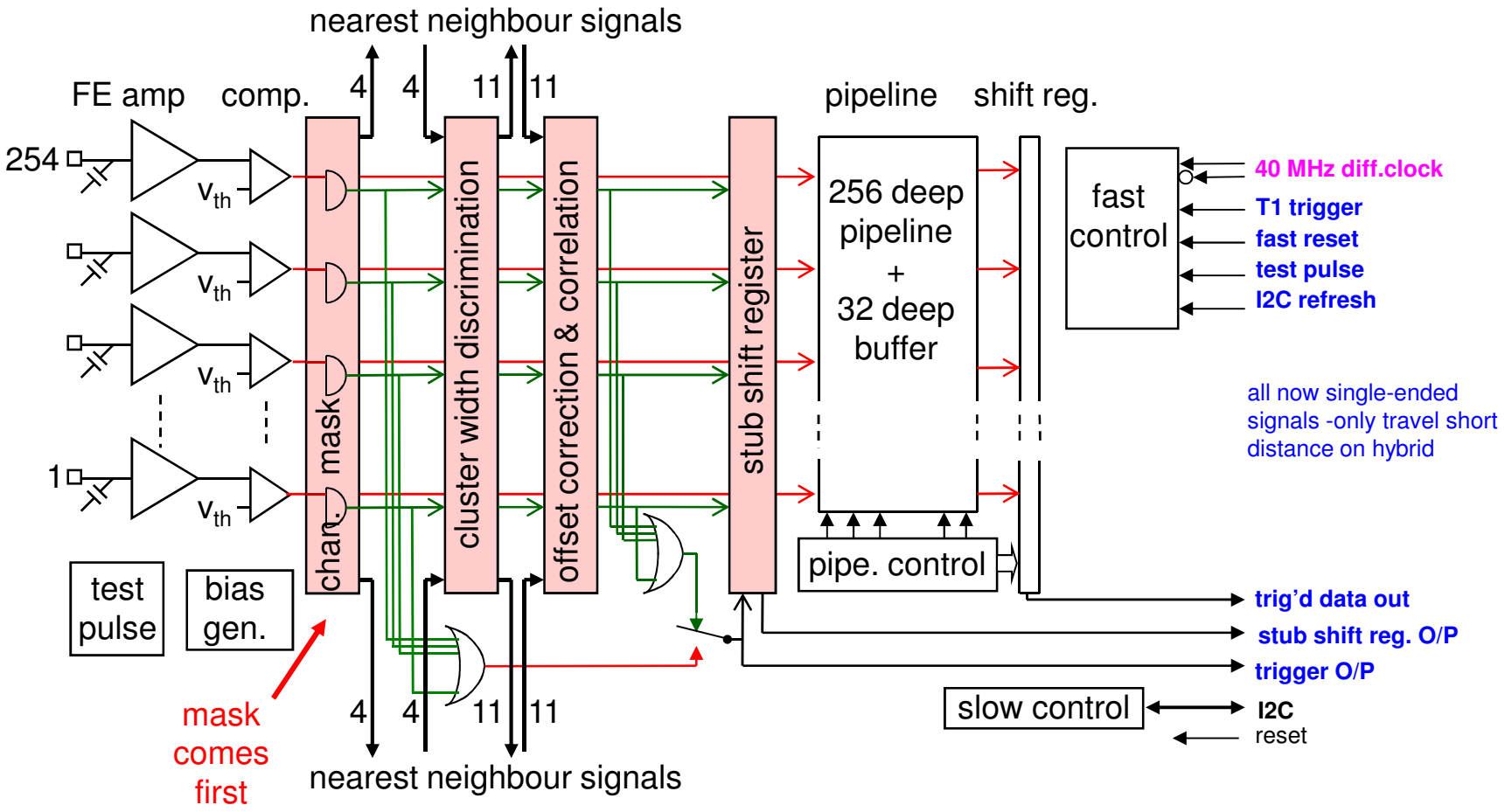
can’t be too definitive till all requirements fixed

try and aim for design ready for manufacture some time in 2nd half 2015

compatible with chip in hand middle 2016

need to be sure that suitable hybrids can be manufactured

CBC2 architecture



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)

cluster width discrimination: exclude wide clusters

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip
for normal operation choose correlation O/P