CBC2 X-ray test results and future irradiation tests

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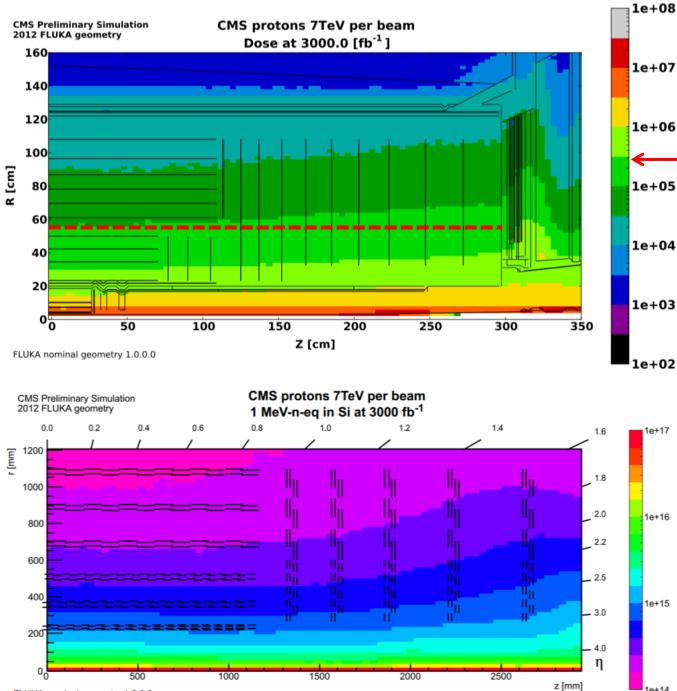
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cience & Technology acilities Council





NB: calculated for 3000 fb⁻¹ but with present Tracker

1e+17

1e+16

1e+15

1e+14

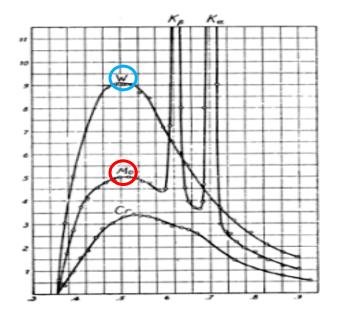
Fluence [cm⁻²]

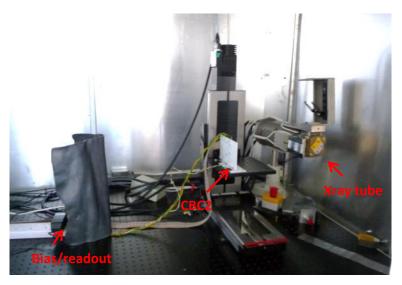
https://twiki.cern.ch/twiki/bin/view/CMSPublic/ BRILRadiationSimulation

FLUKA nominal geometry 1.0.0.0

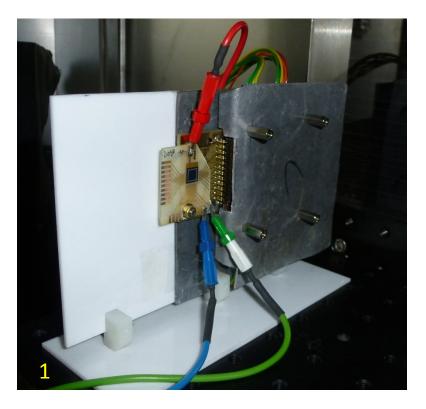
Total Ionizing Dose test at Diamond Xray facility

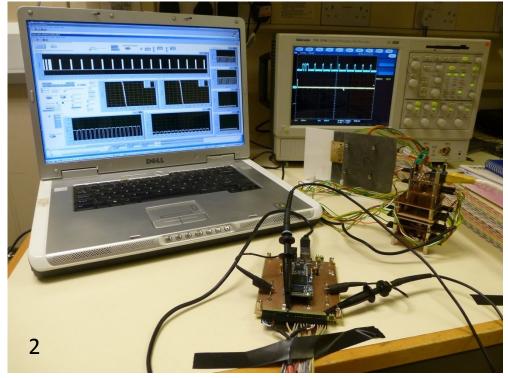
- Mo tube (3000W max)
- Wire-bonded CBC2 ("face-up")
- Thanks to the Diamond Detector Group, in particular Jonathan Spiers, Julien Marchal, Richard Plackett and Nicola Tartoni.
- Irradiation up to ~10Mrads





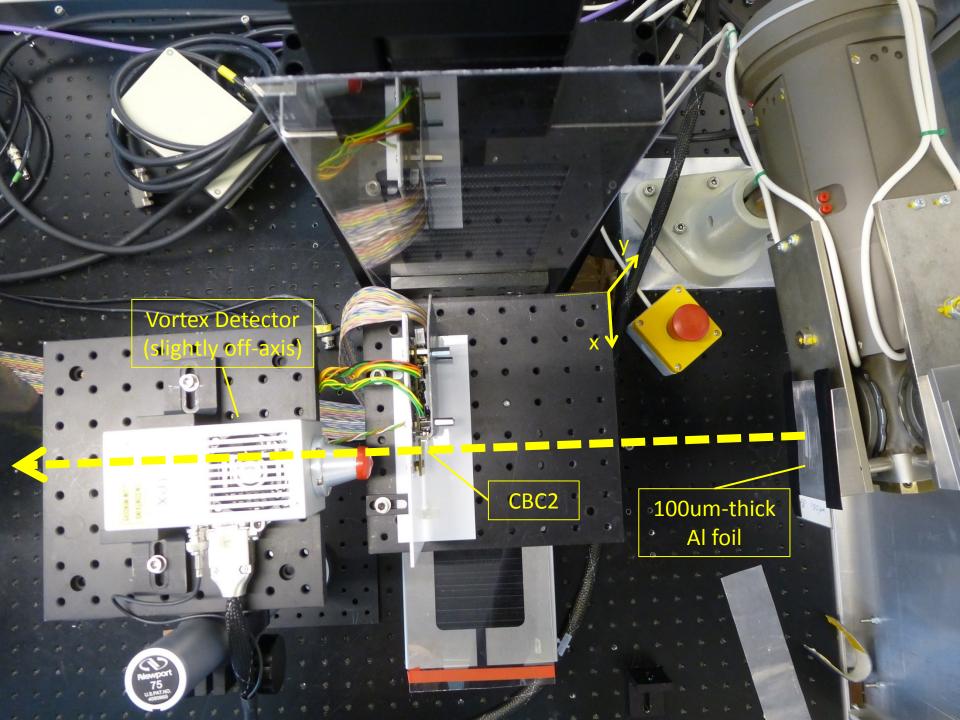




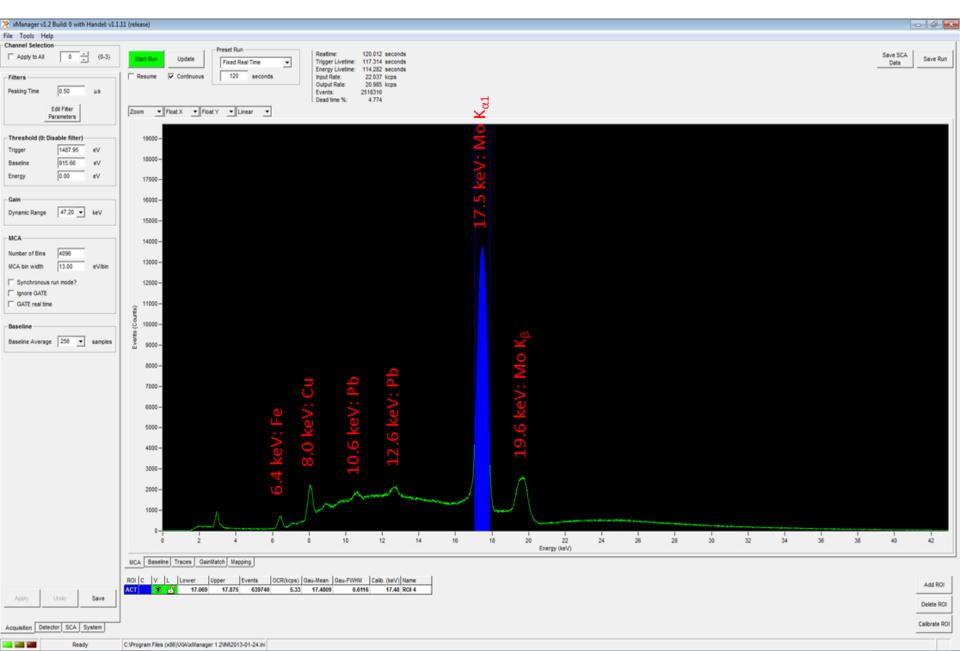


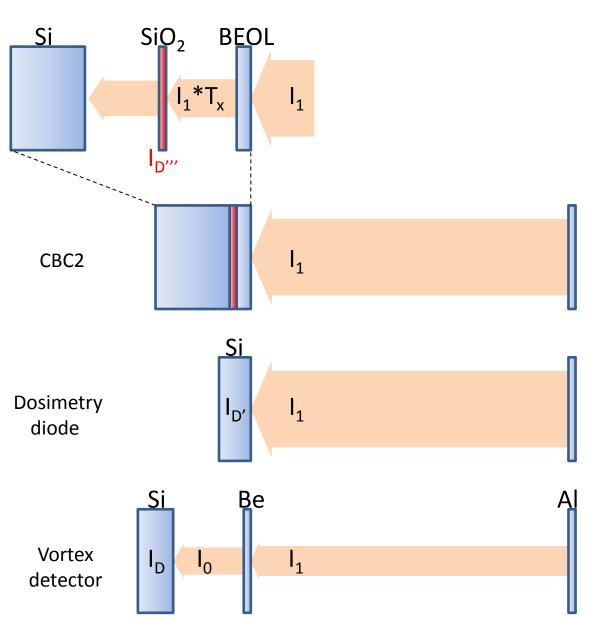
- 1. Dosimetry diode in place of CBC2
- 2. Test-set up
- 3. Spectrometer (Si-drift)





Measured Spectrum



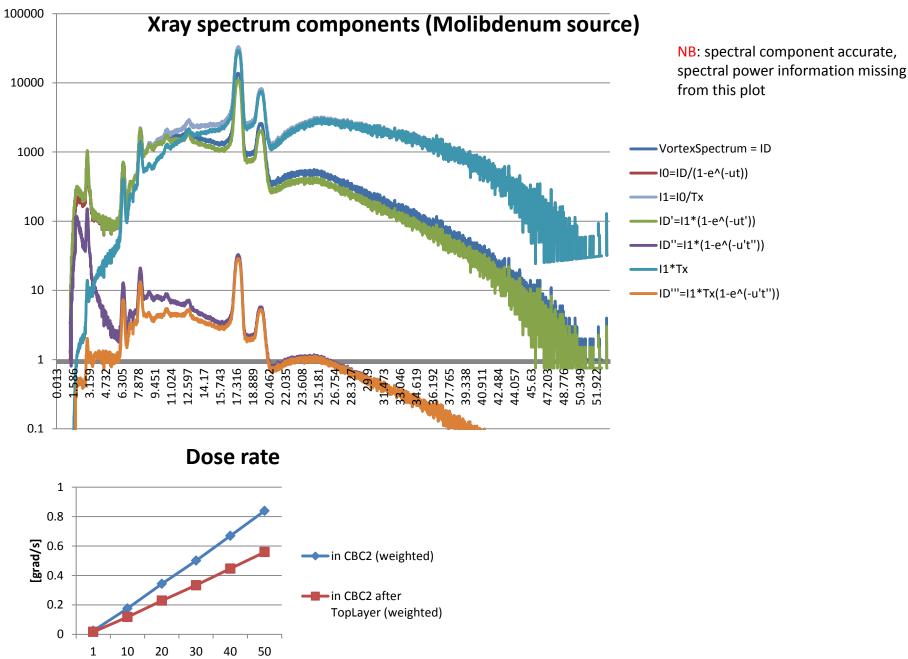


Radiation measured in Vortex sensor I_{D} $\rightarrow \text{Incident radiation (before Si sensor)}$ $I_{0}=I_{D}/(1-e^{(-\mu t)})$ Linear attenuation coefficient $\rightarrow \text{ Incident radiation (before Be window)}$ $I_{1}=I_{0}/T_{x}$ $\rightarrow \text{ Radiation measured in dosimetry diode}$ $I_{D'}=I_{1}*(1-e^{(-\mu t')})$ $\rightarrow \text{ Incident radiation after CBC2 top layer}$ $I_{1}*T_{x}$ $\rightarrow \text{ Radiation stopping in CBC2 oxide}$ $I_{D'''}=I_{1}*T_{x}(1-e^{(-\mu't'')})$

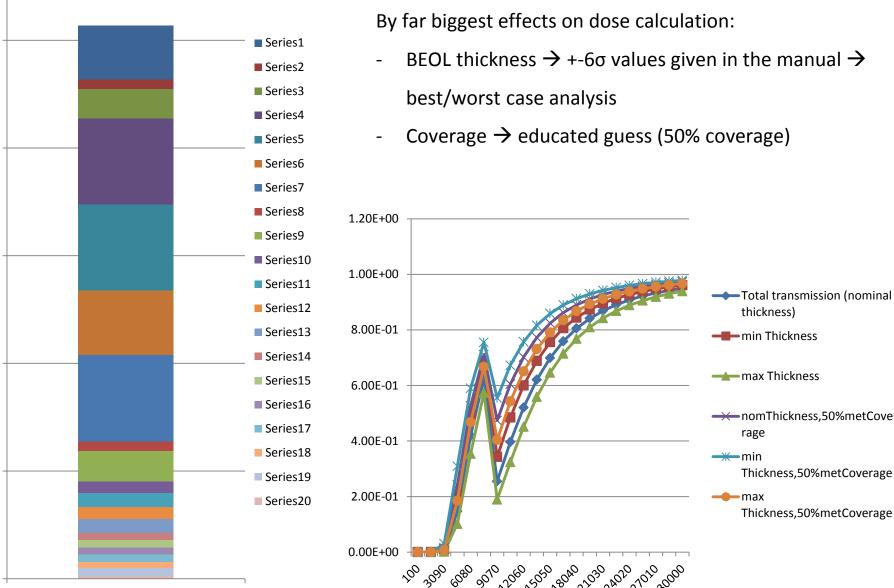
NB: this in terms of spectrum (not yet spectral power)

NB: all calculations done over 4096 photon energy slices (13eV sampling)

- diodeCurrent→Energy deposited in diode [J/s]
- spectralPowerl_{D'}, $I_{D''} \rightarrow$ Energy deposited in CBC2
- Sensitive volume mass diode & CBC2 → dose rate [Rad/h]
- IrradiationLog → integratedDose [Rad]



Xray tube current [uA]



process cross-section

§15

Sources of Error

Numbers!

TID: 10358400 rads in 1µm-thick CBC2 gate/field oxide

(compare to 15542000 rads in top 1 μ m of CBC2

or

12348000 rads in top 50µm of CBC2

or

7542100 rads in total 737µm of CBC2)

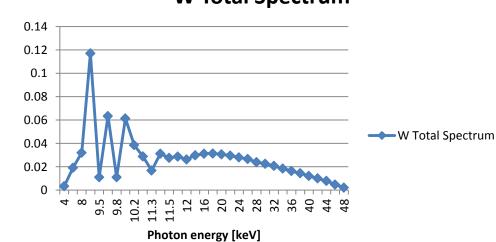
		epi thickness										
		MIN		nom		MAX						
		surface	after epi	surface	after epi	surface	after epi				TOT uncerta	inties
	253		11161245.11	15997690.23	10662167.72		10207192.72	r	nax	1.07750267		8%
	263		10843298.83	15541969.92	10358438.47		9916424.179	r	nin	0.931241237		, -7%
diode thickness	273		10547822.69	15118456.62	10076174.61		9646205.054				/	
								r	nax	1.029321914		3%
								r	nin	0.972750346		-3%

well within +-10%

(remember these are $+-6\sigma$ limits!)

Tungsten tube

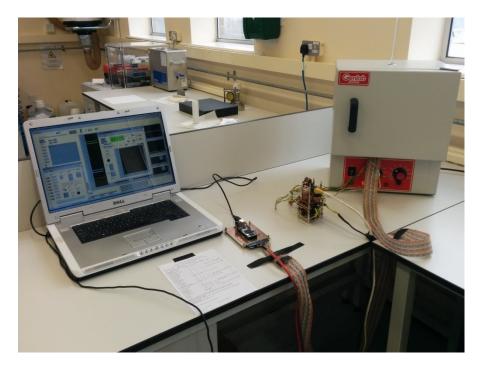
- Same calculation done with W spectrum (from literature) to cross-check with APV irradiation
- Unfortunately no indication of spectral power, so cannot compare dose (W-tube have higher efficiency (output power) so cannot assume same spectral power than Moly tube)
- Plans to use W-tube in the future



W Total Spectrum

Operation during irradiation

- CBC2 continuously operated during irradiation and annealing
- Initial room temperature annealing followed by accelerated annealing @ 100C (~6 days)
- Ibias, offsets, temperature and currents (total+ analogue switched off), S-curves constantly monitored
- Data analysis still ongoing, for now focused on the increase in current → after annealing current back to baseline with no measurable difference to starting value



Effects of TID

Main effects of TID:

- charge trapped in gate oxide → threshold shift (small/moderate in 130nm process, peaks at a few MRads for nmos)
- Charge trapped in the STI oxide

ightarrow parasitic lateral transistors ightarrow increase in Ileak, especially for narrow channel devices

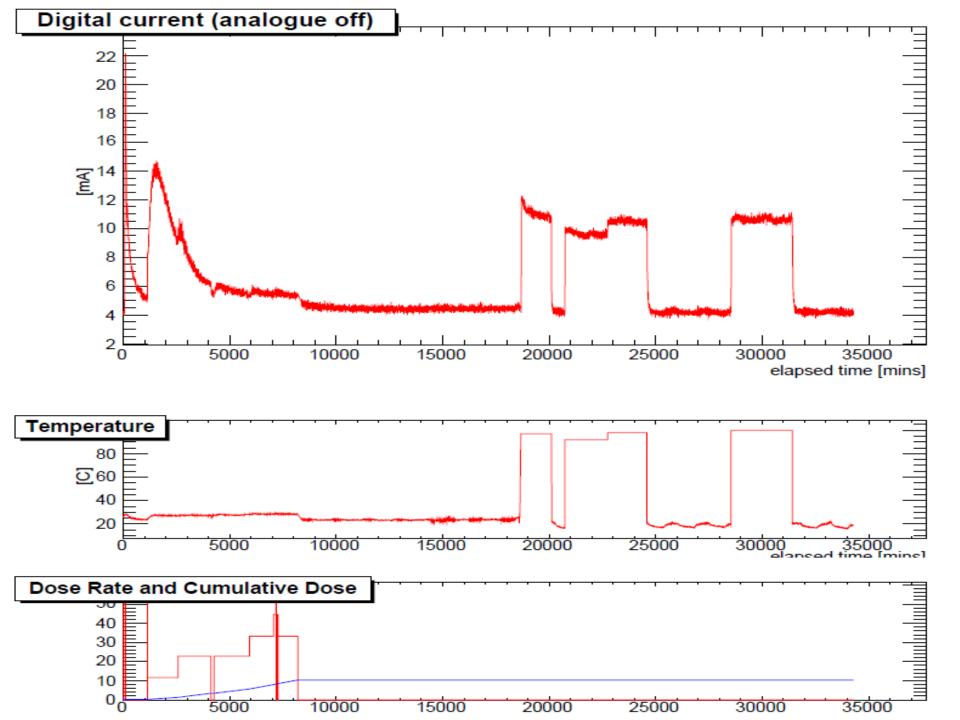
 \rightarrow parasitic FOXFETs and leakage paths between adjacent diffusions and wells (especially for closely spaced devices)

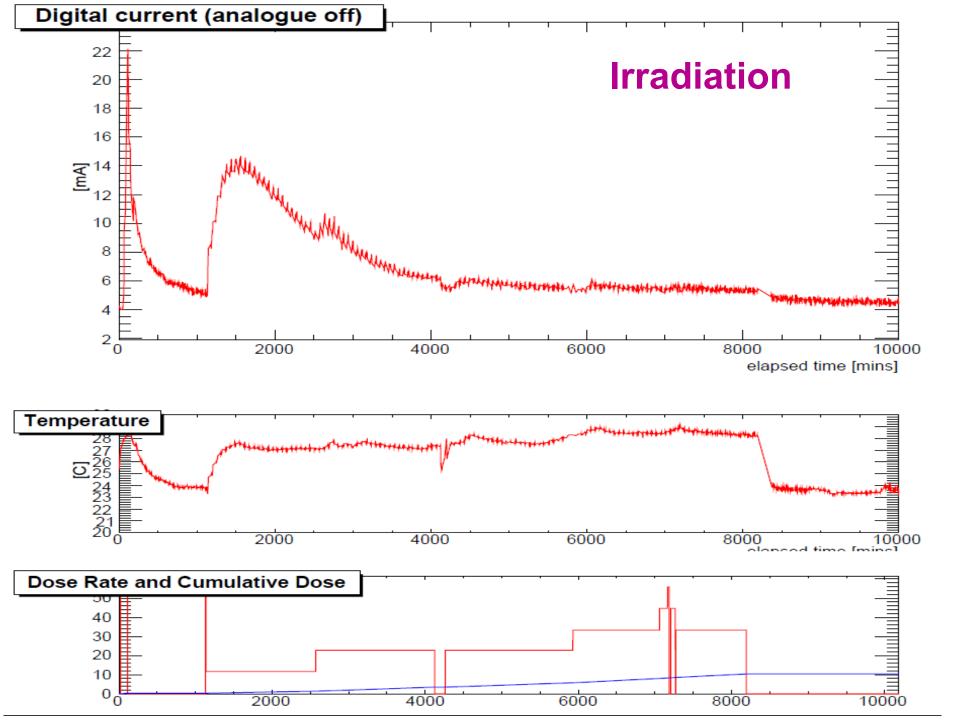
• Effect of Ileak could be significant in SRAM:

76K transistor

minimum-size access transistors

diffusions and wells at different potentials closely spaced

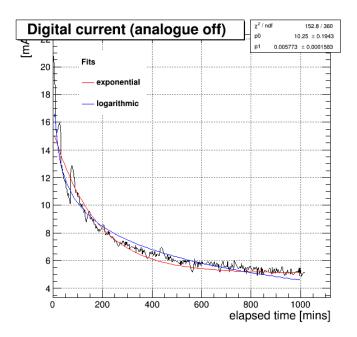




Remarks

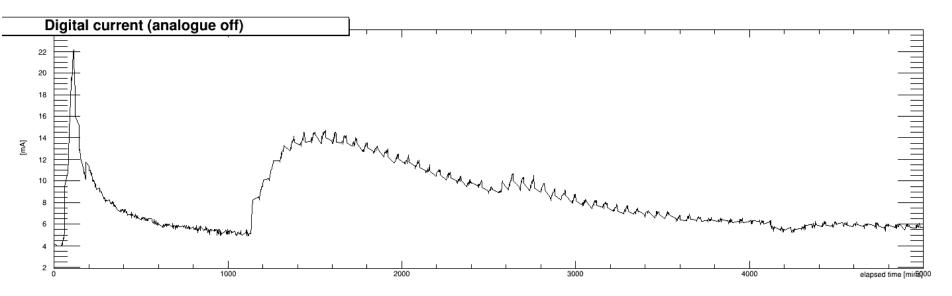
- Remember we are operating the chip at >300 times the expected dose rate at HL-LHC!
- → Fast transients are no real concern but interesting per se and to prevent initial spikes in next irradiation

Tried to study the behaviour behind dose rate/recovery



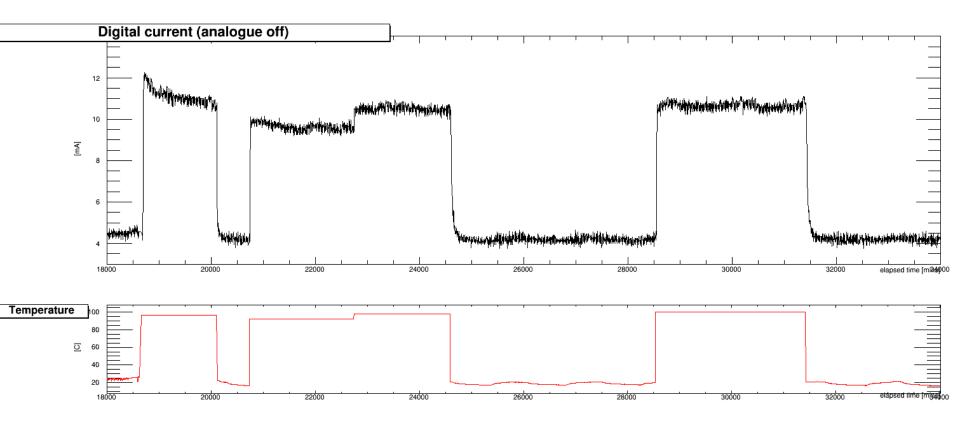
 \rightarrow Will need more points to verify either model

Effect of chip operation on current



- Evident 1-hour structure corresponding to the cycle of operations of the chip
- There seems to be a recovery in the response after threshold tuning (once an hour)
- This could be due to:
 - Digital: change in bias of SRAM buffer due to registering of many frames during threshold tuning
 - Analogue: effect of test pulse on readout channel
 - Others?
- Difficult to know before we pinpoint the source of the extra current \rightarrow to be studied in next test

Annealing

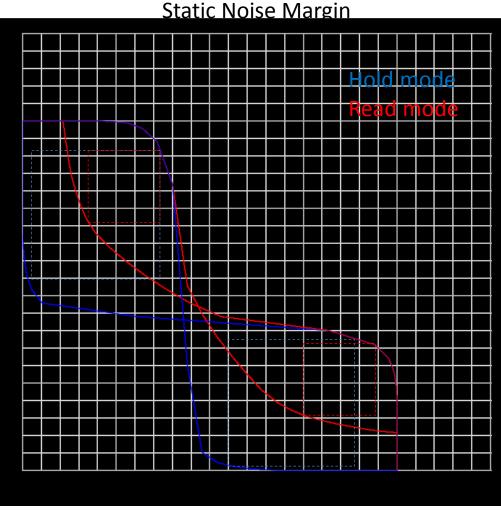


- Strong function of temperature
- Differences due to temperature (oven stable but tricky to set precisely)
- Complete recovery to baseline \rightarrow no measurable difference wrt initial value

Conclusions and Future plans

- Irradiation to 10Mrad showed only a moderate increase in current which recovers completely after standard annealing
- Flexible, portable test setup working well, useful for future SEU study too
- Source of extra current not yet identified
- Irradiation to high-dose (>50Mrads) with W-tube (RAL)
- New board (M.Raymond) to measure independently digital and analogue currents
- New set-up (M.R.) to run the chip cool (~-10C)
- Investigate effect of chip operation on dose response & current increase vs. dose rate
- \rightarrow several low-dose (<1Mrad) irradiations

SRAM post-irradiation Static Noise Margin Simulation



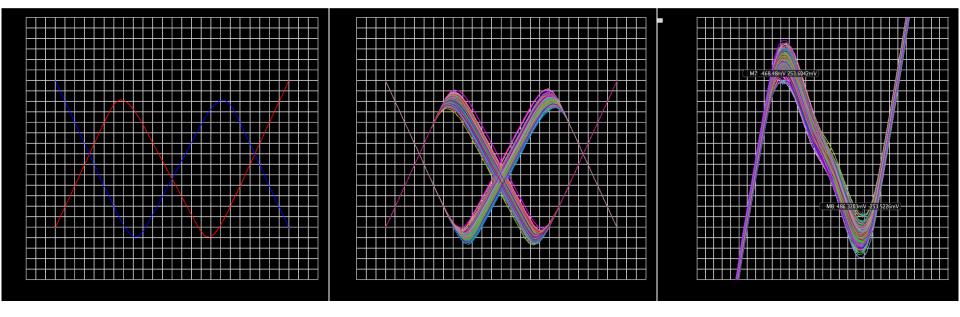
Vin vs Vout

Butterfly plots for hold and read modes

The **static noise** between the two inverters of a SRAM cell is a dc perturbance caused by offsets and process mismatch, it is therefore the ideal parameter to account for the radiationinduced transistor threshold shifts when investigating the operation of the SRAM under irradiation.

The **Static Noise Margin** (**SNM**) is defined as the maximum value of dc-offset between the two nodes in the SRAM cell before the cell flips status.

The standard way to visualize the SNM is to plot the so-called **butterfly plot**, which plots the DC transfer function of the two inverters in the SRAM cell [fig]. The SNM is defined as the length of the side of the biggest square that can fit in the eyes of the butterfly plot. Write, read and hold modes have different SNM: the content of the cell is more easily perturbed during the read operation, as shown in [fig], therefore only the read SNM is considered since this failure analysis is pertained only with the worst case scenario.



Seevinck et al. [Seevinck] describe a convenient way to investigate the SNM from circuit simulation and to plot the butterfly curves on a transpose plane where the SNM can easily be calculated. [Fig] shows such butterfly plot where the eyes are still clearly visible: the SNM can in this case be calculated by simply finding the maximum and minimum points of the difference between the two curves [fig. c], and multiply the smaller of the two by 1/sqrt(2) to find the length of the side of the square.

When transistor mismatches are included in the simulation [fig. b], the SNM is reduced, so it is important to account for such effect when assessing the robustness of the design.

