# CBC2 SEU test

Mark Pesaresi, Mark Raymond, Kirika Uchida
Imperial College London

Juan Cabrera, Christophe Delaere, Jérôme de Favereau
Universite Catholique de Louvain

# Testing overview

- Goal

  Empirical estimation of SEU rate of CBC2 at HL-LHC.

- Method

  The rate estimation using SEU rate of CBC2 in a proton beam line.

  - A beamtest at UCLouvain on $8^{th}$ & $9^{th}$ in Sep. 2014
  - Participants

    Juan Cabrera, Christophe Delaere, Jérôme de Favereau, Mark Pesaresi, Mark Raymond, Kirika Uchida

# Knowledge database and estimated error rate

- ✓ Particle flux at r∼60 cm for HL-LHC

  $\Phi_{HL\text{-}LHC}$ **=1x10$^{7}$ cm$^{-2}$s$^{-1}$**
- ✓ Maximum proton flux at LIF

  $\Phi_{LIF}$ **=5x10$^{8}$ cm$^{-2}$s$^{-1}$ (50 times the HL-LHC)**
- ✓ SEU cross section of ABCD

  $\sigma$**=5x10$^{-13}$ cm$^{2}$/cell for pipeline SEUs**

- ➢ ***# of SEU on 1 cells in the CBC2 pipeline in 1 hour of LIF proton beam (50 hours at r∼60 cm for HL-LHC )***

  60 x 60 x $\Phi_{LIF}$ x $\sigma$
  ∼10$^{12}$ cm$^{-2}$ x 10$^{-10}$cm$^{2}$
  ∼1 SEUs in pipeline?

**FLUKA estimation**

https://cms-project-fluka-flux-map.web.cern.ch/

***L*=5x10$^{34}$ cm$^{-2}$s$^{-1}$**

***CMS_pp_7TeV_v3.0.0.0_FLUKA,***

***r=60cm, z=260cm,***

| | |
|---|---|
| $\Phi_{HL\text{-}LHC}^{charged\ pion}$ | **=1.8x10$^{6}$ cm$^{-2}$s$^{-1}$** |
| $\Phi_{HL\text{-}LHC}^{p}$ | **=4.8x10$^{5}$ cm$^{-2}$s$^{-1}$** |
| $\Phi_{HL\text{-}LHC}^{n(>20MeV)}$ | **=9.5x10$^{5}$ cm$^{-2}$s$^{-1}$** |
| $\Phi_{HL\text{-}LHC}^{n}$ | **=2.0x10$^{7}$ cm$^{-2}$s$^{-1}$** |
| $\Phi_{HL\text{-}LHC}^{Hadron(>20MeV)}$ | **=3.4x10$^{6}$ cm$^{-2}$s$^{-1}$** |

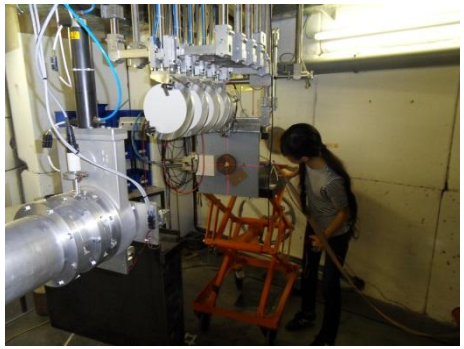
The SEU contribution from 2-20 GeV and thermal neutrons is one order smaller than hadrons with more than 20 MeV. Hadrons with more than 20 MeV has similar of cross sections except for some high energy range. (Computational method to estimate Single Event Upset rates in an accelerator environment, M. Huhtinen, F.Faccio, NIM A 450(2000)155-172)

SEU cross section for proton at 60 MeV would give rough estimate of SEU rate at HL-LHC

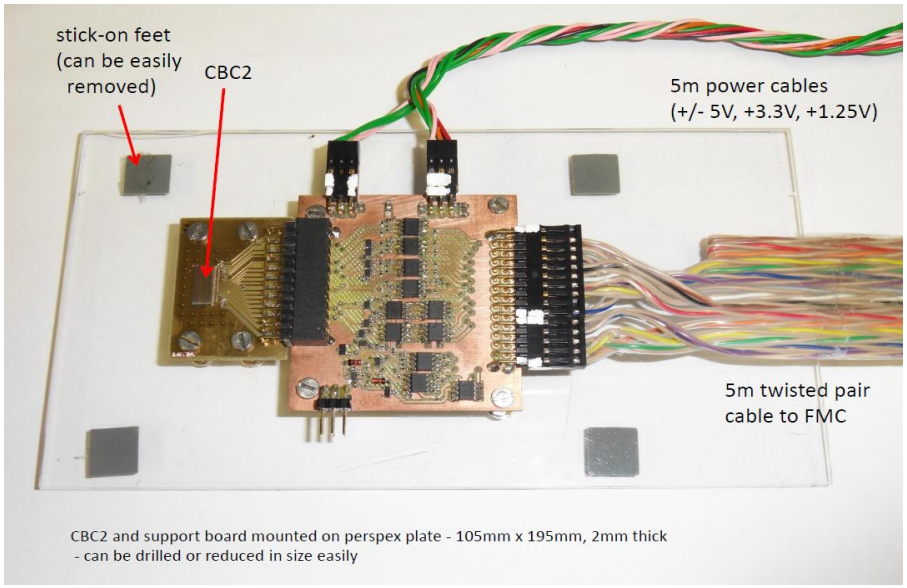
# Beamtest setup

- **Beam : Proton Cyclotron of Light Ion Irradiation Facility (LiF) at UC Louvain.**

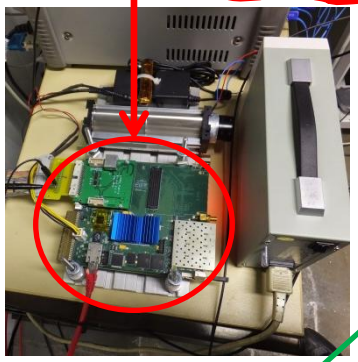
| Property | Value |
|---|---|
| Energy | Up to 62 MeV |
| Max Flux | $5x10^8$ p $cm^{-2}s^{-1}$ |
| Homogeneity | 10% |
| Spot size | 8cm |

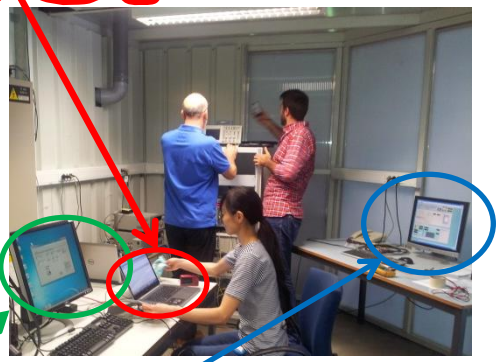


- **CBC2 module setup : 1 CBC2**




- **Error monitoring :**
  **1 BE GLIB (Modified firmware)**
  **& CbcTest software**



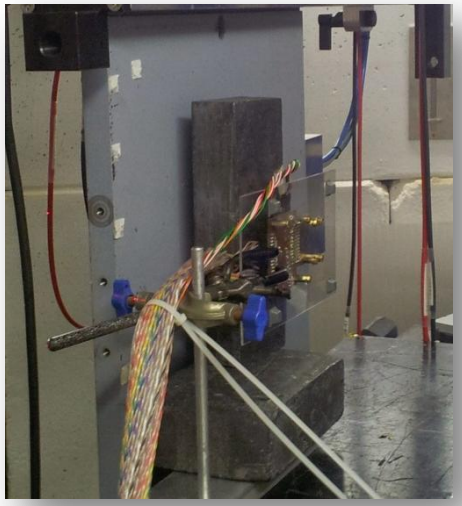


- **CBC current and beam monitoring system**
  **Thanks to Christophe and his colleagues**

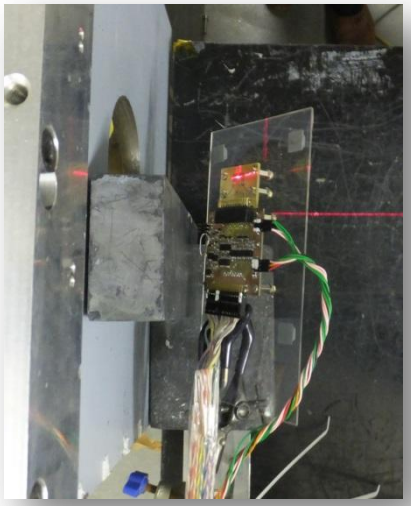
# Other conditions

- CBC was placed in 45 degree angled in Day2.

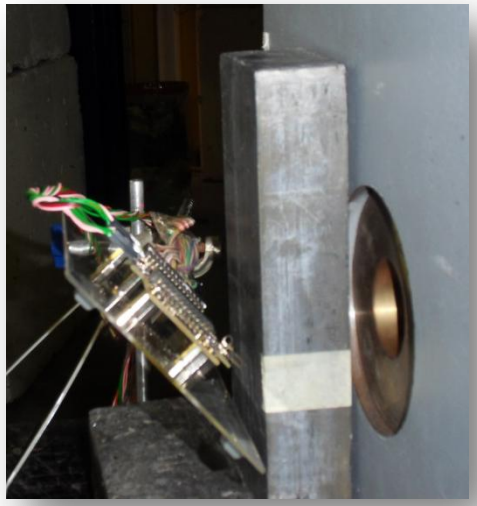
**Day 1**



**Day 2**



**Top view**



**Side view**

# Three types of SEU test for different components

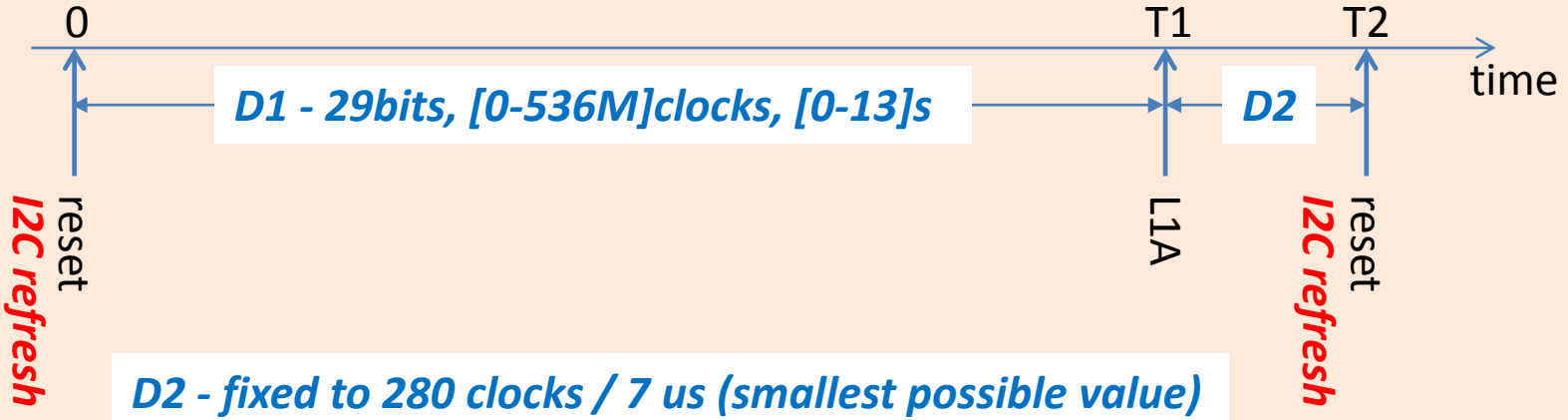
- Test 1: I2C registers
- Test 2: Pipeline logic
- Test 3: Pipeline cells

# Test 1 for I2C registers

***Procedure in the software***

- Send ***Hard reset***,
- I2C register setting,
- wait for N mins
  ***I2C refresh signals*** are sent periodically from software(~1ms pulse) or firmware loop(25ns pulse) as shown below for some runs,
- I2C register reading and recording the number of flipped bits.

***Loop in the firmware – modified commissioning mode to send short 25ns I2C refresh pulse***

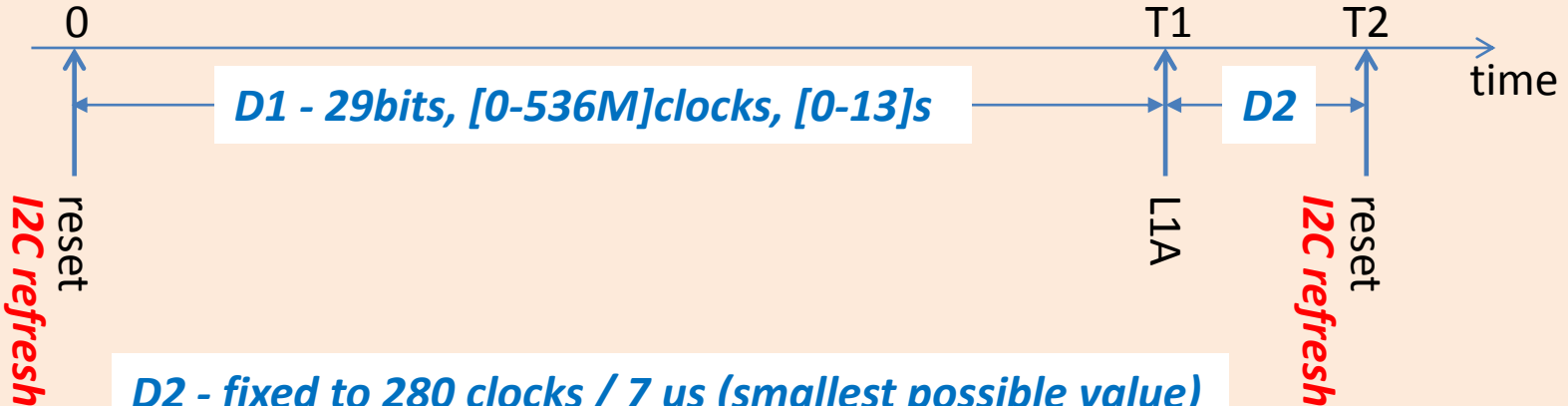


# Test 2 for pipeline logic

***Procedure in the software***

- Waiting 1 event data from the commissioning loop,
- acquisition of the data and recording and analysing the data,
- send ***hard reset*** if errors are detected.

***Loop in the firmware – modified commissioning mode to send short 25ns I2C refresh pulse***

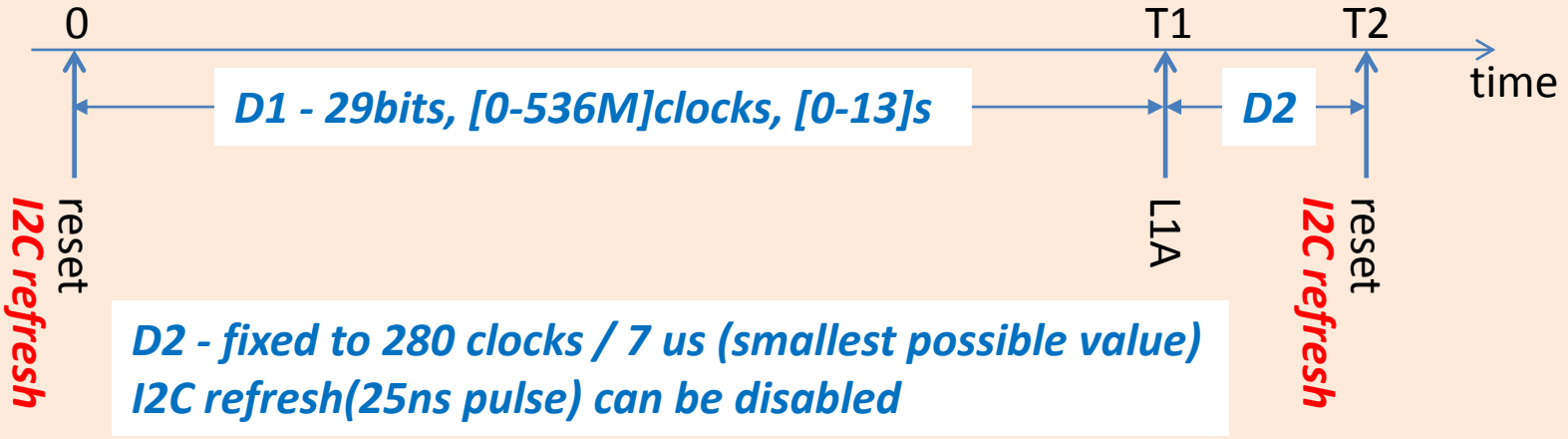


# Test 3 for pipeline registers

***Procedure in the software***

- Waiting 1 event data from the commissioning loop,
- acquisition of the data and monitoring of the number of flipped channel bits,
- send ***hard reset*** if errors are detected.

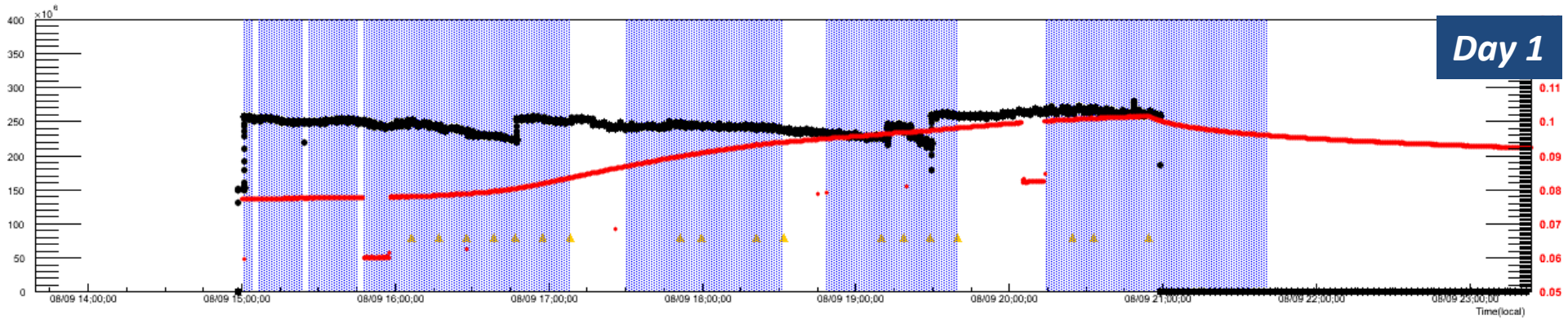
***Loop in the firmware – modified commissioning mode to send short 25ns I2C refresh pulse***

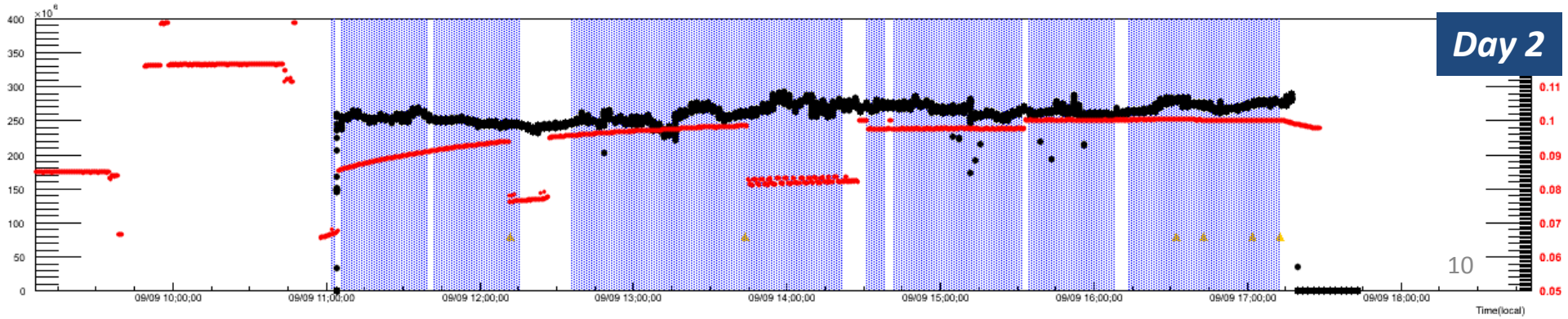



***Stop CBC clock after 40 clocks from the reset to 2 clock before L1A to store an event data in the pipeline for long D1 period. Trigger latency in CBC is set to 5 clocks.***

# LIF proton flux & CBC2 current vs. Time

- LIF proton flux in black, CBC2 current in red, filled area are the run periods, error timings are in orange triangles.
- LIF proton flux ~ 2.55±0.14x$10^{8}$ p $cm^{-2}s^{-1}$ with the energy 62.0 MeV where *LET* = 8.39 MeV$cm^{2}$/mg.
- Total fluence : 1.1x$10^{13}$$cm^{-2}$
- Total radiation : Total fluence x *LET* = 1.5 MRad. <- large?
- CBC2 current drop seems to be correlated with hard reset. (Not always?)



# Test1 (I2C register test) result

***CBC2 is tilted by 45 degree in day2***

| | Beam | SEU | | | T sec | N read | I2C refresh Hz | Hard reset |
|---|---|---|---|---|---|---|---|---|
| | | Total | 0->1 | 1->0 | | | | |
| Day1Run1 | ON | 0 | 0 | 0 | 10 | 20 | Disabled | Enabled |
| Day1Run4 | ON | 16 | 5 | 11 | 600 | 7 | Disabled | Enabled |
| Day1Run6 | ON | 6 | 1 | 5 | 600 | 7 | 1(*) | Enabled |
| Day1Run8 | ON | 10 | 6 | 4 | 600 | 6 | 10(*) | Enabled |
| Day1Run9A | ON | 26 | 5 | 21 | 600 | 4 | 10 | Enabled |
| Day1Run9B | OFF | 0 | 0 | 0 | 600 | 3 | 10 | Enabled |
| Day2Run12 | ON | 20 | 4 | 16 | 600 | 6 | Disabled | Disabled |
| Total | | 78 | 21 | 57 | | | | |

- (*) : I2C refresh is controlled from software. The pulse length sent to CBC2 is ~1ms.
- I2C refresh is enabled and frequency is raised from Day1Run6 to Day1Run8 by factor 10, but the result does not show a better performance.
- The long pulse length was suspected to be causing the problem, so firmware commissioning loop is enabled which creates 25ns I2C refresh pulse. But result shows no improvement.
- In Day2, hard reset seems to be causing a problem in Trigger Latency in CBC sometimes, so hard reset is turned off for Day2Run12.

# Test2(Pipeline logic test) result

***CBC2 is tilted by 45 degree in day2***

| | Beam | SEU | t /loop sec | Total live time sec | I2C Refresh | Hard reset after an Error |
|---|---|---|---|---|---|---|
| Day1Run2 | ON | 0 | 1 | 1120 | Enabled | Enabled |
| Day1Run3 | ON | 0 | 1 | 1099 | Enabled | Enabled |
| Day2Run3 | ON | 0 | 1 | 2149 | Enabled | Enabled |
| Day2Run4 | ON | 1? | 10 | 1750 | Enabled | Enabled |
| Day2Run8 | ON | 1? | 0.1 | 4136 | Enabled | Enabled |
| Day2Run11 | ON | 1? | 1 | 1937 | Enabled | Disabled |

- ✓ Day2Run11 has an event with all channel 1 instead of 0 (VCTH is set so that no channel is fired.)
- ✓ Day2Run4 and Day2Run8 had different pipeline address than expected from the loop but CBC does not recognise as an error -> *error source is not unidentified*.

  After those errors, the pipeline address stays at a certain position which is also not expected value. The wrong address was found out to be the one calculated from the default latency(0xC8). Hard reset after the error seems to be causing the problem even though there is no error in write and read I2C register values after the reset.

  (Before Day2Run2, there was the default latency pipeline address problem from the beginning. Hard reset was done manually and the system recovered for Run3.)

- ❖ Total live time = $1.2 \times 10^4$sec -> 83 hour @HL-HLC

  ->***SEU(might be related to pipeline logic) rate per chip at HL-LHC = [3.6 ±2.0] x $10^{-2}$ (3/83) hour$^{-1}$***

# Test3(Pipeline cell test) result

***CBC2 is tilted by 45 degree in day2***

| | Beam | SEU | t /loop sec | Total live time sec | Refresh | Hard reset after an Error |
|---|---|---|---|---|---|---|
| Day2Run10 | ON | 0 | 10 | 3110 | Enabled | Enabled |

Corresponds to 22 hours @HL-LHC but the test is done for only 1 out of 256 pipeline cell.
SEU rate upper limit $r_0$ on one cell at 90% CL : $r_0 = -1 / 22 \times \ln(0.1) \rightarrow r_0 = 0.10$
***-> SEU rate on pipeline cells per chip at HL-LHC upper limit $R_0 = 27\ hour^{-1}$ (CL=90%)***

# Test 1 Analysis

SEU on I2C registers

# Measured SEU cross section on I2C registers

- 3 state voting scheme is used in each bit of I2C registers.
  At least 2 out of 3 cells have to have SEU to flip the bit.

| Symbol | Description |
|---|---|
| $\sigma$ | SEU cross section per cell [$cm^2$/cell] |
| r | SEU rate per cell [$cell^{-1}sec^{-1}$] |
| $\Phi$ | Proton beam flux [$cm^{-2}sec^{-1}$] |
| $P(T_0)$ | probability to flip two cells out of 3 in time window $T_0$ sec [$bit^{-1}$] |
| $N^{bit}$ | # of I2C register bits in a chip |
| $N^{read}$ | # of register read in the run |
| $N^{SEU}$ | # of I2C register bits flipped in the run |

The probability of two cell flips out of three cells in time $T_0$ is

$$P(T_0) = {}_3C_2 \int_0^{T_0} r dt_1 \int_0^{T_0} r dt_2 = 3r^2 \int_0^{T_0} dt_1 \int_0^{T_0} dt_2 = 3r^2 T_0^2$$

where $r$ is the rate of a flip on a cell and $rT_0 << 1$ is assumed.

The probability of a flip on a cell at time $t_1$ for $dt_1$ and a flip on another cell at time $t_2$ for $dt_2$ are integrated over $t_1$ and $t_2$ from 0 to $T_0$, and multiplied by the combination of two cells out of three.

$N^{SEU} = N^{bit} \times P(T_0) \times N^{read}$
where $P(T_0) = 3r^2T_0^2$

→ $\sigma = r/\Phi$

*Correlation between cells is not taken into account*

# Measured SEU cross section on I2C registers

*r & σ calculation without taking into account the refresh.*

*CBC2 is tilted by 45 degree in day2*

**SEU 0->1 ($N^{bit}$ = 1208)**

| Run | $T_0$ | $N^{read}$ | $N^{SEU}$ | I2C refresh Hz | $\Phi$ $10^8$ cm$^{-2}$ | r | $\sigma$ |
|---|---|---|---|---|---|---|---|
| Day1Run4 | 600 | 7 | 5 | Disabled | 2.44±0.09 | [2.3±0.5]x10$^{-5}$ | [9.4±2.1]x10$^{-14}$ |
| Day1Run6 | 600 | 7 | 1 | 1(*) | 2.42±0.03 | [1.0±0.5]x10$^{-5}$ | [4.2±2.1]x10$^{-14}$ |
| Day1Run8 | 600 | 6 | 6 | 10(*) | 2.39±0.14 | [2.8±0.6]x10$^{-5}$ | [1.1±0.2]x10$^{-13}$ |
| Day1Run9A | 600 | 4 | 5 | 10 | 2.64±0.01 | [3.1±0.7]x10$^{-5}$ | [1.2±0.3]x10$^{-13}$ |
| Day2Run12 | 600 | 6 | 4 | Disabled | 2.57±0.61 | [2.3±0.6]x10$^{-5}$ | [9.1±2.3]x10$^{-14}$ |

**Average of Day1Run4 & Day2Run12 : $\sigma$=[9.2±1.6]x10$^{-14}$**

**SEU 1->0 ($N^{bit}$ = 1248)**

| Run | $T_0$ | $N^{read}$ | $N^{SEU}$ | I2C refresh Hz | $\Phi$ $10^8$ cm$^{-2}$ | r | $\sigma$ |
|---|---|---|---|---|---|---|---|
| Day1Run4 | 600 | 7 | 11 | Disabled | 2.44±0.09 | [3.4±0.5]x10$^{-5}$ | [1.4±0.2]x10$^{-13}$ |
| Day1Run6 | 600 | 7 | 5 | 1(*) | 2.42±0.03 | [2.3±0.5]x10$^{-5}$ | [9.2±2.1]x10$^{-14}$ |
| Day1Run8 | 600 | 6 | 4 | 10(*) | 2.39±0.14 | [2.2±0.6]x10$^{-5}$ | [8.9±2.2]x10$^{-14}$ |
| Day1Run9A | 600 | 4 | 21 | 10 | 2.64±0.01 | [6.2±0.7]x10$^{-5}$ | [2.5±0.3]x10$^{-13}$ |
| Day2Run12 | 600 | 6 | 16 | Disabled | 2.57±0.61 | [4.4±0.6]x10$^{-5}$ | [1.8±0.2]x10$^{-13}$ |

**Average of Day1Run4 & Day2Run12 : $\sigma$=[1.6±0.1]x10$^{-13}$**

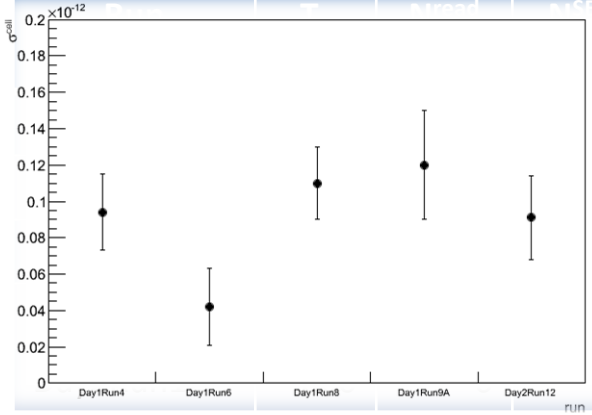
***It seems like that the refresh is not working properly and not reducing the SEU effect well. Higher frequency, shorter refresh pulse does not help.***

# Measured SEU cross section on I2C registers

***r & σ calculation without taking into account the refresh.***

***CBC2 is tilted by 45 degree in day2***

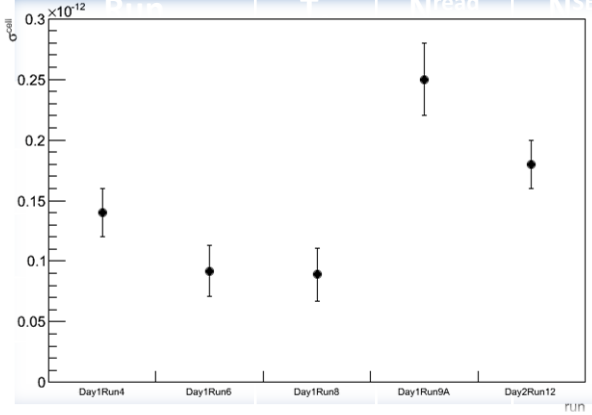
**SEU 0->1 ($N^{bit}$ = 1208)**




| I2C refresh Hz | Φ $10^8$ cm$^{-2}$ | r | σ |
|---|---|---|---|
| Disabled | 2.44±0.09 | [2.3±0.5]x10$^{-5}$ | [9.4±2.1]x10$^{-14}$ |
| 1(*) | 2.42±0.03 | [1.0±0.5]x10$^{-5}$ | [4.2±2.1]x10$^{-14}$ |
| 10(*) | 2.39±0.14 | [2.8±0.6]x10$^{-5}$ | [1.1±0.2]x10$^{-13}$ |
| 10 | 2.64±0.01 | [3.1±0.7]x10$^{-5}$ | [1.2±0.3]x10$^{-13}$ |
| Disabled | 2.57±0.61 | [2.3±0.6]x10$^{-5}$ | [9.1±2.3]x10$^{-14}$ |

**Average of Day1Run4 & Day2Run12 : σ=[9.2±1.6]x10$^{-14}$**

**SEU 1->0 ($N^{bit}$ = 1248)**




| I2C refresh Hz | Φ $10^8$ cm$^{-2}$ | r | σ |
|---|---|---|---|
| Disabled | 2.44±0.09 | [3.4±0.5]x10$^{-5}$ | [1.4±0.2]x10$^{-13}$ |
| 1(*) | 2.42±0.03 | [2.3±0.5]x10$^{-5}$ | [9.2±2.1]x10$^{-14}$ |
| 10(*) | 2.39±0.14 | [2.2±0.6]x10$^{-5}$ | [8.9±2.2]x10$^{-14}$ |
| 10 | 2.64±0.01 | [6.2±0.7]x10$^{-5}$ | [2.5±0.3]x10$^{-13}$ |
| Disabled | 2.57±0.61 | [4.4±0.6]x10$^{-5}$ | [1.8±0.2]x10$^{-13}$ |

**Average of Day1Run4 & Day2Run12 : σ=[1.6±0.1]x10$^{-13}$**

***It seems like that the refresh is not working properly and not reducing the SEU effect well. Higher frequency, shorter refresh pulse does not help.***

# Other problems

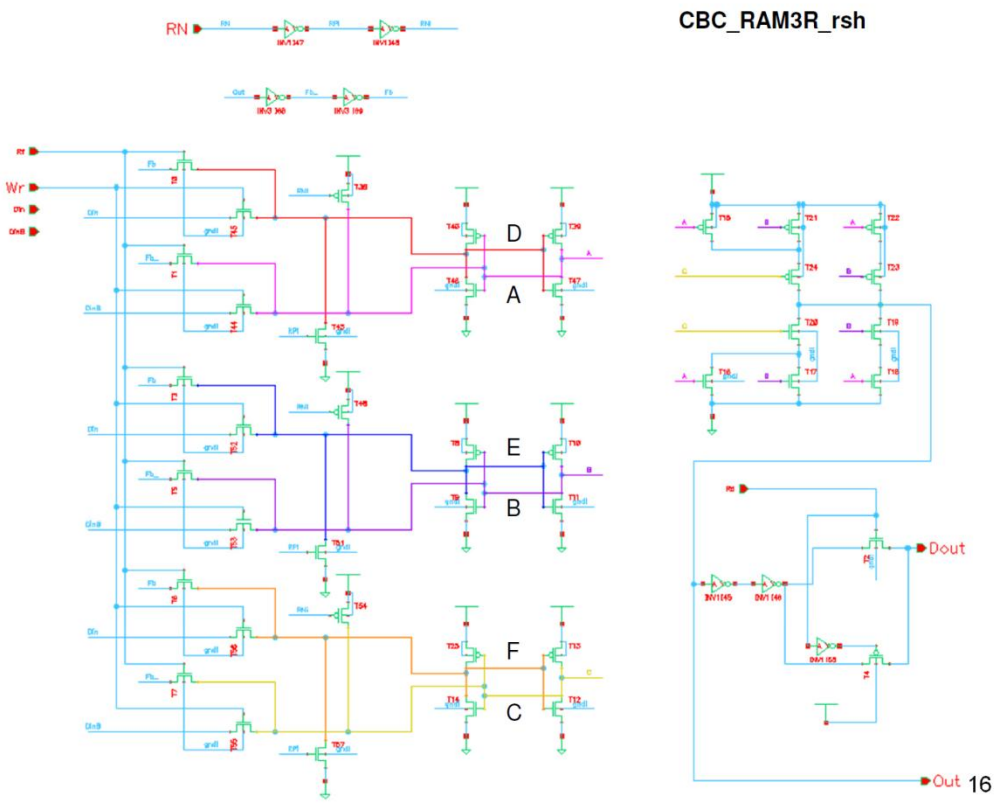
- The overall SEU rate is low, but in some SEU, some bit flips are happening in a single 8-bits register.

**Day1Run 6**

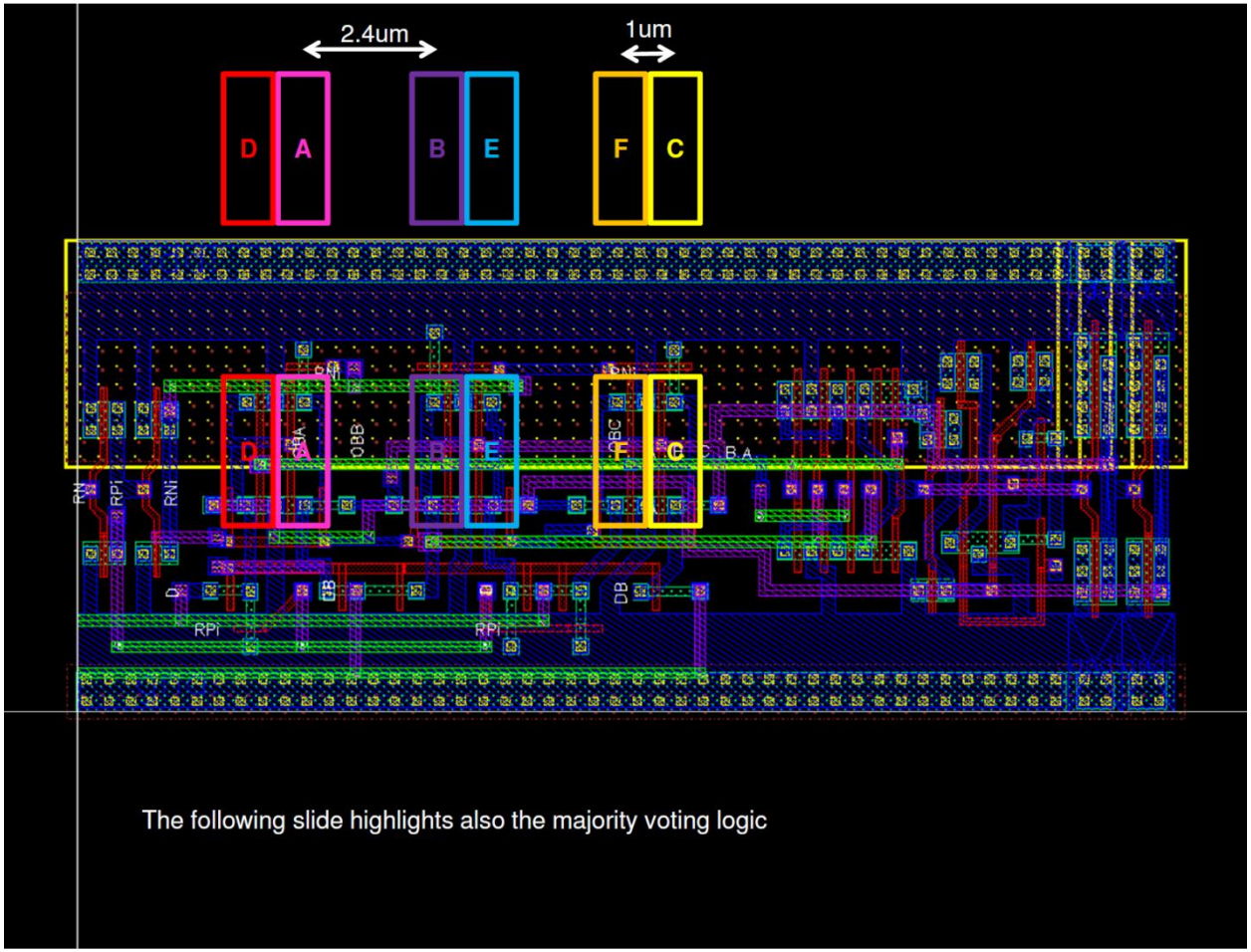
| Time | Page | Address | Written | Read | |
|---|---|---|---|---|---|
| Sep 8 19:09:24 | 1 | A9 | 0101,0111 | 1101,0111 | |
| Sep 8 19:09:24 | 1 | B1 | 0100,0110 | 0101,0101 | ! |
| Sep 8 19:09:24 | 1 | D2 | 0100,0011 | 0100,0001 | |
| Sep 8 19:19:51 | 1 | E0 | 0101,0000 | 0101,0101 | ! |
| Sep 8 19:30:19 | 1 | 6D | 0101,1100 | 0101,1000 | |
| Sep 8 19:40:45 | 0 | 45 | 0100,1100 | 0100,0101 | ! |

- Also, the triple cells for register bit are very close to each other.

# CBC I2C register bit triplicated logic



# CBC I2C register bit triplicated logic layout



# Another possibility on the measured SEU cross section on I2C registers

- Are the cells in I2C register bit too close to each other so that multiple cells flip at the same time?
- Considering that a flip on I2C register bits comes from single SEU on multiple cells, the flip rate per bit($R^{bit}$) & cross section($\sigma^{bit}$ ) are simply obtained from

$$N^{SEU} = N^{bit} \times R^{bit} \times N^{read} \times T^{0}$$

$$\sigma^{bit} = R^{bit} / \Phi$$

# Measured SEU cross section on I2C registers with the assumption of single SEU on multiple cells

*r & σ calculation without taking into account the refresh.*

*CBC2 is tilted by 45 degree in day2*

**SEU 0->1 ($N^{bit}$ = 1208)**

| Run | $T_0$ | $N^{read}$ | $N^{SEU}$ | I2C refresh Hz | $\Phi$ $10^8$ cm$^{-2}$ | $R^{bit}$ | $\sigma^{bit}$ |
|---|---|---|---|---|---|---|---|
| Day1Run4 | 600 | 7 | 5 | Disabled | 2.44±0.09 | $[9.9\pm4.4]\times10^{-7}$ | $[4.0\pm1.8]\times10^{-15}$ |
| Day1Run6 | 600 | 7 | 1 | 1(*) | 2.42±0.03 | $[2.0\pm2.0]\times10^{-7}$ | $[7.9\pm7.9]\times10^{-16}$ |
| Day1Run8 | 600 | 6 | 6 | 10(*) | 2.39±0.14 | $[1.4\pm0.6]\times10^{-6}$ | $[5.6\pm2.3]\times10^{-15}$ |
| Day1Run9A | 600 | 4 | 5 | 10 | 2.64±0.01 | $[1.7\pm0.8]\times10^{-6}$ | $[6.9\pm3.1]\times10^{-15}$ |
| Day2Run12 | 600 | 6 | 4 | Disabled | 2.57±0.61 | $[9.3\pm4.6]\times10^{-7}$ | $[3.7\pm1.9]\times10^{-15}$ |

**Average of Day1Run4 & Day2Run12 : $\sigma=[3.9\pm1.3]\times10^{-15}$**

**SEU 1->0 ($N^{bit}$ = 1248)**

| Run | $T_0$ | $N^{read}$ | $N^{SEU}$ | I2C refresh Hz | $\Phi$ $10^8$ cm$^{-2}$ | $R^{bit}$ | $\sigma^{bit}$ |
|---|---|---|---|---|---|---|---|
| Day1Run4 | 600 | 7 | 11 | Disabled | 2.44±0.09 | $[2.1\pm0.6]\times10^{-6}$ | $[8.4\pm2.5]\times10^{-15}$ |
| Day1Run6 | 600 | 7 | 5 | 1(*) | 2.42±0.03 | $[9.5\pm4.2]\times10^{-7}$ | $[3.8\pm1.7]\times10^{-15}$ |
| Day1Run8 | 600 | 6 | 4 | 10(*) | 2.39±0.14 | $[8.9\pm4.5]\times10^{-7}$ | $[3.6\pm1.8]\times10^{-15}$ |
| Day1Run9A | 600 | 4 | 21 | 10 | 2.64±0.01 | $[7.0\pm1.5]\times10^{-6}$ | $[2.8\pm0.6]\times10^{-14}$ |
| Day2Run12 | 600 | 6 | 16 | Disabled | 2.57±0.61 | $[3.6\pm0.9]\times10^{-6}$ | $[1.4\pm0.4]\times10^{-14}$ |

**Average of Day1Run4 & Day2Run12 : $\sigma=[1.1\pm0.3]\times10^{-14}$**

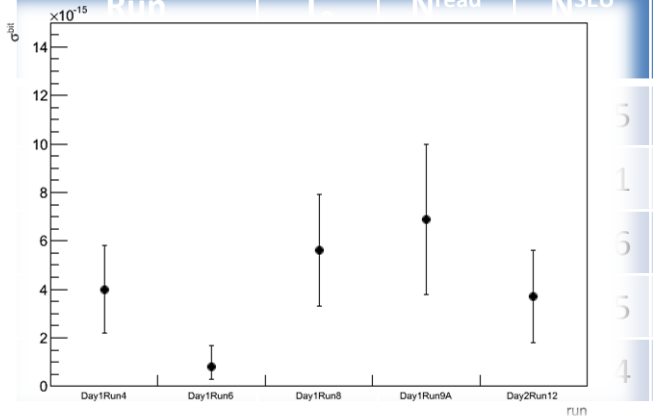
***If the multiple cells flip, refresh does not restore the initial value, so in this case, it is understandable that there is no improvement with the refresh.***

# Measured SEU cross section on I2C registers with the assumption of single SEU on multiple cells

***r & σ calculation without taking into account the refresh.***

***CBC2 is tilted by 45 degree in day2***

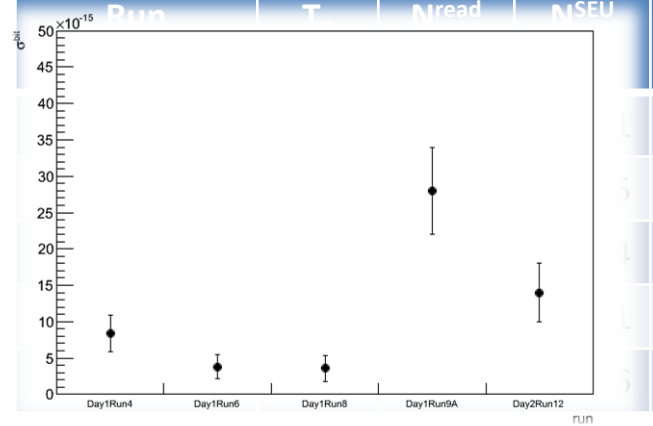
**SEU 0->1 ($N^{bit}$ = 1208)**




| I2C refresh Hz | $\Phi$ $10^8$ cm$^{-2}$ | $R^{bit}$ | $\sigma^{bit}$ |
|---|---|---|---|
| Disabled | 2.44±0.09 | [9.9±4.4]x10$^{-7}$ | [4.0±1.8]x10$^{-15}$ |
| 1(*) | 2.42±0.03 | [2.0±2.0]x10$^{-7}$ | [7.9±7.9]x10$^{-16}$ |
| 10(*) | 2.39±0.14 | [1.4±0.6]x10$^{-6}$ | [5.6±2.3]x10$^{-15}$ |
| 10 | 2.64±0.01 | [1.7±0.8]x10$^{-6}$ | [6.9±3.1]x10$^{-15}$ |
| Disabled | 2.57±0.61 | [9.3±4.6]x10$^{-7}$ | [3.7±1.9]x10$^{-15}$ |

**Average of Day1Run4 & Day2Run12 : $\sigma$=[3.9±1.3]x10$^{-15}$**

**SEU 1->0 ($N^{bit}$ = 1248)**

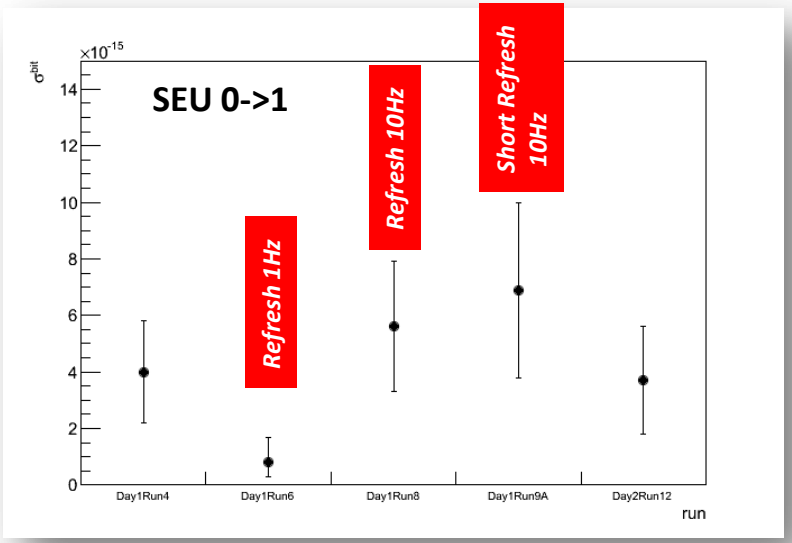


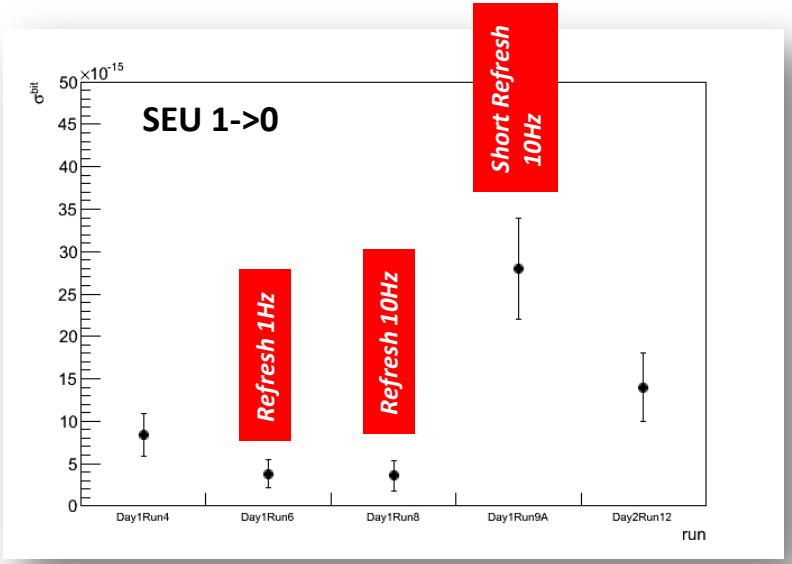

| I2C refresh Hz | $\Phi$ $10^8$ cm$^{-2}$ | $R^{bit}$ | $\sigma^{bit}$ |
|---|---|---|---|
| Disabled | 2.44±0.09 | [2.1±0.6]x10$^{-6}$ | [8.4±2.5]x10$^{-15}$ |
| 1(*) | 2.42±0.03 | [9.5±4.2]x10$^{-7}$ | [3.8±1.7]x10$^{-15}$ |
| 10(*) | 2.39±0.14 | [8.9±4.5]x10$^{-7}$ | [3.6±1.8]x10$^{-15}$ |
| 10 | 2.64±0.01 | [7.0±1.5]x10$^{-6}$ | [2.8±0.6]x10$^{-14}$ |
| Disabled | 2.57±0.61 | [3.6±0.9]x10$^{-6}$ | [1.4±0.4]x10$^{-14}$ |

**Average of Day1Run4 & Day2Run12 : $\sigma$=[1.1±0.3]x10$^{-14}$**

***If the multiple cells flip, refresh does not restore the initial value, so in this case, it is understandable that there is no improvement with the refresh.***

# Measured SEU cross section on I2C registers with the assumption of single SEU on multiple cells




- If the multiple cells flip, refresh does not restore the initial value, so in this case, it is understandable that there is not very good improvement with the refresh.
- Short refresh in Day1Run9A might not be working at all?

***There might be combination of independent SEUs on different cells, single SEU on multiple cells, and a possibility that refresh is not working properly.***

# Summary

**Estimation of SEU at HL-LHC with the assumption of $\Phi_{HL\text{-}LHC}$ =1x10$^{7}$ cm$^{-2}$s$^{-1}$**

- SEU rate per chip in pipeline logic

  ***$r_{chip}$= [3.6 ±2.0] x 10$^{-2}$ SEU/hour***

  (If we consider the all 3 errors are due to the pipeline logic. )

- SEU rate per chip in pipeline cell

  ***$r_{chip}$< 27 SEU/hour (CL=90%)***

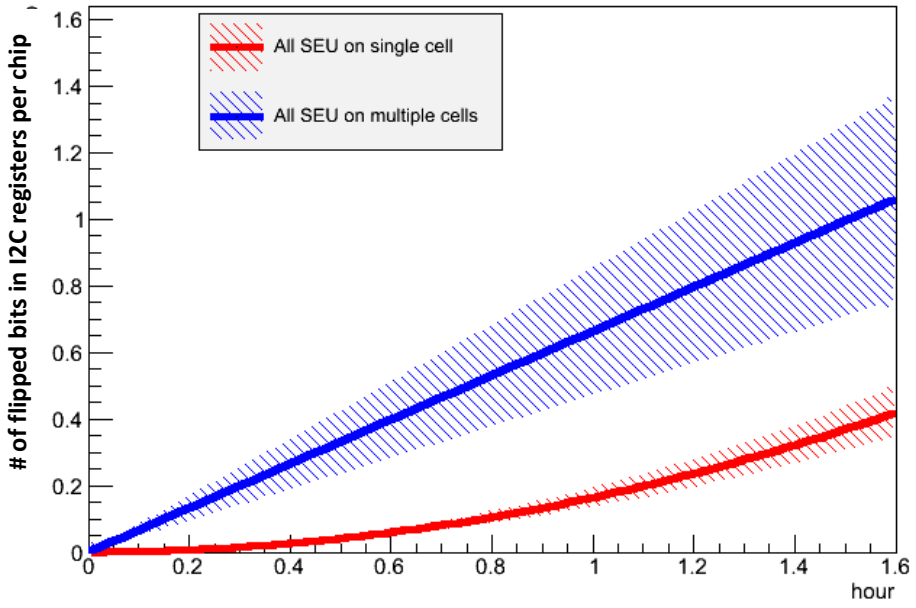
- Expected # of flipped bits in I2C register per chip without refresh using data from Day1Run4 & Day2Run12

  ***$N_{chip}$=[1.6±0.3]x10$^{-1}$ SEU in an hour***

  with the assumption that SEU happens on each cell independently.

  ***$N_{chip}$=[6.6±1.9]x10$^{-1}$ SEU per hour***

  with the assumption that SEU happens on multiple cells at the same time.




- ✓ ***Pipeline logic and pipeline cells are performing very well, considering that we could send fast reset frequently enough.***
- ✓ ***I2C registers need to be mitigated more to be stable for a single run period. (The SEU on multiple cell case still does not take into account correlations between bits. Multiple bit flips in a single register is still not understood.)***
- ✓ ***We radiated the chip up to 1.5 Mrad. This may be causing time dependent SEU rate.***

# Register changes in Test 1

# Run 4

| | Beam | SEU | T sec | N read | Refresh Hz | Hard reset |
|---|---|---|---|---|---|---|
| Day1Run4 | ON | 16 | 600 | 7 | Disabled | Enabled |

| Time | Page | Address | Written | Read | |
|---|---|---|---|---|---|
| Sep 8 16:07:38 | 1 | BF | 0101,0001 | 0101,0101 | |
| Sep 8 16:07:38 | 1 | FD | 0110,1000 | 0101,0000 | ! |
| Sep 8 16:17:38 | 0 | 01 | 0000,0101 | 0000,1101 | |
| Sep 8 16:17:38 | 1 | 70 | 0100,1110 | 0100,1100 | |
| Sep 8 16:27:38 | 1 | DF | 0100,1010 | 0100,1000 | |
| Sep 8 16:37:38 | 1 | 98 | 0110,0010 | 0110,0000 | |
| Sep 8 16:47:38 | 1 | 80 | 0101,1000 | 0101,0100 | ! |
| Sep 8 16:57:38 | 1 | 25 | 0101,1001 | 0101,0101 | ! |
| Sep 8 16:57:38 | 1 | 7B | 0101,0100 | 0100,0100 | |
| Sep 8 17:07:38 | 0 | 23 | 1111,1111 | 1101,1111 | |
| Sep 8 17:07:38 | 1 | 3D | 0100,0100 | 0000,0100 | |
| Sep 8 17:07:38 | 1 | 77 | 0110,0111 | 0010,0111 | |

0 to 1 : 5
1 to 0 : 11

! : multiple bit flips in an 8 bit register.

# Run 6

| | Beam | SEU | T sec | N read | Refresh Hz | Hard reset |
|---|---|---|---|---|---|---|
| Day1Run6 | ON | 6 | 600 | 7 | 1(*) | Enabled |

| Time | Page | Address | Written | Read |
|---|---|---|---|---|
| Sep 8 17:50:51 | 1 | 8B | 0101,0111 | 0001,0111 |
| Sep 8 18:01:01 | 1 | CF | 0011,1011 | 0001,0111 |
| Sep 8 18:01:01 | 1 | D7 | 0101,1001 | 1101,1001 |
| Sep 8 18:21:23 | 0 | 28 | 1111,1111 | 1111,1101 |
| Sep 8 18:31:33 | 0 | 32 | 1111,1111 | 1111,1011 |
| Sep 8 18:31:33 | 1 | A8 | 0101,0001 | 0001,0001 |

0 to 1 : 1
1 to 0 : 5

# Run 8

| | Beam | SEU | T sec | N read | Refresh Hz | Hard reset |
|---|---|---|---|---|---|---|
| Day1Run6 | ON | 10 | 600 | 6 | 10(*) | Enabled |

| Time | Page | Address | Written | Read | |
|---|---|---|---|---|---|
| Sep 8 19:09:24 | 1 | A9 | 0101,0111 | 1101,0111 | |
| Sep 8 19:09:24 | 1 | B1 | 0100,0110 | 0101,0101 | ❗ |
| Sep 8 19:09:24 | 1 | D2 | 0100,0011 | 0100,0001 | |
| Sep 8 19:19:51 | 1 | E0 | 0101,0000 | 0101,0101 | ❗ |
| Sep 8 19:30:19 | 1 | 6D | 0101,1100 | 0101,1000 | |
| Sep 8 19:40:45 | 0 | 45 | 0100,1100 | 0100,0101 | ❗ |

0 to 1 : 6
1 to 0 : 4

❗ : multiple bit flips in an 8 bit register.

# Run 9A

| | Beam | SEU | T sec | N read | Refresh Hz | Hard reset |
|---|---|---|---|---|---|---|
| Day1Run9A | ON | 26 | 600 | 4 | 10 | Enabled |

| Time | Page | Address | Written | Read | |
|---|---|---|---|---|---|
| Sep 8 20:24:08 | 1 | 1D | 0100,1110 | 0000,0100 | ! |
| Sep 8 20:24:08 | 1 | 64 | 0100,1100 | 1000,0000 | ! |
| Sep 8 20:24:08 | 1 | 68 | 0101,0101 | 1101,0101 | |
| Sep 8 20:24:08 | 1 | 93 | 0101,1110 | 0101,0101 | ! |
| Sep 8 20:34:12 | 0 | 28 | 1111,1111 | 0101,0101 | ! |
| Sep 8 20:34:12 | 0 | 2A | 1111,1111 | 1111,0111 | |
| Sep 8 20:34:12 | 0 | 3A | 1111,1111 | 1110,1111 | |
| Sep 8 20:34:12 | 1 | 10 | 0100,0011 | 0000,0000 | ! |
| Sep 8 20:54:18 | 1 | 01 | 0100,1110 | 0100,1100 | |
| Sep 8 20:54:18 | 1 | 29 | 0101,0000 | 0101,0101 | ! |
| Sep 8 20:54:18 | 1 | 3A | 0101,0011 | 0001,0011 | |
| Sep 8 20:54:18 | 1 | E9 | 0101,1110 | 0101,1100 | |
| Sep 8 20:54:18 | 1 | F0 | 0110,0101 | 0110,0001 | |

0 to 1 : 5
1 to 0 : 21

! : multiple bit flips in an 8 bit register.

# Run 12

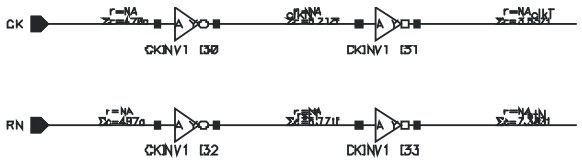
| | Beam | SEU | T sec | N read | Refresh Hz | Hard reset |
|---|---|---|---|---|---|---|
| Day2Run12 | ON | 20 | 600 | 6 | Disabled | Disabled |

| Time | Page | Address | Written | Read | |
|---|---|---|---|---|---|
| Sep 9 16:32:21 | 1 | 6D | 0101,1100 | 0101,1000 | |
| Sep 9 16:32:21 | 1 | 74 | 0101,1011 | 0101,0011 | |
| Sep 9 16:32:21 | 1 | 90 | 0101,0100 | 0101,0101 | |
| Sep 9 16:42:23 | 0 | 00 | 1100,0011 | 1100,0111 | |
| Sep 9 16:42:23 | 0 | 3D | 1111,1111 | 1110,1111 | |
| Sep 9 16:42:23 | 1 | 0F | 0101,1111 | 0101,1110 | |
| Sep 9 16:42:23 | 1 | 31 | 0100,1110 | 1100,1110 | |
| Sep 9 16:42:23 | 1 | 50 | 0100,1010 | 0000,1010 | |
| Sep 9 16:42:23 | 1 | 92 | 0100,0110 | 0100,0100 | |
| Sep 9 16:42:23 | 1 | D7 | 0101,1001 | 0100,1001 | |
| Sep 9 17:02:28 | 0 | 28 | 1111,1111 | 0101,0101 | ! |
| Sep 9 17:02:28 | 1 | 53 | 0101,0000 | 0100,0000 | |
| Sep 9 17:02:28 | 1 | 62 | 0100,0101 | 0000,0101 | |
| Sep 9 17:12:30 | 1 | 33 | 0101,1011 | 0101,0101 | ! |
| Sep 9 17:12:30 | 1 | D9 | 0100,1110 | 0100,1010 | |

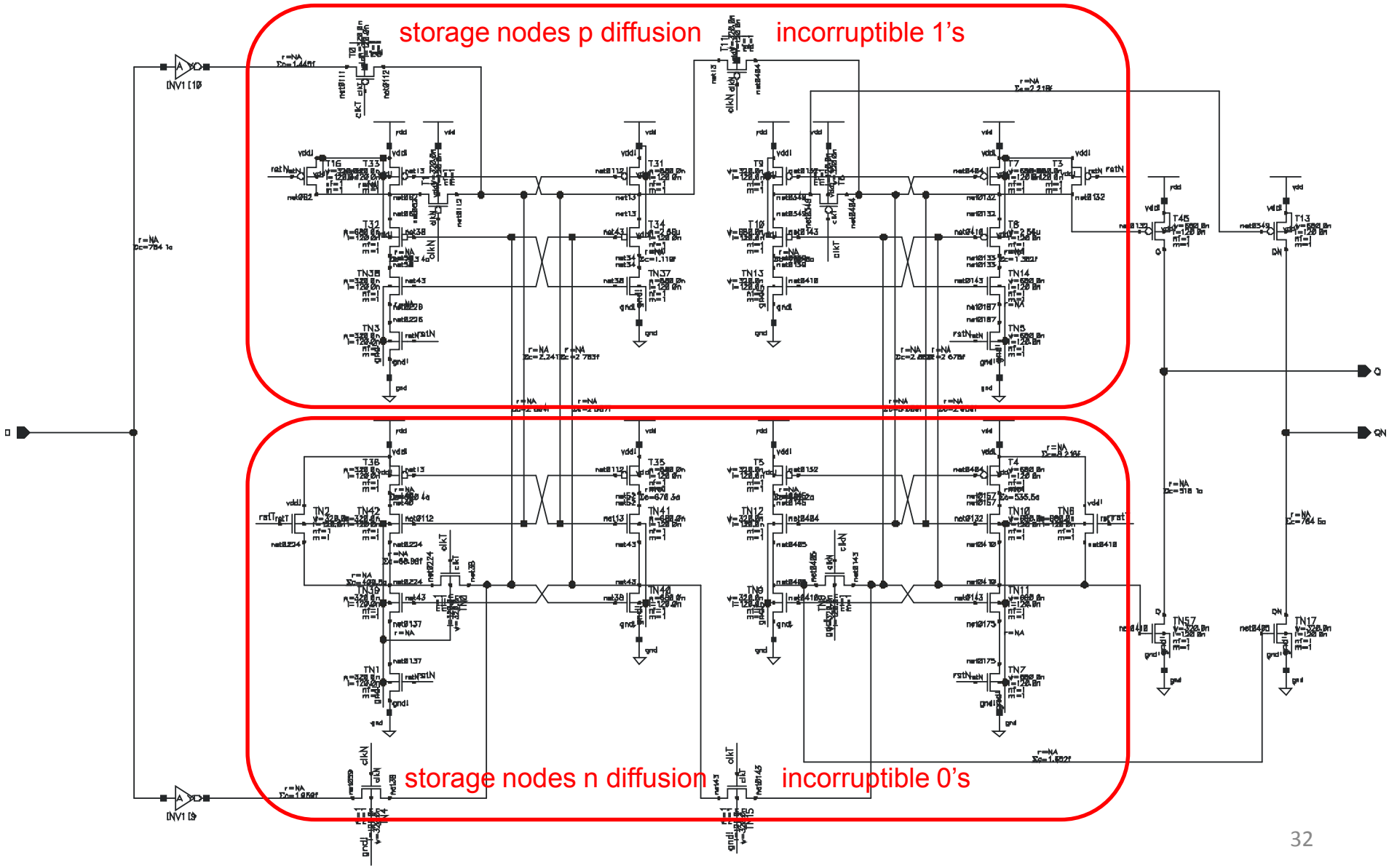
0 to 1 : 4
1 to 0 : 16

! : multiple bit flips in an 8 bit register.

# SEU tolerant D-type




data in uncorrupted section provides feedback to recover any corruption in other block



# I2C triple redundant RAM cell