

# CBC2 wafer testing results

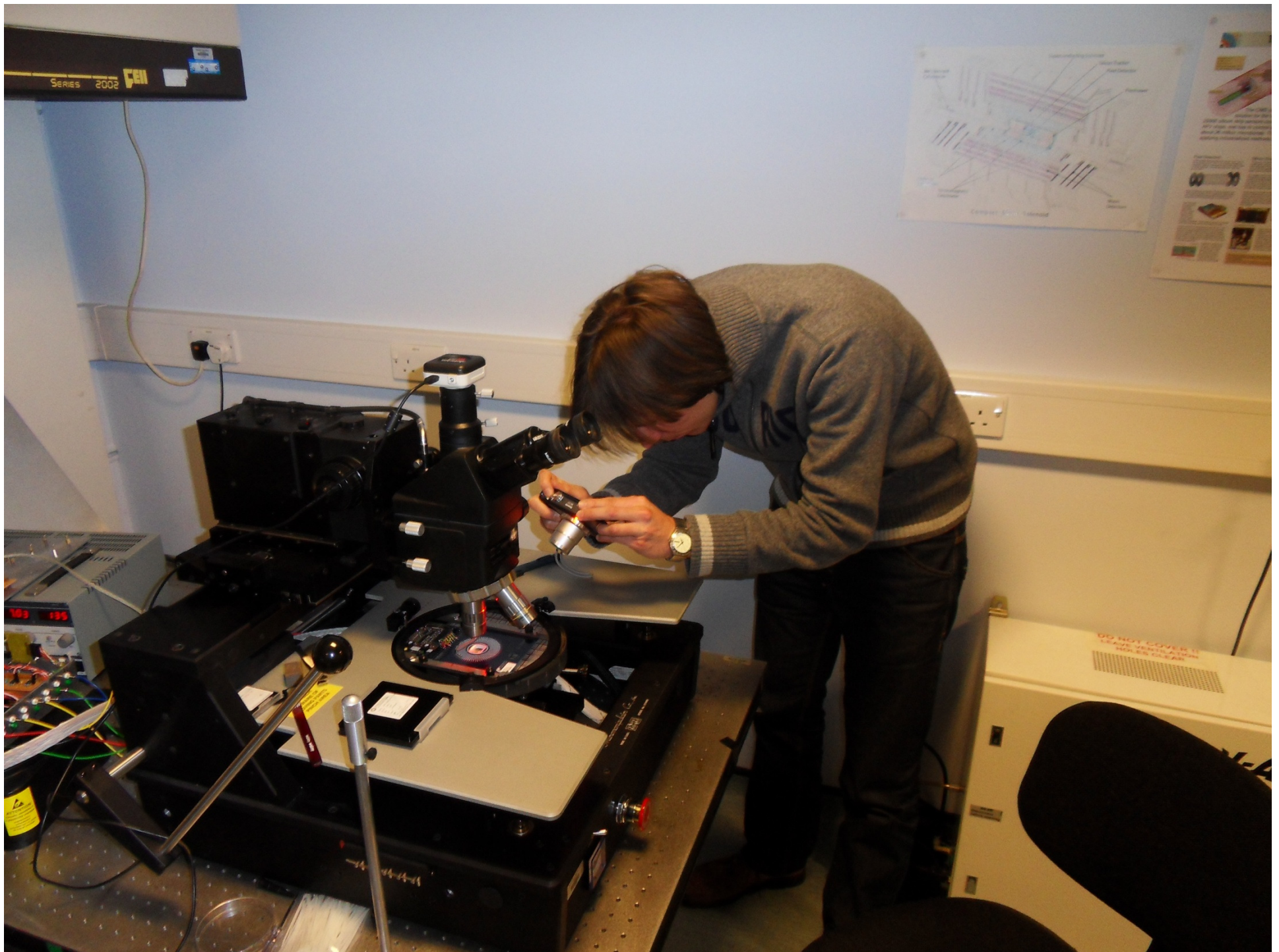
4 (of 8) wafers now probed

1<sup>st</sup> wafer - March 2013 -> 2CBC2 hybrids

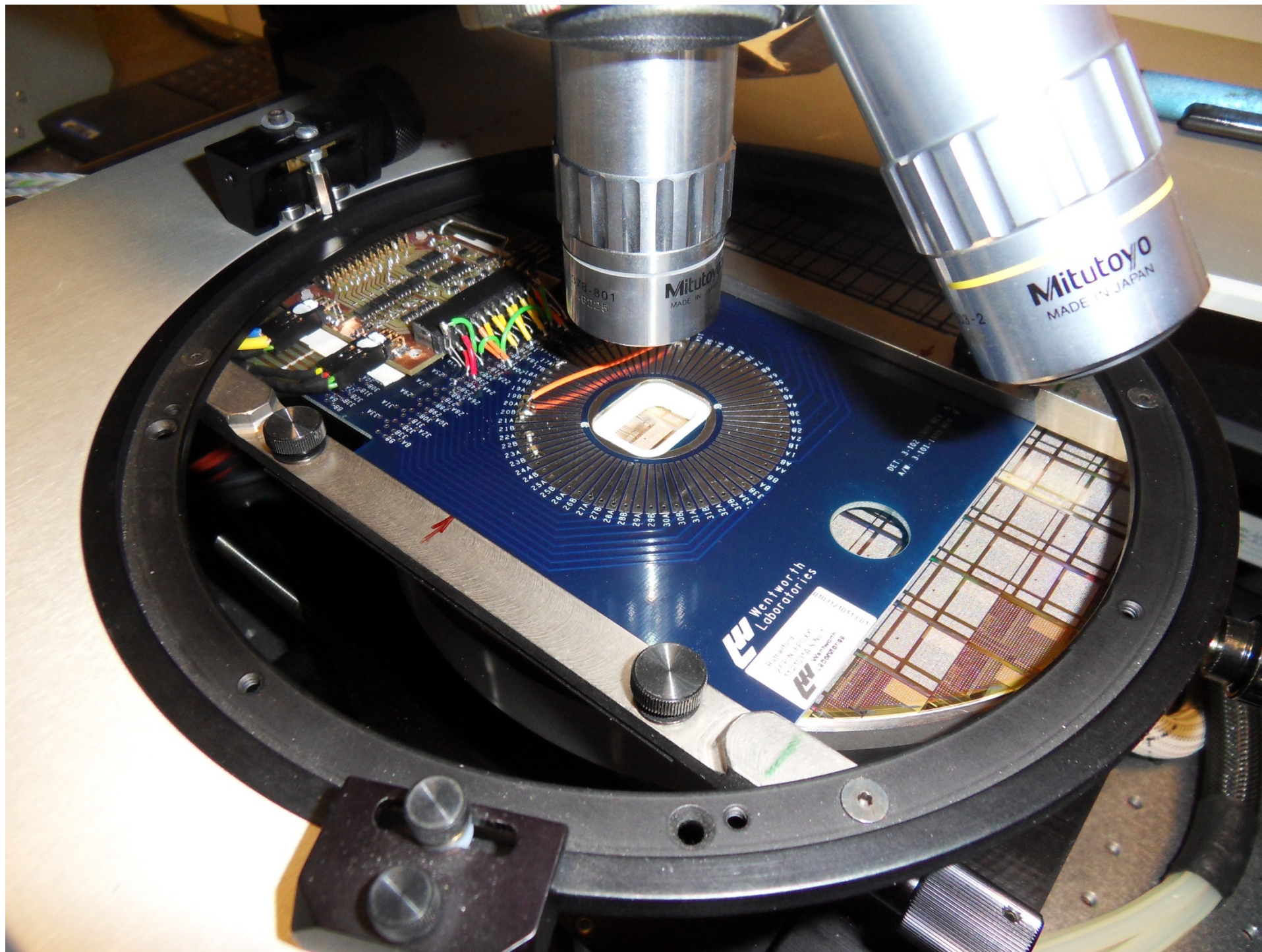
2<sup>nd</sup> - September 2013 -> 8CBC2flex hybrids

3<sup>rd</sup> & 4<sup>th</sup> - August 2014 -> new 8CBC2flex hybrids

will describe evolution of test procedures  
& show some analysis of results







# wafer test development

## **1<sup>st</sup> wafer**, A4PNFAH

- no I2C registers contain stuck bits (write & read back all 1's and all 0's)
- all channels respond to test pulse
- power consumption and some biases swept

## **2<sup>nd</sup> wafer**, ADPNF1H, some additional tests

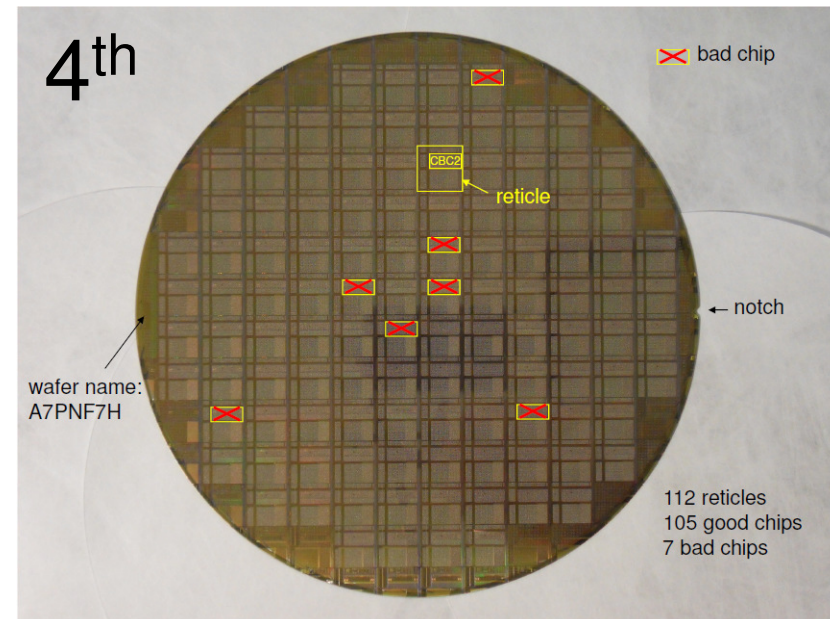
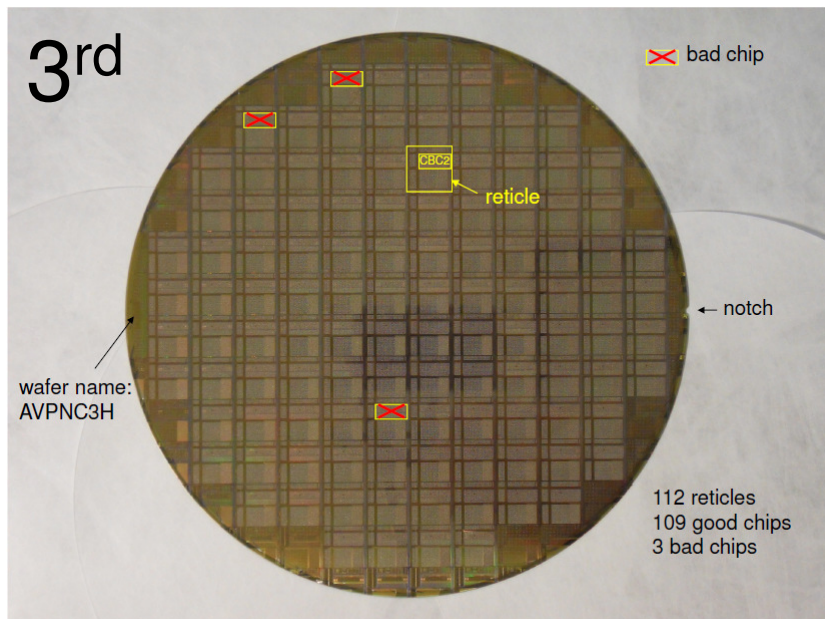
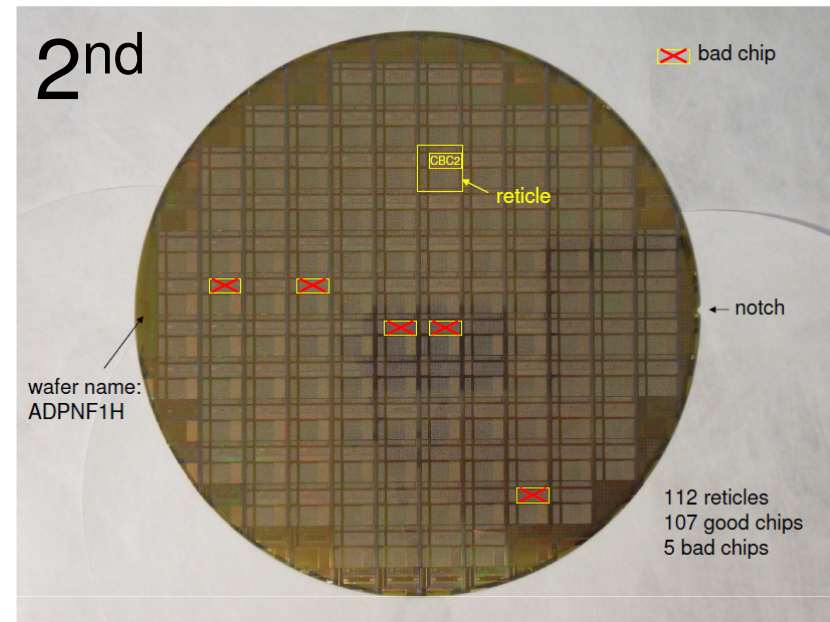
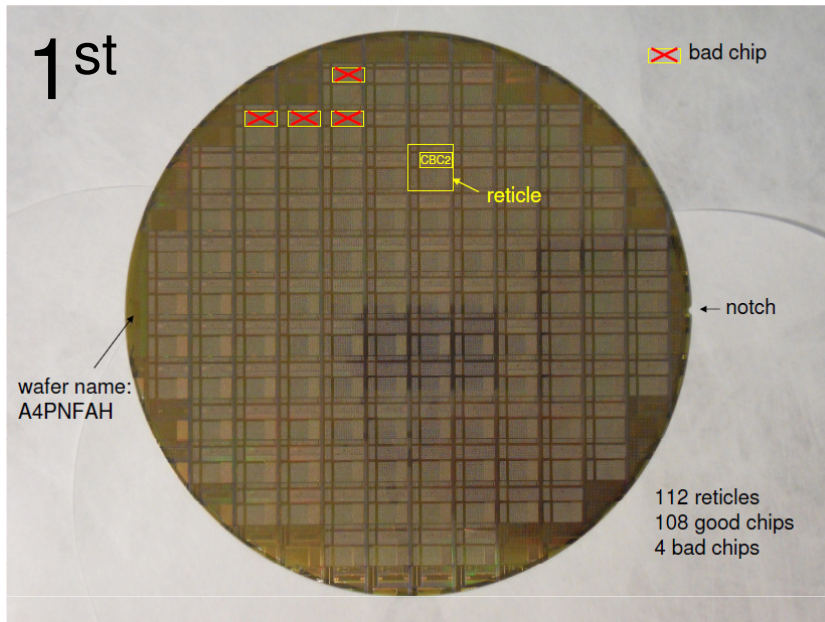
- basic offset tuning
- all pipeline locations accessed looking for stuck cells

## **3<sup>rd</sup> & 4<sup>th</sup> wafers**, A7PNF7H & AVPNC3H, further refinements

- implemented recommended offset tuning procedure
- s-curves for pedestals & s-curves with test pulse acquired
- fully automated procedure - takes ~ 5 mins per chip



# wafer results maps



# LabView front panel for individual chip test

latest version used for wafers 3 and 4



analysis of data from wafers 3 and 4 follows



# histograms

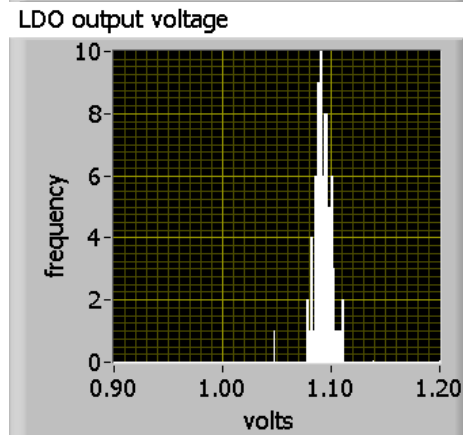
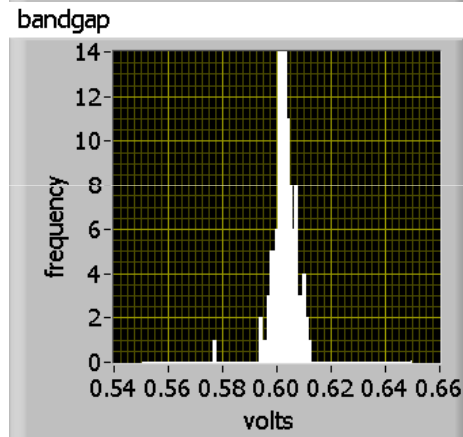
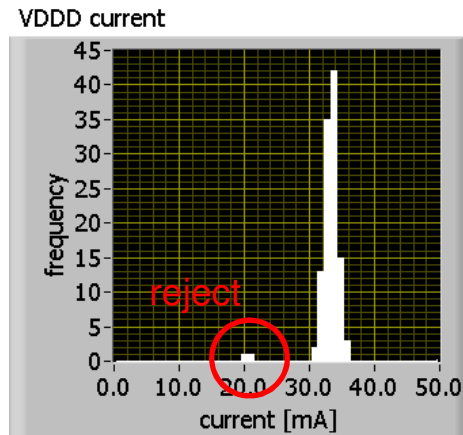
data from all chips from both latest wafers

including rejects **VDDD current**

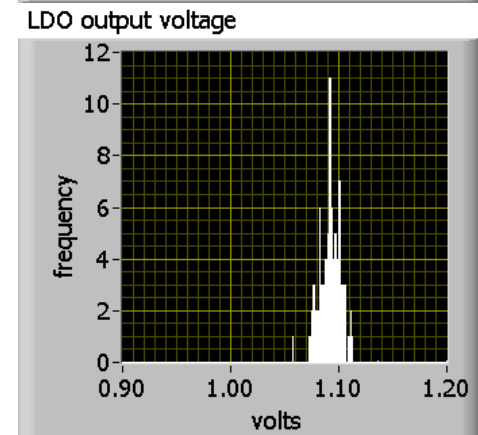
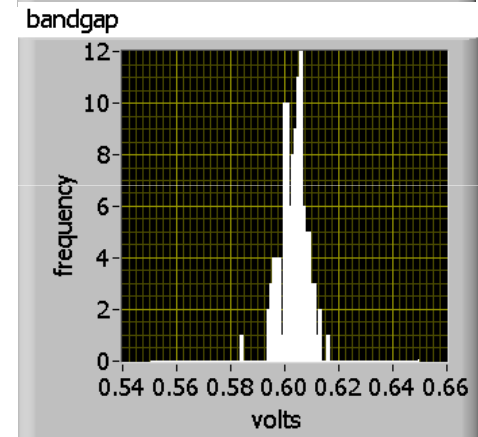
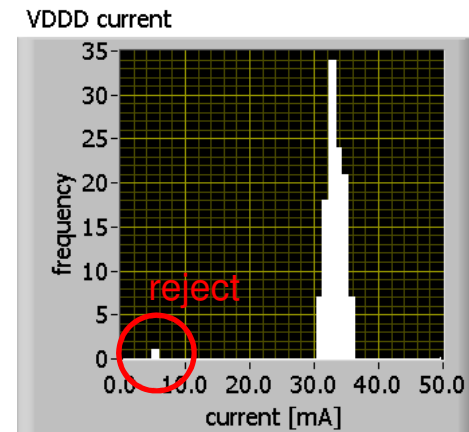
**bandgap voltage**

**LDO output**

**A7PNF7H**

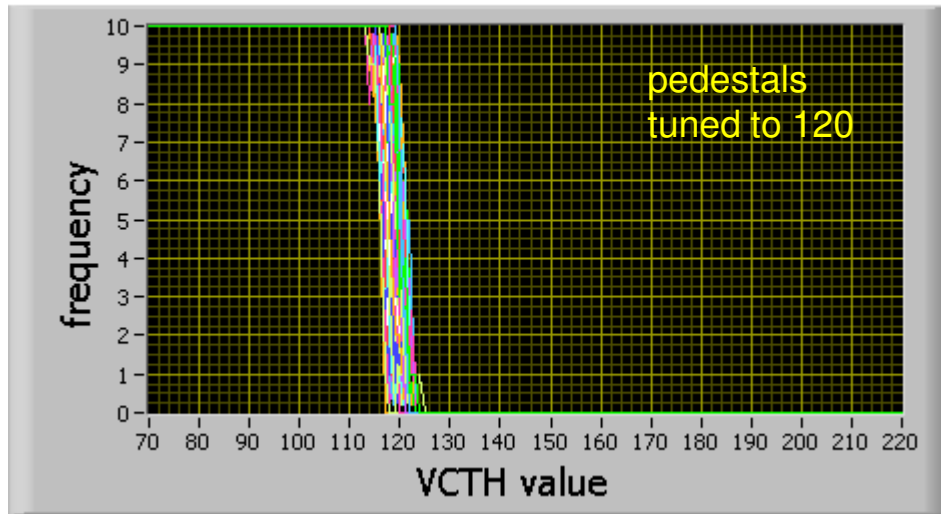


**AVPNC3H**

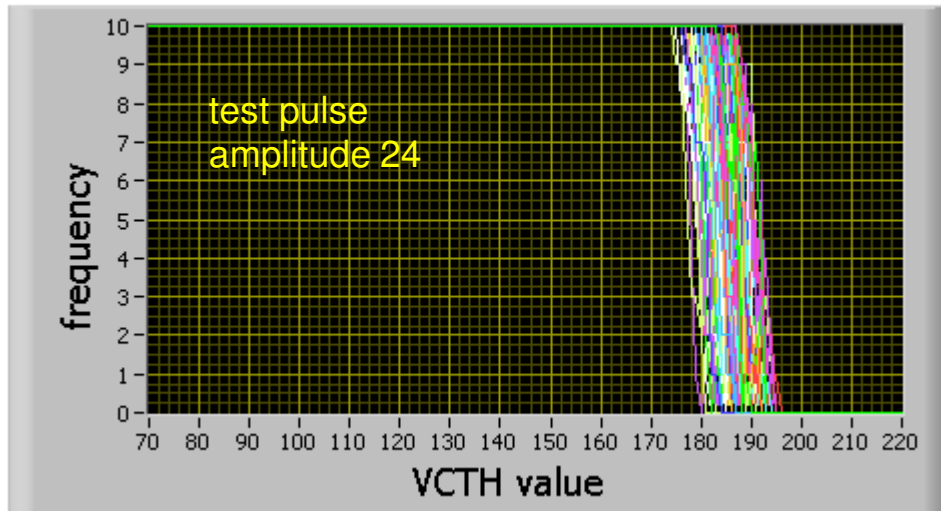


# s-curves

pedestal s-curves



test pulse s-curves



for each channel subtract pedestal from test pulse  
(s-curve mid-points)

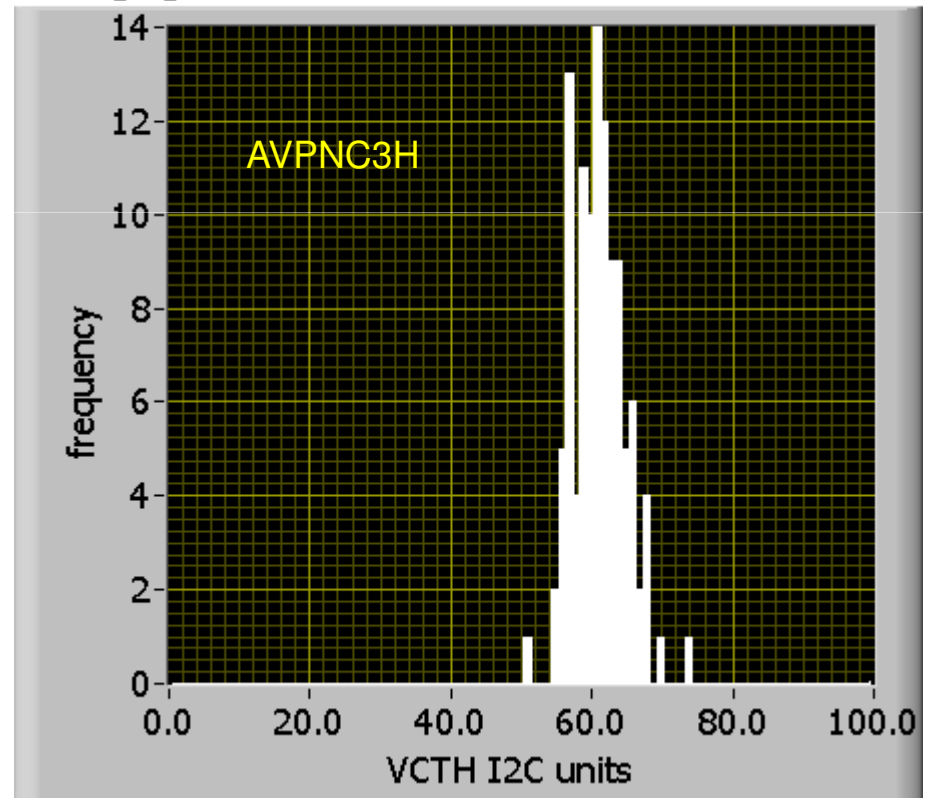
-> gain for each channel

take average of all 254 channels on the chip

do this for all chips on the wafer and histogram

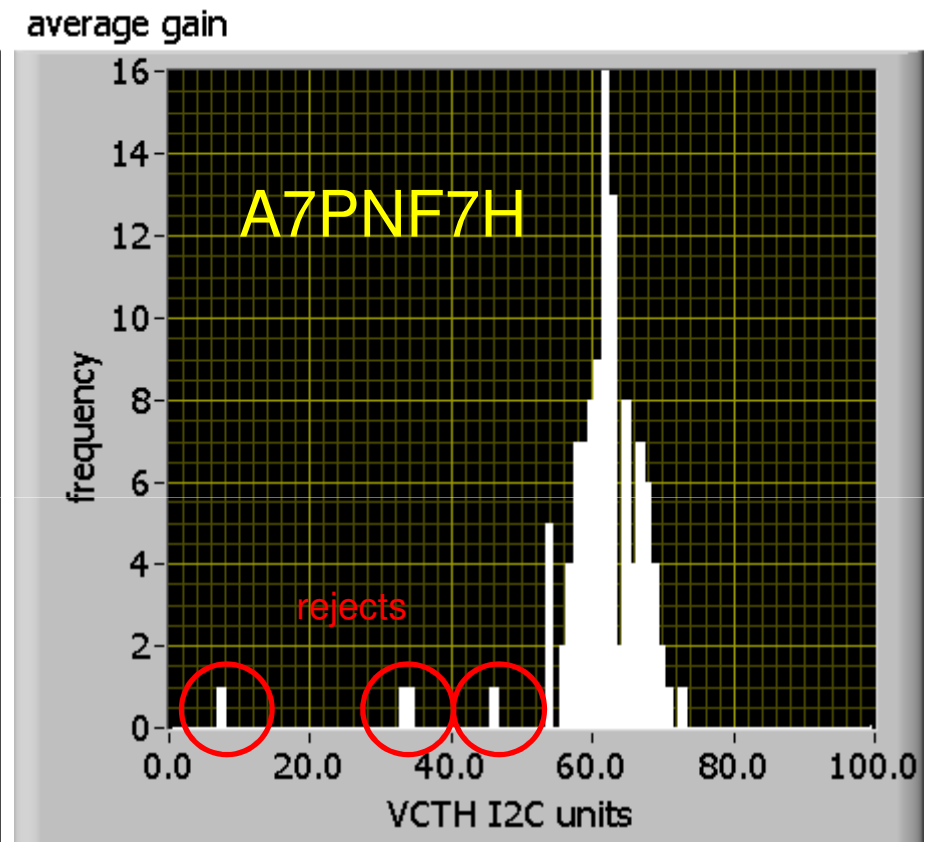
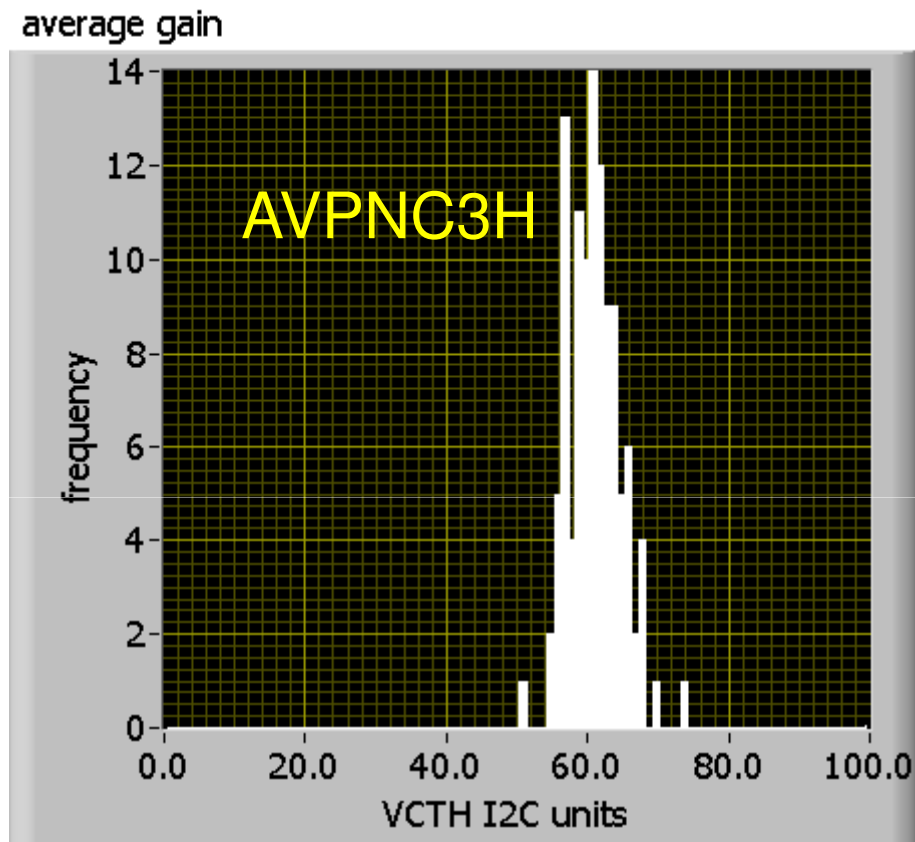


average gain





# comparing wafers

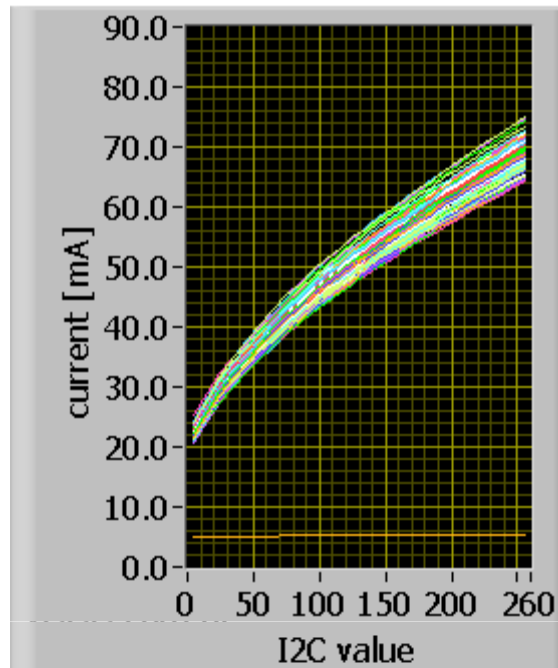


not much difference in average gain for these two wafers

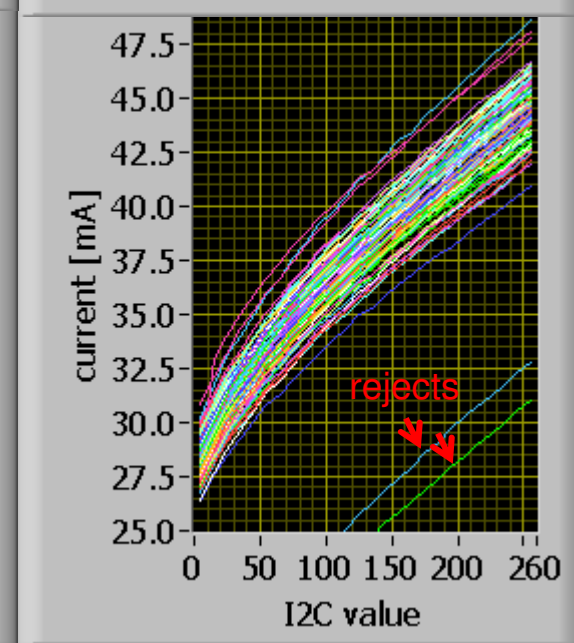
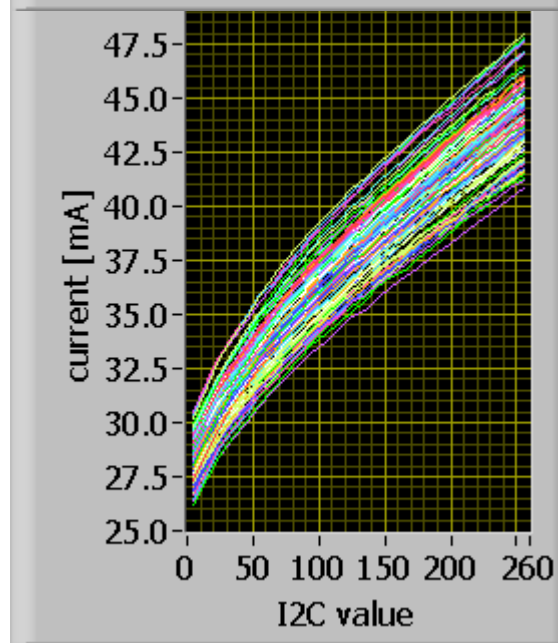
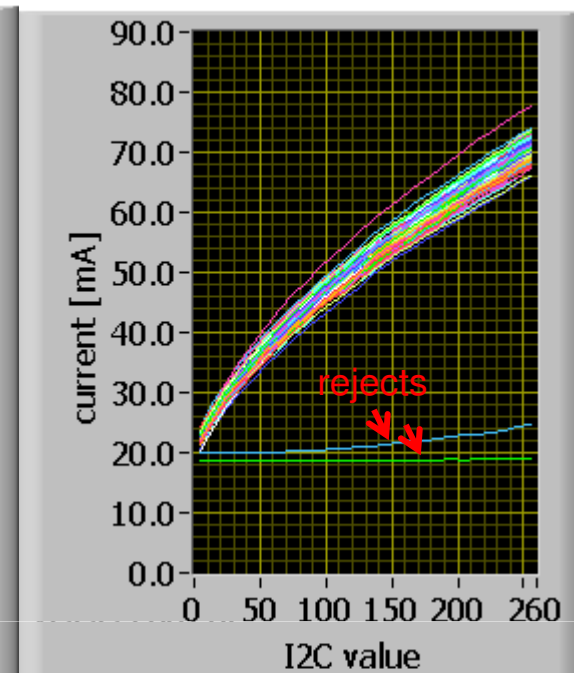
but relies on test pulse charge injection capacitors matching

# bias current sweeps

VDDD current AVPNC3H



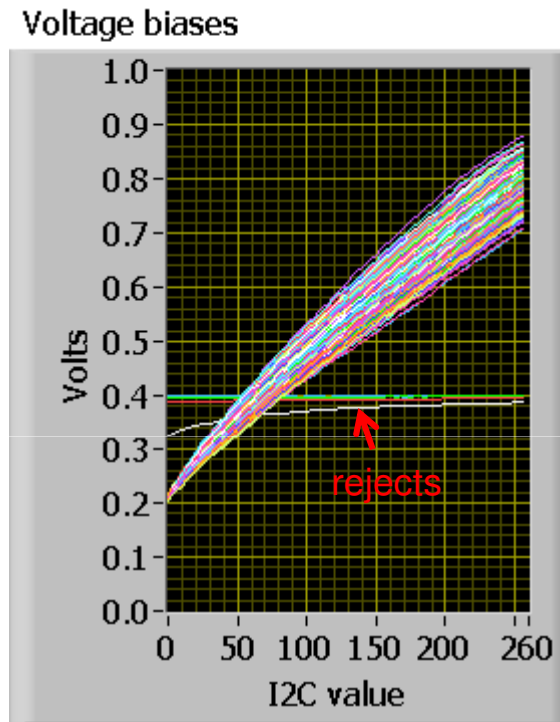
VDDD current A7PNF7H



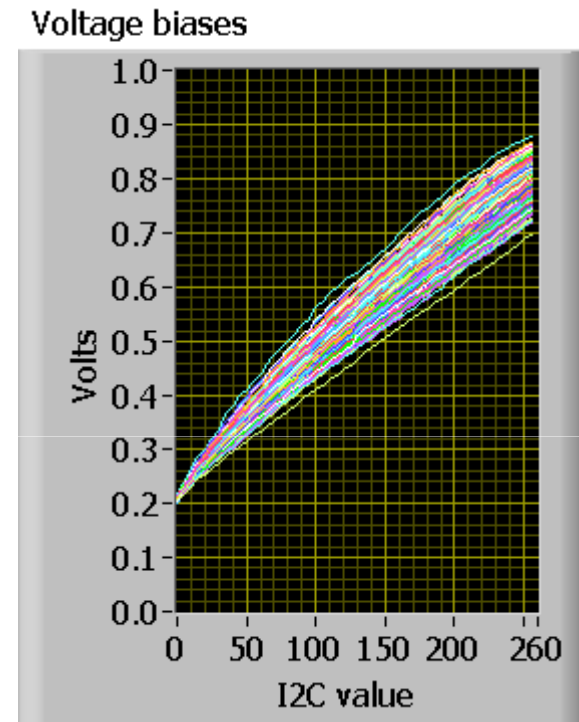


# bias voltage sweeps

## AVPNC3H

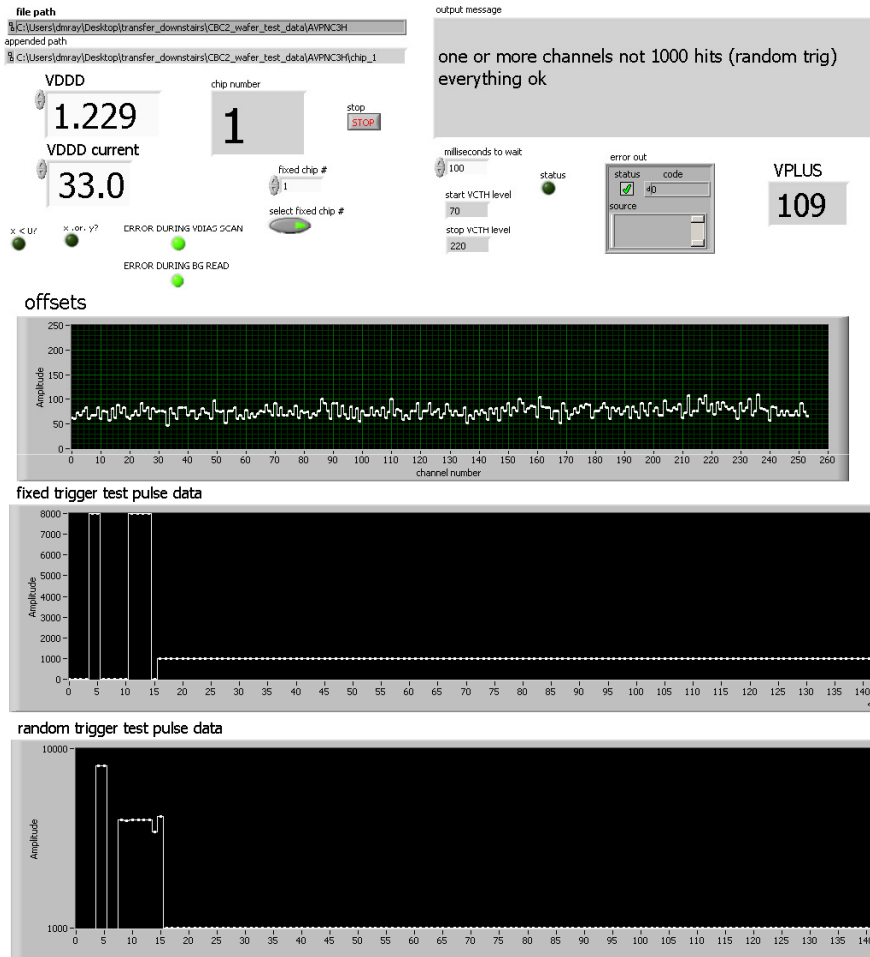


## A7PNF7H

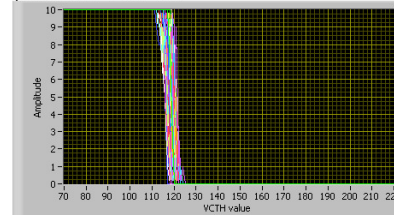


all voltage biases (VPC,VPLUS,VCTH,VPAFB) for all chips

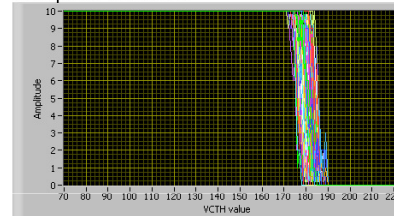
# AVPNC3H chip#1 - small problem



pedestals s-curves



test pulse s-curves



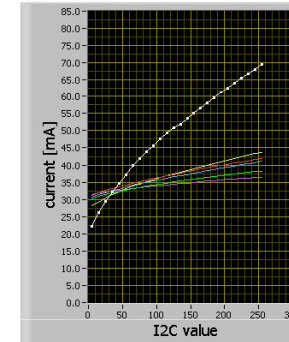
BG voltage

0.595

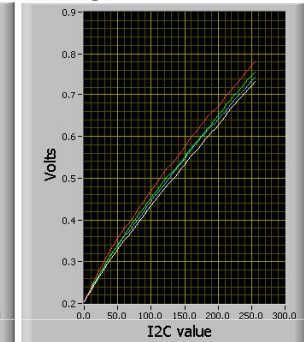
LDO output

1.073

bias currents



bias voltages



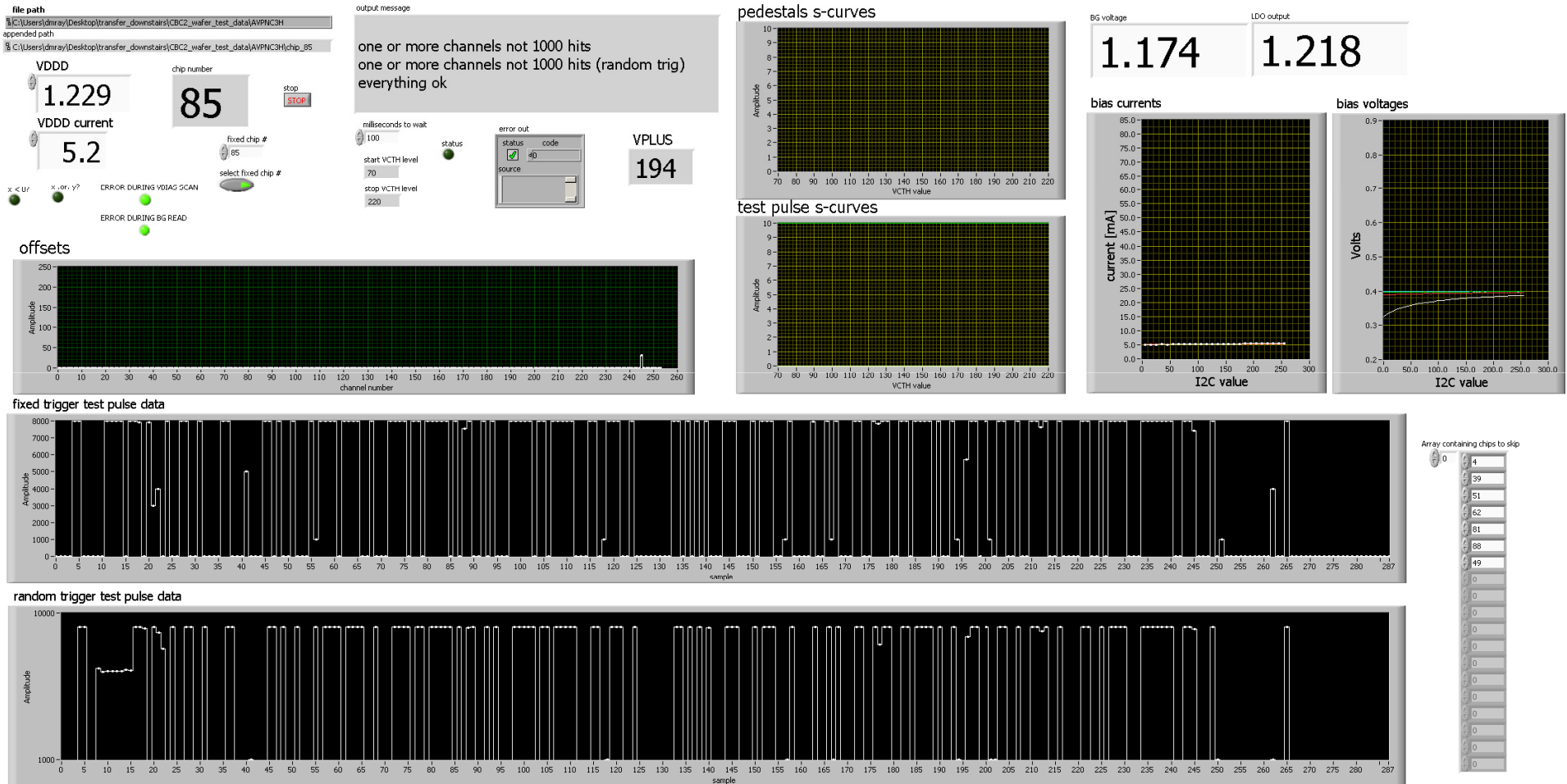
Array containing chips to skip



1 bit in pipeline stuck high



# AVPNC3H chip#85 - big problem



file path  
C:\Users\dmray\Desktop\transfer\_downstairs(CBC2\_vafer\_test\_data)A7PNF7H.chip\_4

VDDD  
1.230  
VDDD current  
33.8

chip number  
4

stop  
STOP

fixed chip #  
4

select fixed chip #

ERROR DURING VDDIAS SCAN

ERROR DURING BG READ

output message  
one or more channels not 1000 hits (random jtag)  
everything ok

milliseconds to wait  
100

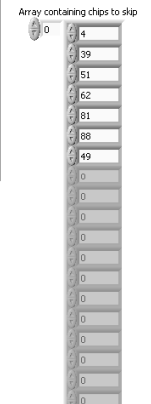
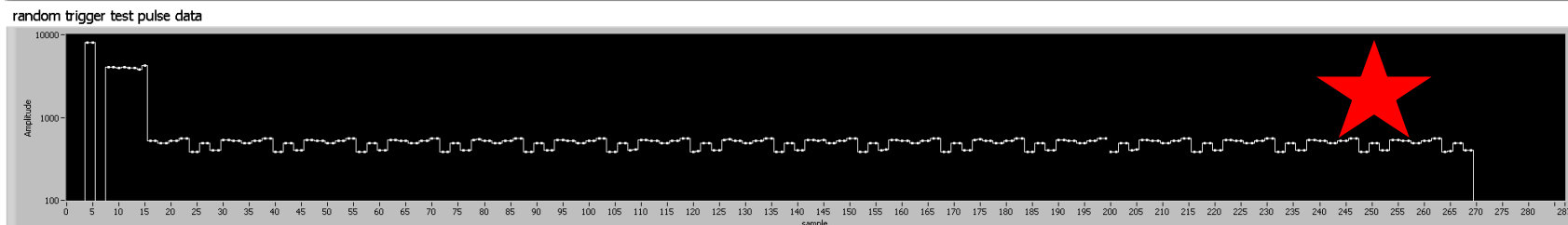
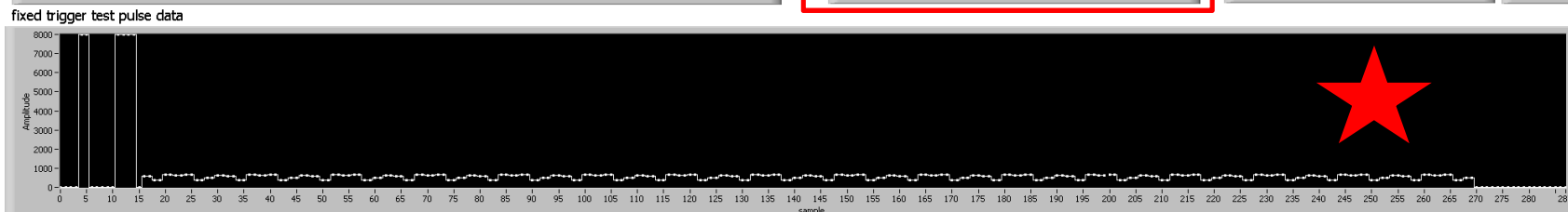
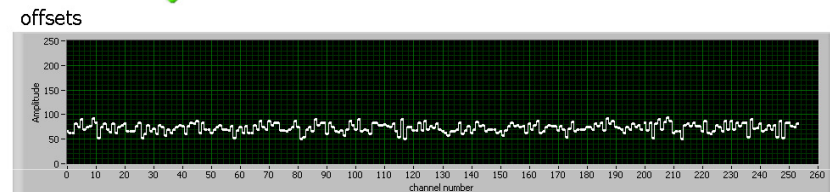
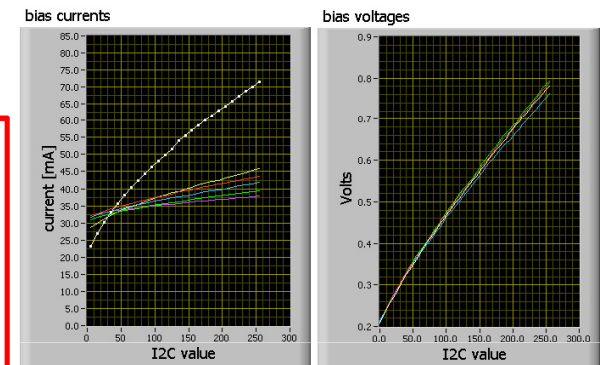
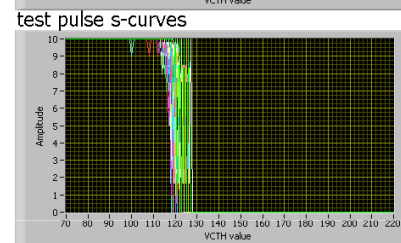
start VCTH level  
70

stop VCTH level  
220

status

error out  
status code  
ok

VPLUS  
92



file path

C:\Users\dmray\Desktop\transfer\_downstars\CB2\_wafer\_test\_data\A7PNF7H\opened path

C:\Users\dmray\Desktop\transfer\_downstars\CB2\_wafer\_test\_data\A7PNF7H\chip\_39

VDDD

1.227

VDDD current

33.2

x < 0? ☐

x, or, y? ☐

ERROR DURING VBIAS SCAN

ERROR DURING BG READ

chip number

39

stop

fixed chip #

39

select fixed chip #

output message

one or more channels not 1000 hits

one or more channels not 1000 hits (random trig)

everything ok

milliseconds to wait

100

start VCTH level

70

stop VCTH level

220

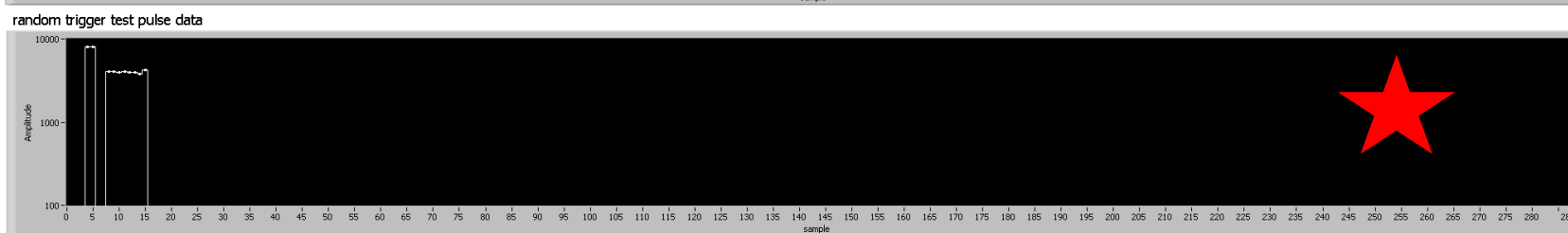
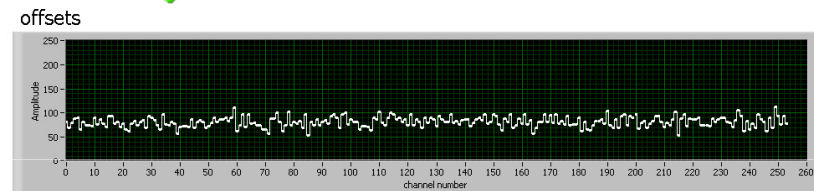
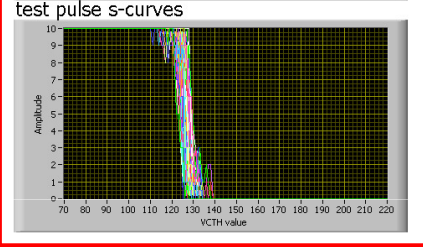
status ☐

error out

| status                              | code |
|-------------------------------------|------|
| <input checked="" type="checkbox"/> | 40   |
| source                              |      |

VPLUS

87

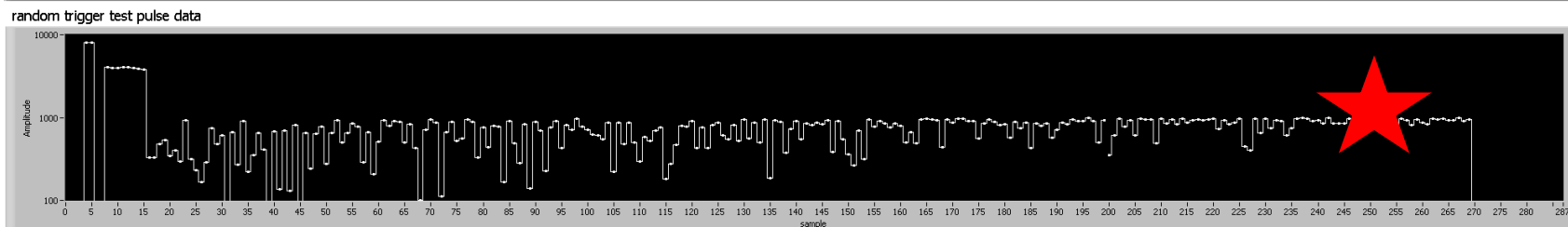
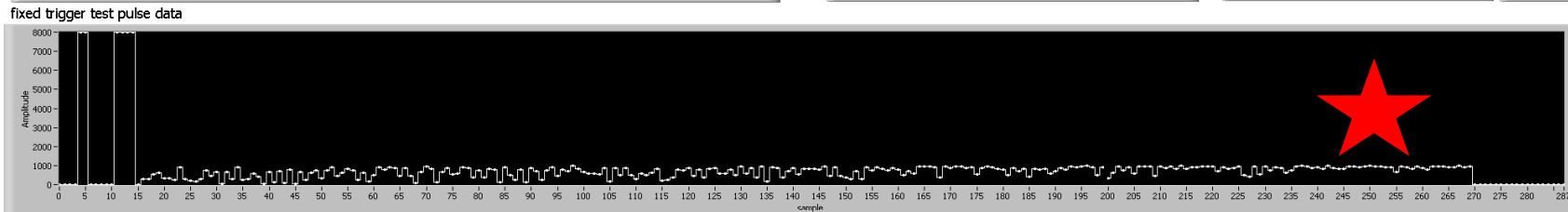
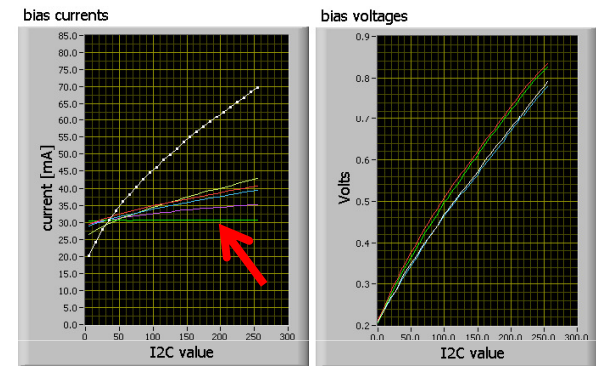
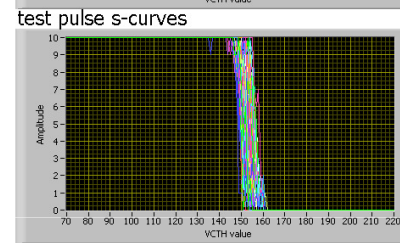


- [illegible]



The screenshot displays the VDDDD test interface with the following elements:

- File path:** C:\Users\dmray\Desktop\transfer\_downstairs\CBC2\_wafer\_test\_data\A7PWF7H
- opened path:** C:\Users\dmray\Desktop\transfer\_downstairs\CBC2\_wafer\_test\_data\A7PWF7H\chip\_49
- VDDDD:** 1.228
- VDDDD current:** 31.6
- chip number:** 49
- stop:** STOP
- fixed chip #:** 49
- select fixed chip #:** (indicated by a green dot on a chip diagram)
- status:** status
- error out:** error out
- status code:** 40
- source:** (empty field)
- VPLUS:** 112
- offsets:** (indicated by a green dot on a chip diagram)
- Waveform:** A plot of Amplitude (0 to 250) versus channel number (0 to 260).

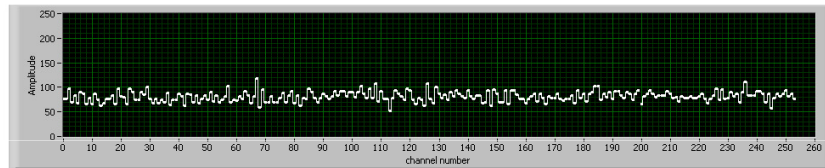


one bias current not working

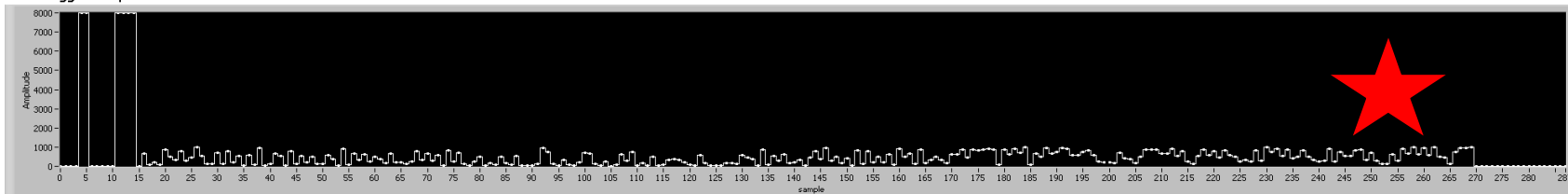
# A7PNF7H chip#51



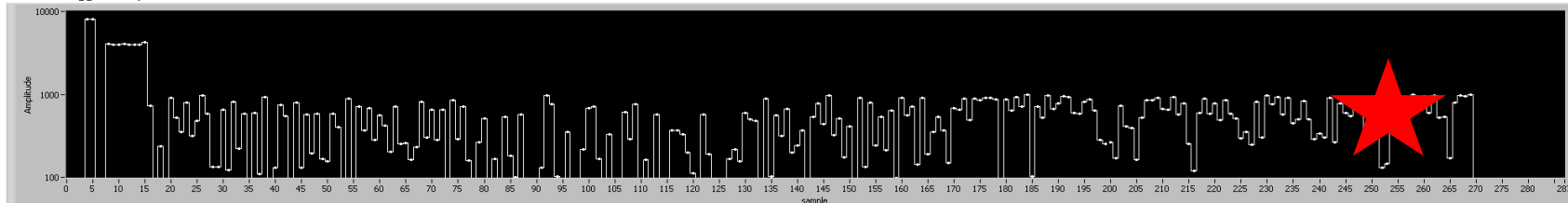
offsets



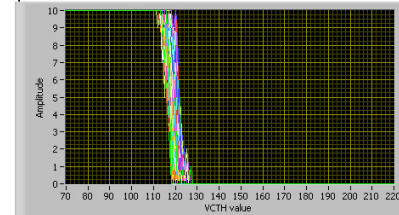
fixed trigger test pulse data



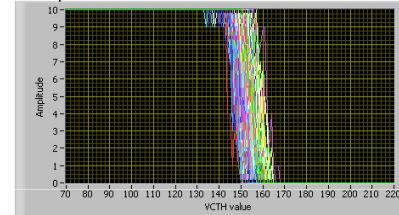
random trigger test pulse data



pedestals s-curves



test pulse s-curves



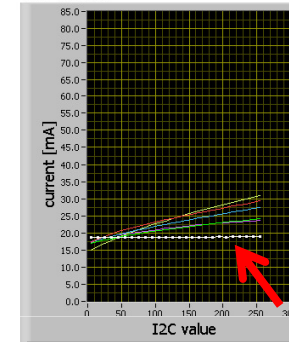
BG voltage

0.600

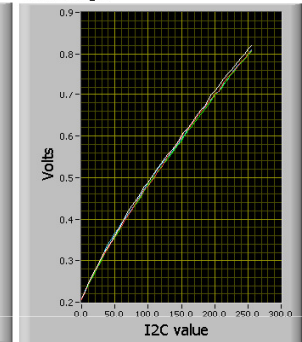
LDO output

1.089

bias currents



bias voltages

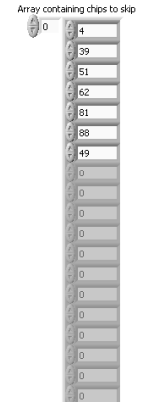
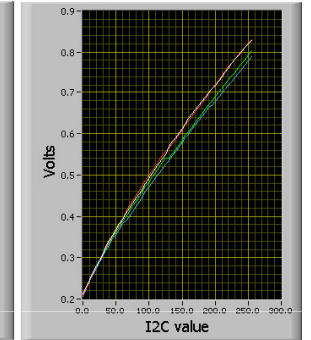
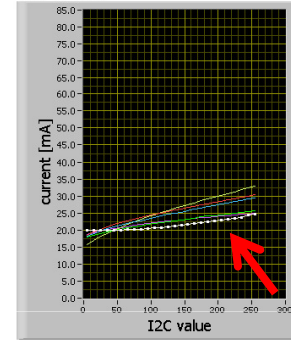
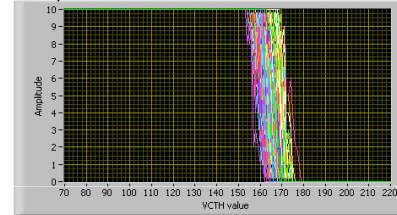
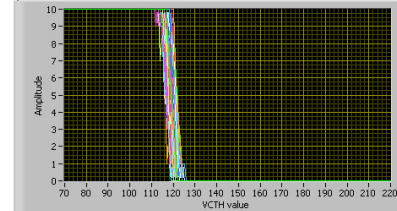
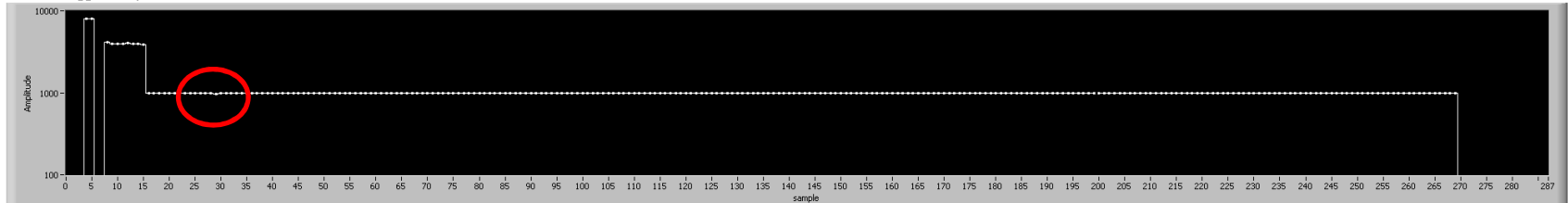
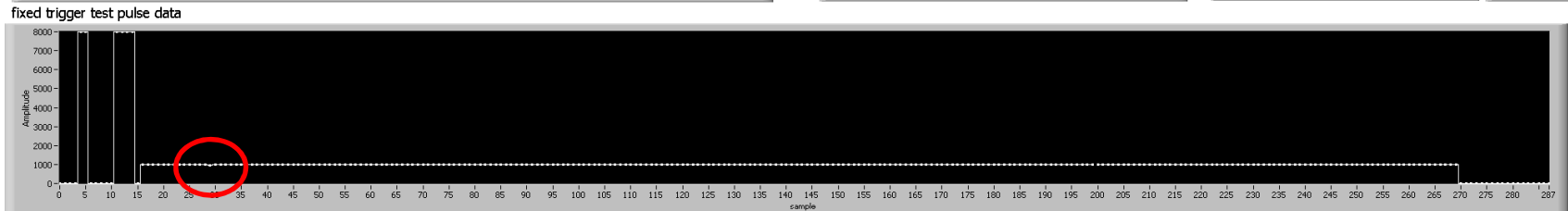
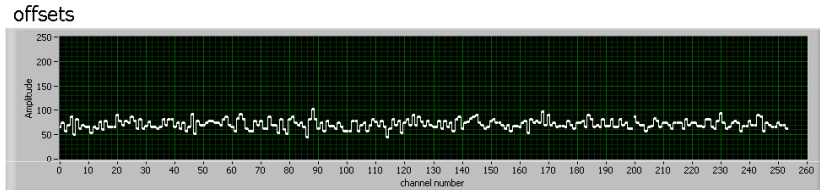


Array containing chips to skip



IPRE1 not working

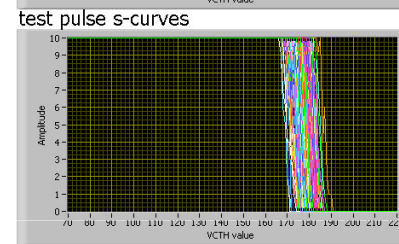
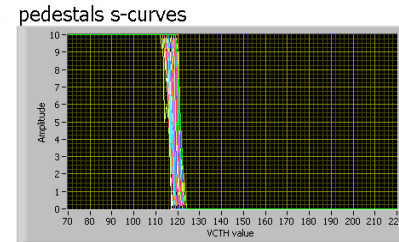
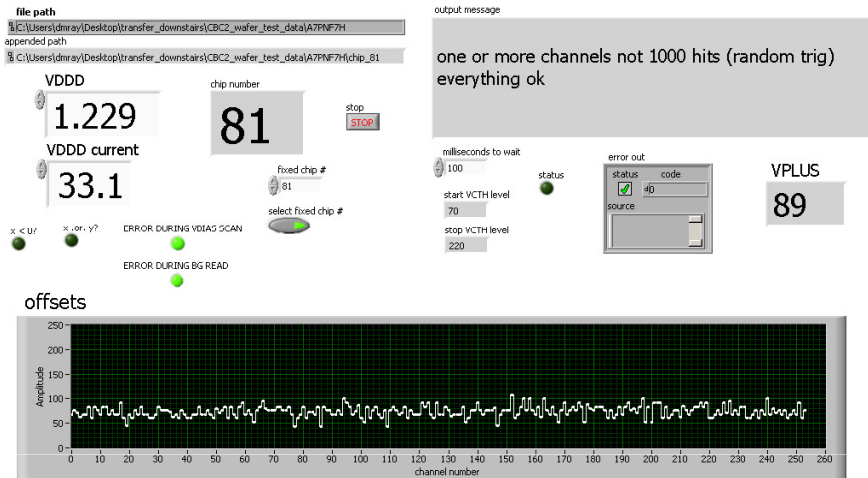
# A7PNF7H chip#62



## IPRE1 not working

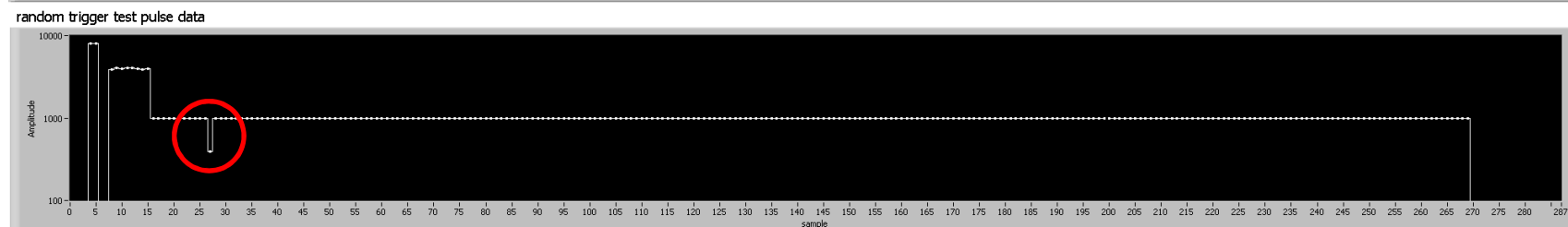
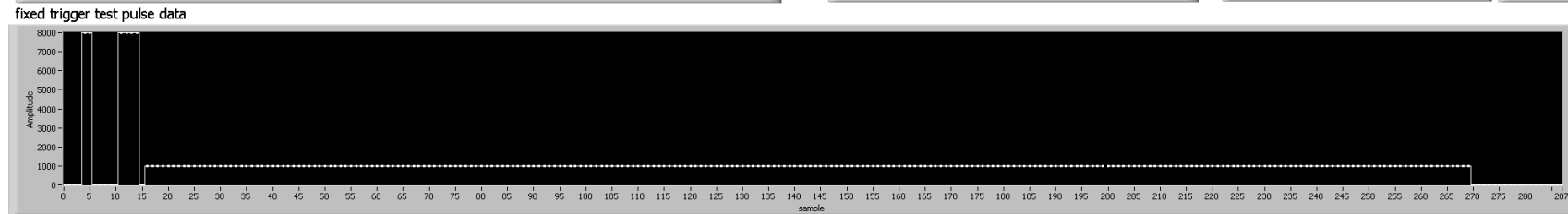
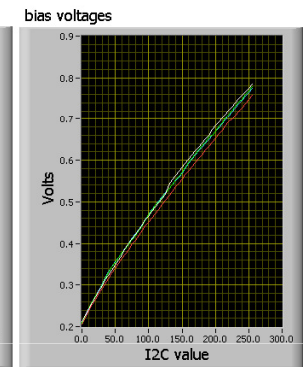
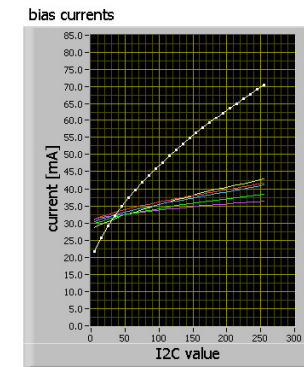


# A7PNF7H chip#81



BG voltage  
0.599

LDO output  
1.082

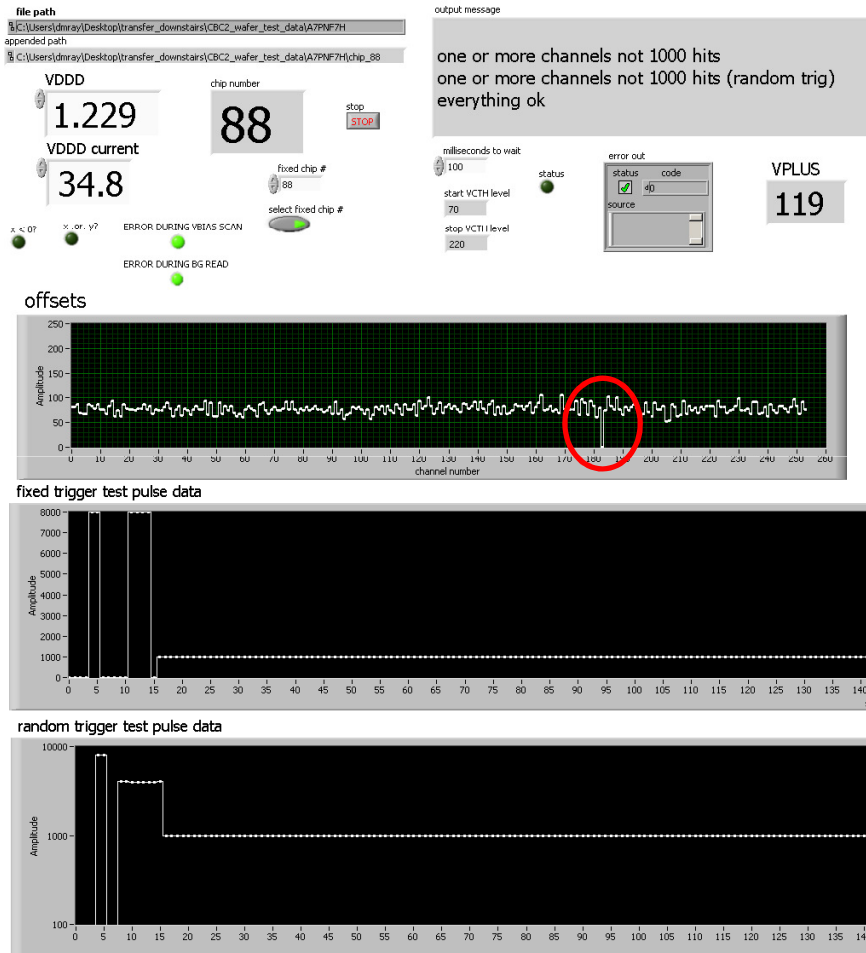


Array containing chips to skip

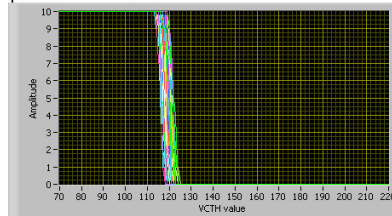
|    |    |
|----|----|
| 0  | 4  |
| 1  | 39 |
| 2  | E1 |
| 3  | 62 |
| 4  | B1 |
| 5  | B8 |
| 6  | M9 |
| 7  | 0  |
| 8  | 0  |
| 9  | 0  |
| 10 | 0  |
| 11 | 0  |
| 12 | 0  |
| 13 | 0  |
| 14 | 0  |
| 15 | 0  |
| 16 | 0  |
| 17 | 0  |
| 18 | 0  |
| 19 | 0  |

1 bit in pipeline stuck low

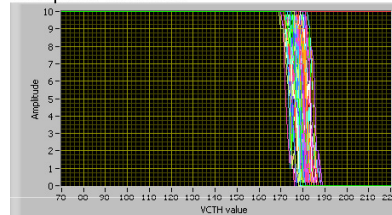
# A7PNF7H chip#88



pedestals s-curves



test pulse s-curves



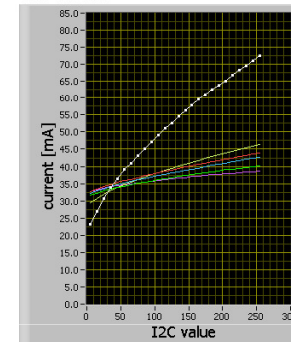
BG voltage

0.611

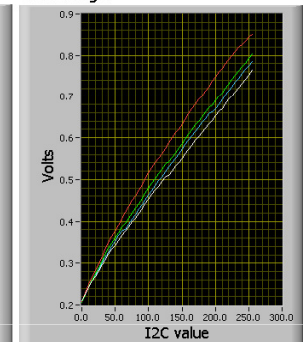
LDO output

1.111

bias currents



bias voltages



Array containing chips to skip



1 channel output stuck high

# summary

wafer yields to date

1<sup>st</sup> , 4 rejects (balls damaged)

2<sup>nd</sup> , 5 rejects

3<sup>rd</sup> , 3 rejects

4<sup>th</sup> , 7 rejects (one rejected by eye)

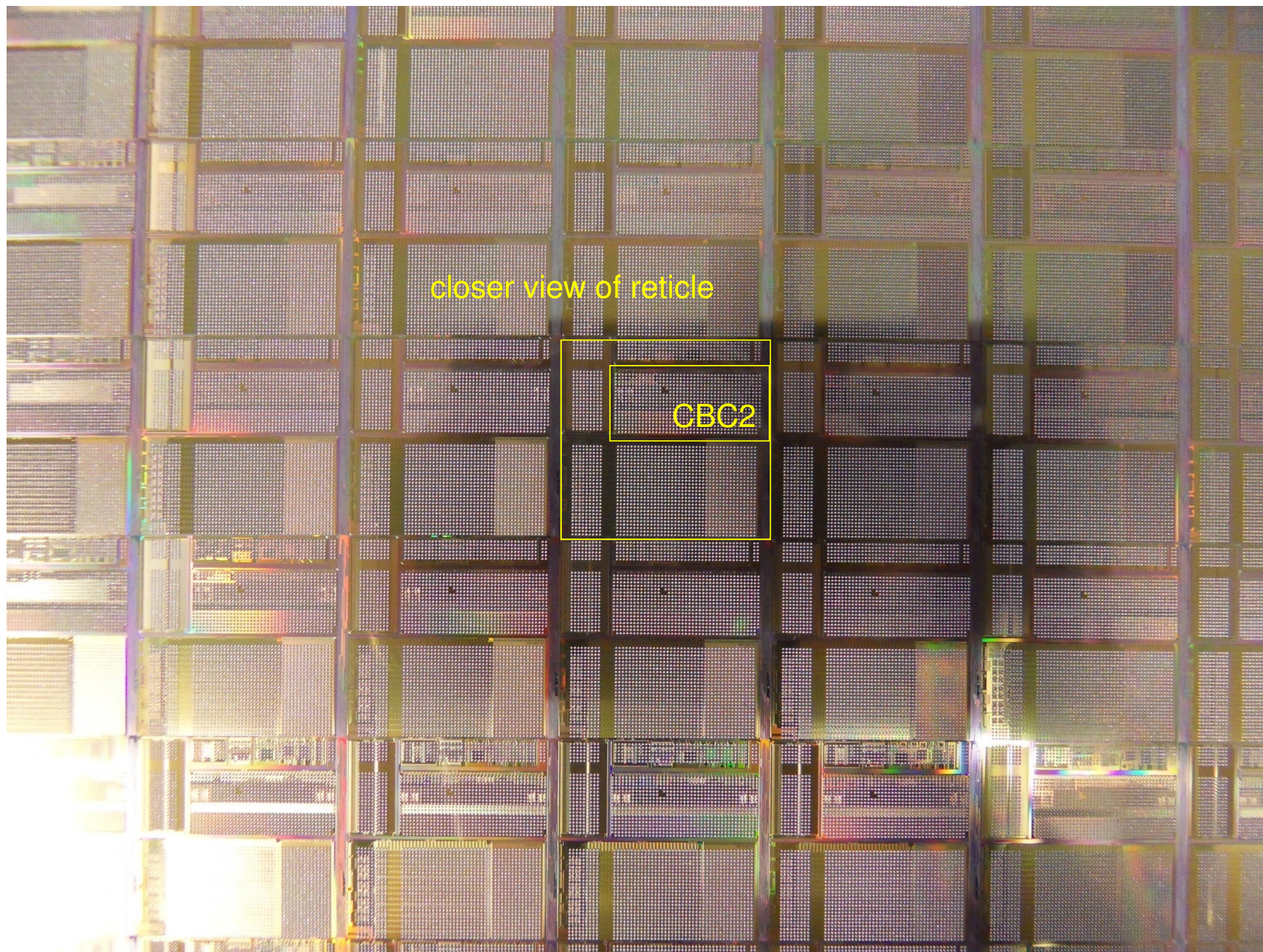
} more rigorous test procedure for last 2

test takes ~5 mins per chip

faster I2C would help - present interface runs at 100 kHz

extra



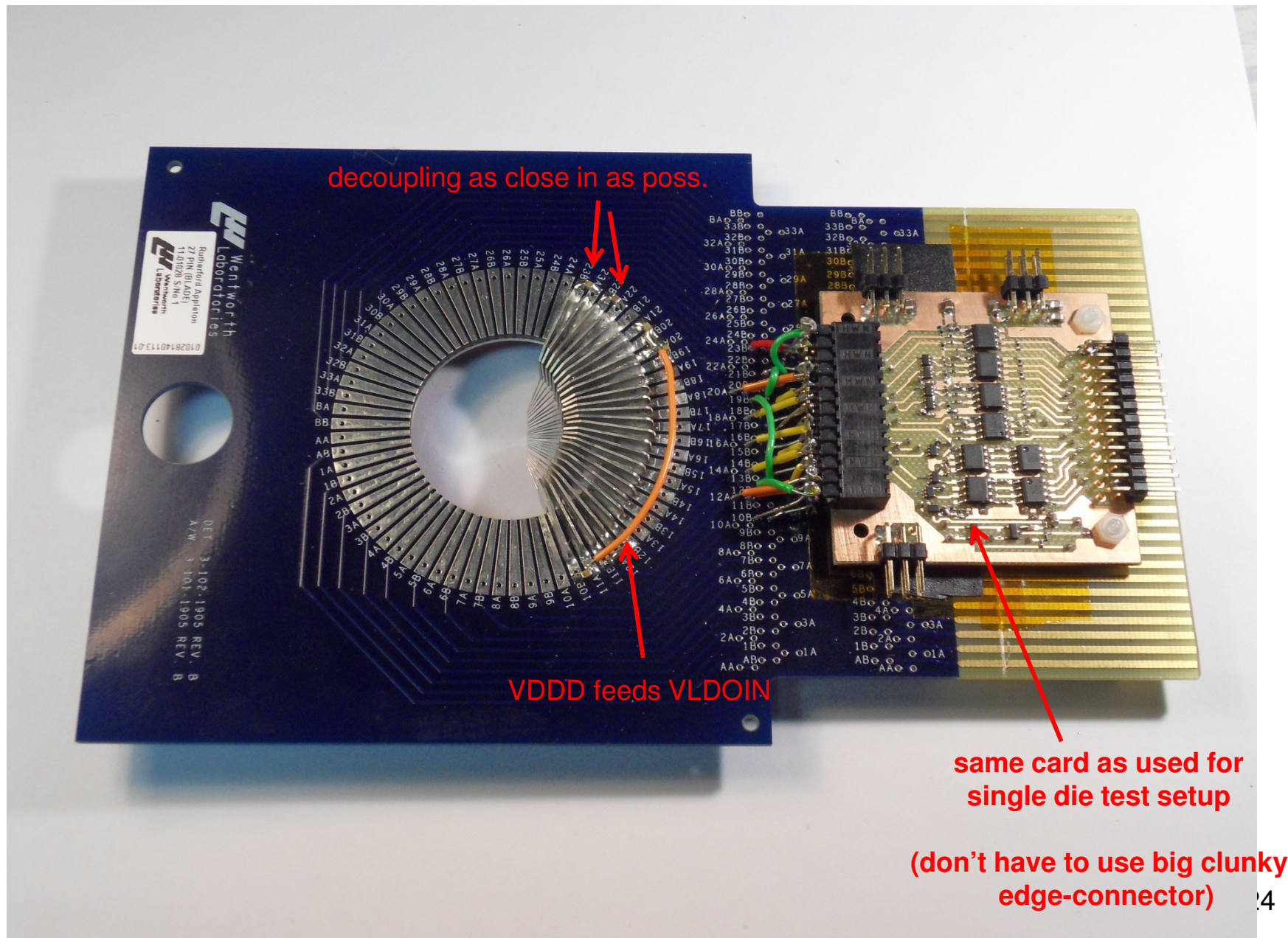


closer view of reticle

CBC2



# blade probe card for CBC2

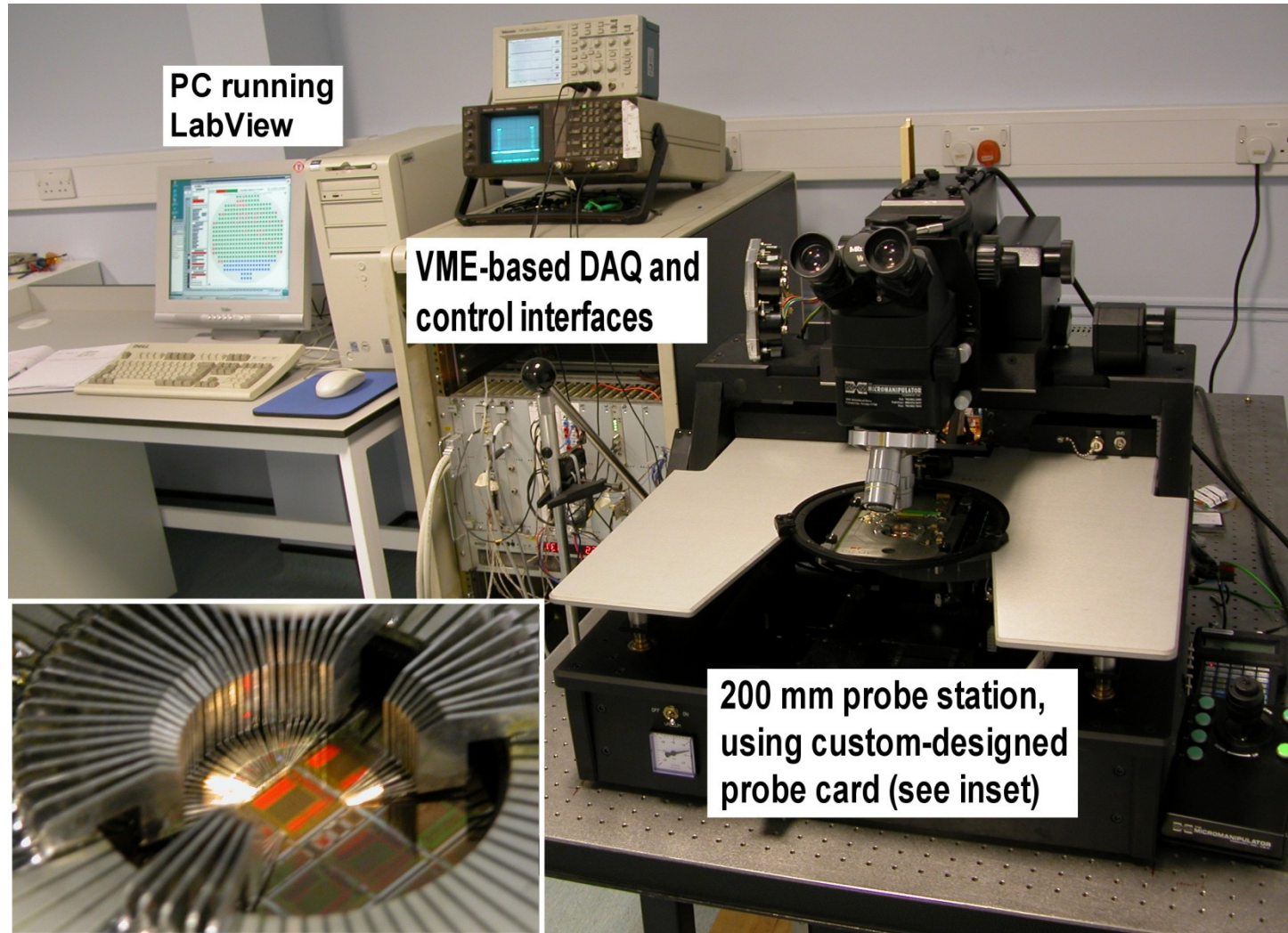




# Wafer Test Probe Station

will re-use some of APV probe-card interface hardware

ancient PC now replaced and probe-station controlling software checked ok



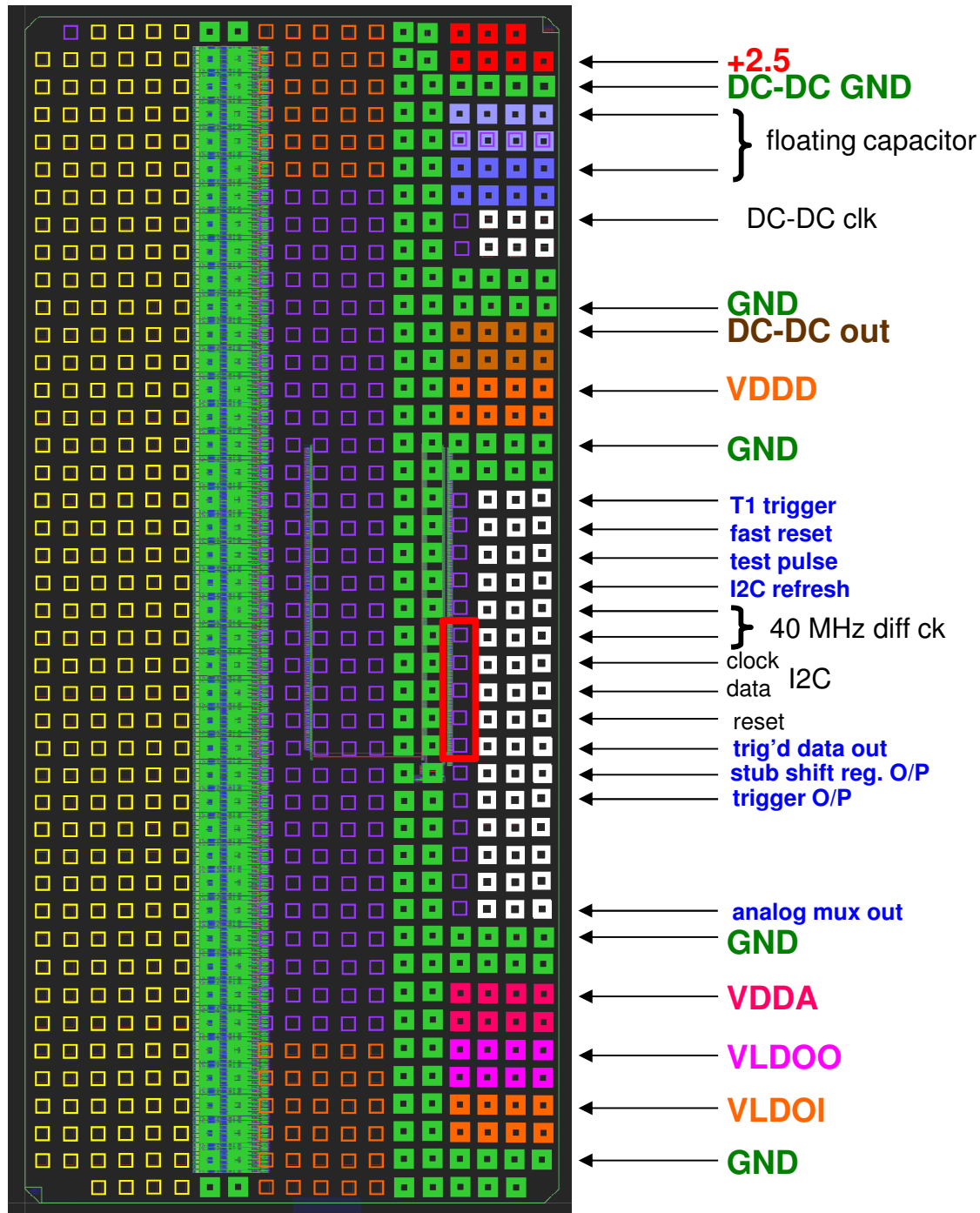
Micromanipulator  
8 inch semi-automatic  
probe station

VME based  
ADC (8 bits)  
RAL SeqSi  
40 MHz CK/T1  
CERN VI2C I/F

PC controls both  
DAQ (VME)  
& probe-station (RS232)



# probe card signals



27 altogether

160 MHz signals left out

can try and use DC-DC and LDO

**but** unlikely to work well

necessary associated capacitors

a long way away from pads