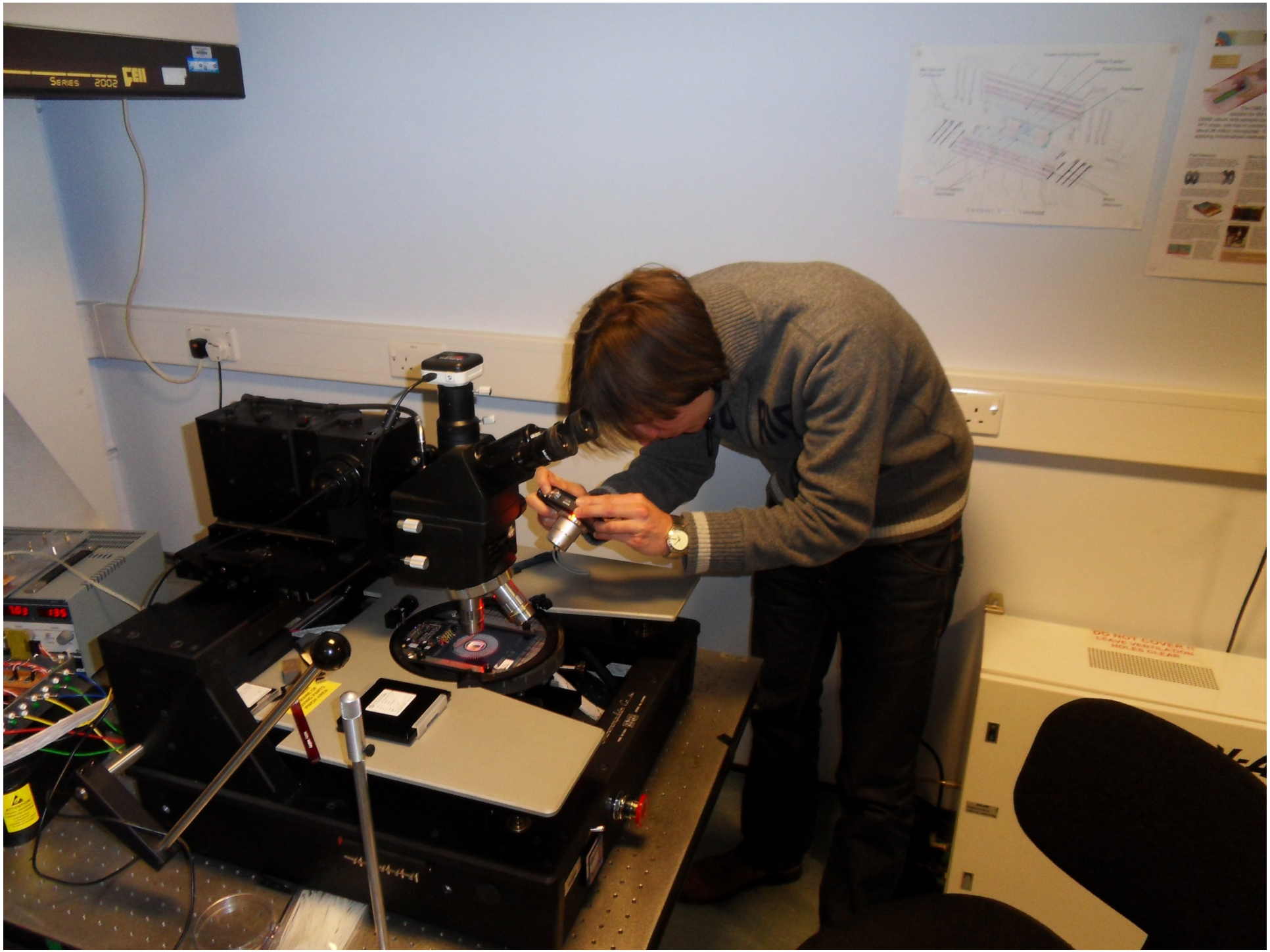
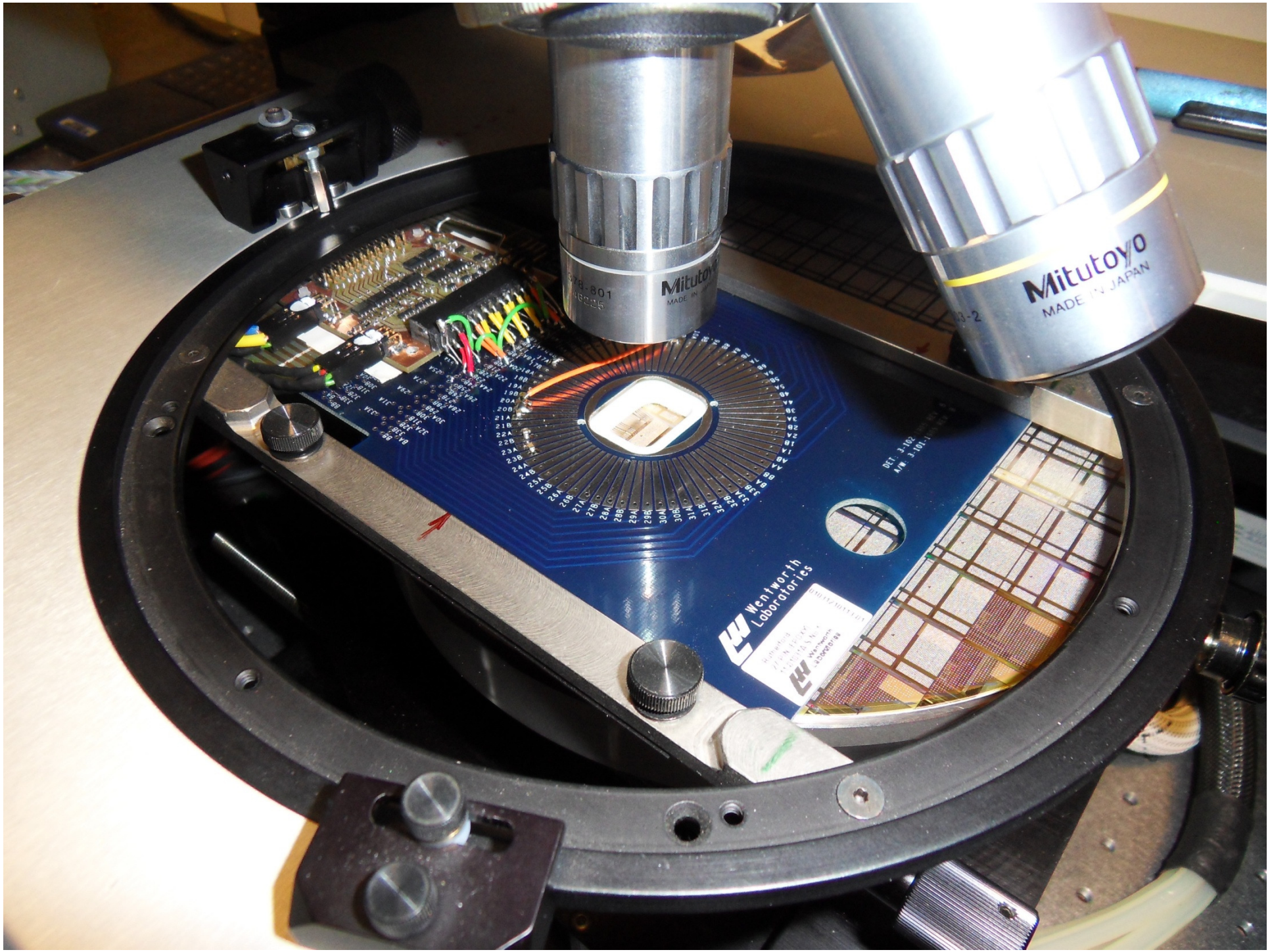
CBC2 wafer testing results

4 (of 8) wafers now probed
- 1st wafer - March 2013 -> 2CBC2 hybrids
- 2nd - September 2013 -> 8CBC2flex hybrids
- 3rd & 4th - August 2014 -> new 8CBC2flex hybrids

will describe evolution of test procedures
& show some analysis of results


SERIES 2002
DO NOT COVER IT


Mitutoyo
MADE IN JAPAN
Wentworth
Laboratories

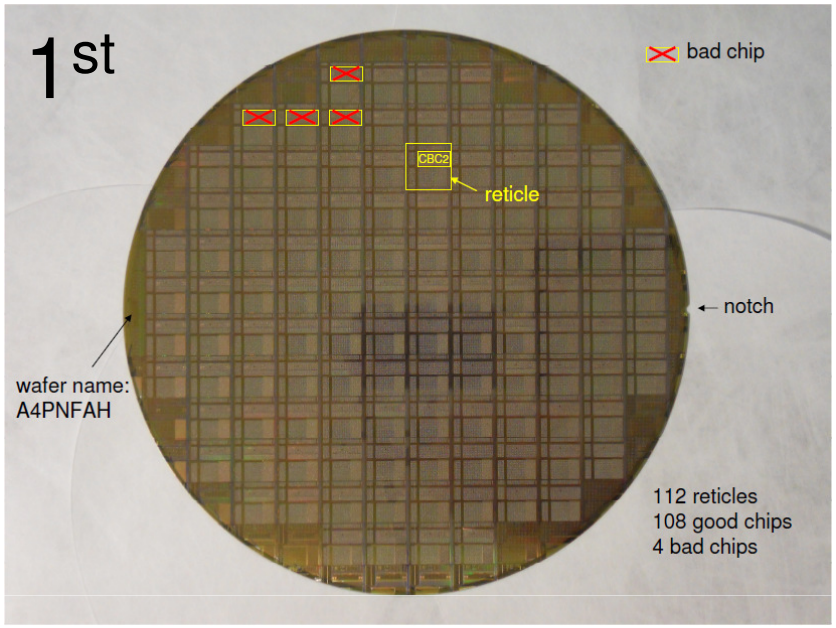
wafer test development

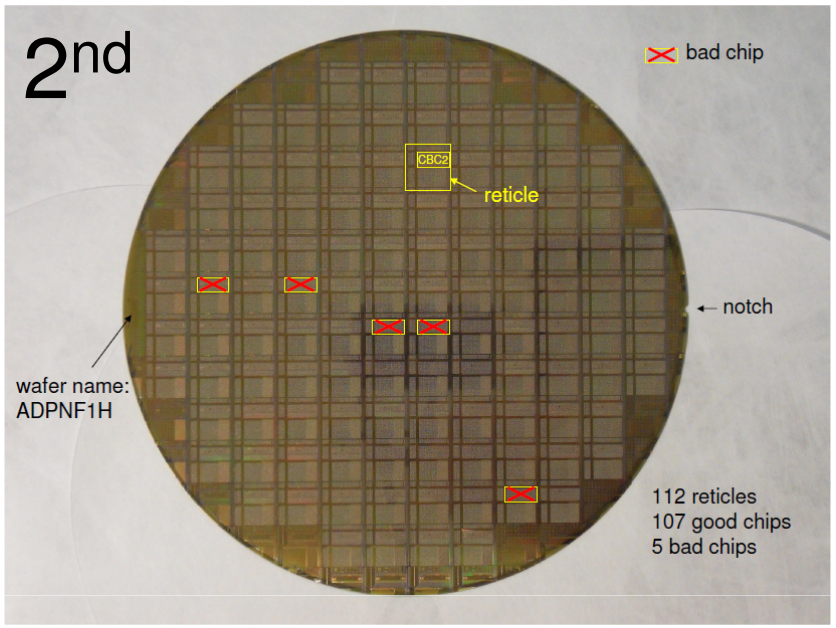
1st wafer, A4PNFAH
- no I2C registers contain stuck bits (write & read back all 1's and all 0's)
- all channels respond to test pulse
- power consumption and some biases swept

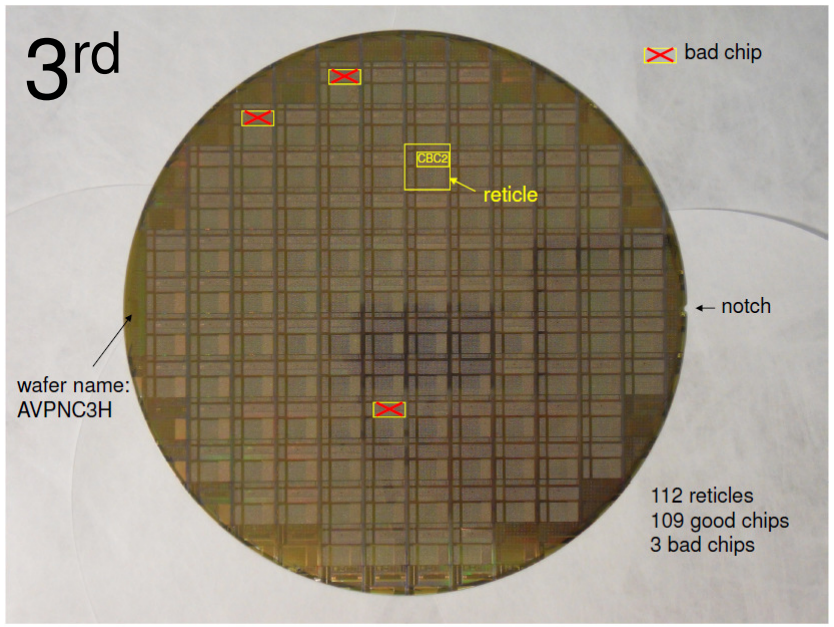
2nd wafer, ADPNF1H, some additional tests
- basic offset tuning
- all pipeline locations accessed looking for stuck cells

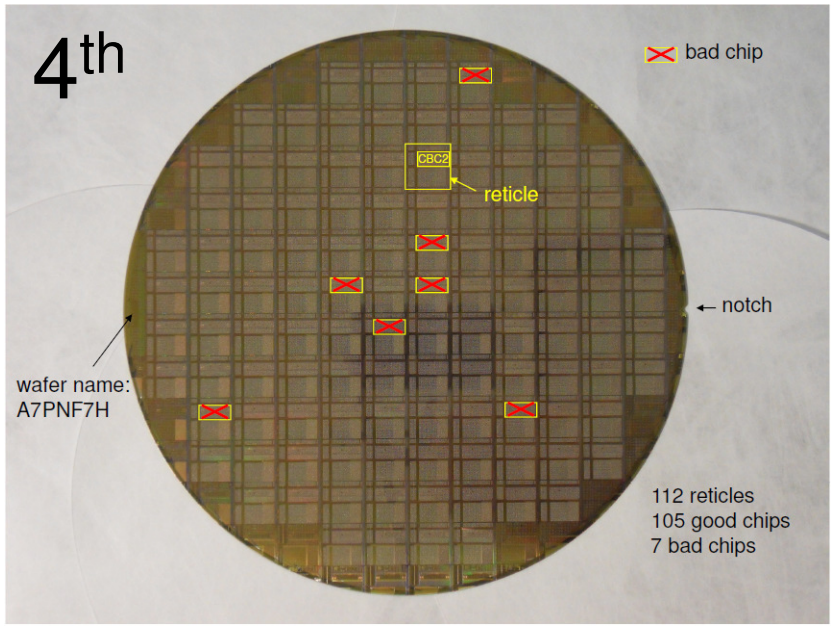
3rd & 4th wafers, A7PNF7H & AVPNC3H, further refinements
- implemented recommended offset tuning procedure
- s-curves for pedestals **&** s-curves with test pulse acquired
- fully automated procedure - takes ~ 5 mins per chip

wafer results maps









LabView front panel for individual chip test

latest version used for wafers 3 and 4

analysis of data from wafers 3 and 4 follows

histograms

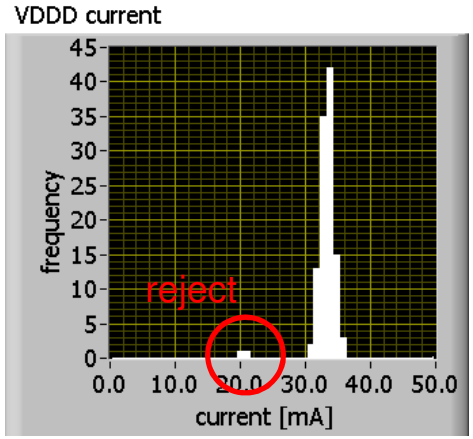
data from all chips from both latest wafers

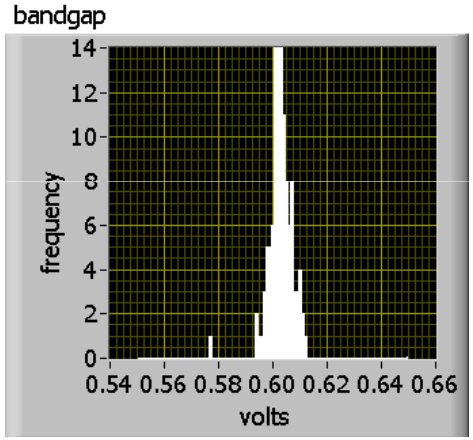
including rejects **VDDD current**

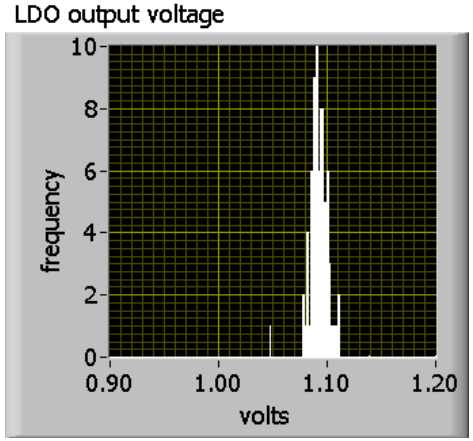
bandgap voltage

LDO output

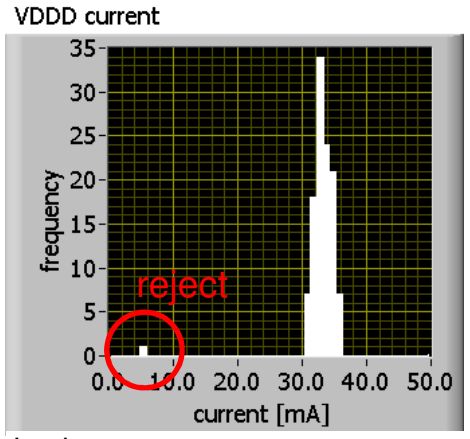
A7PNF7H

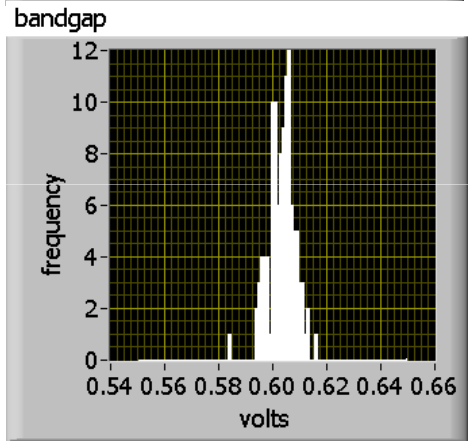


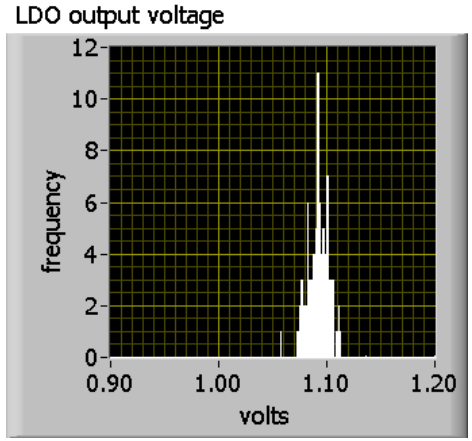




AVPNC3H







s-curves

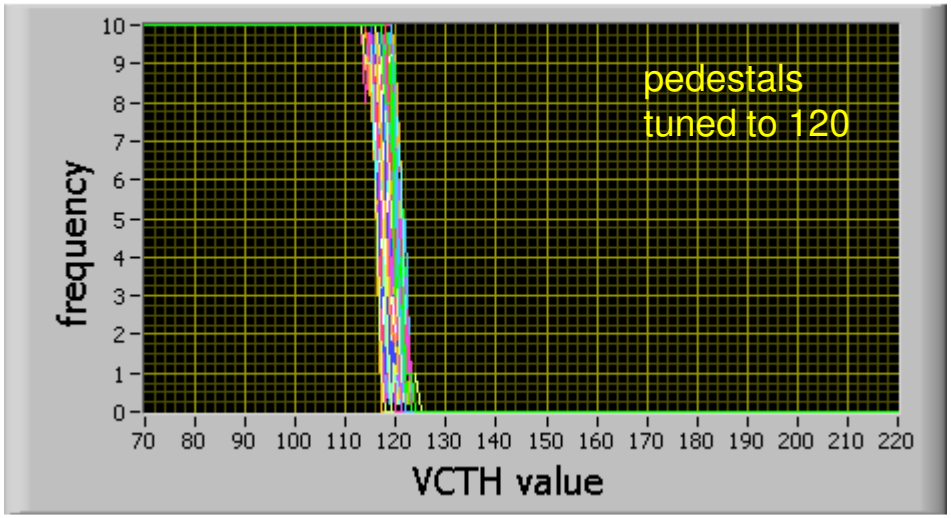
for each channel subtract pedestal from test pulse (s-curve mid-points)

-> gain for each channel

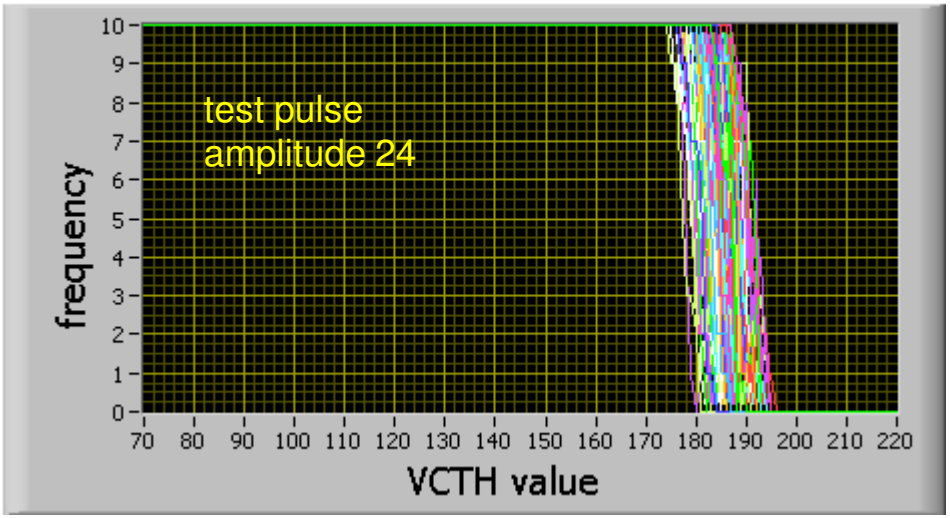
take average of all 254 channels on the chip

do this for all chips on the wafer and histogram

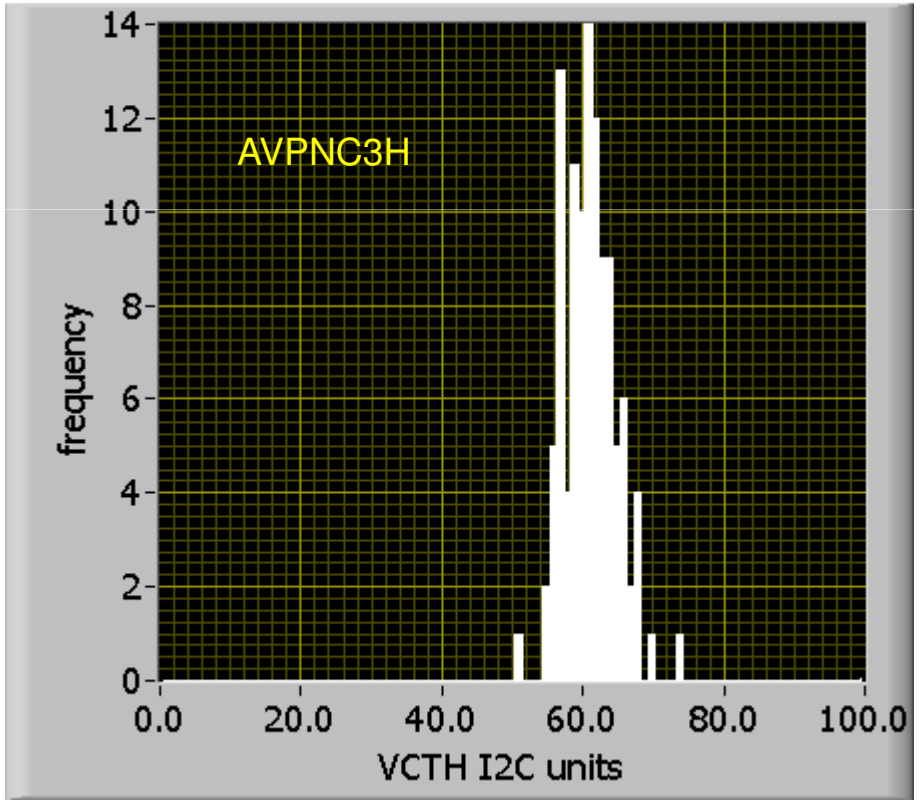
pedestal s-curves



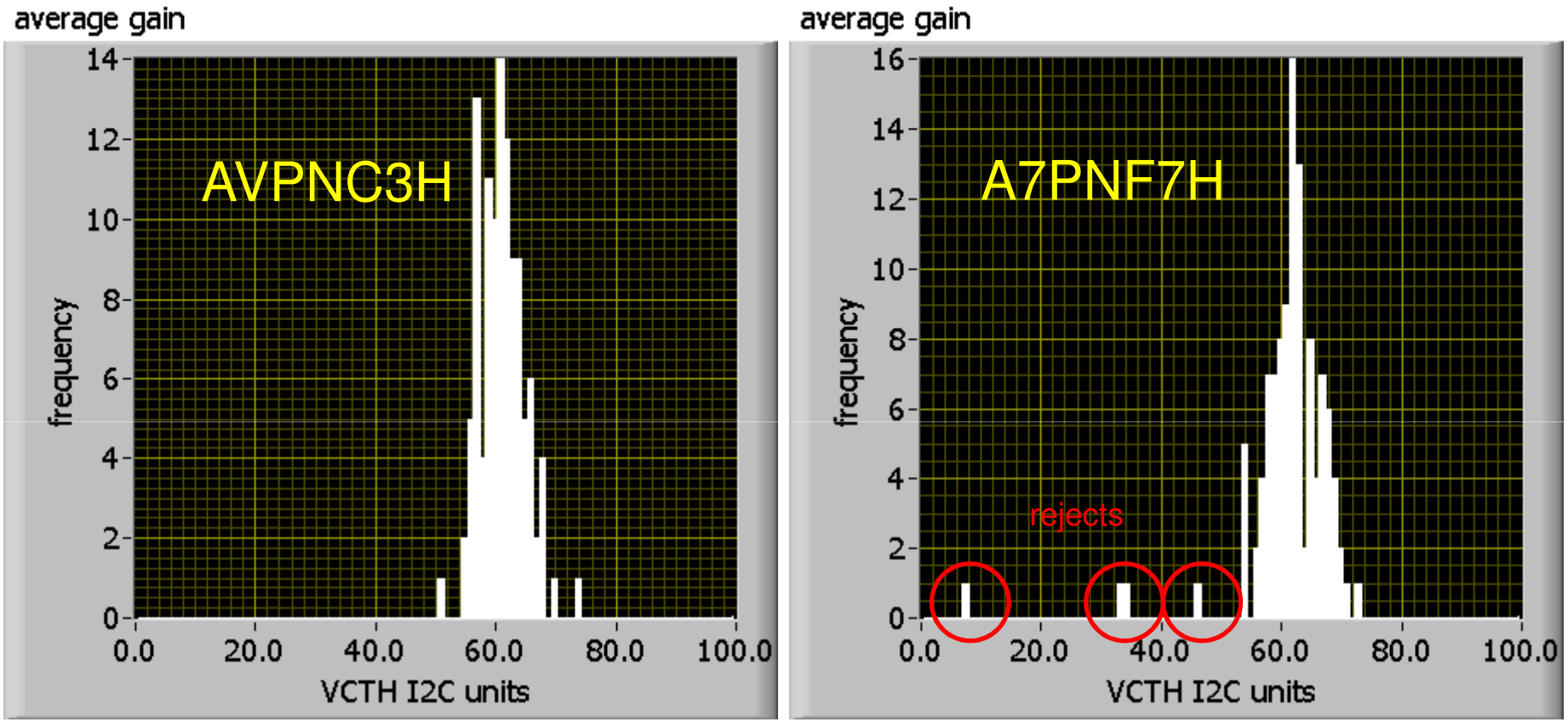
test pulse s-curves



average gain



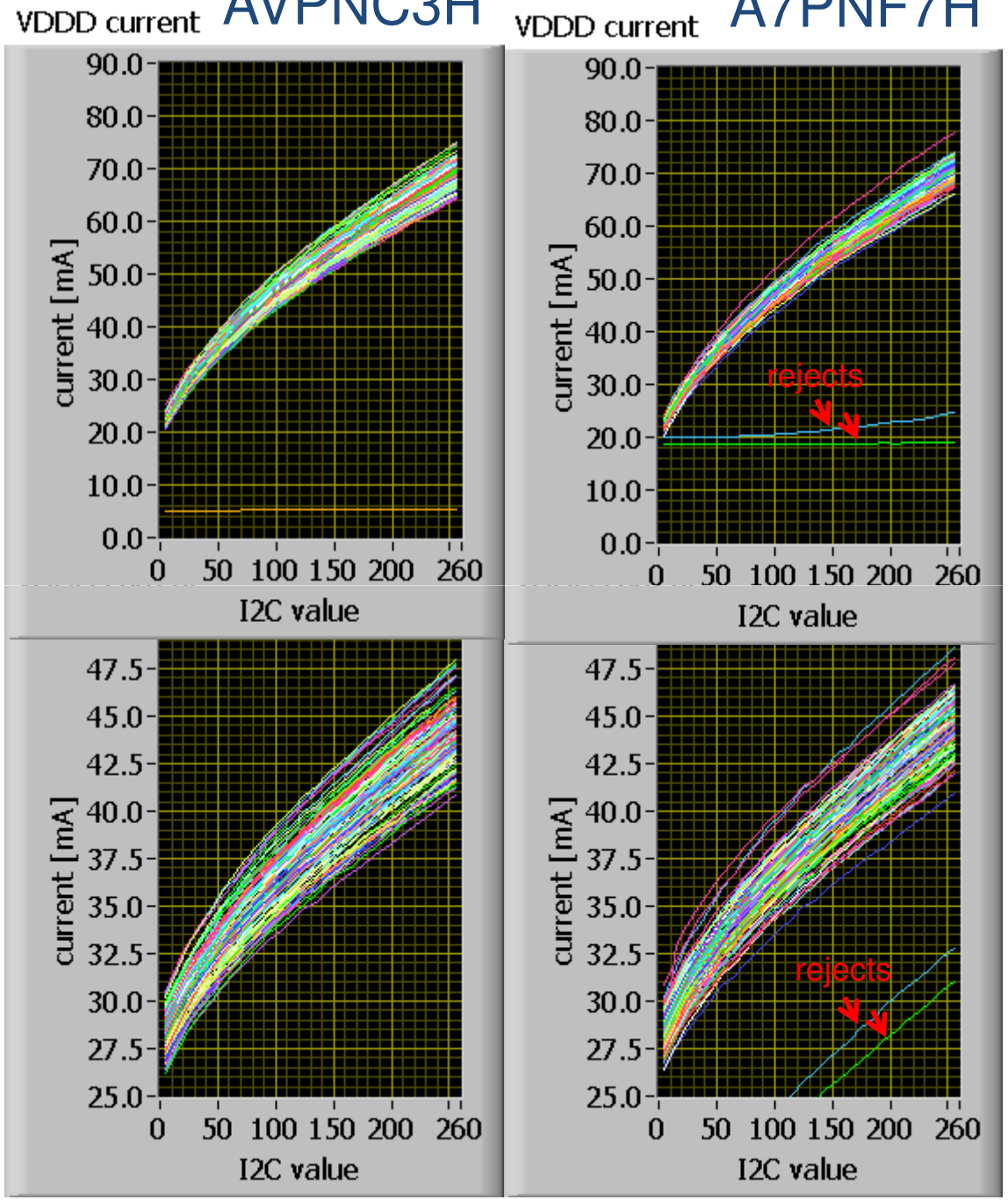
comparing wafers



not much difference in average gain for these two wafers

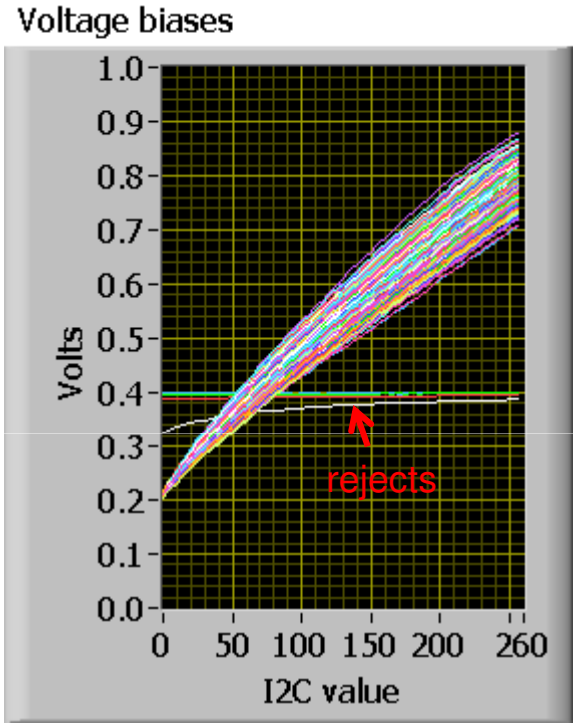
but relies on test pulse charge injection capacitors matching

bias current sweeps

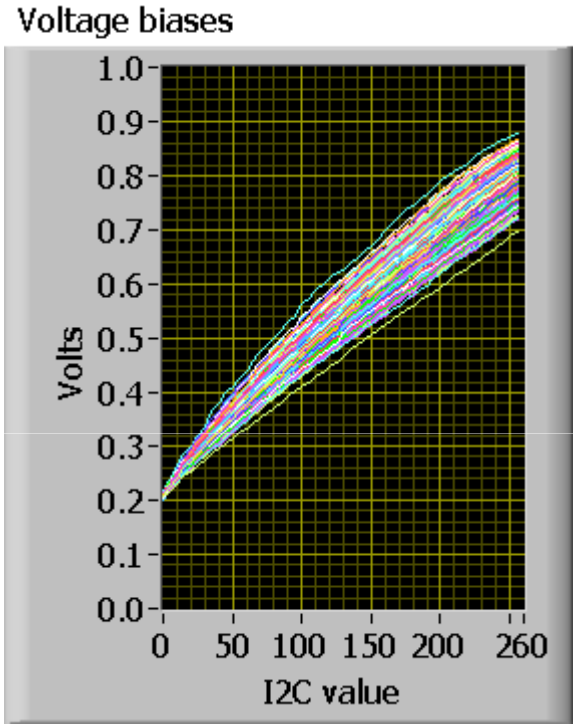


bias voltage sweeps

AVPNC3H

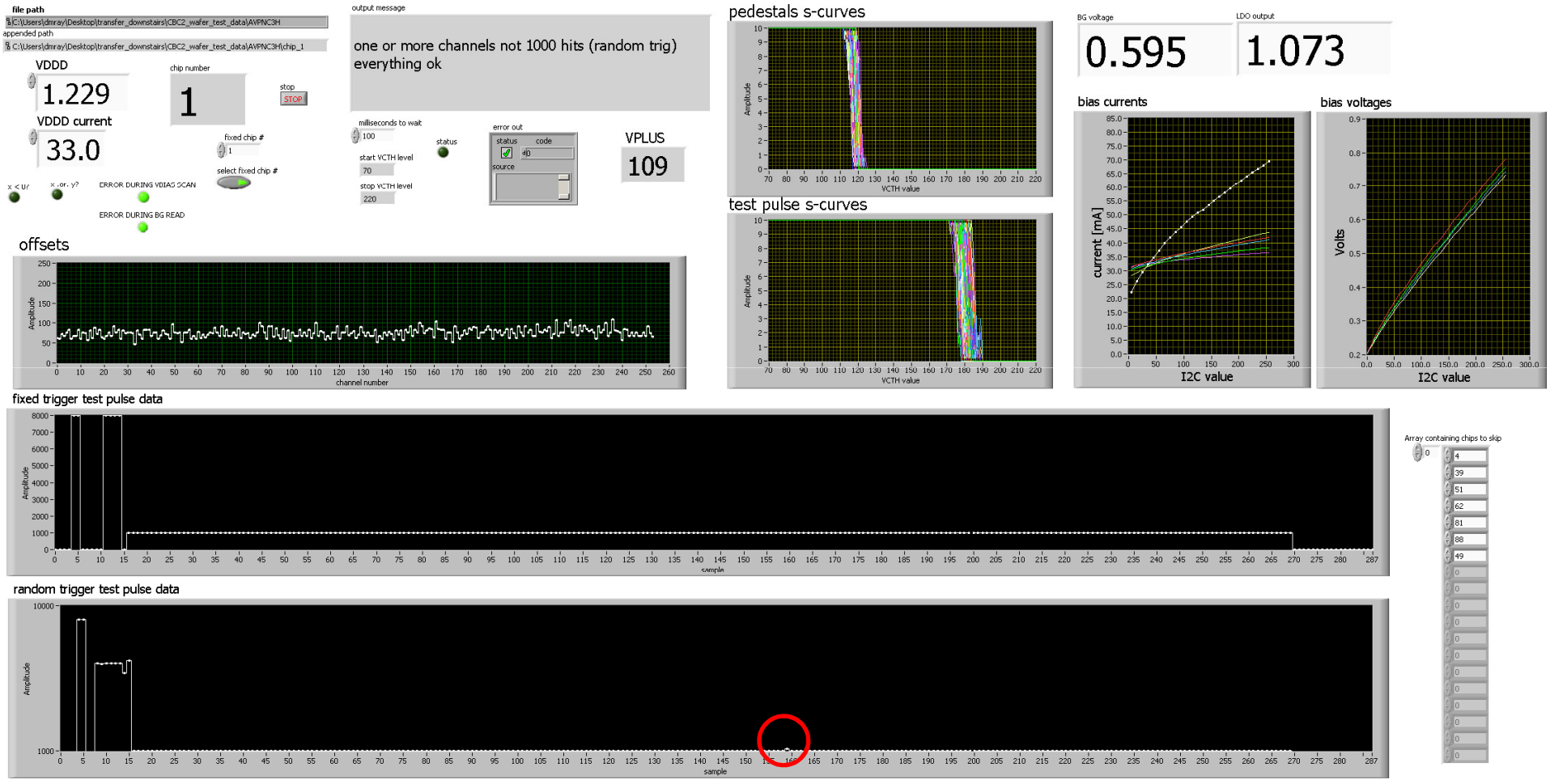


A7PNF7H



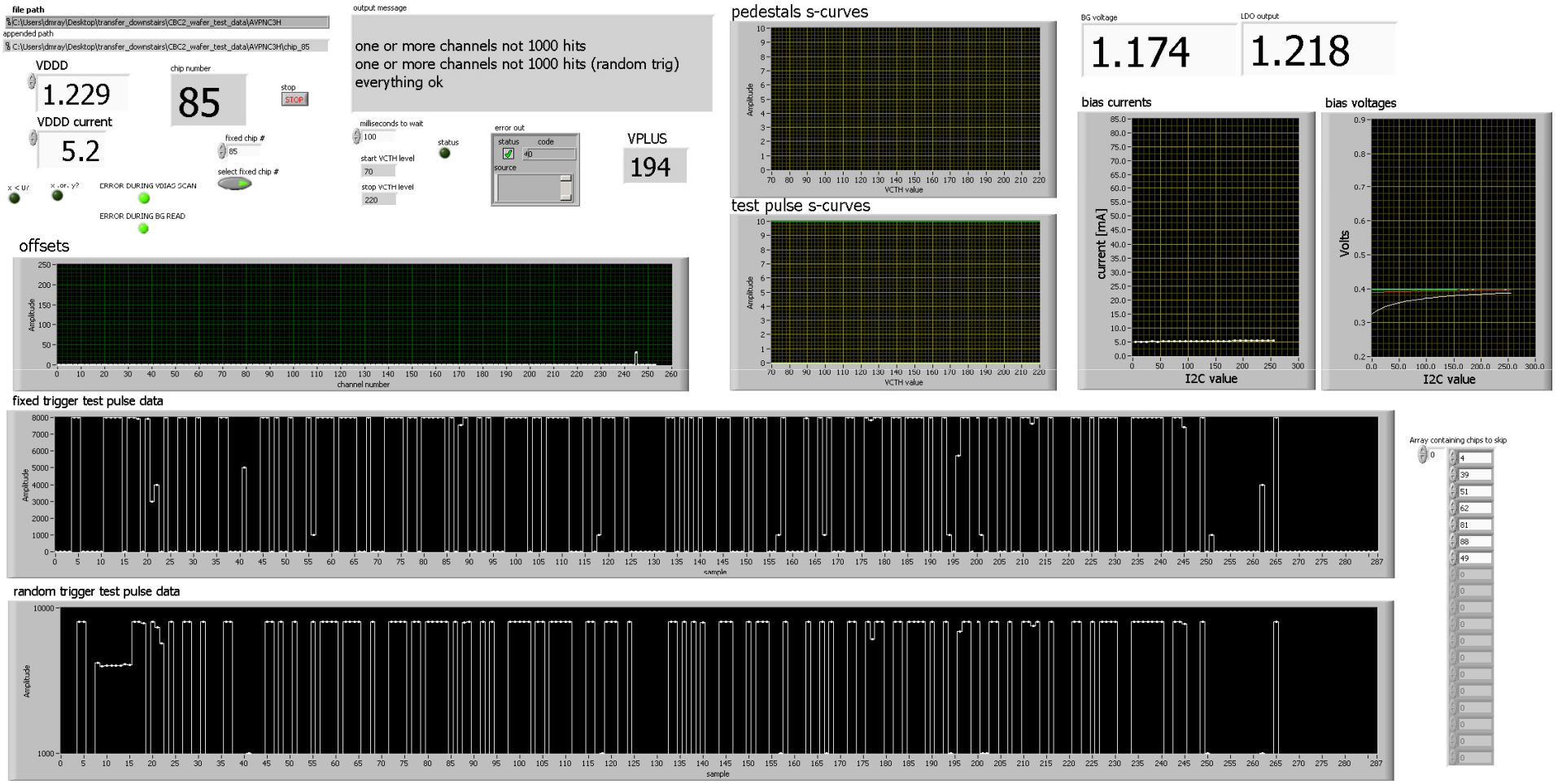
all voltage biases (VPC,VPLUS,VCTH,VPAFB) for all chips

AVPNC3H chip#1 - small problem

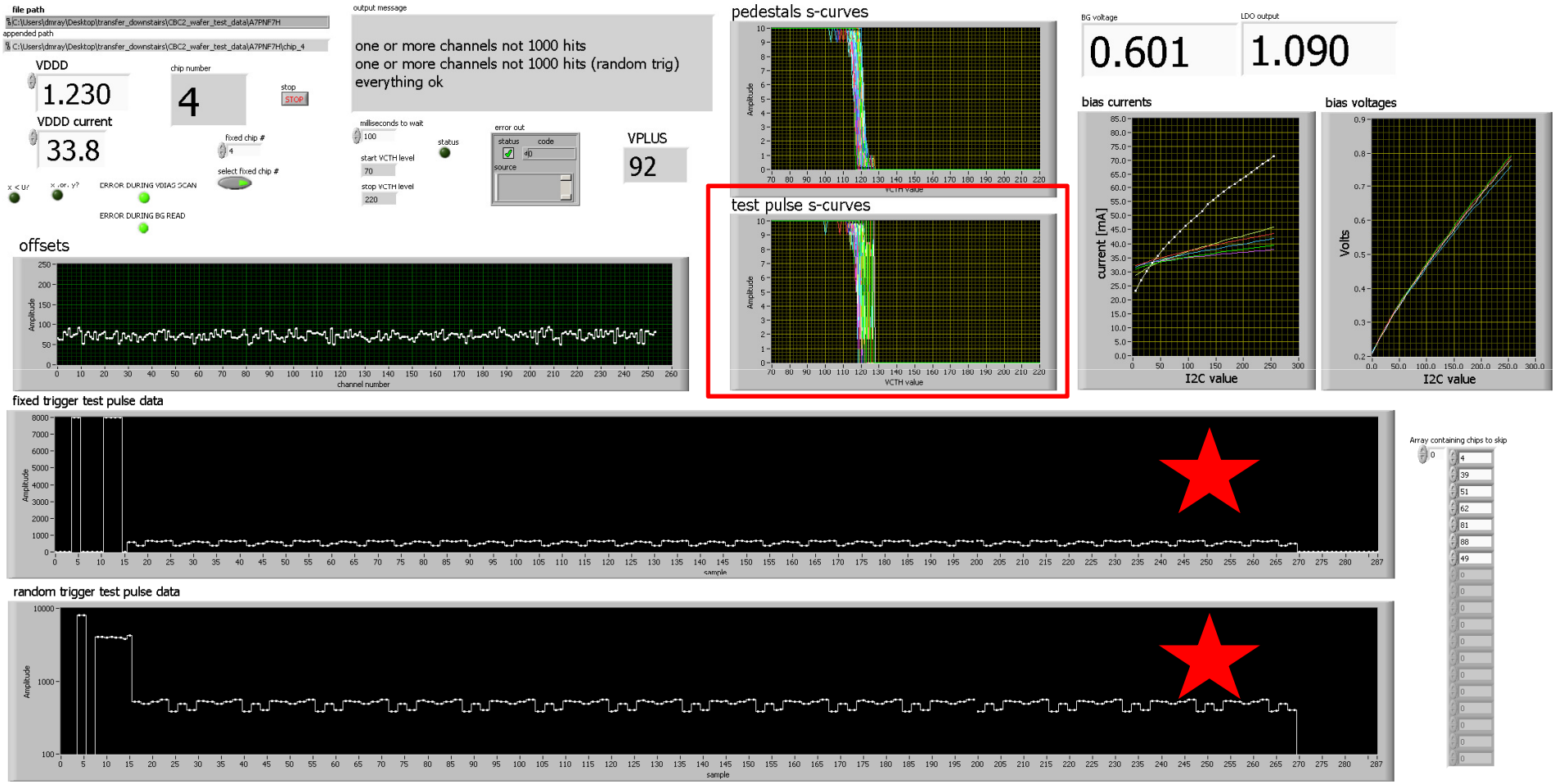


1 bit in pipeline stuck high

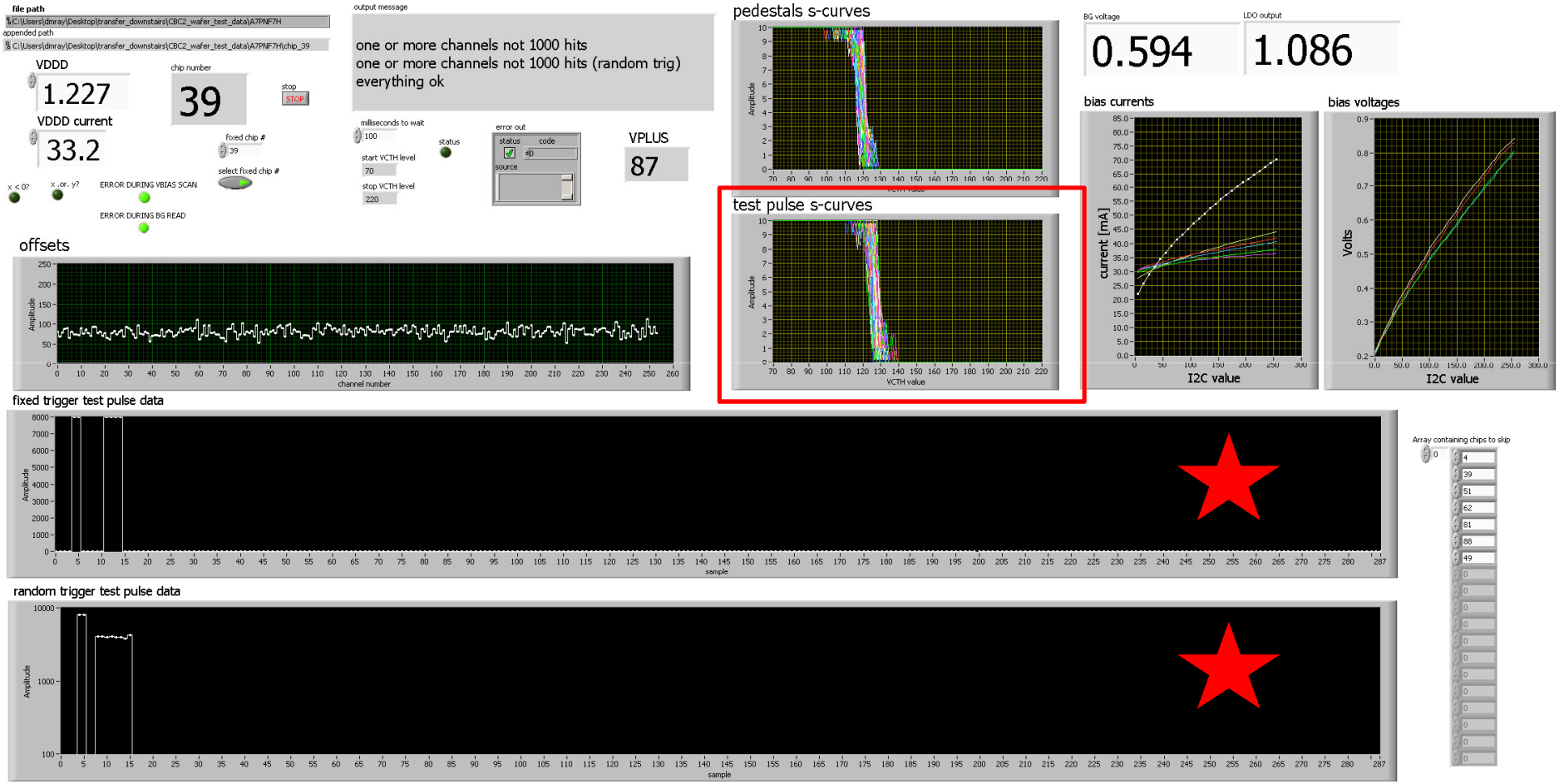
AVPNC3H chip#85 - big problem



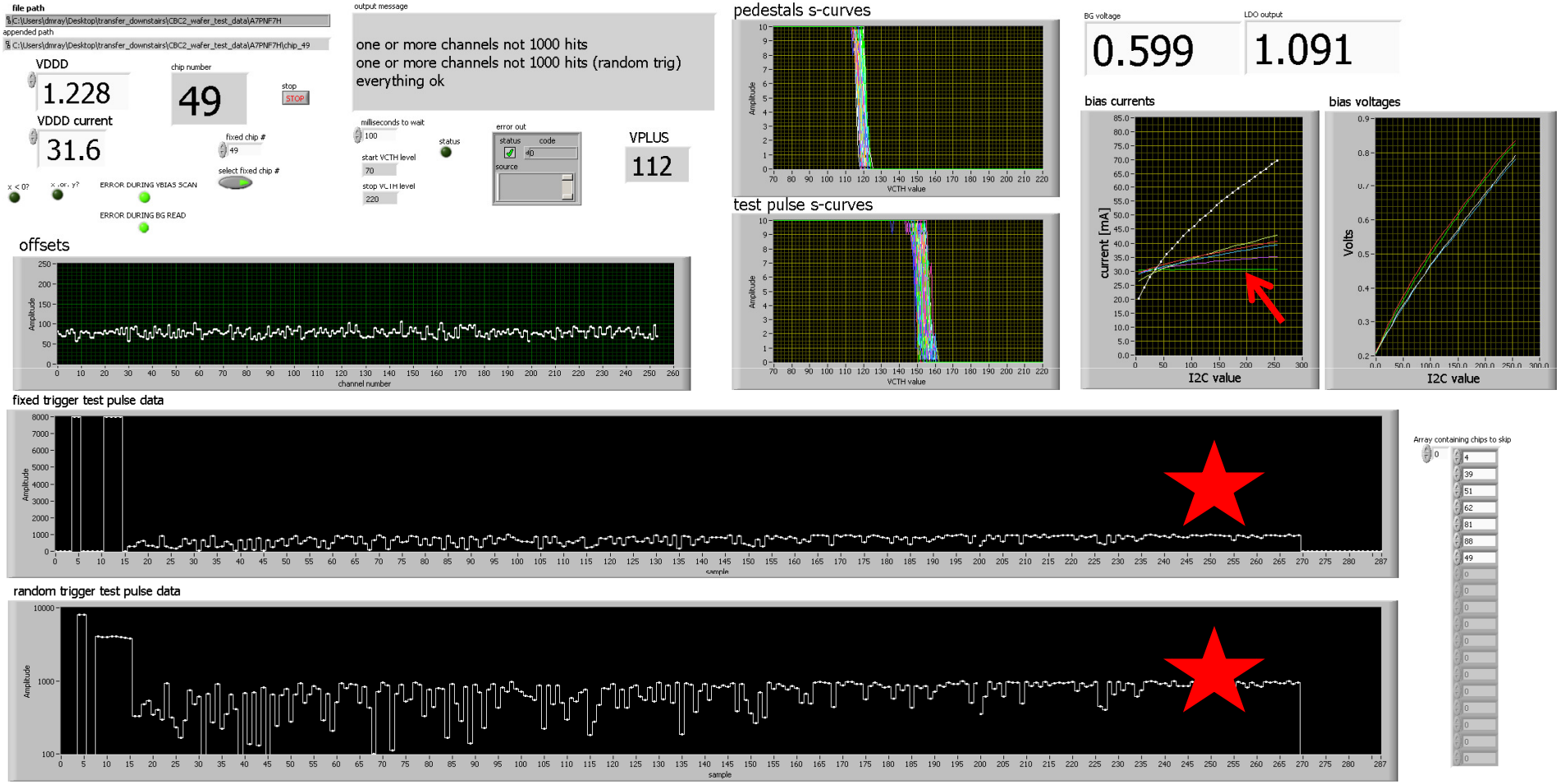
A7PNF7H chip#4



A7PNF7H chip#39

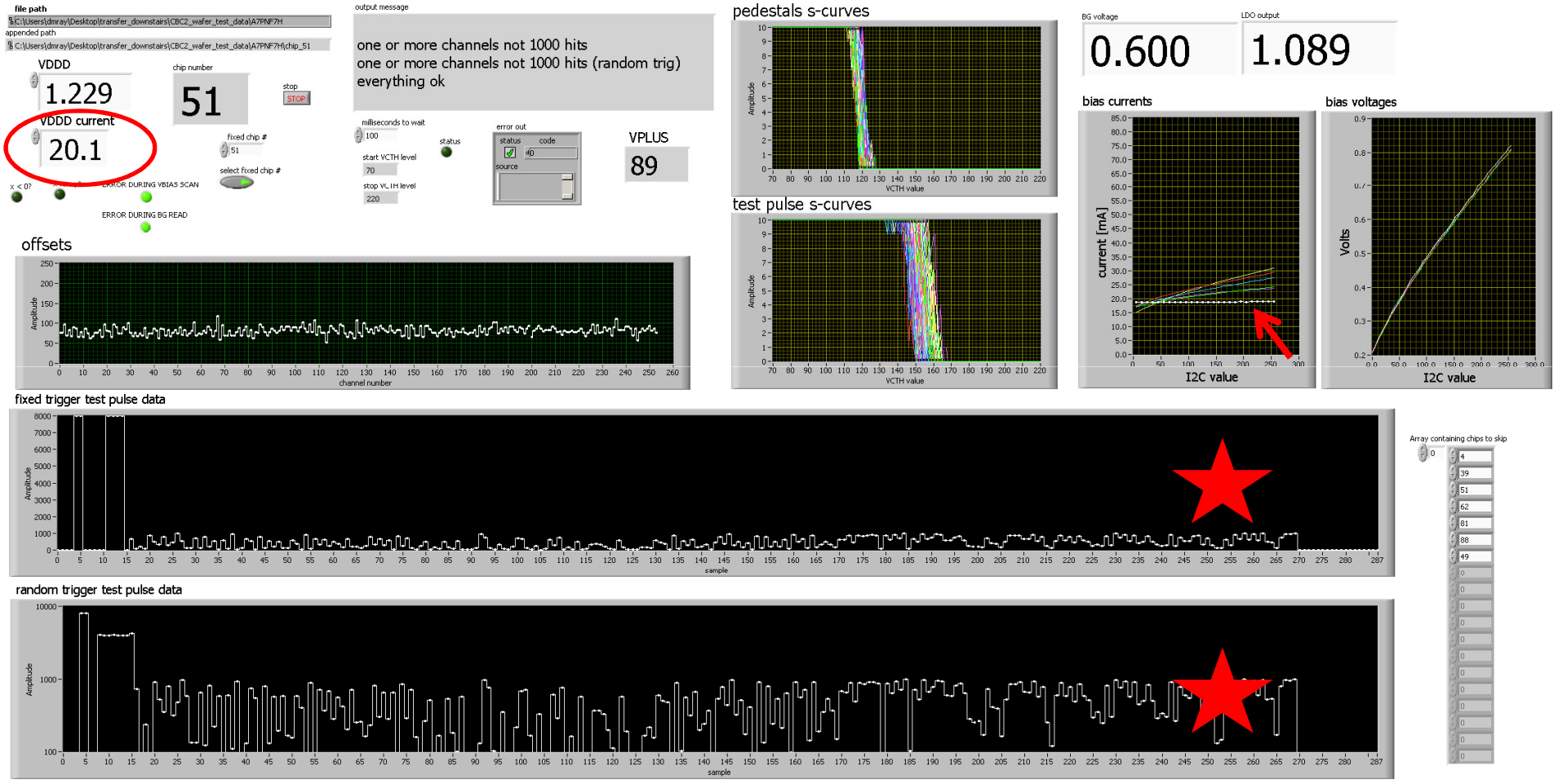


A7PNF7H chip#49



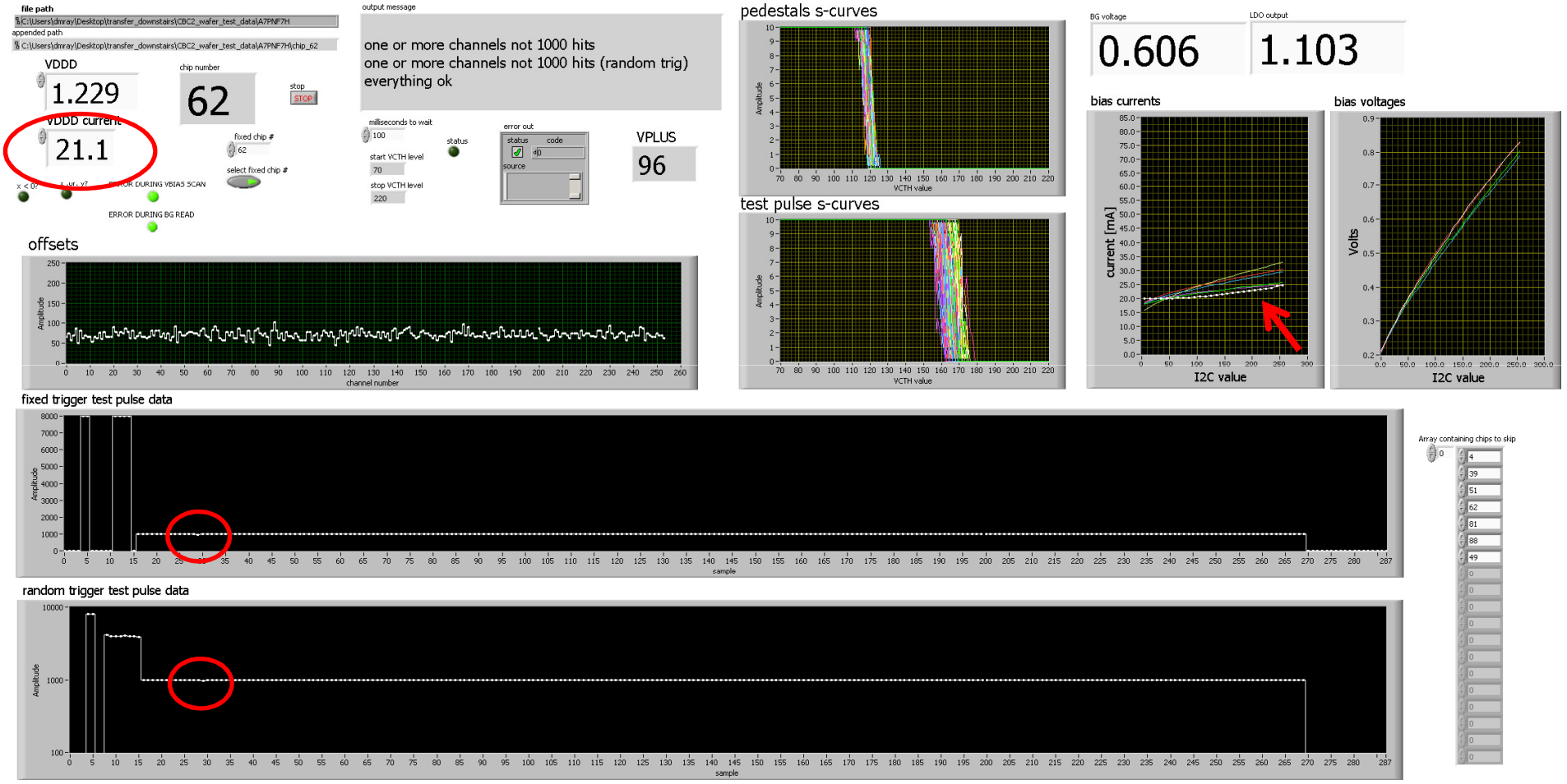
one bias current not working

A7PNF7H chip#51



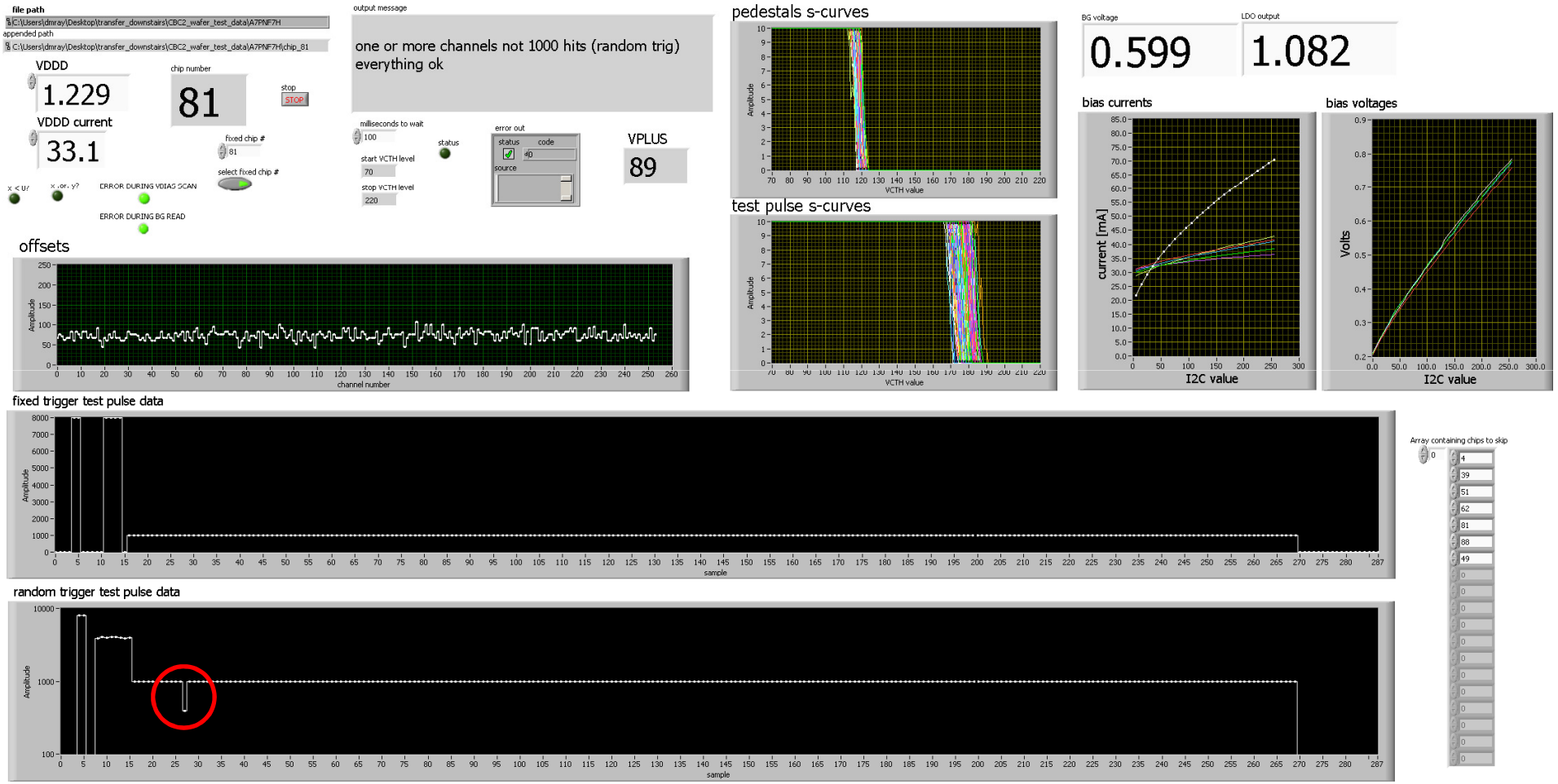
IPRE1 not working

A7PNF7H chip#62



IPRE1 not working

A7PNF7H chip#81



1 bit in pipeline stuck low

A7PNF7H chip#88

1 channel output stuck high

summary

wafer yields to date

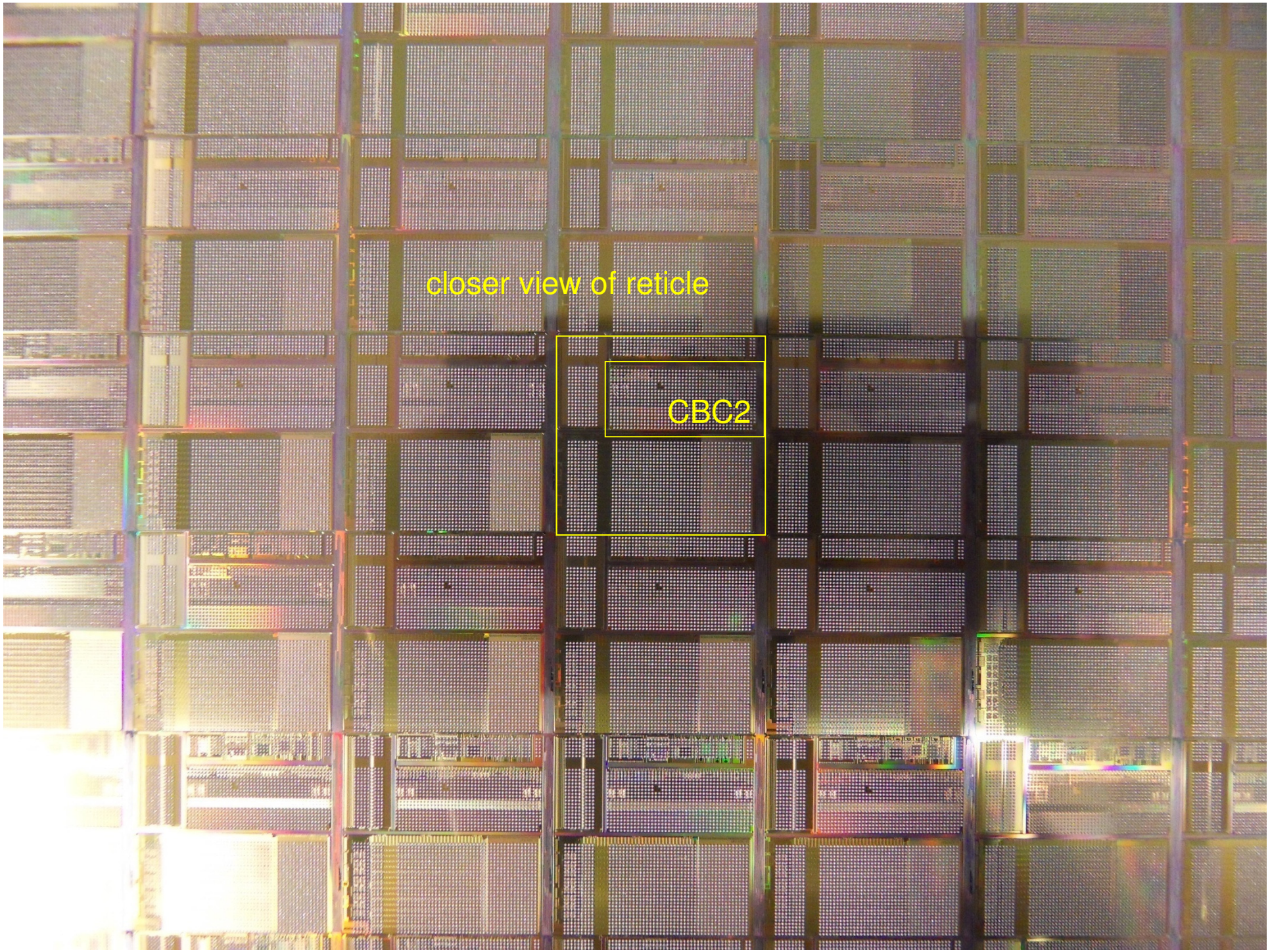
1st , 4 rejects (balls damaged)
2nd , 5 rejects
3rd, 3 rejects
4th, 7 rejects (one rejected by eye)

} more rigorous test procedure for last 2

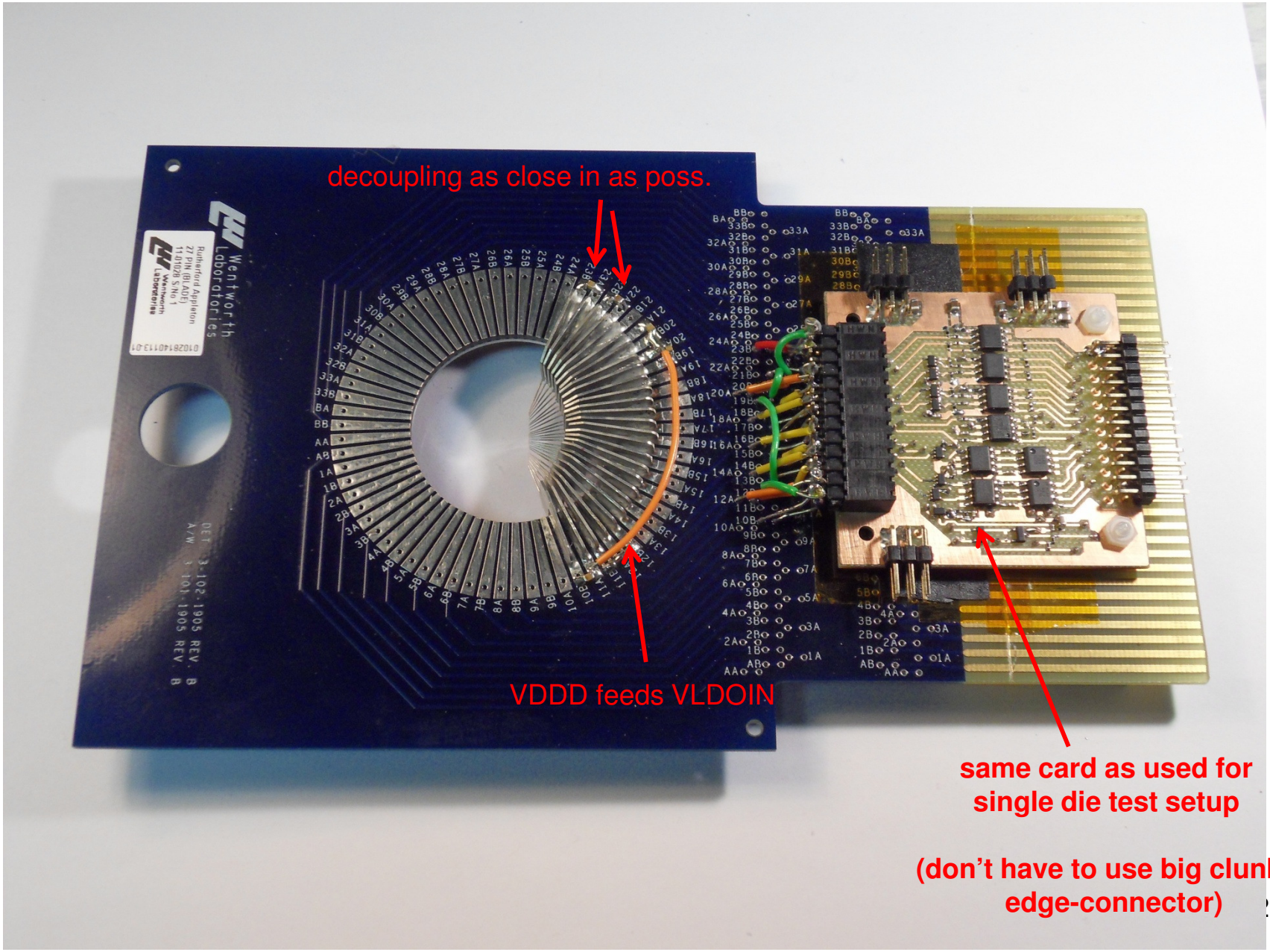
test takes ~5 mins per chip

faster I2C would help - present interface runs at 100 kHz

extra


closer view of reticle
CBC2

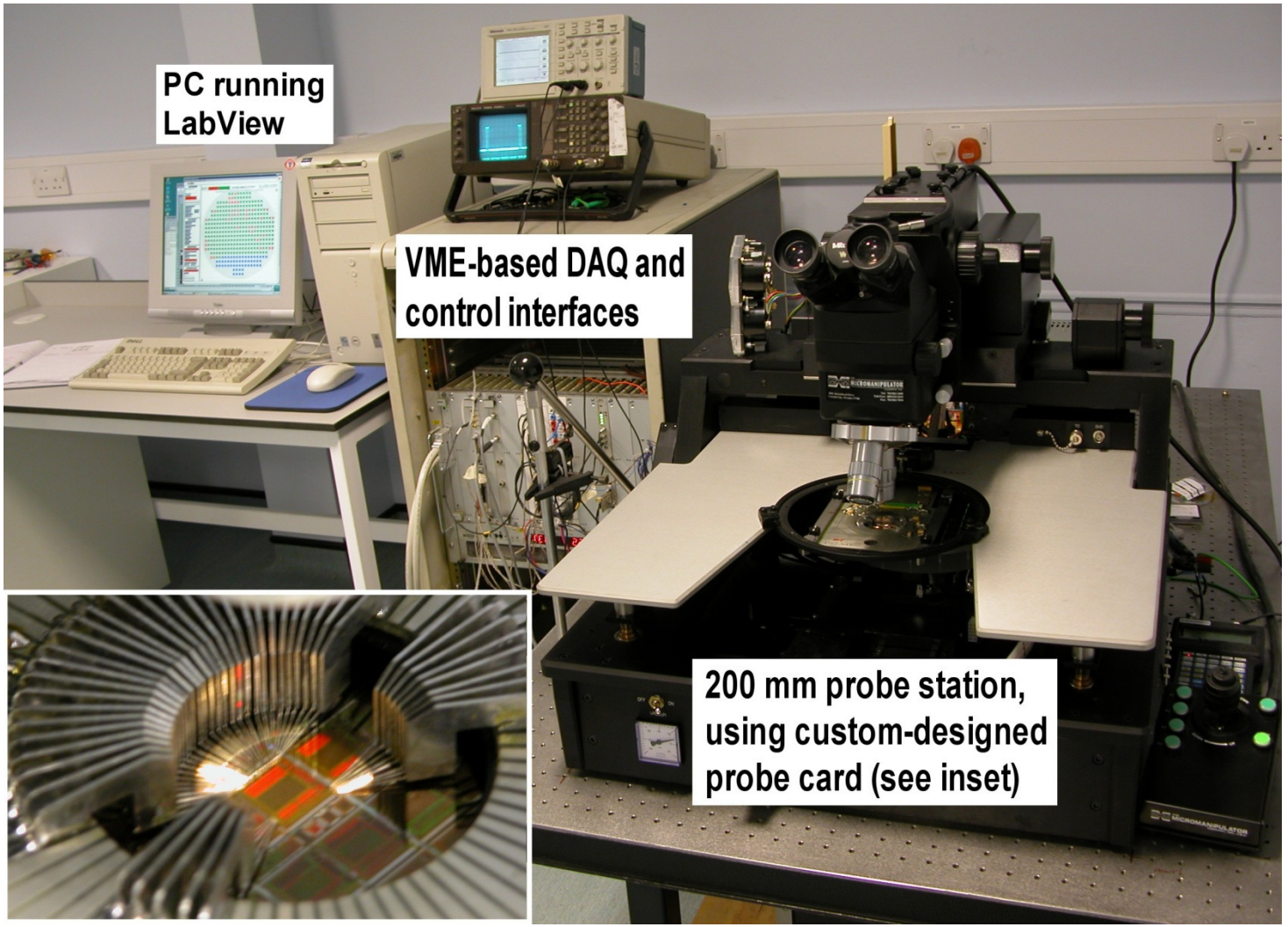
blade probe card for CBC2



Wafer Test Probe Station

will re-use some of APV probe-card interface hardware

ancient PC now replaced and probe-station controlling software checked ok

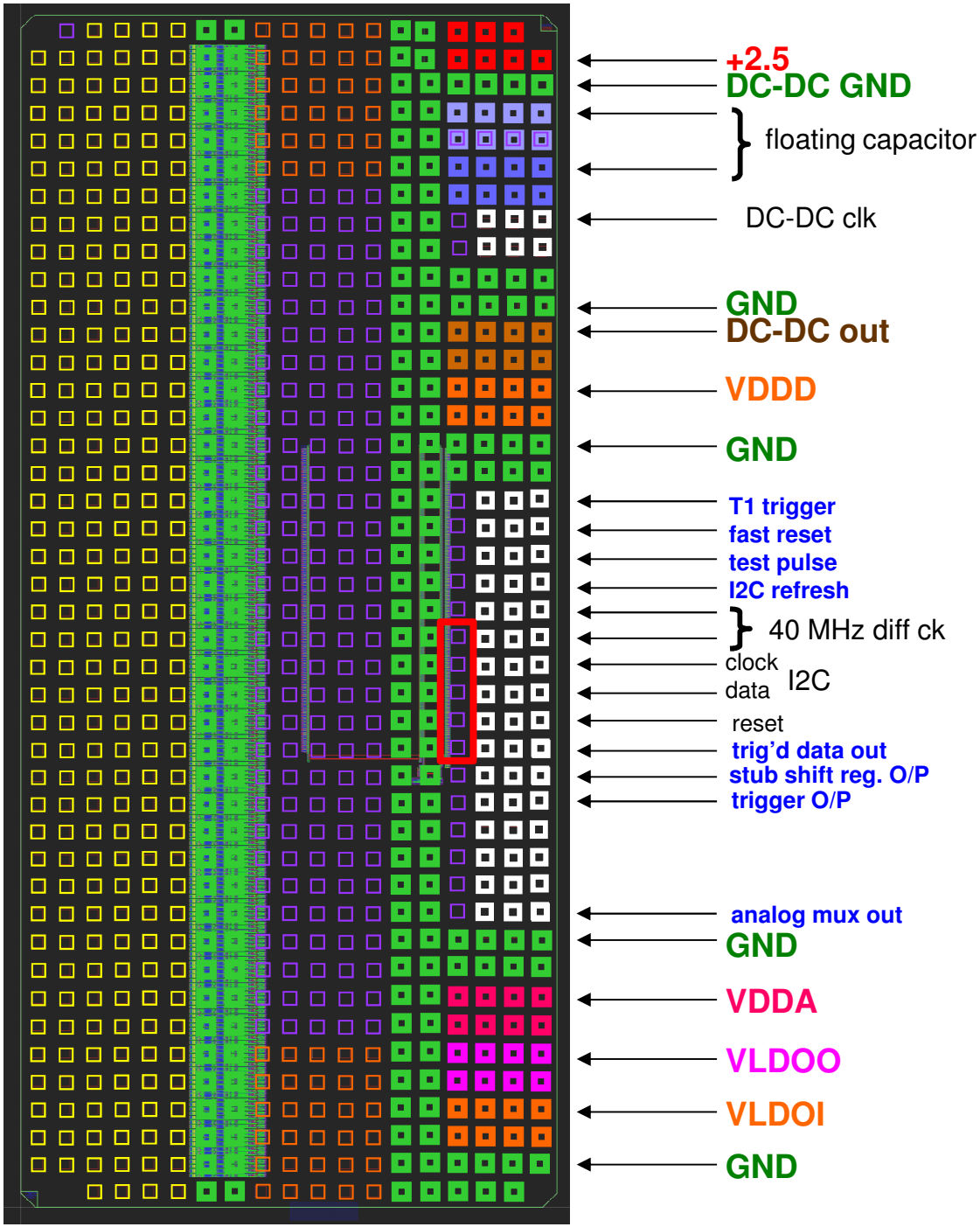


Micromanipulator
8 inch semi–automatic
probe station

VME based
ADC (8 bits)
RAL SeqSi
40 MHz CK/T1
CERN VI2C I/F

PC controls both
DAQ (VME)
& probe-station (RS232)

probe card signals



27 altogether

160 MHz signals left out

can try and use DC-DC and LDO
but unlikely to work well
necessary associated capacitors
a long way away from pads