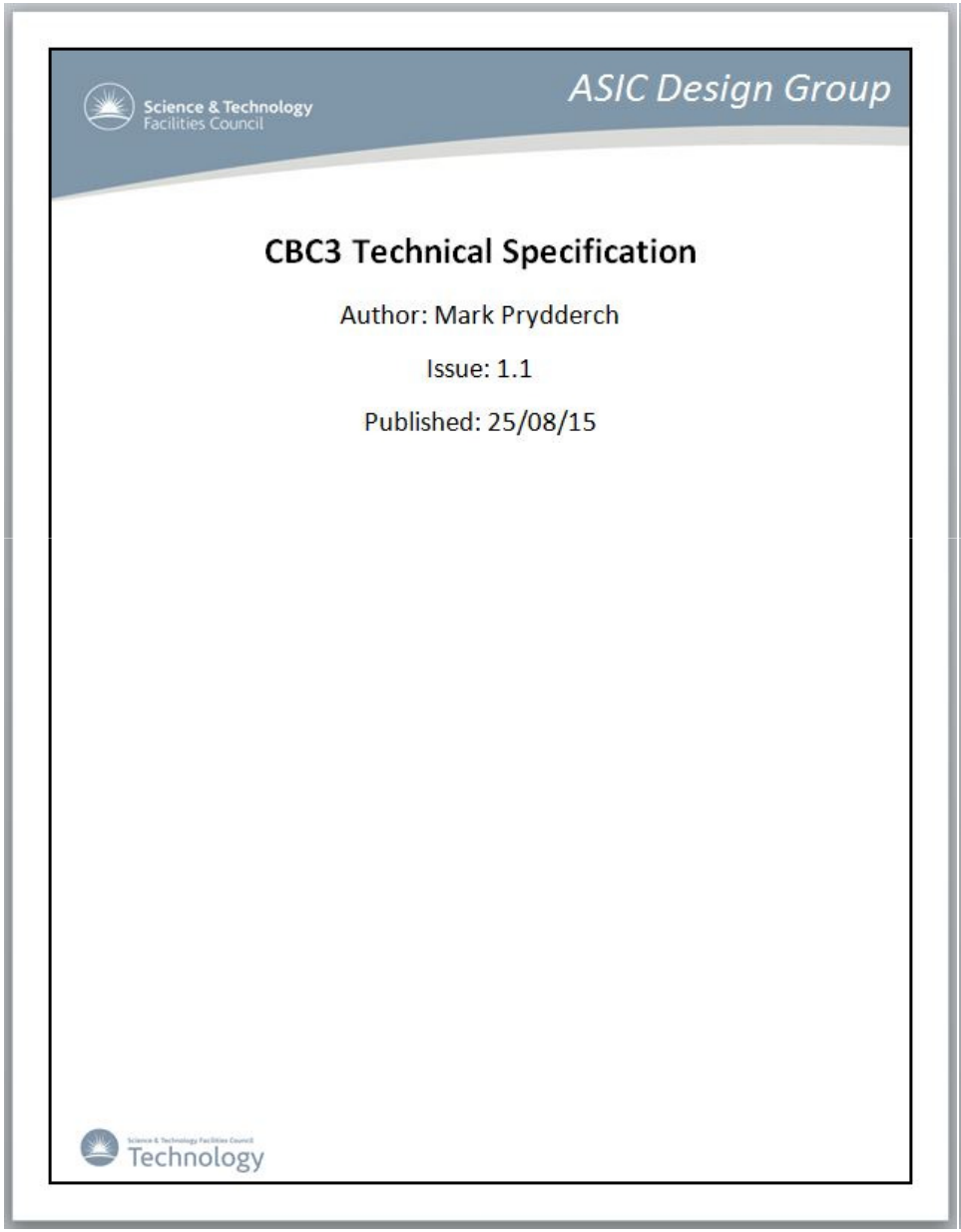
# CBC3 Progress


Imperial College London

Science & Technology Facilities Council

# Updated Technical Spec Document



Science & Technology Facilities Council

ASIC Design Group

**CBC3 Technical Specification**

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Issue: 1.1

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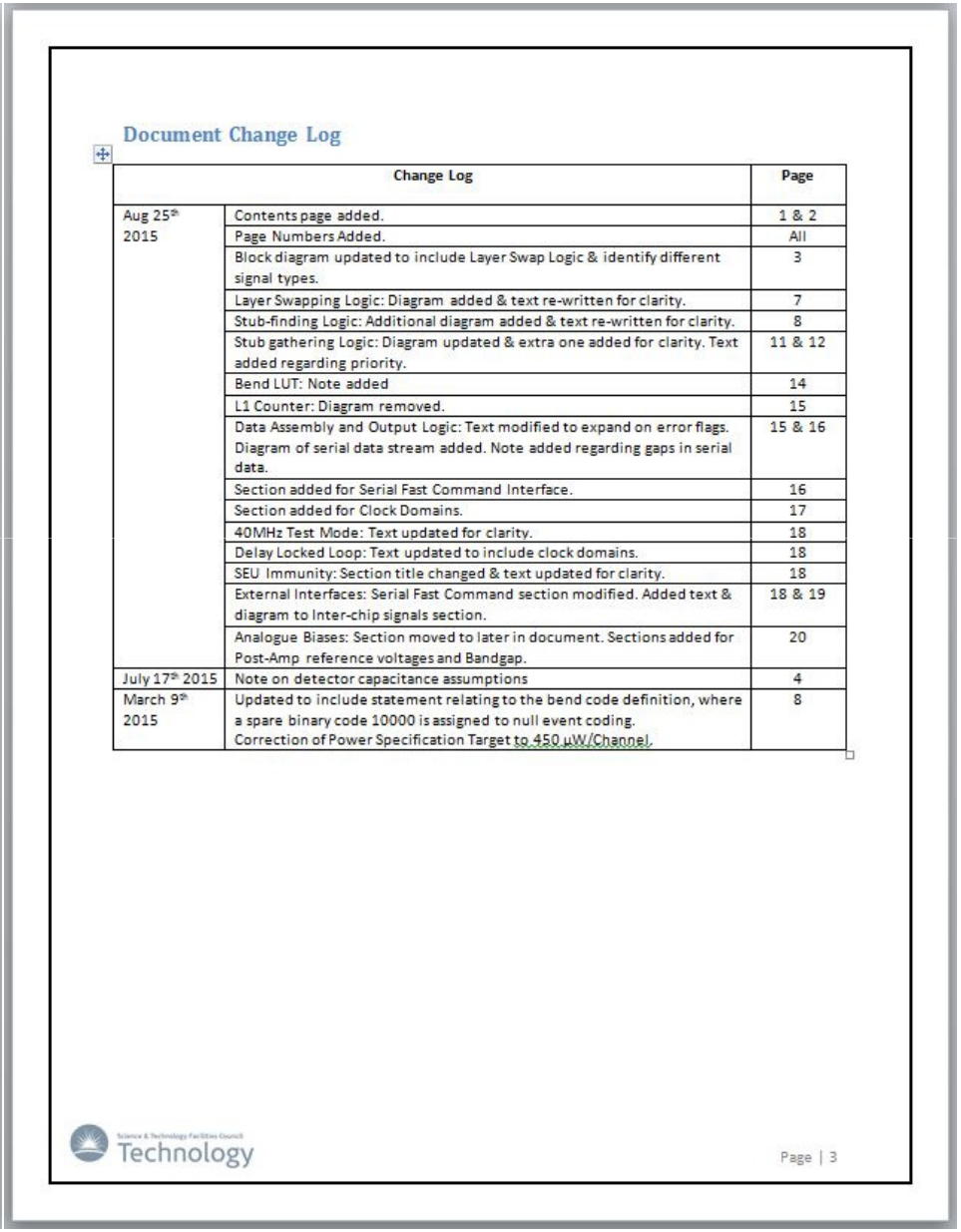

**Document Change Log**

| Change Log | | Page |
|---|---|---|
| Aug 25th 2015 | Contents page added. | 1 & 2 |
| | Page Numbers Added. | All |
| | Block diagram updated to include Layer Swap Logic & identify different signal types. | 3 |
| | Layer Swapping Logic: Diagram added & text re-written for clarity. | 7 |
| | Stub-finding Logic: Additional diagram added & text re-written for clarity. | 8 |
| | Stub gathering Logic: Diagram updated & extra one added for clarity. Text added regarding priority. | 11 & 12 |
| | Bend LUT: Note added | 14 |
| | L1 Counter: Diagram removed. | 15 |
| | Data Assembly and Output Logic: Text modified to expand on error flags. Diagram of serial data stream added. Note added regarding gaps in serial data. | 15 & 16 |
| | Section added for Serial Fast Command Interface. | 16 |
| | Section added for Clock Domains. | 17 |
| | 40MHz Test Mode: Text updated for clarity. | 18 |
| | Delay Locked Loop: Text updated to include clock domains. | 18 |
| | SEU Immunity: Section title changed & text updated for clarity. | 18 |
| | External Interfaces: Serial Fast Command section modified. Added text & diagram to Inter-chip signals section. | 18 & 19 |
| | Analogue Biases: Section moved to later in document. Sections added for Post-Amp reference voltages and Bandgap. | 20 |
| July 17th 2015 | Note on detector capacitance assumptions | 4 |
| March 9th 2015 | Updated to include statement relating to the bend code definition, where a spare binary code 10000 is assigned to null event coding. Correction of Power Specification Target to 450 µW/Channel. | 8 |

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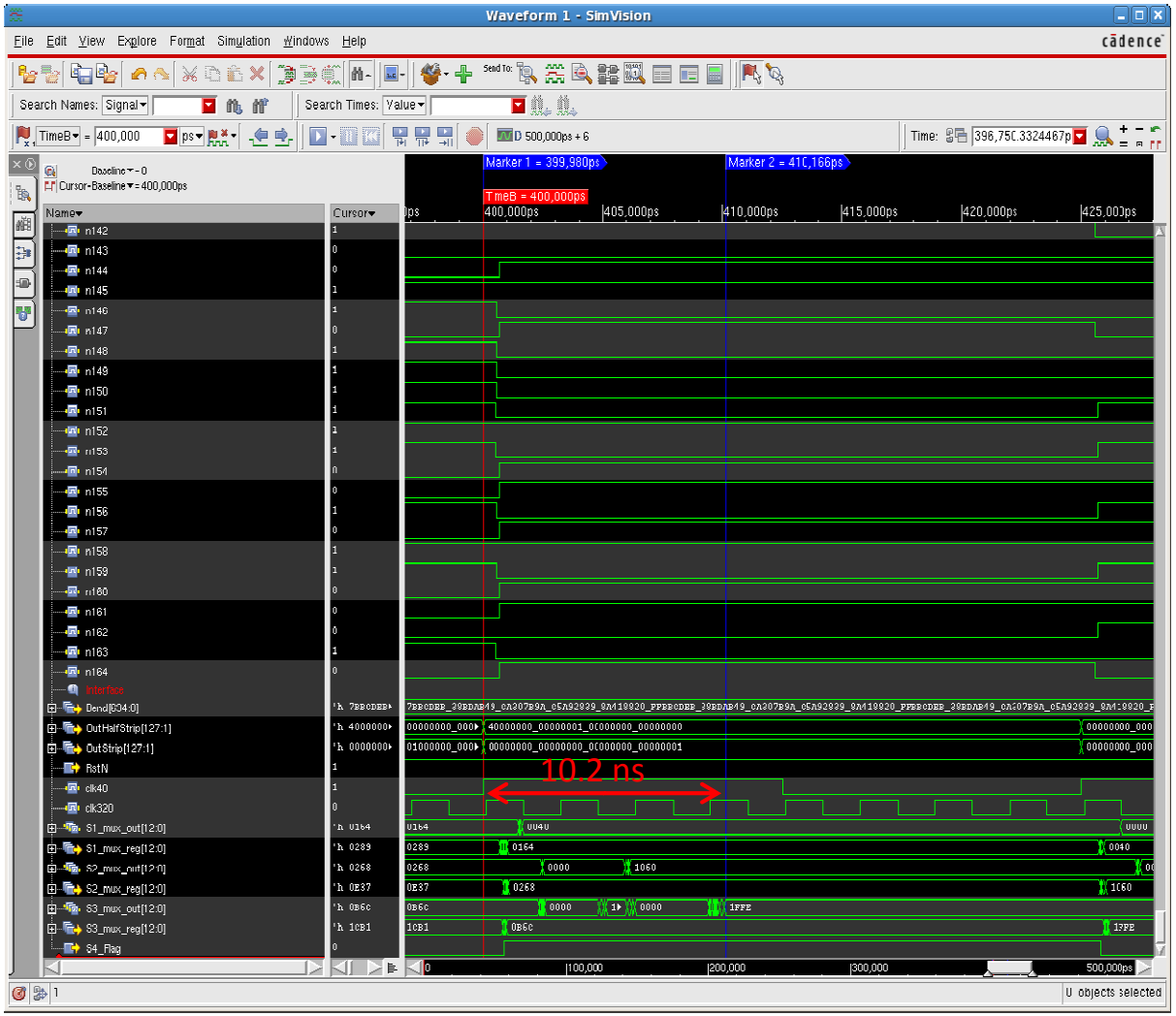
Page | 3

# Post Design Review actions

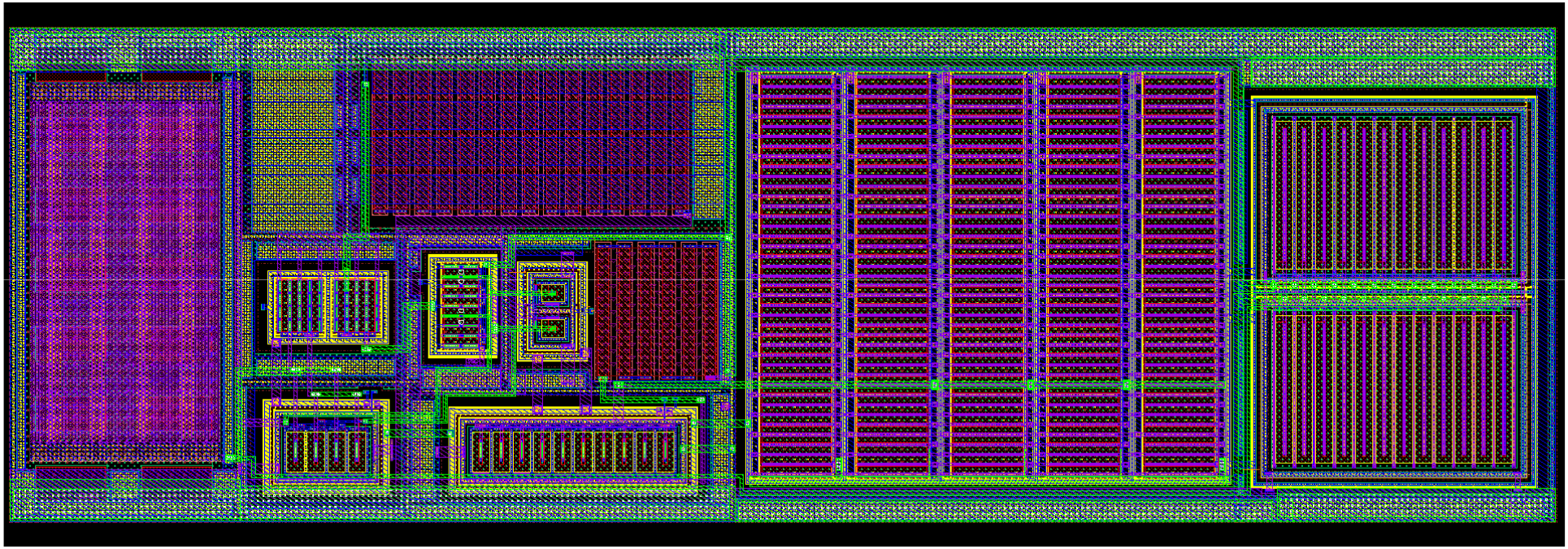
**Worst case Propagation for Stub Gathering Logic (SGL): 10.2ns**

(1 stub on 0 and 1 stub on half stub 127, with a mid range stub active on half stub 65.)

**Dynamic Power Dissipation for SGL: 7.62mW** (with 3 stubs every 25ns)



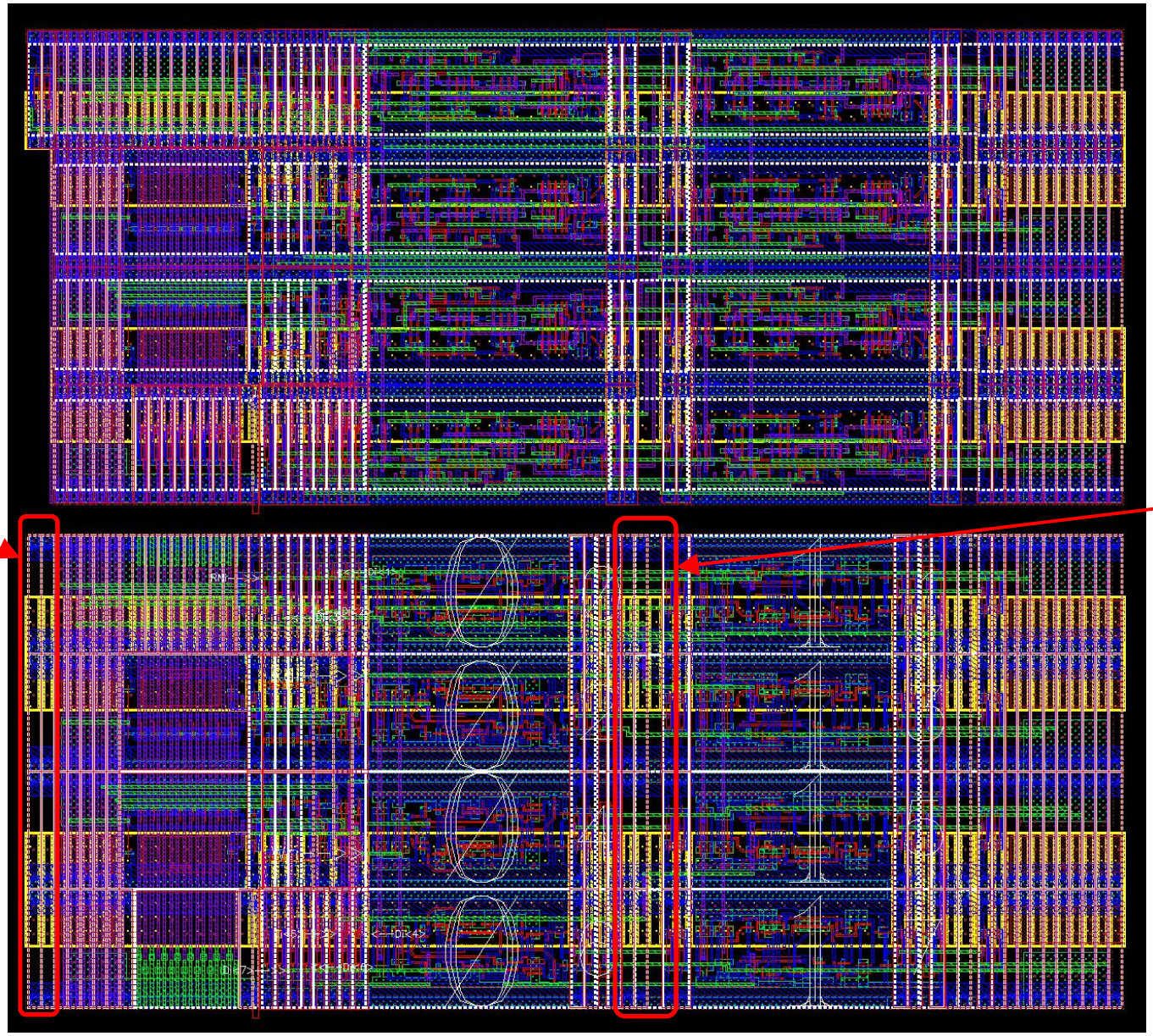
# Current Reference layout complete



# New I2C register

**OLD**

Unused space

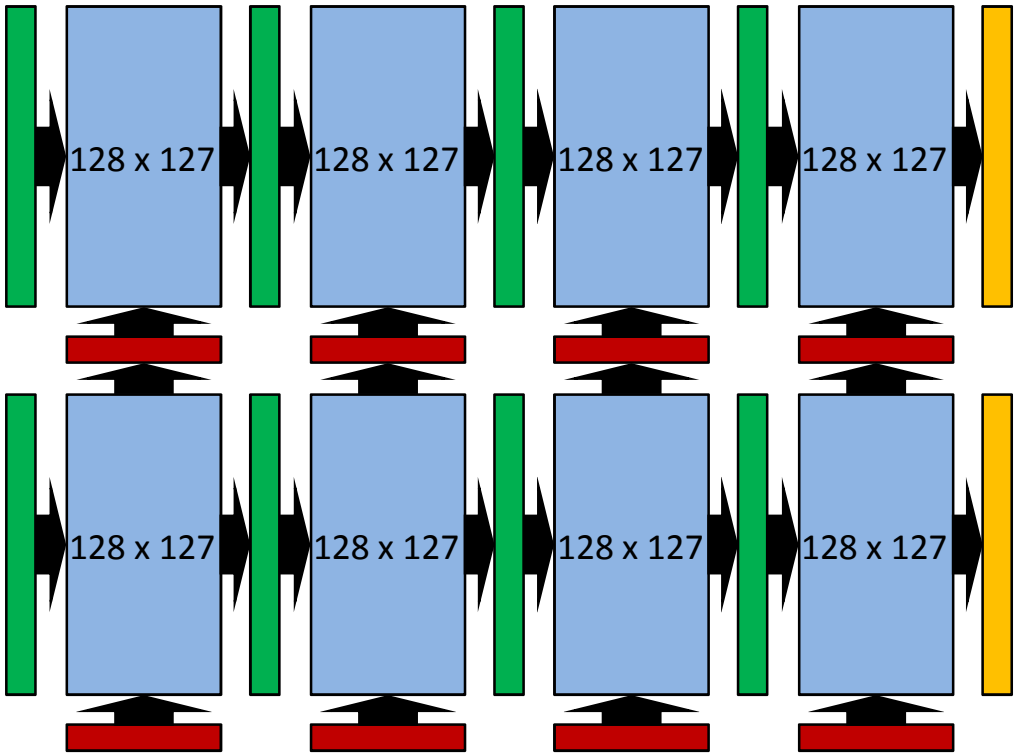


Unused space

**NEW**

- Same footprint as old cell for direct swap out.

# Pipeline




WRITE/READ Pointer Buffers

WRITE/READ Data line Buffers

Output Latches

# Summary

- Technical Specification document Updated to Version 1.1.
- Current reference circuit layout completed.
- I2C Register – Layout modified to replace the TRL with the Whitaker latch.
- SRAM simulated: Buffer sizes and architecture decided following simulation and re-sizing of the READ & WRITE transistors in the cell.
- Post Design Review actions ongoing.
- Provision of Top level code to IPNL – On hold for minor changes.