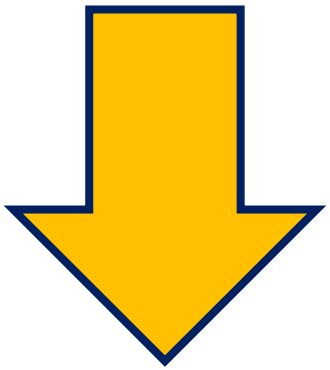
CBC3 Progress

Imperial College London

Science & Technology Facilities Council

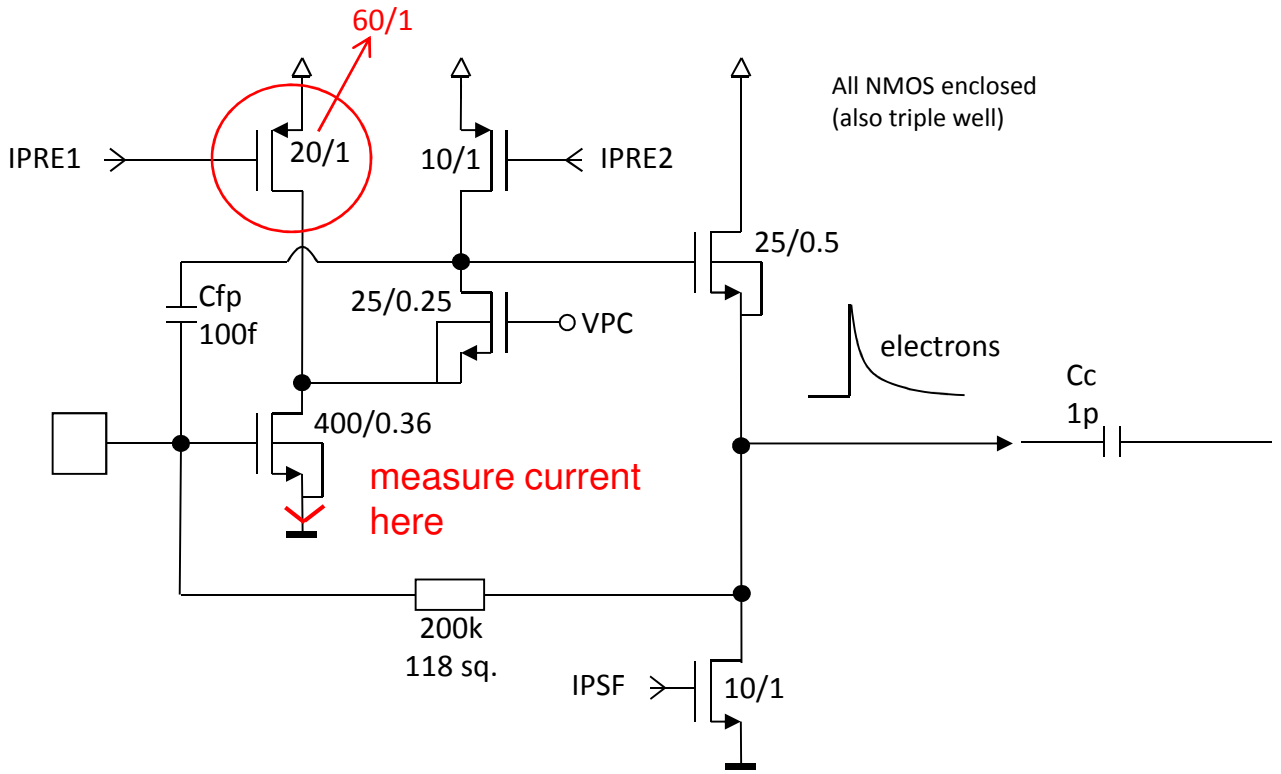
Preamp Changes

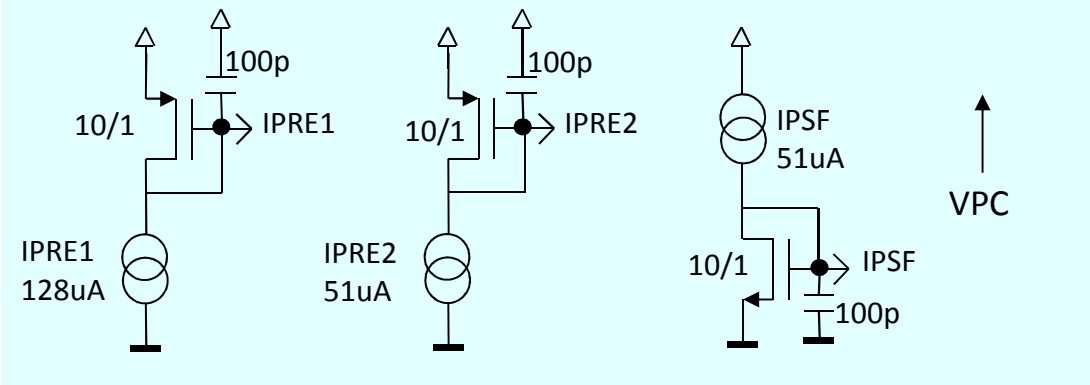


CBC3 Preamp current increase

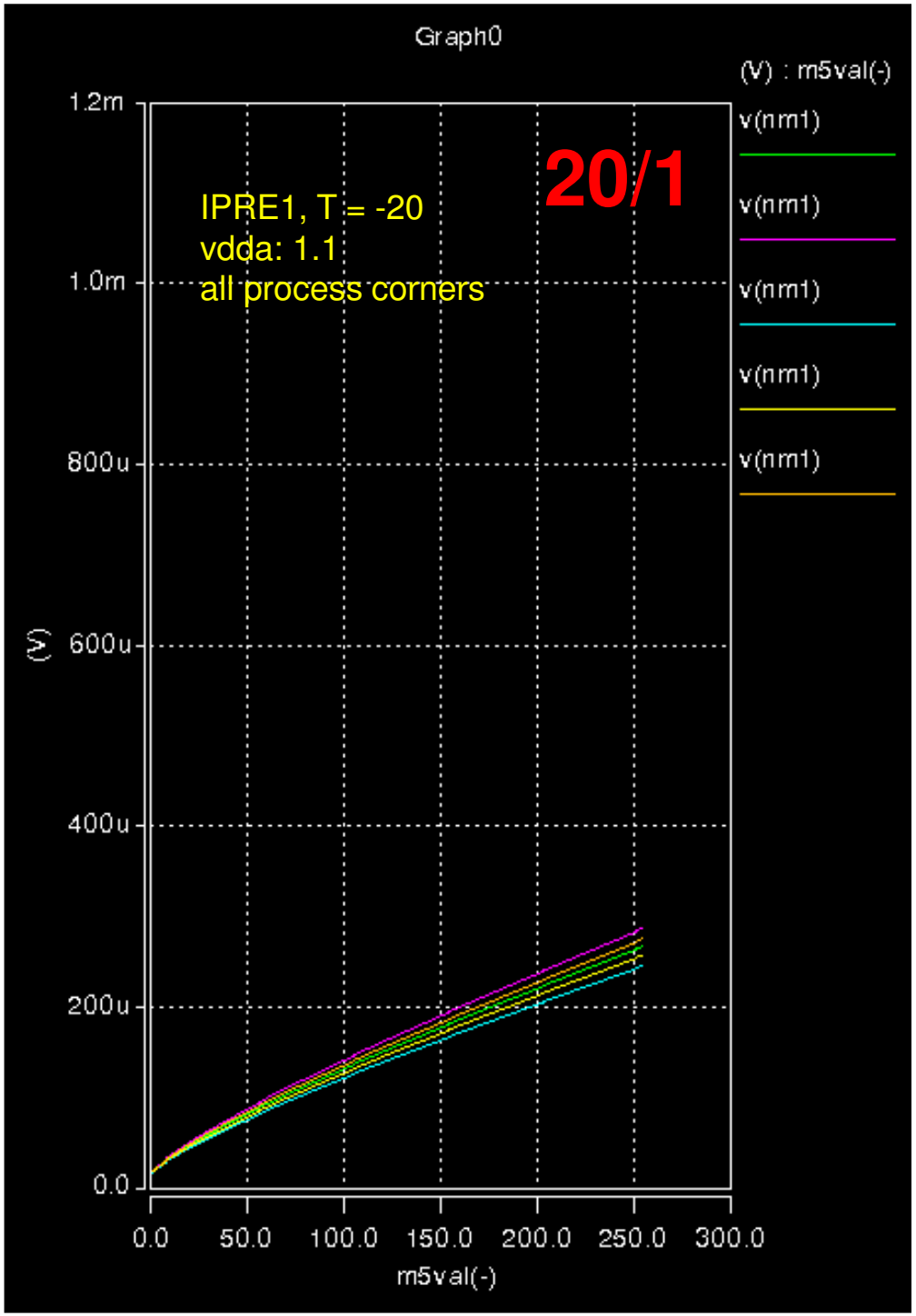
Want to increase by ~3x

try increasing 20/1 to 60/1





Mark Raymond

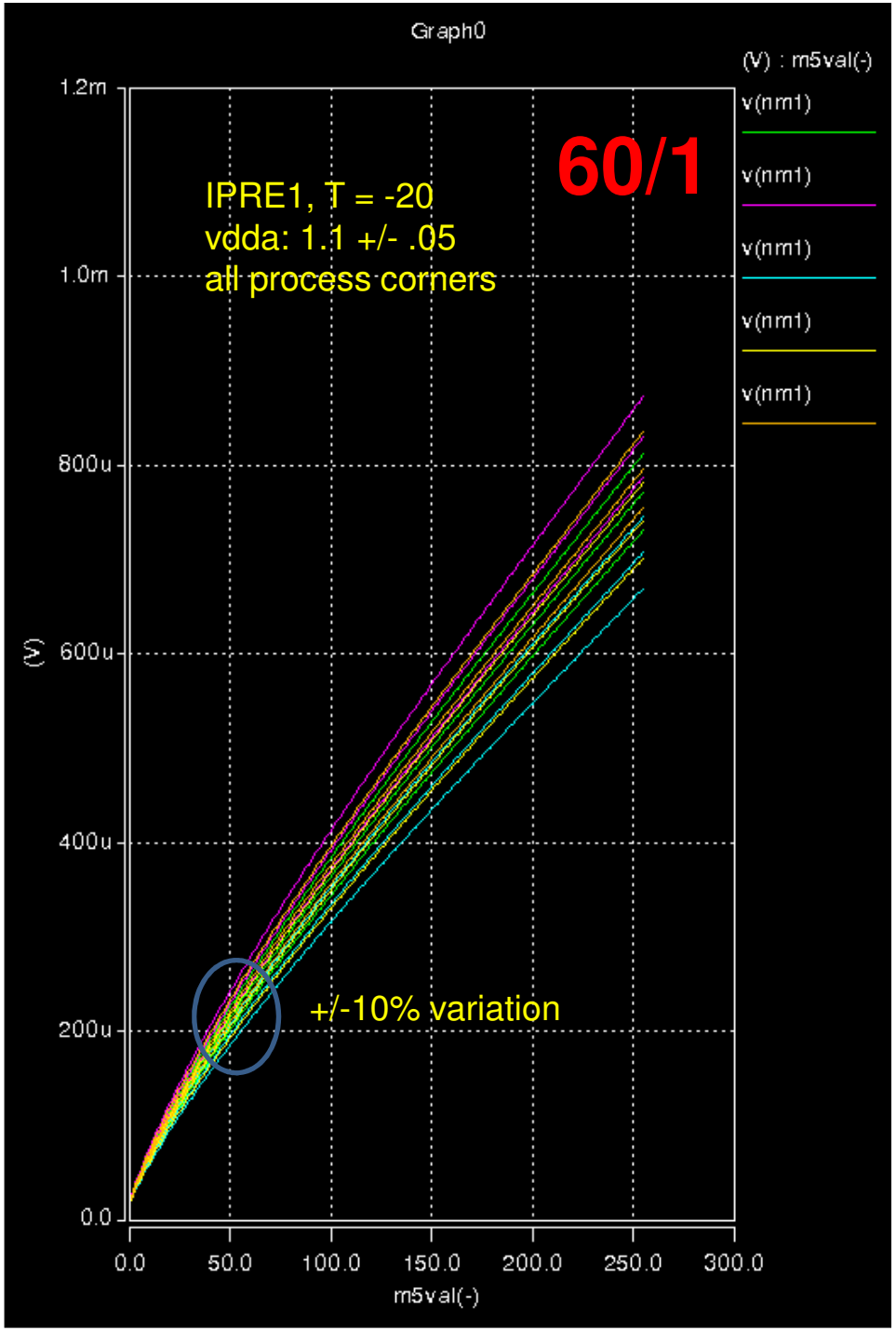


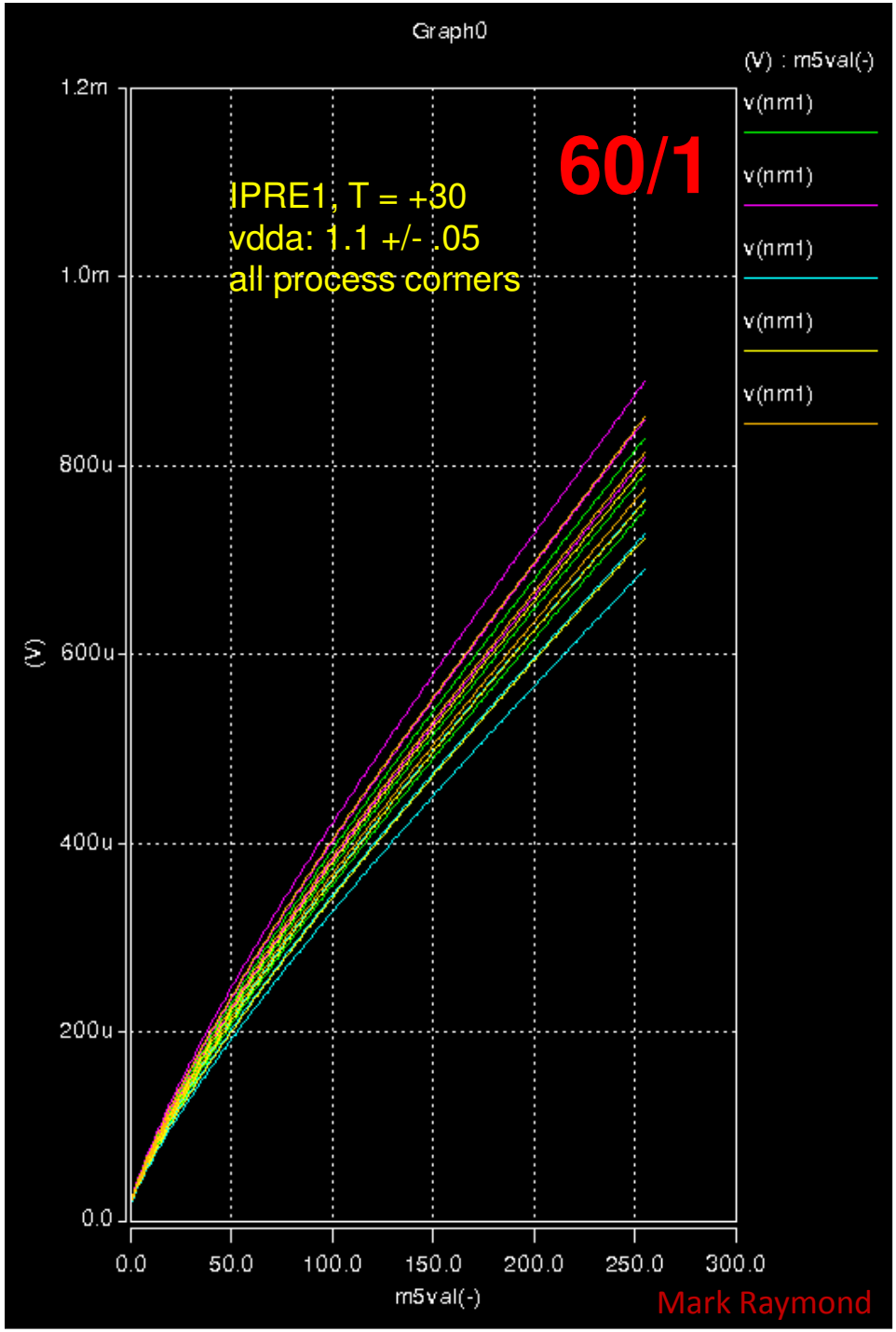
CBC2 Mirror size performance

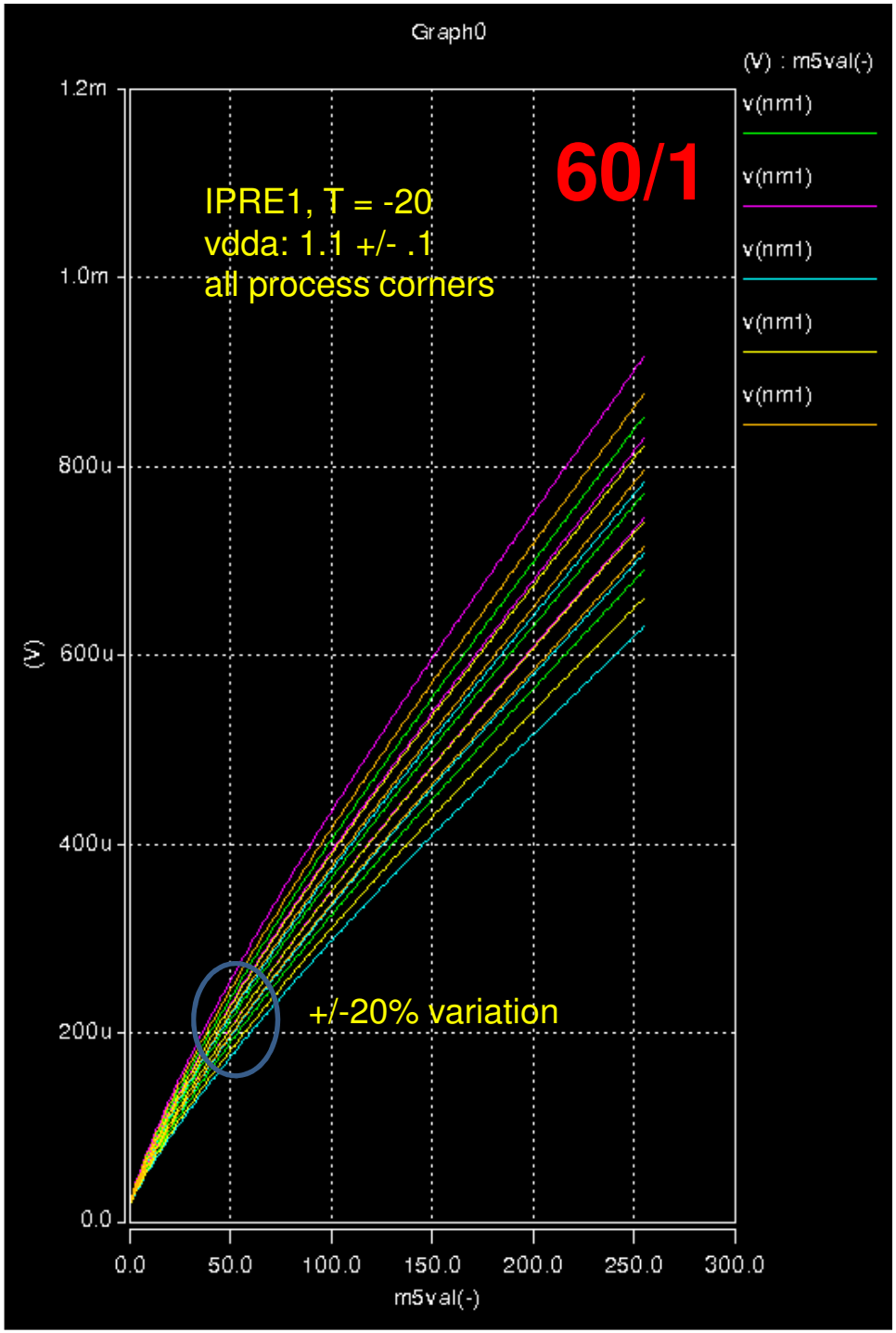
current in input transistor dependence on IPRE1 I2C parameter setting

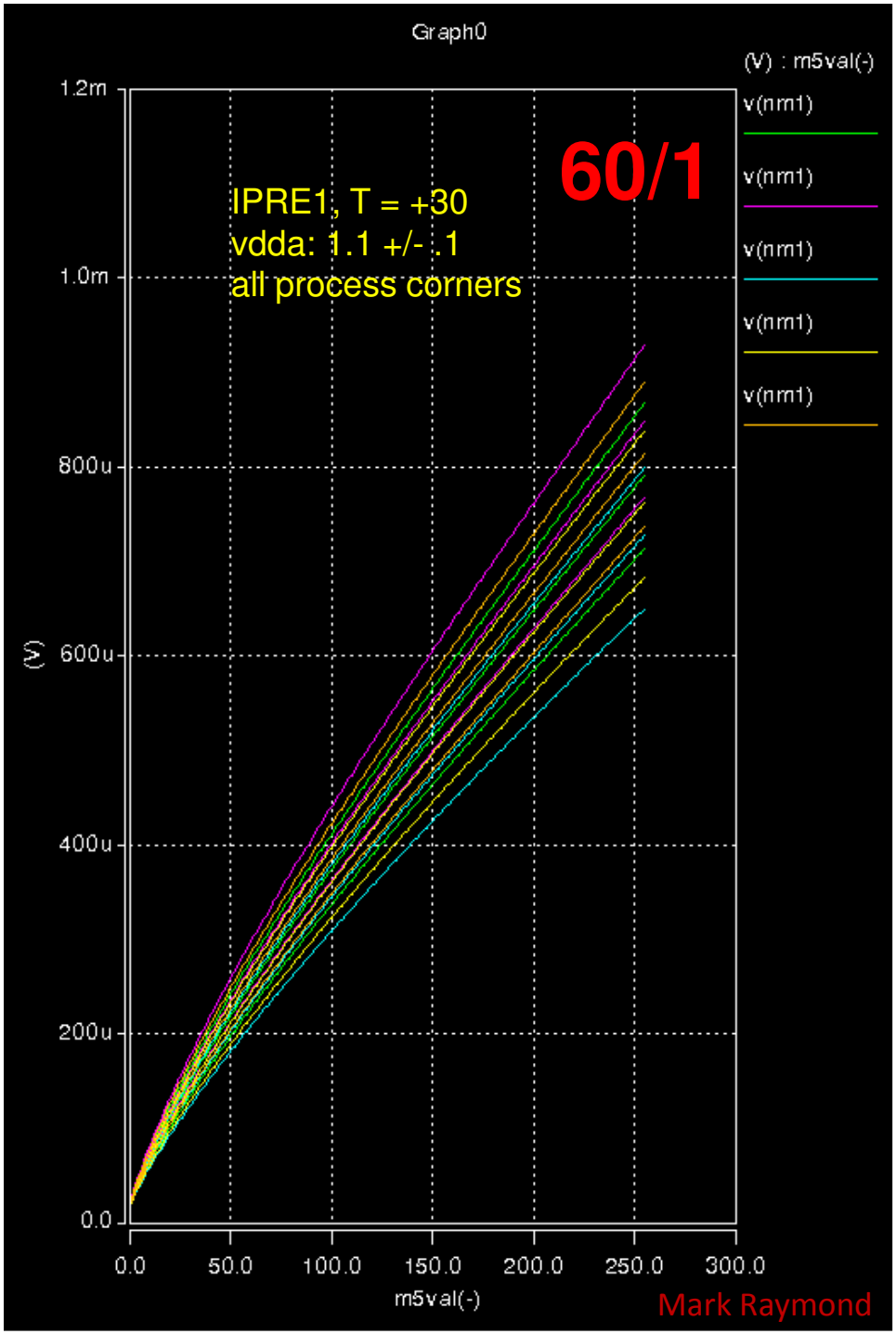
current source device 20/1

maximum current ~ 250 uA


Graph0
(V) : m5val(-)
v(nm1)
v(nm1)
v(nm1)
v(nm1)
v(nm1)
60/1
IPRE1, T = -20
vdda: 1.1 +/- .05
all process corners
+/-10% variation
1.2m
1.0m
800u
600u
400u
200u
0.0
(V)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
m5val(-)


Graph0
(V) : m5val(-)
v(nm1)
v(nm1)
v(nm1)
v(nm1)
v(nm1)
60/1
IPRE1, T = +30
vdda: 1.1 +/- .05
all process corners
1.2m
1.0m
800u
600u
400u
200u
0.0
(V)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
m5val(-)
Mark Raymond


Graph0
(V) : m5val(-)
v(nm1)
v(nm1)
v(nm1)
v(nm1)
v(nm1)
60/1
IPRE1, T = -20
vdda: 1.1 +/- .1
all process corners
+/-20% variation
1.2m
1.0m
800u
600u
400u
200u
0.0
(V)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
m5val(-)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v(nm1)
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IPRE1, T = +30
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1.2m
1.0m
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600u
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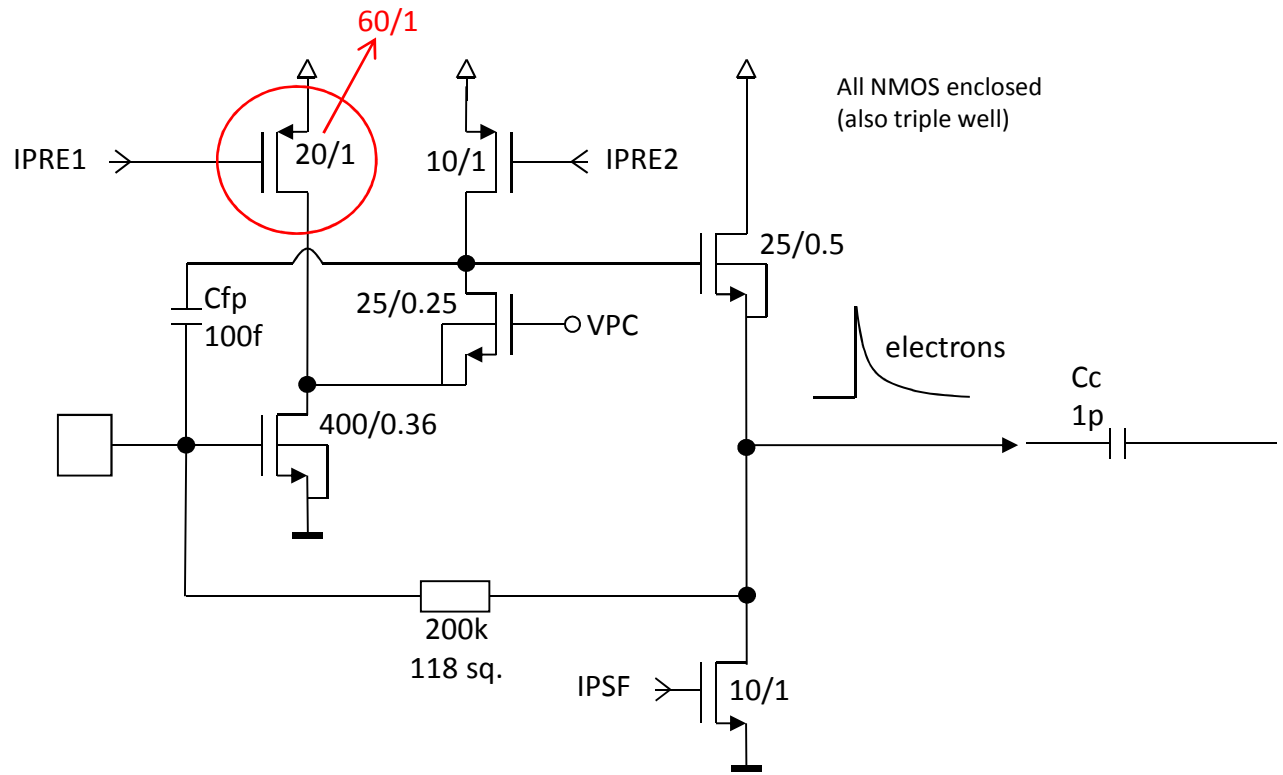
0.0
(V)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
m5val(-)
Mark Raymond

CBC3 Preamp bias conclusion

just increase current source to 60/1



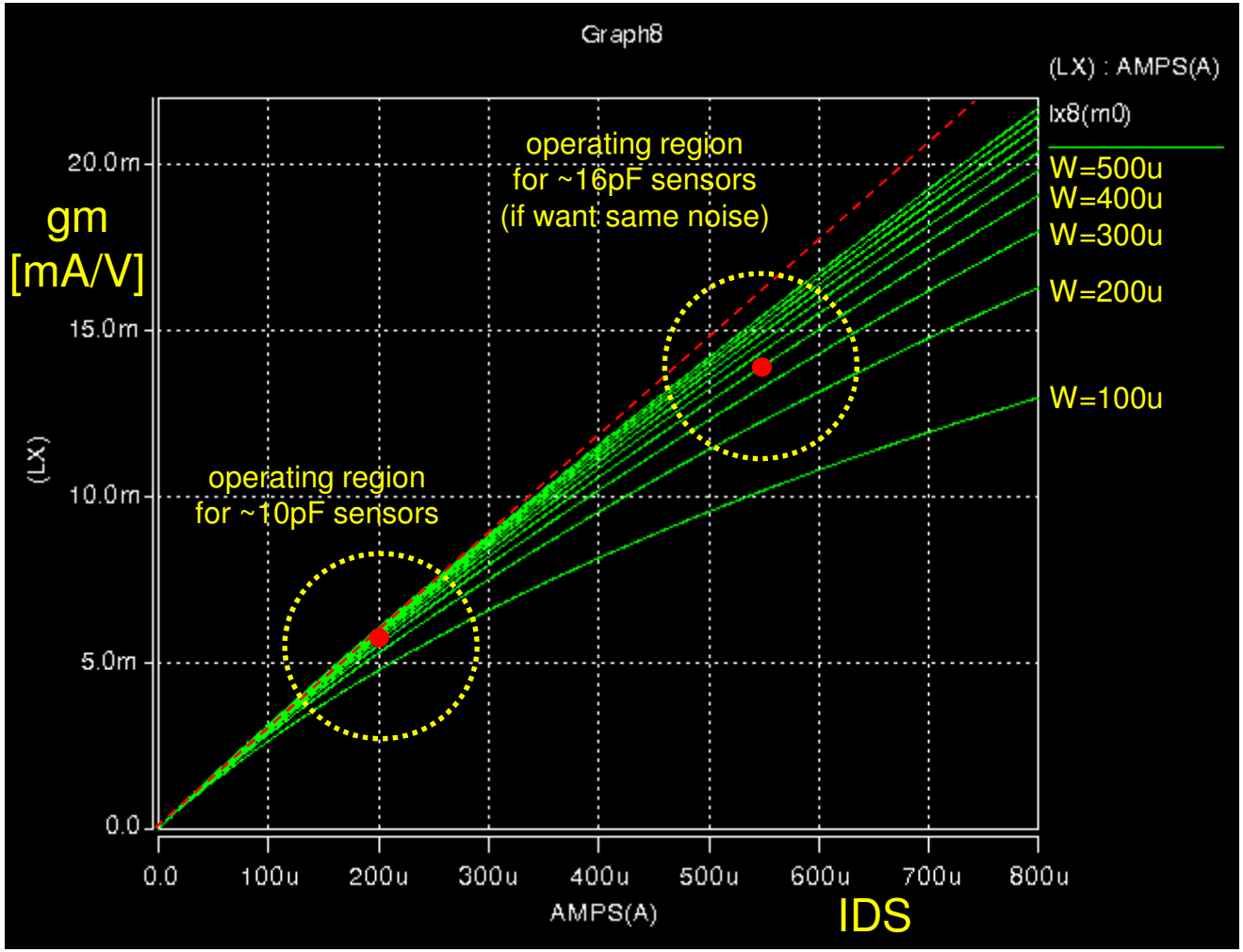
CBC3 Input device choice

CBC2 I/P device = 400/0.36 (C_{GS} ~ 1pF) (length chosen to avoid 1/f corner penalty)

Noise α C/$\sqrt{I_{DS}}$ ($g_m \alpha I_{DS}$)

Do we need to increase width if need to run at higher IDS to cope with higher sensor capacitance?

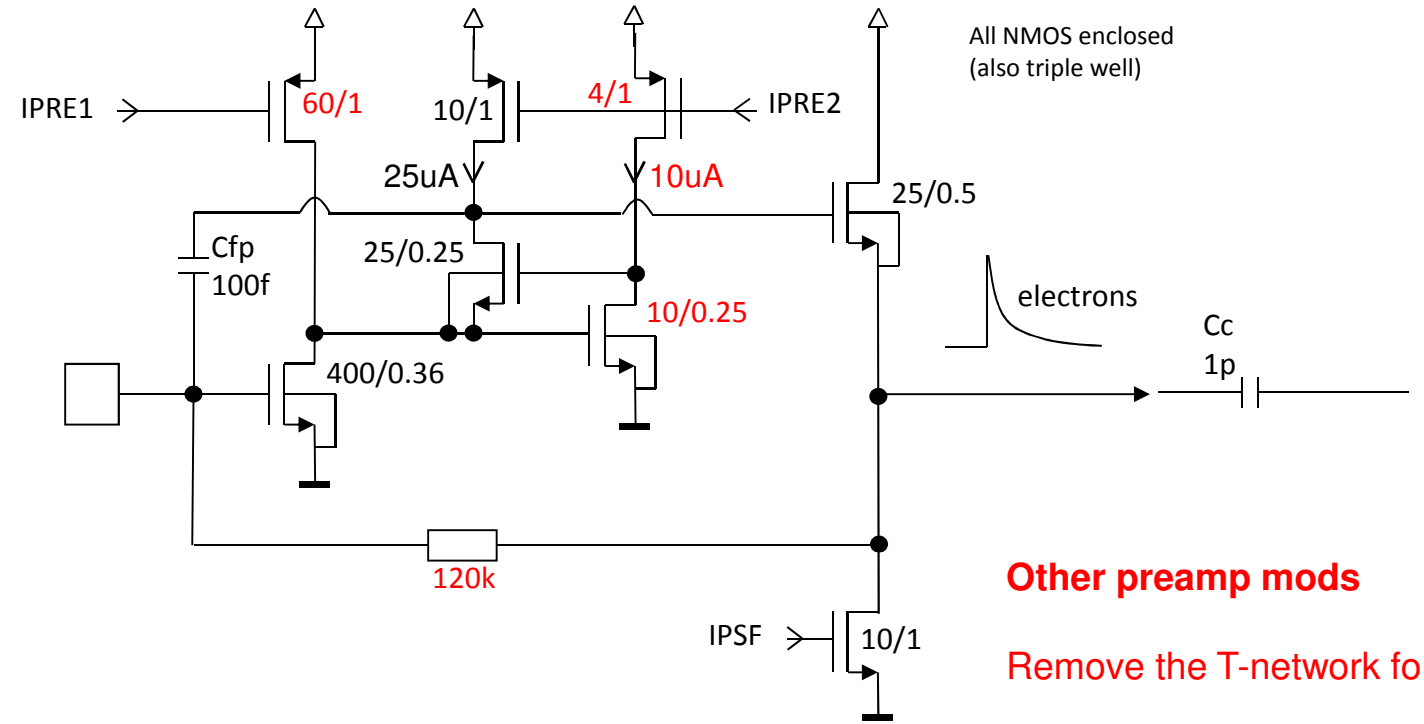
- Plot suggests there's not much to be gained - still in weak inversion for higher currents
- Most likely to be operating in 150 - 300 uA range
- Increasing width significantly will only give C_{GS} penalty with no gm enhancement

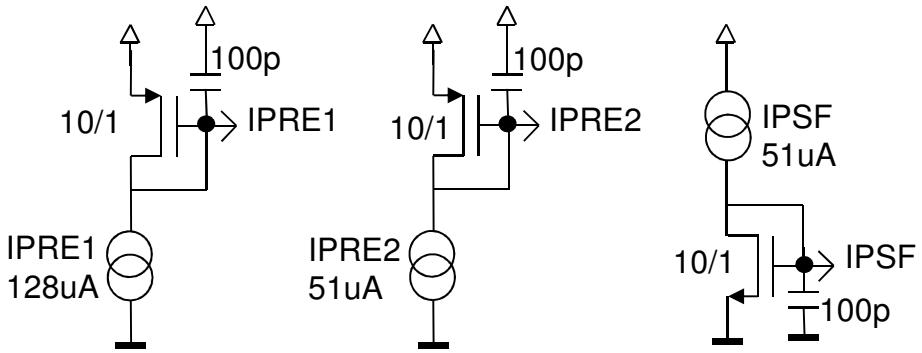


Decision: Keep W/L = 400/0.36

Mark Raymond

CBC3 Preamp with regulated cascode





Other preamp mods

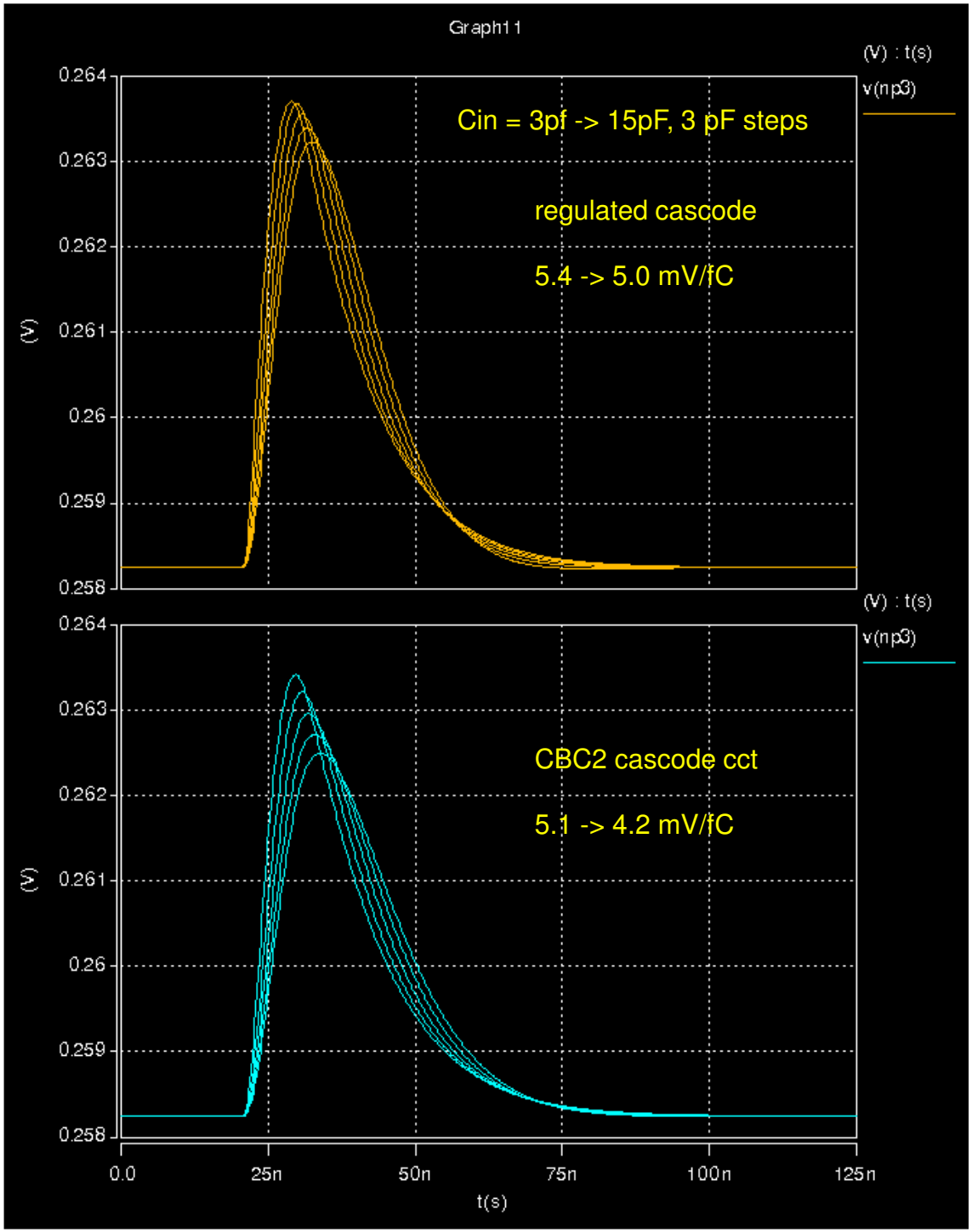
Remove the T-network for holes polarity

Reduce Rf to 120k (needed for reduced pulse peaking time)

Use a regulated cascode circuit

- Larger open loop gain
- Self biasing so no need for gate voltage bias or any adjustment
- Small power penalty

Mark Raymond



Effect of regulated cascode

higher OL gain => reduced effect of Cin
on overall preamp gain

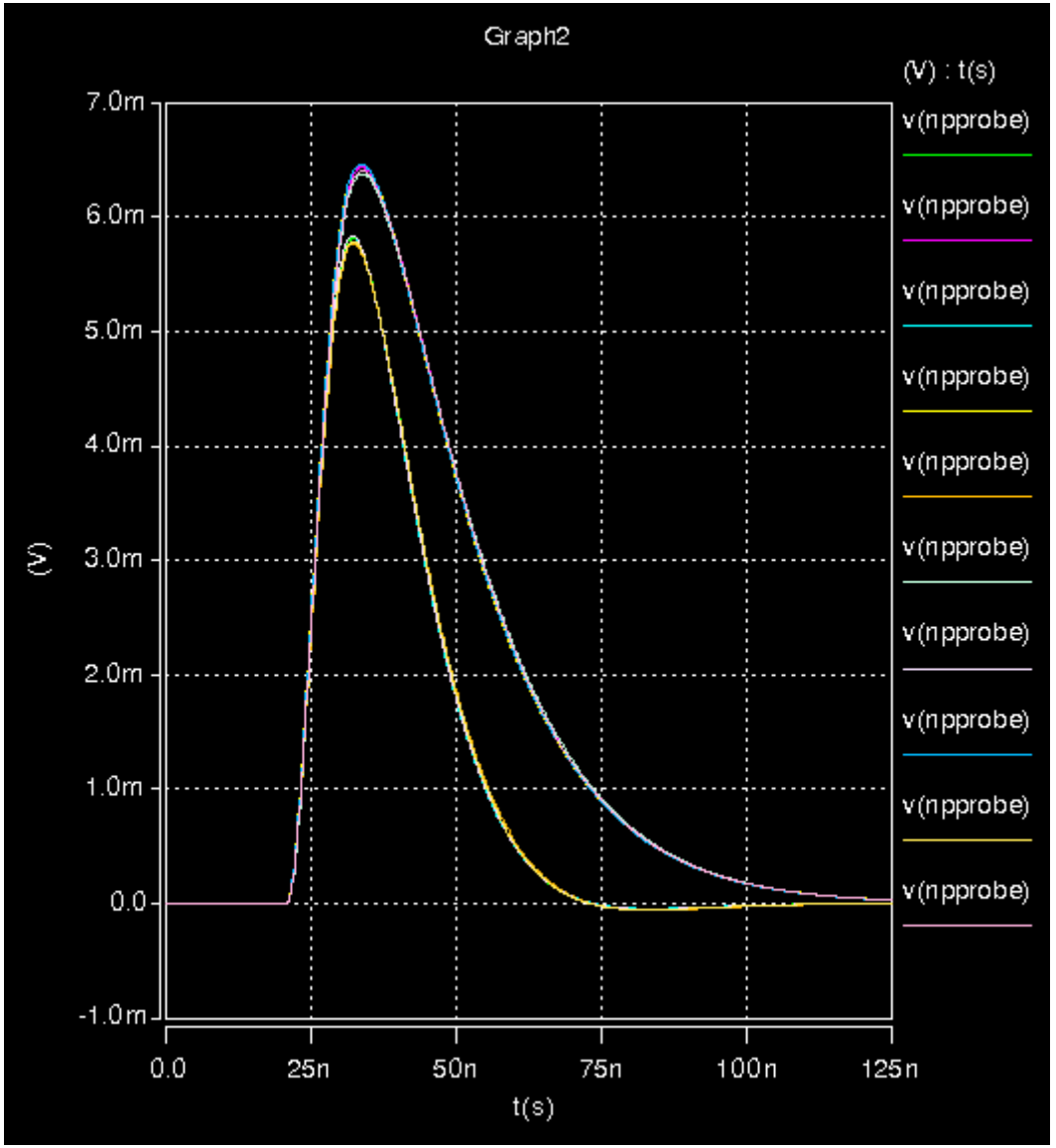
self biasing - no need to generate cascode
gate voltage

worth having
can derive bias from ipre2 (factor 2.5) so
for ipre2 = 25u, need extra 10uA for reg casc

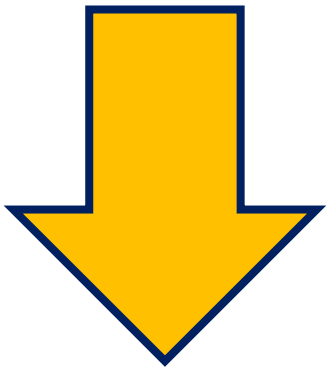
Effect of reducing preamp feedback resistor

200k -> 120k

1 fC pulse shape now within 50nsec overall duration

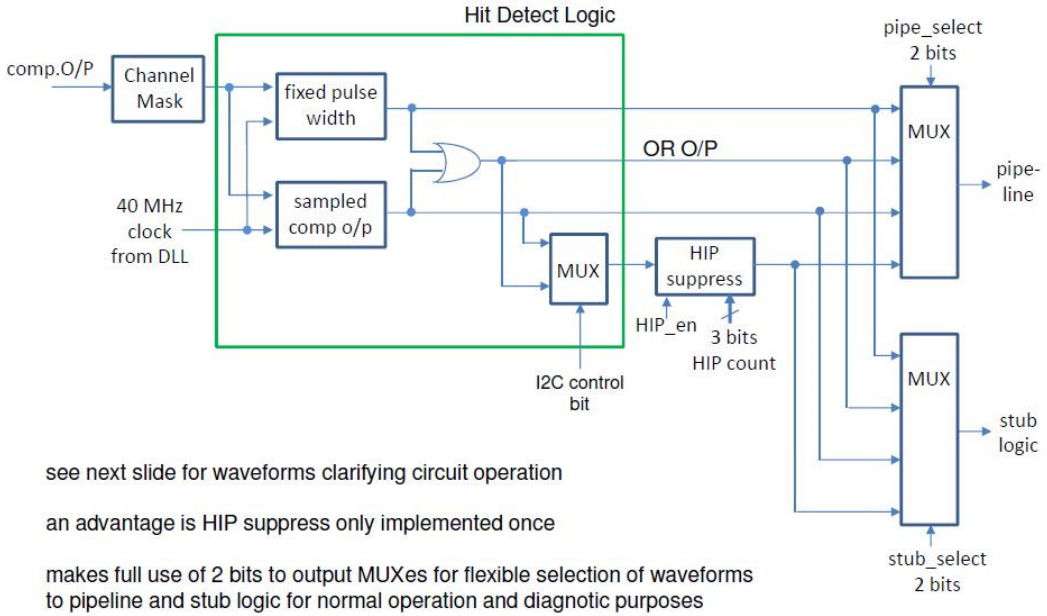


Hit Detect Circuit



Hit Detect Spec

CBC3 Hit Detect

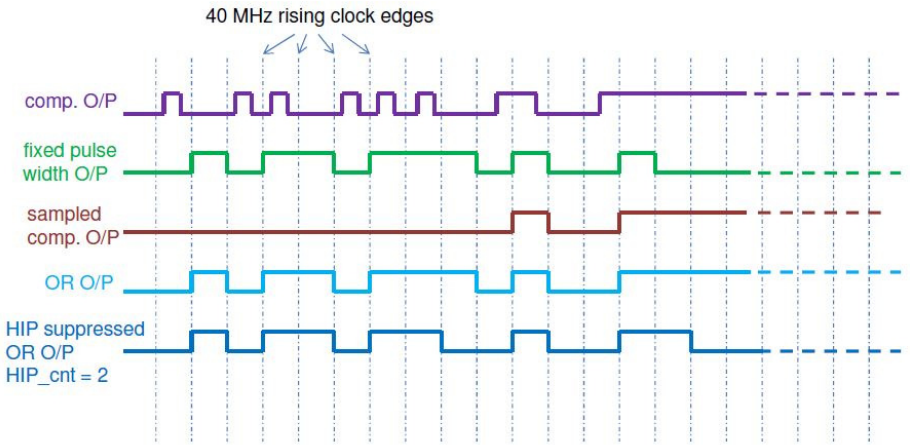


see next slide for waveforms clarifying circuit operation

an advantage is HIP suppress only implemented once

makes full use of 2 bits to output MUXes for flexible selection of waveforms to pipeline and stub logic for normal operation and diagnotic purposes

As specified by Mark Raymond



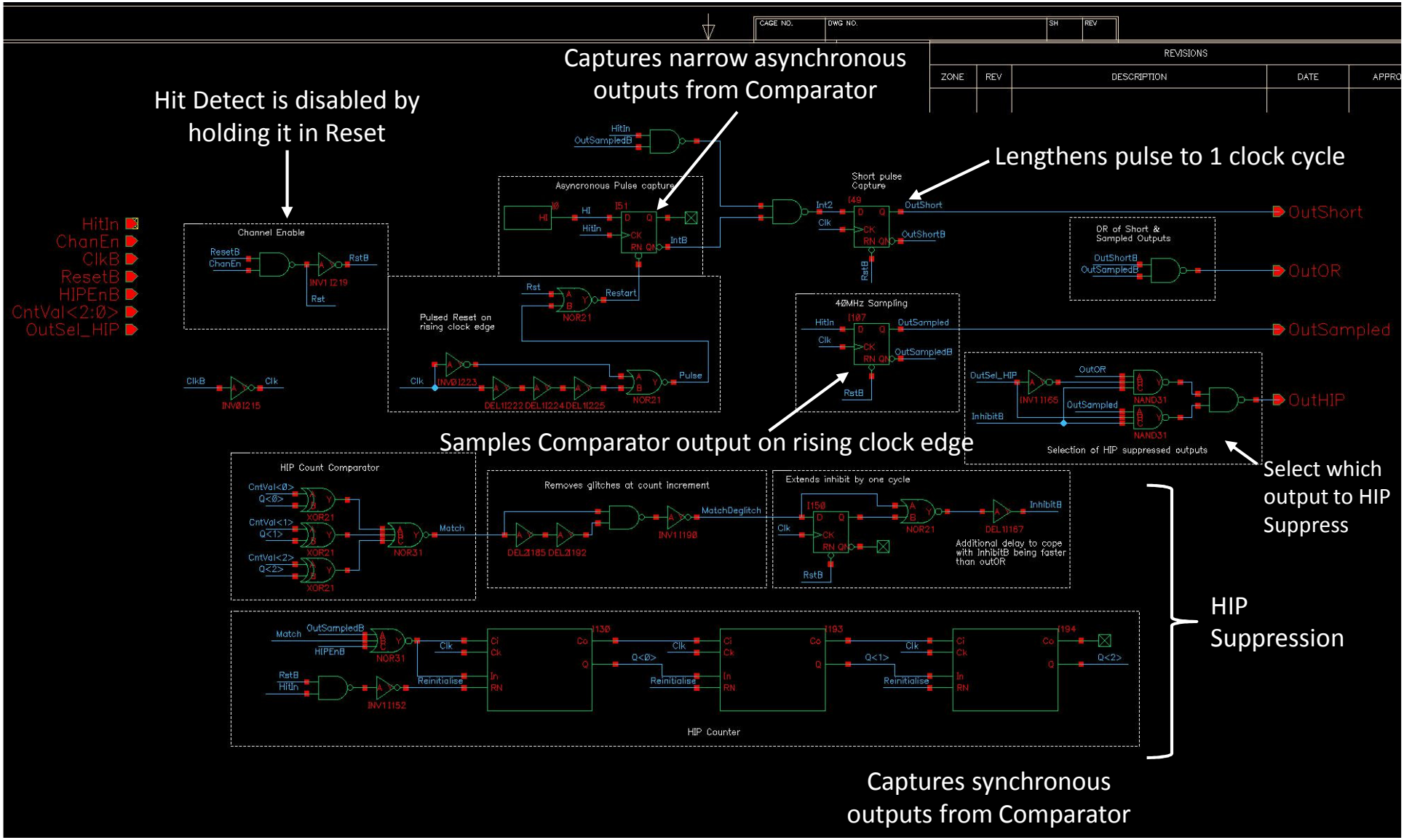
definitions

fixed pulse width looks for a rising edge on the comparator O/P and produces a single 40 MHz clock cycle pulse beginning at the next 40 MHz clock rising edge

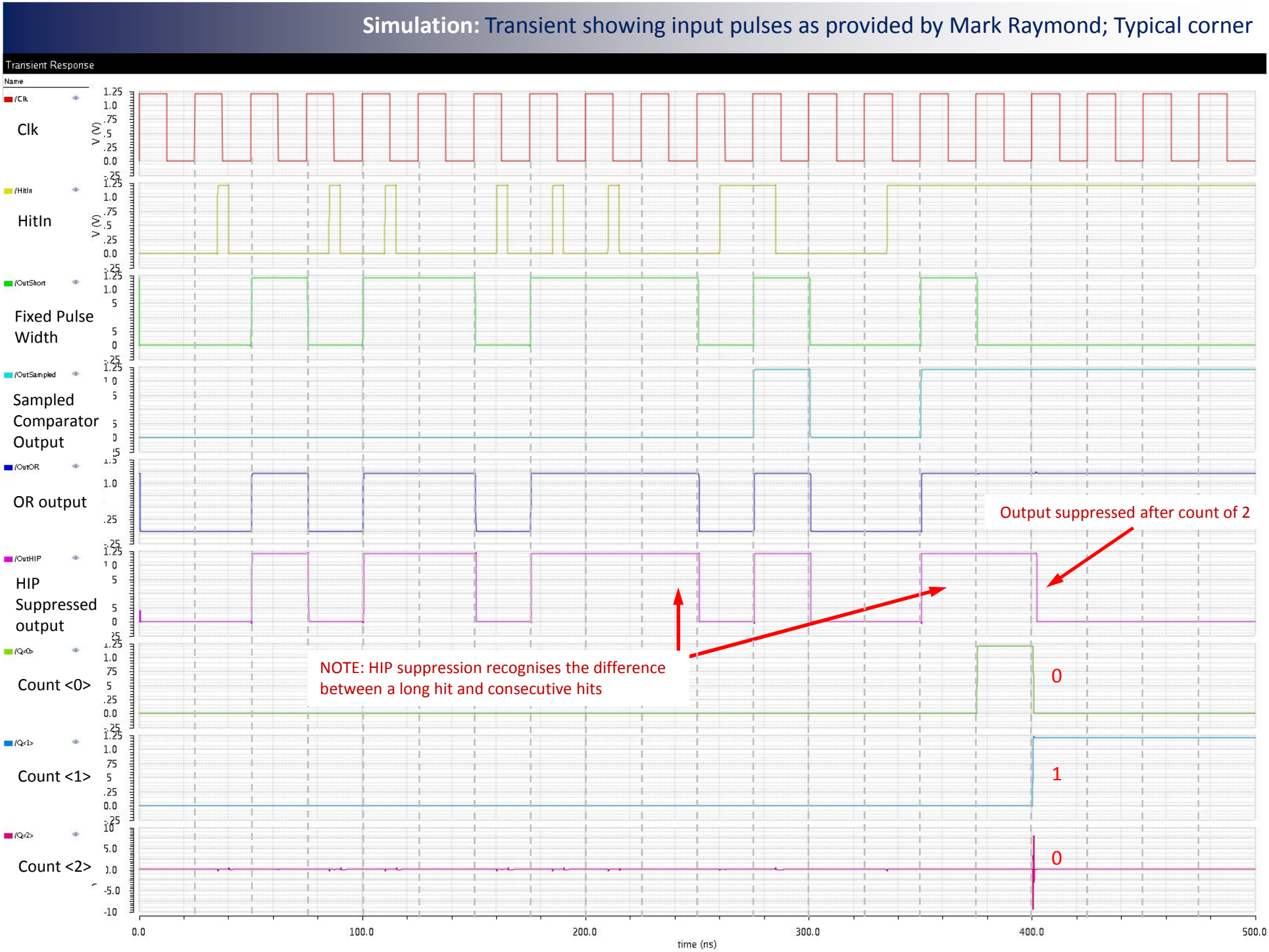
sampled comp. O/P goes high if the comparator output is high at the 40 MHz rising clock edge. It could be implemented by a single D-type.

OR O/P is the logical OR of fixed pulse width O/P and sampled comp. O/P.

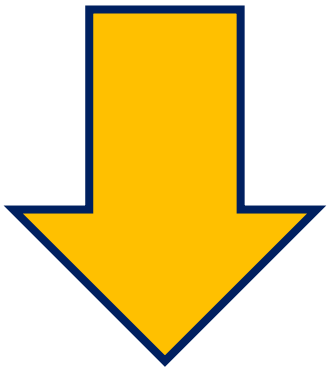
Hit Detect Circuit



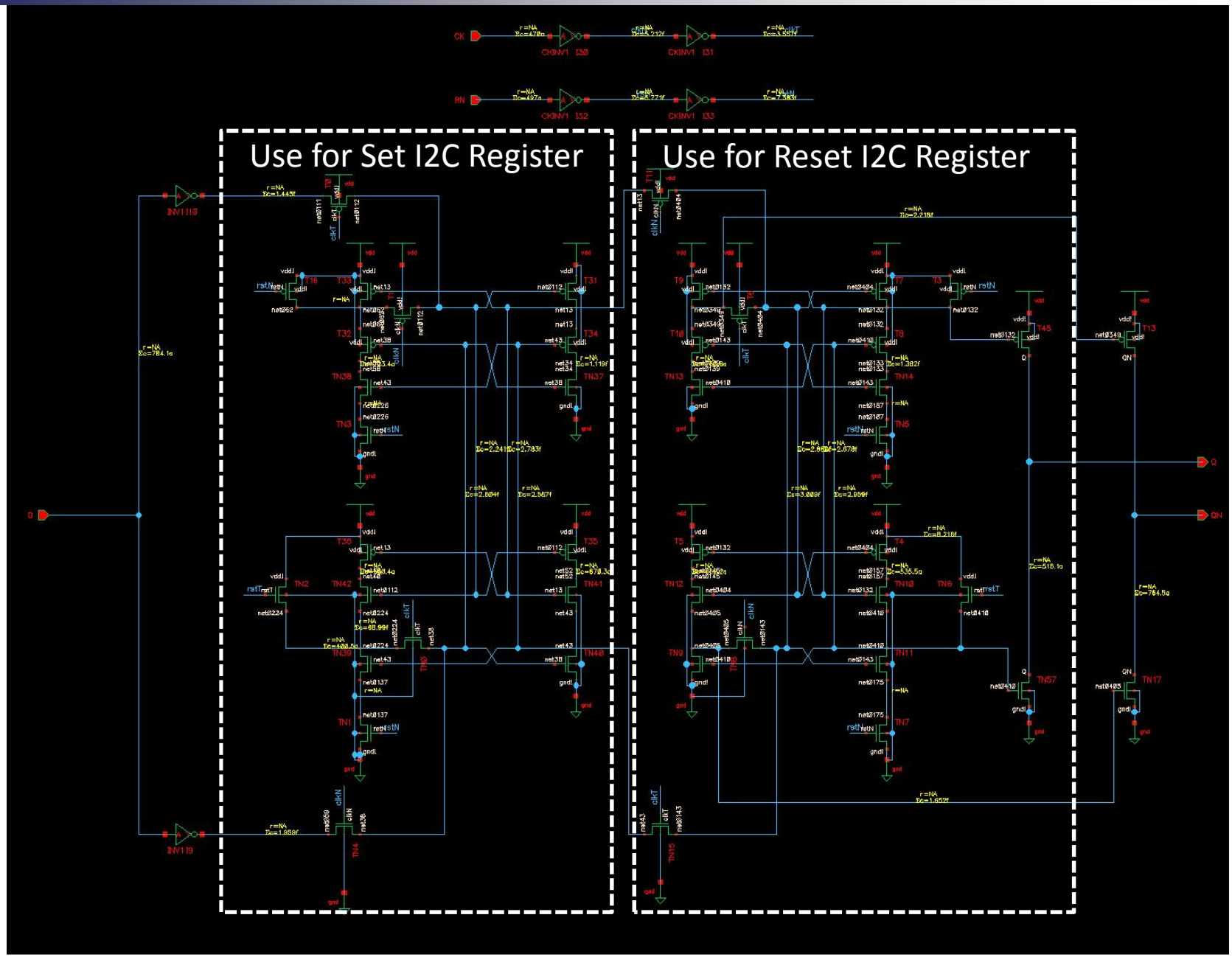
Simulation: Transient showing input pulses as provided by Mark Raymond; Typical corner



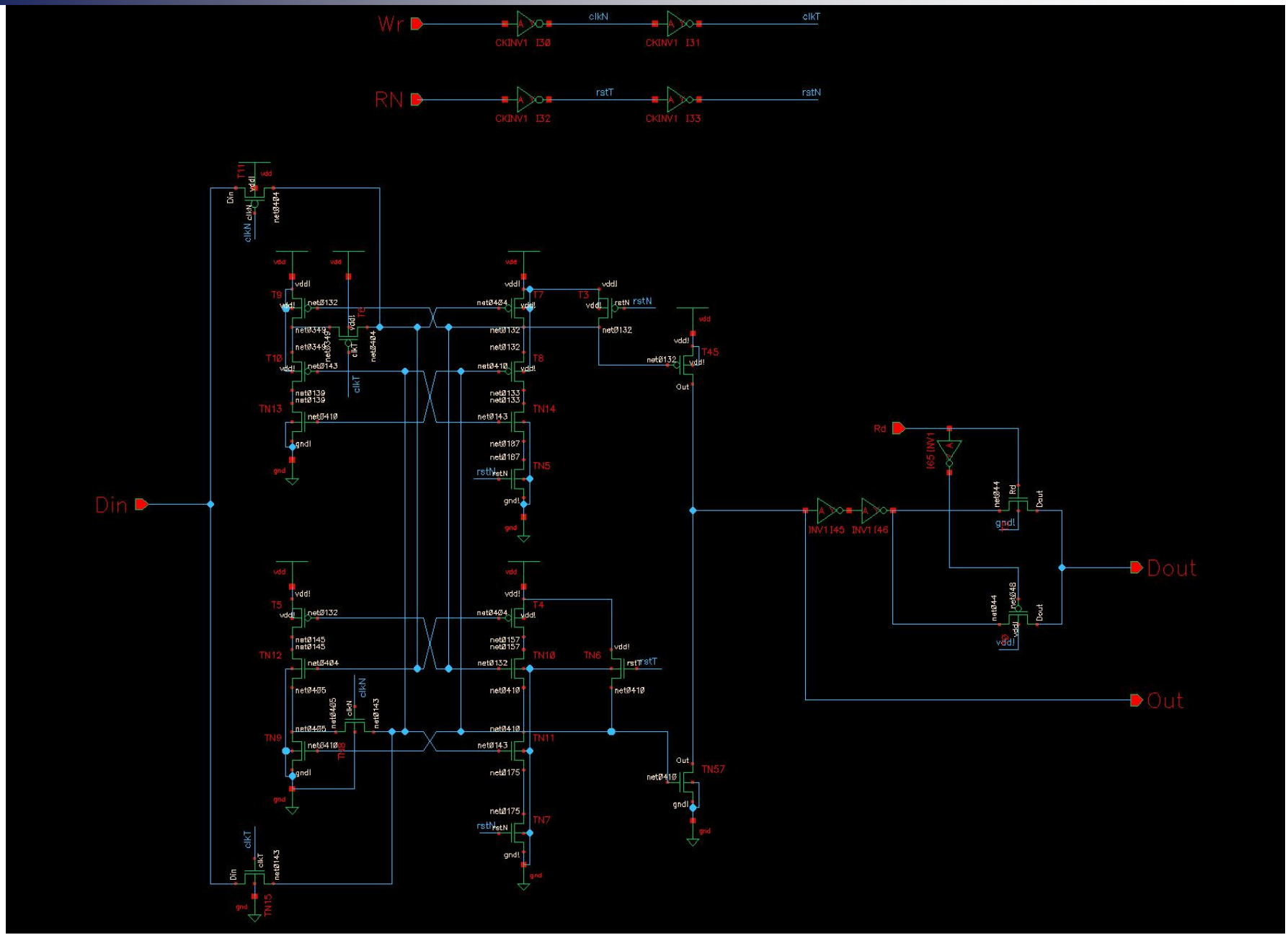
I^2C Register Replacement



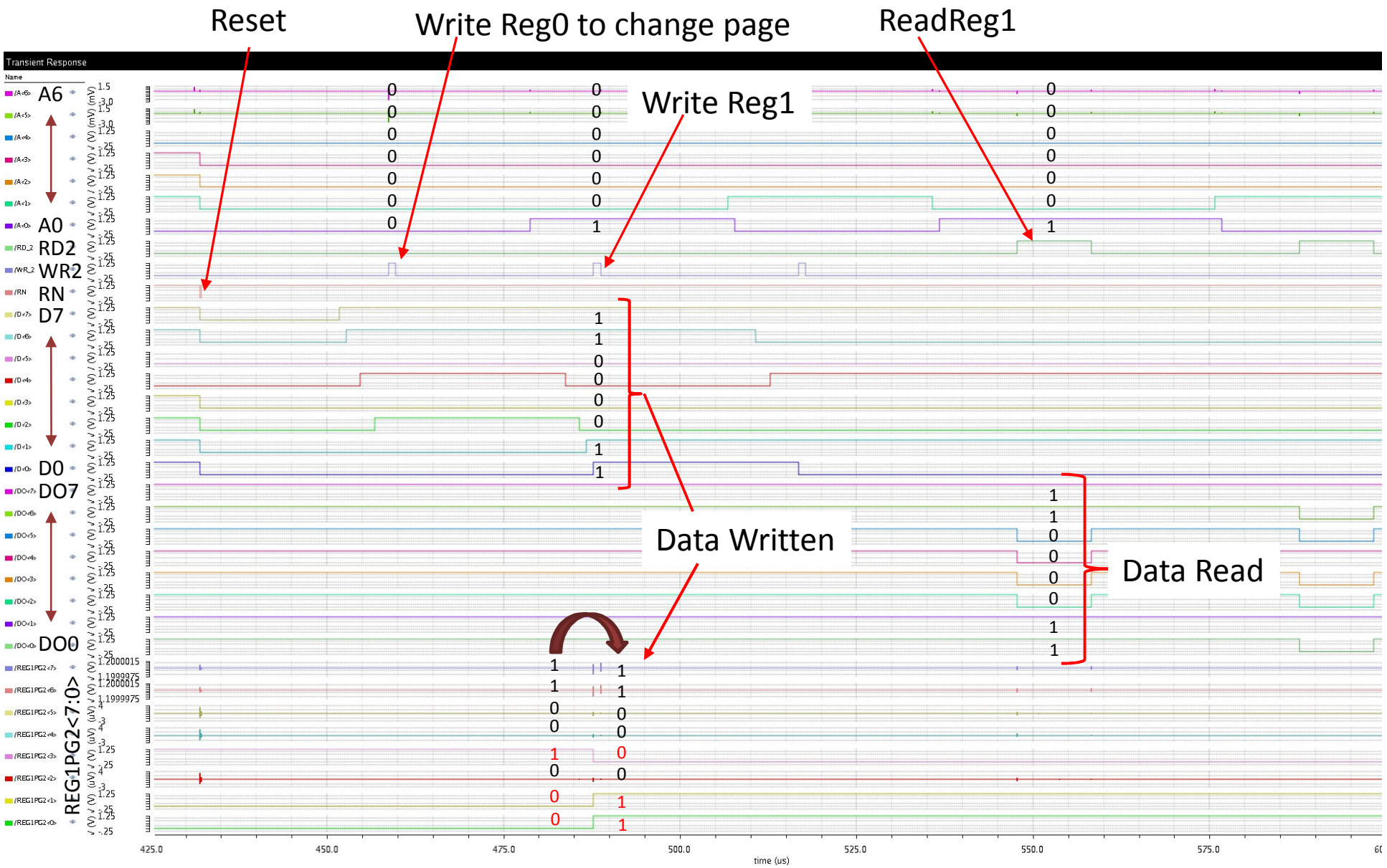
Existing Whitaker Flip Flop



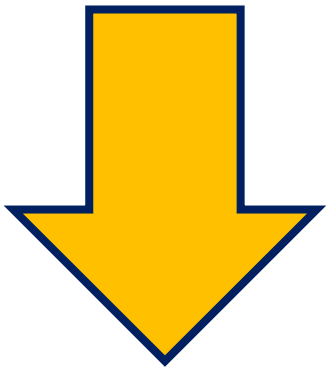
Whitaker I²C Register



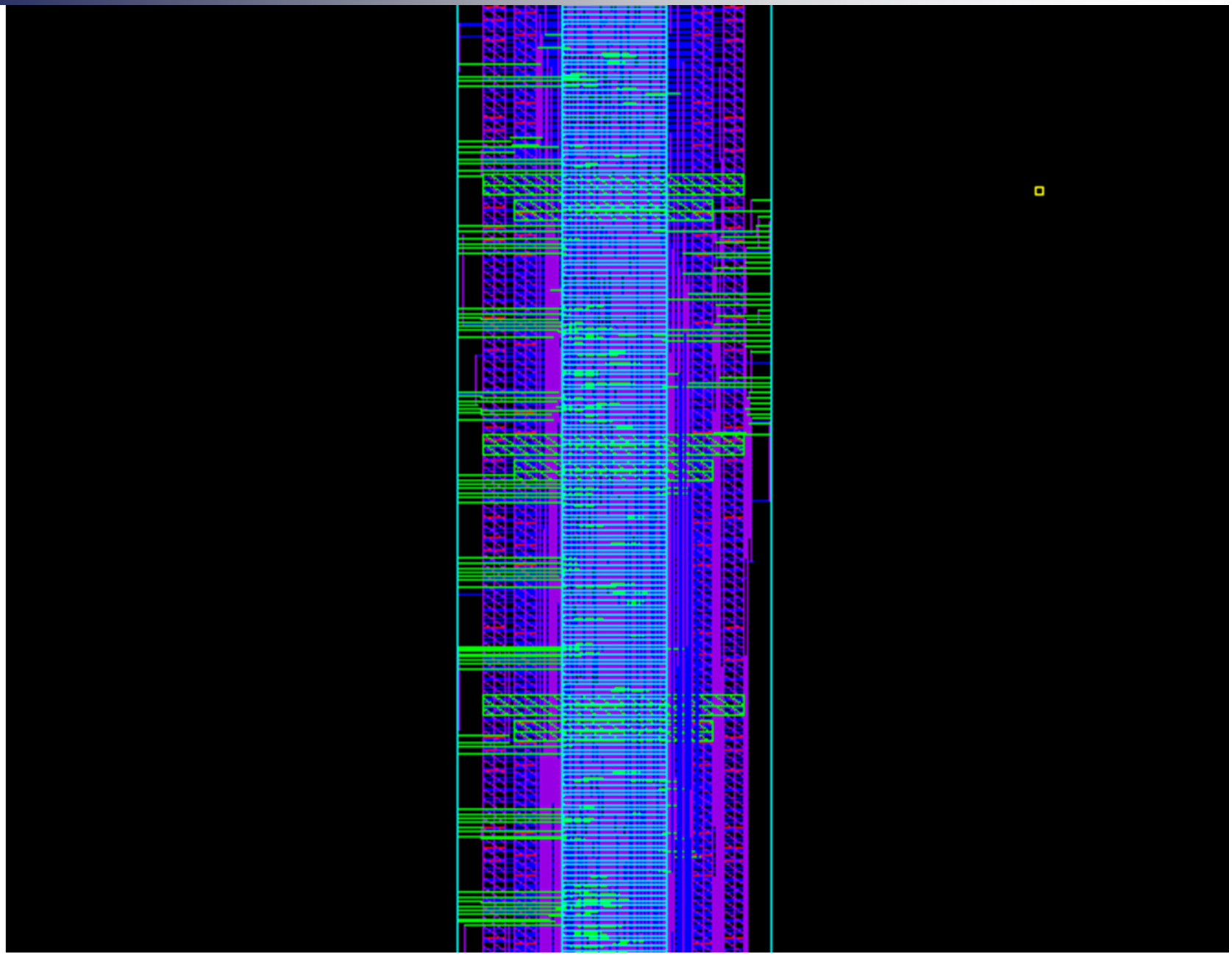
Simulation: I²C with Register 1 on Page 2 replaced by a Whitaker equivalent



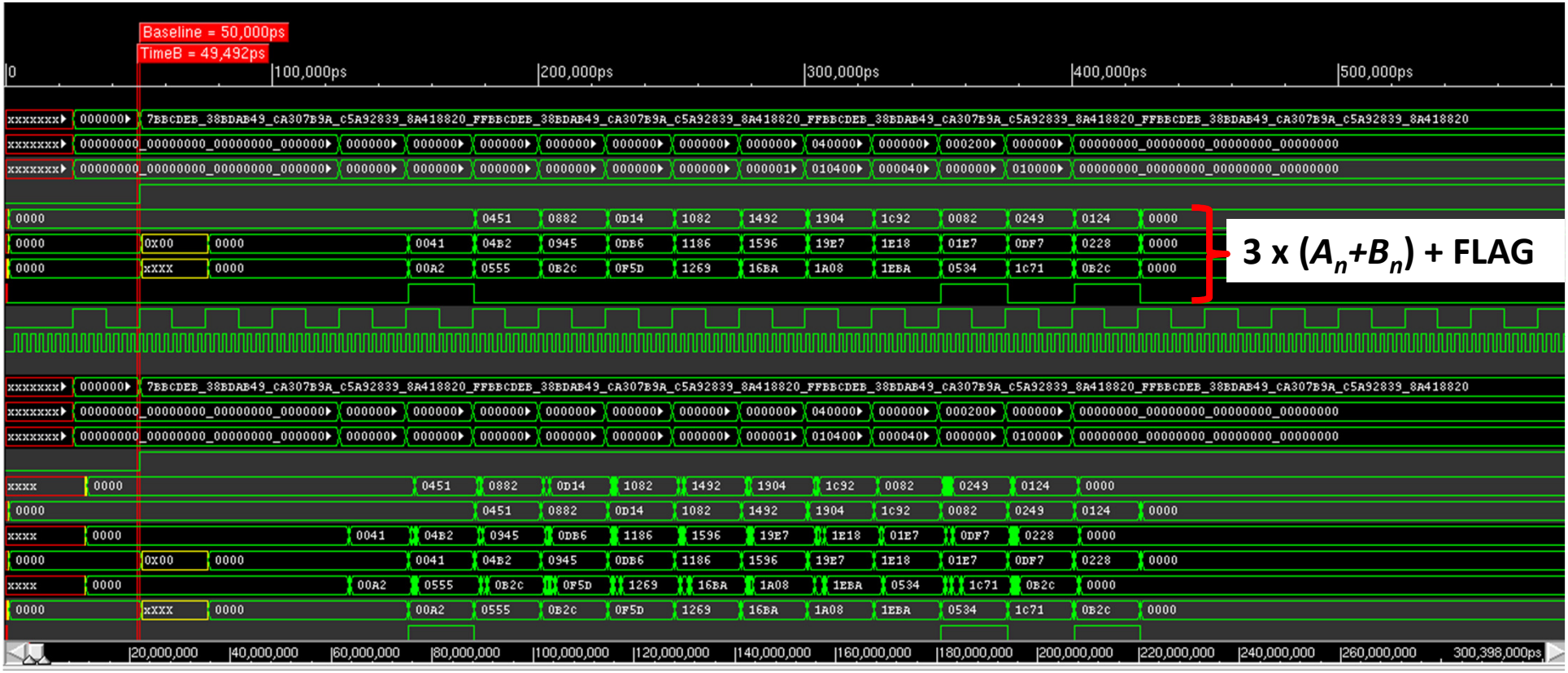
Stub Gathering Logic



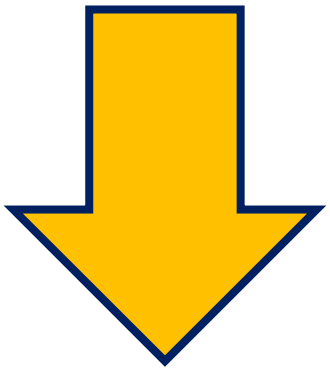
Stub Gathering Logic Layout



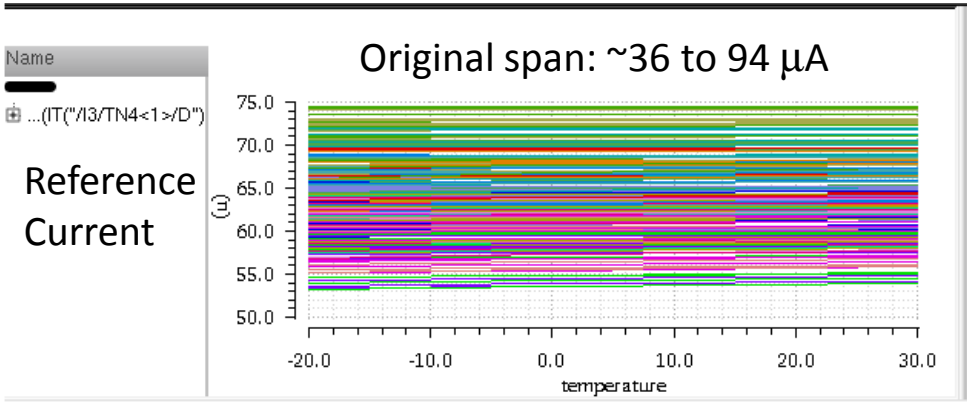
Post Layout Simulation

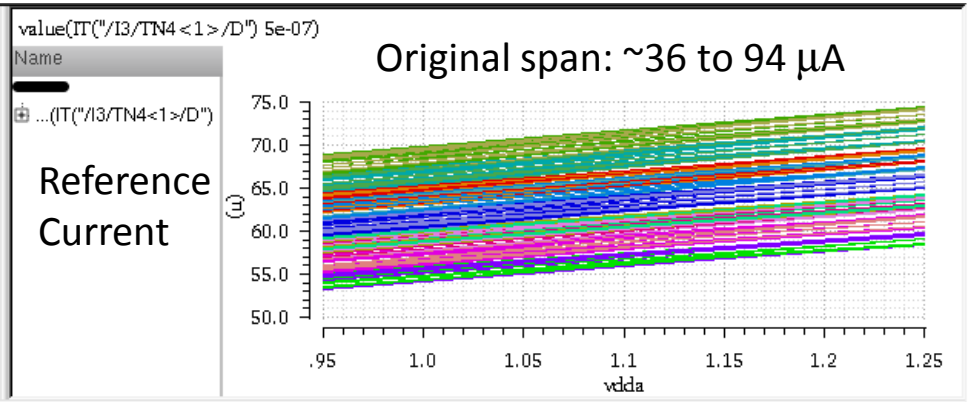


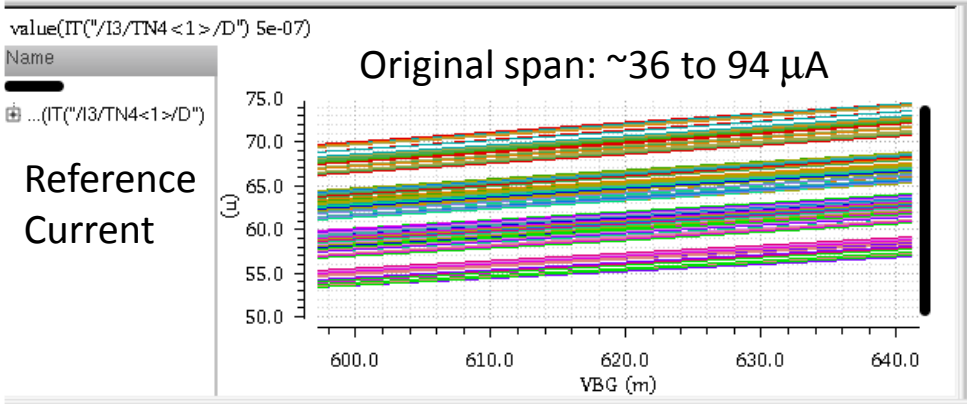
Current Reference

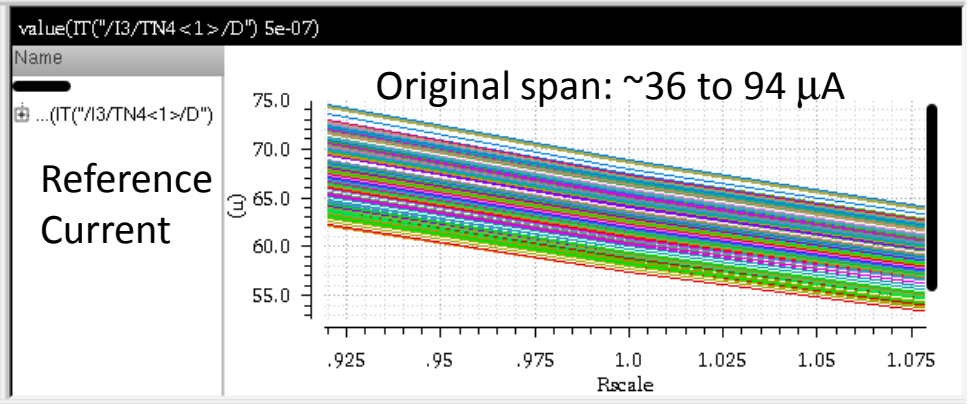


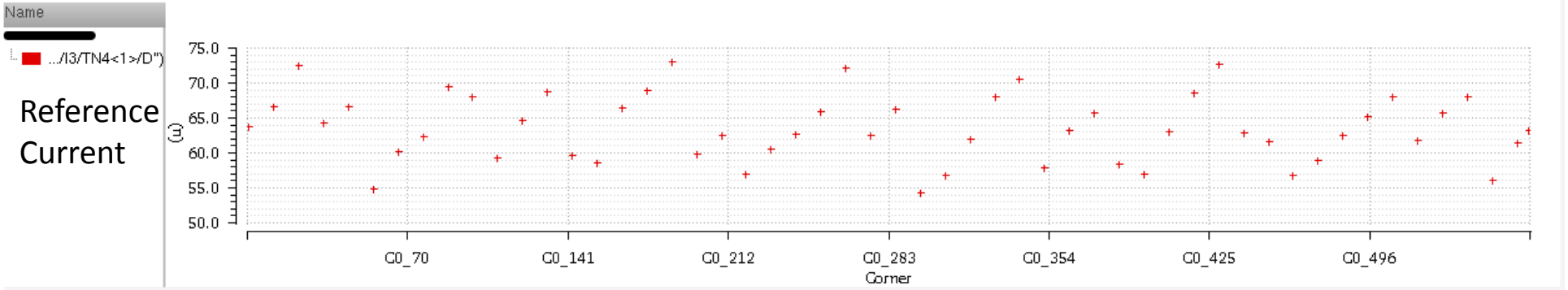
Schematic Simulation



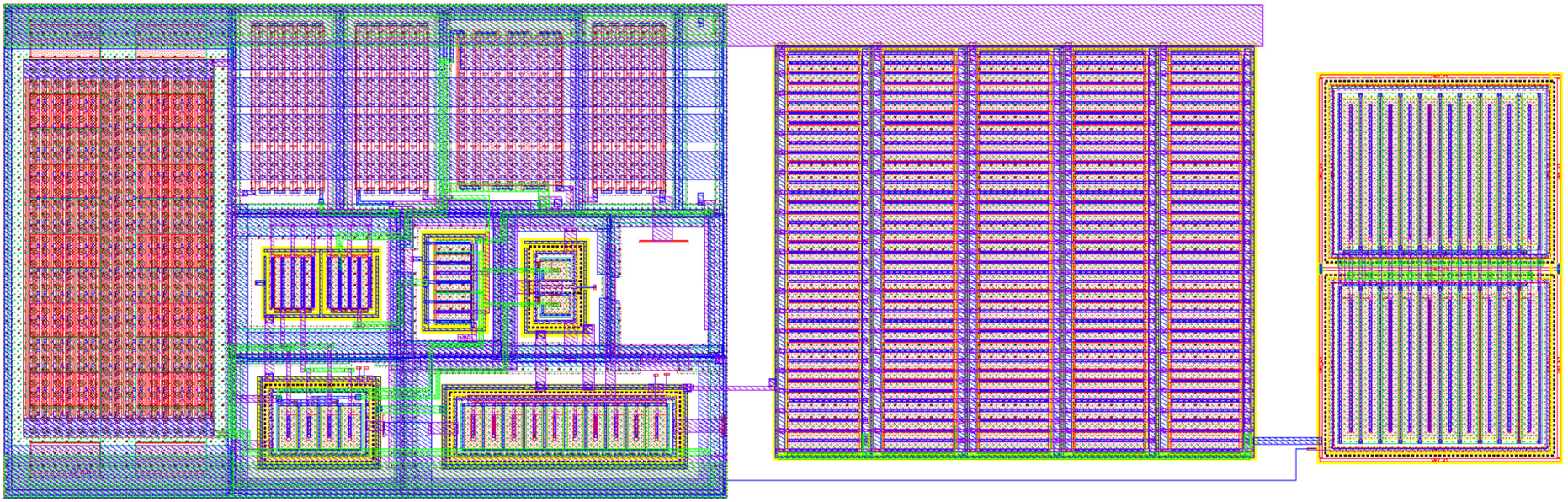




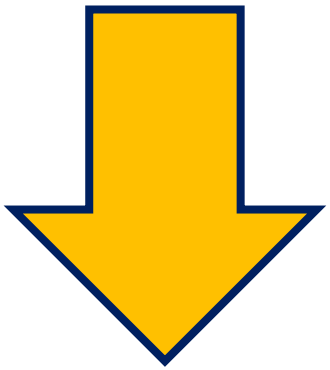




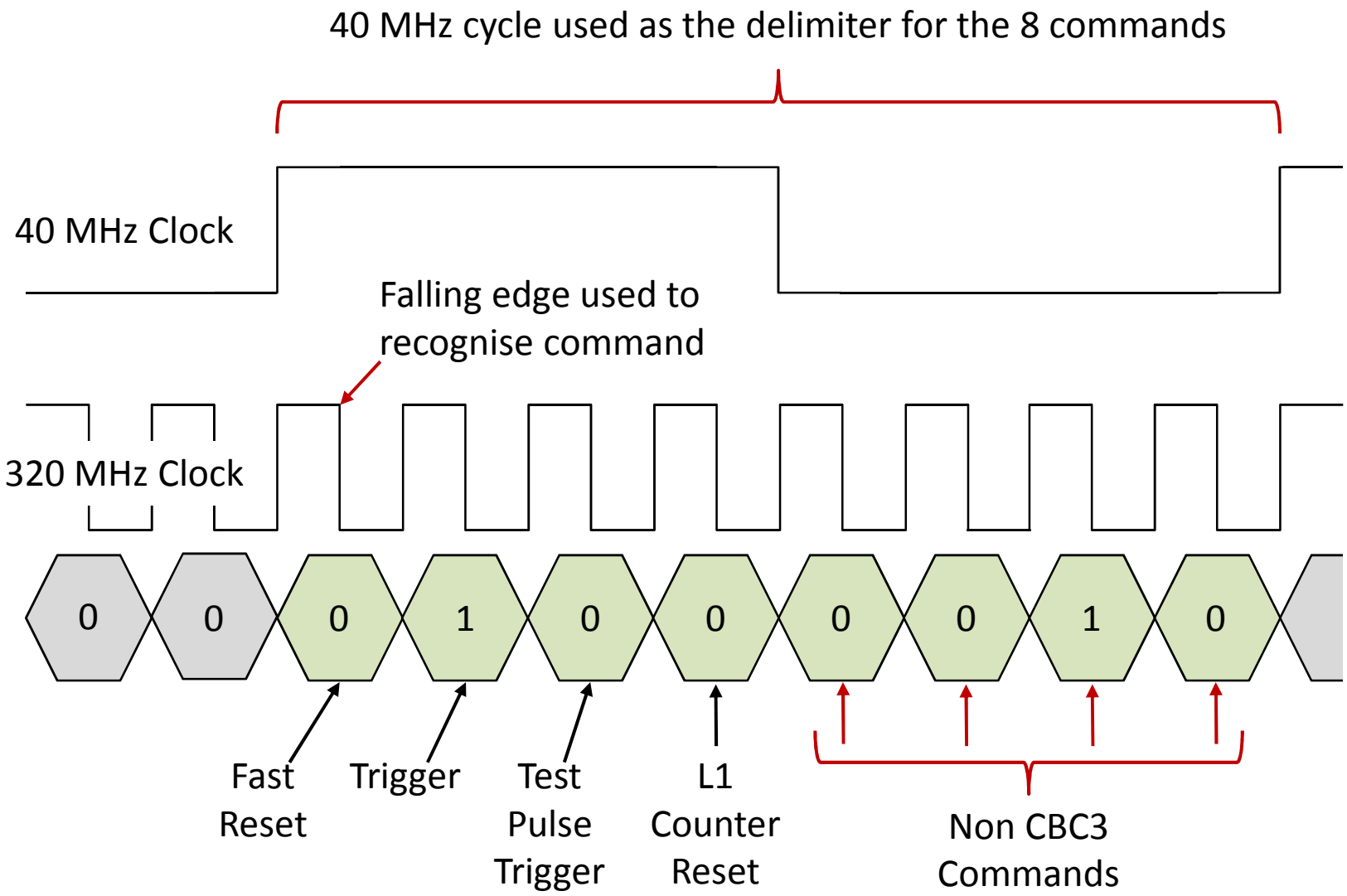
Layout in progress



Fast Command Interface



Fast Command Interface



Summary

- Technical Specification document – Complete
- Cluster Width Discrimination – Verified Layout complete
- Offset Correction and Correlation – Verified Layout complete
- Stub Gathering Logic – Verified Layout complete
- L1 Counter – Verified Layout complete
- Pipeline SRAM – DRC & LVS clean version of layout complete
- Current Reference – Circuit modifications complete. Layout almost completed
- Channel Mask – Included with Hit Detect circuit
- Hit Detect – Schematic designed and simulated across corners
- Bend Look-up table – Coded
- Data Assembly – Coded
- Fast Command Interface – Coded
- I2C Register – Whitaker latch simulated with I^2C controller

Backup Slides

CBC3 Architecture